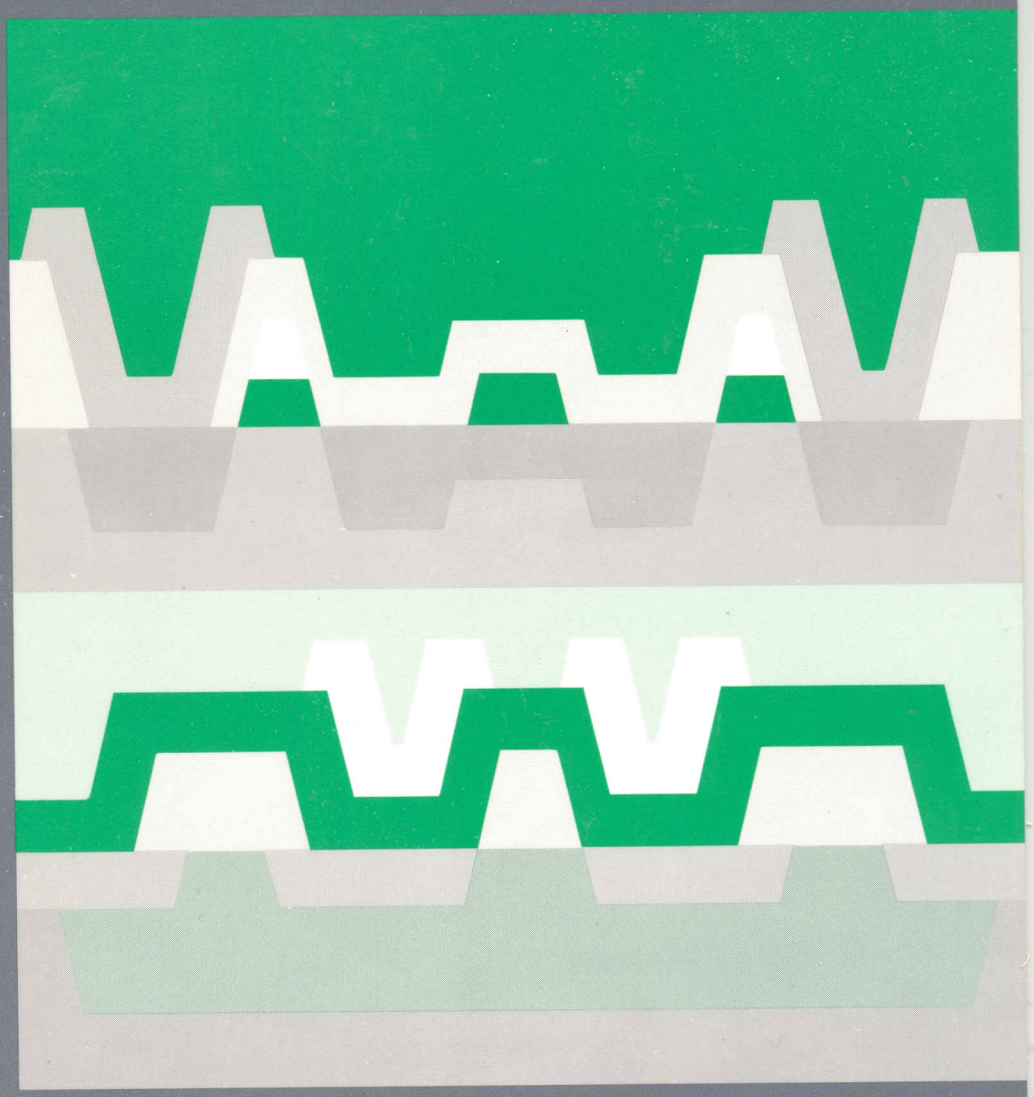
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  HN27512P-25/30 — 65,536-word × 8-bit One Time Electrically Programmable Read Only Memory 1215
- HN27C101P/FP SERIES
  HN27C101P-20/25
  HN27C101FP-20/25 — 131,072-word × 8-bit CMOS One Time Electrically Programmable ROM 1222
- HN27C301P/FP SERIES
  HN27C301P-20/25
  HN27C301FP-20/25 — 131,072-word × 8-bit CMOS One Time Electrically Programmable ROM 1229
- HN27C101AG SERIES
  CMOS 1Mb EPROM — 131,072-word × 8-bit CMOS UV Erasable and Programmable ROM . . 1237
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  HN27C4096G-10/12/15
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ECL RAM

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QUICK REFERENCE GUIDE TO HITACHI MEMORIES

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	16k-b	HM6116-2*2	CMOS	2048 × 8	120	120	+5	0.1m/0.2	24		●	●							64
		HM6116-3*2			150	150		0.1m/0.175			●	●							64
		HM6116-4*2			200	200					●	●							64
		HM6116L-2*2			120	120		10μ/0.175			●	●							64
		HM6116L-3*2			150	150		10μ/0.15			●	●							64
		HM6116L-4*2			200	200					●	●							64
		HM6116A-12*2			120	120		0.1m/15m			●		●						69
		HM6116L-15*2			150	150					●		●						69
		HM6116A-20*2			200	200					●		●						69
		HM6116AL-12*2			120	120		5μ/10m			●		●						69
		HM6116AL-15*2			150	150					●		●						69
		HM6116AL-20*2			200	200					●		●						69
		HM6716-25	Bi-CMOS	2048 × 8 (with OE)	25	25		0.28					●						74
		HM6716-30			30	30							●						74
		HM6719-25			25	25							●						74
		HM6719-30			30	30							●						74
		HM6268-25	CMOS	4096 × 4	25	25		0.1μ/0.25	20		●								80
		HM6268-35			35	35					●								80
		HM6268-45			45	45					●								80
		HM6268L-25			25	25		5μ/0.25			●								80
		HM6268L-35			35	35					●								80
		HM6268L-45			45	45					●								80
		HM6267-35		16384 × 1	35	35		0.1m/0.2			●								87
		HM6267-45			45	45					●								87
		HM6267-55			55	55					●								87
		HM6267L-35			35	35		5μ/0.2			●								87
		HM6267L-45			45	45					●								87
		HM6267L-55			55	55					●								87
	18k-b	HM6719-25	Bi-CMOS	2048 × 9	25	25		0.28	24				●						74
		HM6719-30			30	30							●						74
	16k-b	HM6264-10*2	CMOS	8192 × 8	100	100		0.1m/0.2	28		●	●							94
		HM6264-12*2			120	120					●	●							94
		HM6264A-10			100	100		0.1m/15m			●	●	●						94
		HM6264A-12			120	120					●	●	●						94
		HM6264A-15			150	150					●	●	●						94
		HM6264AL-10			100	100		10μ/15m			●	●	●						94
		HM6264AL-12			120	120					●	●	●						94
		HM6264AL-15			150	150					●	●	●						94
		HM6264AL-10L			100	100		10μ/15m			●	●	●						94
		HM6264AL-12L			120	120					●	●	●						94
		HM6264AL-15L			150	150					●	●	●						94
		HM6288-25		16384 × 4	25	25		0.1m/0.3	22 24 (SOJ)				●				●		103
		HM6288-35			35	35							●				●		103
		HM6288L-25			25	25							●				●		103
		HM6288L-35			35	35							●				●		103
		HM6788-25	Bi-CMOS		25	25		10m/0.23	22				●						111
		HM6788-35			35	35							●						111
		HM6788H-20			20	20		0.28					●						115
		HM6788HA-12			12	12		.3					●						119
		HM6788HA-15			15	15							●						119
		HM6788HA-20			20	20							●						119
	64k-b	HM6289-25	CMOS	16384 × 4 (with OE)	25	25		0.1m/0.3	24								●		124
		HM6289-35			35	35											●		124
		HM6289L-25			25	25											●		124
		HM6289L-35			35	35											●		124

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Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256k-b	HM6789-25	Bi-CMOS	16384 × 4 (with $\overline{OE}$)	25	25	+5	10μ/0.23	24				●				●		135
		HM6789-30			30	30							●				●		135
		HM6789H-15			15	15		0.28					●				●		142
		HM6789H-20			20	20							●				●		142
		HM6789HA-12			12	12							●				●		149
		HM6789HA-15			15	15							●				●		149
		HM6789HA-20			20	20							●				●		149
		HM6287-45	CMOS	65536 × 1	45	45		0.1m/0.3	22				●						157
		HM6287-55			55	55							●						157
		HM6287-70			70	70							●						157
		HM6287L-45			45	45		10μ/0.3					●						157
		HM6287L-55			55	55							●						157
		HM6287L-70			70	70							●						157
		HM6287H-25			25	25		0.1m/0.3					●				●		164
		HM6287H-35			35	35							●				●		164
		HM6287HL-25			25	25		10μ/0.3					●				●		164
		HM6287HL-35			35	35							●				●		164
		HM6787-25	Bi-CMOS		25	25		38m/0.18	22 24 (SOJ)				●						173
		HM6787-35			35	35							●						173
		HM6787H-15			15	15		0.21					●				●		178
		HM6787H-20			20	20							●				●		178
		HM6787HAJP-12			12	12		.3					●				●		178
		HM6787HAJP-15			15	15							●				●		183
		HM6787HAJP-20			20	20							●				●		183
		HM62256-8	CMOS	32768 × 8	85	85		0.2m/40m	28		●	●							189
		HM62256-10			100	100					●	●							189
		HM62256-12			120	120					●	●							189
		HM62256-15			150	150					●	●							189
		HM62256L-8			85	85		10μ/40m			●	●							189
		HM62256L-10			100	100					●	●							189
		HM62256L-12			120	120					●	●							189
		HM62256L-15			150	150					●	●							189
		HM62256L-10SL			100	100		10μ/40m			●	●							189
		HM62256L-12SL			120	120					●	●							189
		HM62256L-15SL			150	150					●	●							189
		HM62832-35			35	35		75m/.3					●				●		197
		HM62832-45			45	45							●				●		197
		HM62832L-35			35	35		10m/.3					●				●		197
		HM62832L-45			45	45							●				●		197
		HM62832H-25			25	25		.1m/.3					●				●		197
		HM62832H-35			35	35							●				●		197
		HM62832H-45			45	45							●				●		197
		HM62832HL-25			25	25		30m/.3					●				●		197
		HM62832HL-35			35	35							●				●		197
		HM62832HL-45			45	45							●				●		197
		HM6208-35		65536 × 4	35	35		0.1m/0.3	24		●								203
		HM6208-45			45	45					●								203
		HM6208L-35			35	35		10μ/0.3			●								203
		HM6208L-45			45	45					●								203
		HM6208H-25			25	25		0.1m/0.3					●				●		203
		HM6208H-35			35	35							●				●		203
		HM6208HL-25			25	25		10μ/0.3					●				●		203
		HM6208HL-35			35	35							●				●		203
		HM6708-20*3	Bi-CMOS		20	20		0.35					●				●		211
		HM6708-25*3			25	25							●				●		211
		HM6708A-15			15	15		.4				●				●			217
		HM6708A-20			20	20						●				●			217
		HM6708A-25			25	25						●				●			217
		HM6709-20			20	20		.35	28								●		222
		HM6709-25			25	25											●		222
		HM6709A-15			15	15		.4					●				●		229
		HM6709A-20			20	15							●				●		229
		HM6709A-25			25	25							●				●		229

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Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256k-b	HM6207-35	CMOS	262144 × 1	35	35	+5	0.1m/0.3	24				●						236
		HM6207-45			45	45							●						236
		HM6207L-35			35	35		10μ/0.3					●						236
		HM6207L-45			45	45							●						236
		HM6207H-25			25	25		0.1m/0.3					●				●		243
		HM6207H-35			35	35							●				●		243
		HM6207HL-25			25	25		10μ/0.3					●				●		243
		HM6207HL-35			35	35							●				●		243
		HM6707-20*3	Bi-CMOS		20	20		0.35					●				●		250
		HM6707-25*3			25	25							●				●		250
		HM6707A-15			15	15		.4					●				●		255
		HM6707A-20			20	20							●				●		255
		HM6707A-25			25	25							●				●		255
	1M-b	HM628128-7*3	CMOS	131072 × 8	70	70		0.1m/75m	32		●	●							261
		HM628128-8*3			85	85					●	●							261
		HM628128-10*3			100	100					●	●							261
		HM628128-12*3			120	120					●	●							261
		HM628128L-7*7			70	70		10μ/75m			●	●							261
		HM628128L-8*7			85	85					●	●							261
		HM628128L-10*7			100	100					●	●							261
		HM628128L-12*7			120	120					●	●							261
		HM624256-35*3		Z62144 × 4	35	35		0.1m/0.35	28				●				●		269
		HM624256-45*3			45	45							●				●		269
		HM624256L-35*3			35	35		.1m/.35					●				●		269
		HM624256L-45*3			45	45							●				●		269
		HM624257-35*4			35	35		0.1m/0.35	32								●		275
		HM624257-45*4			45	45											●		275
		HM624257L-35*4			35	35											●		275
		HM624257L-45*4			45	45											●		275
Static RAM Module		HM66204-12*4		131072 × 8 (with decoder)	120	120		0.8m/50m										●	283
		HM66204-15*4			150	150												●	283
		HM66204L-12*4			120	120		40μ/50m										●	283
		HM66204L-15*4			150	150												●	283
FIFO	18k-bit	HM63921-20		2k × 9	20	30		1.0W max.	28		●								289
		HM63921-25			25	35					●								289
		HM63921-35			35	45					●								289
	36k-bit	HM63941-25		4k × 9	25	35					●								289
		HM63941-35			35	45					●								289
		HM63941-45			45	60					●								289
Cache Static RAMs	120k-b	HM62A168-25		8k × 16 (2 way)	25	25		1.1 (max.)	52							●			311
		HM62A168-35			35	35										●			311
		HM62A168-45			45	45										●			311
	128k-b	HM62A188-25		8k × 18 (2 way)	25	25										●			311
		HM62A188-35			35	35										●			311
		HM62A188-45			45	45										●			311
	256k-b	HM67C932-20	Bi-CMOS	32k × 9 (4 way)	20	20		TBD	44							●			319
		HM67C932-25			25	25										●			319
		HM67B932-20			20	20										●			†
		HM67B932-25			25	25										●			†
Fast SRAM Module	2M-b	HB66B1616A-25	CMOS	16k × 16 (module)	25	25		.4m/1.2	36									●	333
		HB66B1616A-35			35	35												●	333
		HB66A2568A-25		256k × 8 (module)	25	25		.8m/2.4	60									●	343
		HB66A2568A-35			35	35												●	343
TAG RAM	32k-b	HM644332-25		2k × 20 (tag ram)	25	25		1.0 max.	64										351
		HM644332-30			30	30													351

†Data sheet not included in this manual. Request data sheet for HM67B932.

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Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Pseudo Static	256k-b	HM65256B-10	CMOS	32768 × 8	100	100		2m/0.175	28		●	●	●						369
		HM65256B-12			120	190					●	●	●						369
		HM65256B-15			150	235					●	●	●						369
		HM65256B-20			200	310					●	●	●						369
		HM65256BL-10			100	180					●	●	●						369
		HM65256BL-12			120	190					●	●	●						369
		HM65256BL-15			150	235					●	●	●						369
		HM65256BL-20			200	310					●	●	●						369
		HM658128D-10		131072 × 8	100	180		5m/0.2	32		●	●							376
		HM658128D-12			120	210					●	●							376
		HM658128D-15			150	250					●	●							376
		HM658128L-10			100	180		0.5m/0.2			●	●							376
		HM658128L-12			120	210					●	●							376
		HM658128L-15			150	250					●	●							376
Video Memory	16k-b	HM63021-28		2048 × 8	20	28		0.25	18										388
		HM63021-34			24	34													388
		HM63021-45			30	45													388
	1M-b	HM53051-45		262144 × 4	35	45		0.2	28		●								402
		HM63021-60			40	60					●								402
	256k-b	HM53461-10		65536 × 4 Multi-port	100	190			24		●			●					412
		HM53461-12			120	220					●			●					412
		HM53461-15			150	260					●			●					412
		HM53462-10			100	190					●			●					425
		HM53462-12			120	220					●			●					425
		HM53462-15			150	260					●			●					425
	1M-b	HM538121-10*3		131072 × 8	100	190	+5		40								●		569
		HM538121-12*3			120	220											●		569
		HM538121-15*3			150	260											●		569
		HM538122-10*3			100	190											●		444
		HM538122-12*3			120	220											●		444
		HM538122-15*3			150	260											●		444
		HM538123-10*3			100	190											●		470
		HM538123-12*3			120	220											●		470
		HM538123-15*3			150	260											●		470
		HM534251-10*3		262144 × 4 Multi-port	100	190		35m/0.55	28					●			●		469
		HM534251-11*3			100	190								●			●		469
		HM534251-12*3			120	220								●			●		469
		HM534251-15*3			150	260								●			●		469
		HM534252-10*3			100	190								●			●		516
		HM534252-11*3			100	190								●			●		516
		HM534252-12*3			120	220								●			●		516
		HM534252-15*3			150	260								●			●		516
		HM534253-10*3			100	190								●			●		542
		HM534253-12*3			120	220								●			●		542
		HM534253-15*3			150	260								●			●		542
Dynamic	256k-b	HM50464-12	NMOS	65536 × 4	120	220			18		●					●			590
		HM50464-15			150	260					●					●			590
		HM50464-20			200	330		20m/0.35			●					●			590
		HM50256-12		262144 × 1	120	220			16 18 (PLCC)		●			●		●			598
		HM50256-15			150	260					●			●		●			598
		HM50256-20			200	330					●			●		●			598
		HM51256-8	CMOS		85	155		10m/0.35			●			●		●			606
		HM51256-10			100	180					●			●		●			606
		HM51256-12			1205	210					●			●		●			606
		HM51256-15			150	250					●			●		●			606
		HM51256L-8			85	155					●			●		●			606
		HM51256L-10			100	185					●			●		●			606
		HM51256L-12			120	210					●			●		●			606
		HM51256L-15			150	250					●			●		●			606

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Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
		HM51258-8			85	150					●								614
		HM51258-10		262144 × 1	100	180		10m/0.35	16		●								614
		HM51258-12			120	210					●								614
		HM51258-15			150	250					●								614
		HM514256-8			80	160					●			●			●		623
		HM514256-10			100	190					●			●			●		623
		HM514256-12			120	220					●			●			●		623
		HM514256-8S			80	160					●			●			●		635
		HM514256-10S			100	190		10m/0.33			●			●			●		635
		HM514256-12S			120	220					●			●			●		635
		HM514256A-8			80	160					●			●			●		635
		HM514256A-10			100	190					●			●			●		635
		HM514256A-12			120	220					●			●			●		635
		HM514256API-6			60	120		11/495			●			●			●		651
		HM514256API-7			70	130		11/440			●			●			●		651
		HM514256API-8			80	160		11/385			●			●			●		651
		HM514256API-10			100	190		11/330			●			●			●		651
		HM514256API-12			120	220		11/275			●			●			●		651
		HM514256H-6			60	120		10m/0.45			●			●			●		667
		HM514256H-7			70	140					●			●			●		667
		HM514258-8S			80	160					●			●			●		696
		HM514258-10S			100	190					●			●			●		696
		HM514258-12S			120	220		10m/0.375			●			●			●		696
		HM514258A-8			80	160					●			●			●		696
		HM514258A-10			100	190					●			●			●		696
		HM514258A-12			120	220					●			●			●		696
		HM514266A-6			60	120		11/495			●			●			●		711
		HM514266A-7			70	130		11/440			●			●			●		711
Dynamic	1M-b	HM514266A-8	CMOS		80	160	+ 5	11/363	18		●			●			●		711
		HM514266A-10			100	190		11/303			●			●			●		711
		HM514266A-12		1048576 × 1	120	220		11/259			●			●			●		711
		HM514256-8			80	160		11/363			●			●			●		711
		HM514256-10			10	190		11/303			●			●			●		711
		HM514256-12			12	220		11/259			●			●			●		711
		HM511000-8S			80	160					●			●			●		725
		HM511000-10S			100	190		10m/0.35			●			●			●		725
		HM511000-12S			120	220					●			●			●		725
		HM511000A-8			80	160					●			●			●		725
		HM511000A-10			100	190		10m/0.375			●			●			●		725
		HM511000A-12			120	220					●			●			●		725
		HM511000ALP-8			80	160		1.7/385			●			●			●		737
		HM511000ALP-10			100	190		1.7/330			●			●			●		737
		HM511000ALP-12			120	220		1.7/275			●			●			●		737
		HM511000ALJP-8			80	160		1.7/385			●			●			●		737
		HM511000ALJP-10			100	190		1.7/330			●			●			●		737
		HM511000ALJP-12			120	220		1.7/275			●			●			●		737
		HM511000H-6			60	125		10m/0.45			●			●			●		751
		HM511000H-7			70	140					●			●			●		751
		HM511001-8S			80	160					●			●			●		762
		HM511001-10S			100	190					●			●			●		762
		HM511001-12S			120	220					●			●			●		762
		HM511001A-8			80	160					●			●			●		773
		HM511001A-10			100	190		10m/0.35			●			●			●		773
		HM511001A-12			80	160					●			●			●		773
		HM511002-8S			80	160					●			●			●		816
		HM511002-10S			100	190					●			●			●		816
		HM511002-12S			120	220					●			●			●		816

(continued)

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1										Page
									Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	
Dynamic	1M-b	HM511002A-8	CMOS	1,048,576 × 1	80	160	5V	10m/0.45	28		●			●			●		816
		HM511002A-10			100	190					●			●			●		816
		HM511002A-12			120	220					●			●			●		816
		HM57100JP-35R	Bi-CMOS	1M × 1	35	70		1W									●		803
		HM57100JP-40R			40	80											●		803
		HM57100JP-45R			45	85											●		803
		HM574256JP-35R			35	70											●		816
		HM574256JP-40R			40	80											●		816
		HM574256JP-45R			45	85											●		816
	4M-b	HM514100-8	CMOS	4,194,304 × 1	80	150	5V	11m/.495	20					●			●		855
		HM514100-10			100	180		11m/.44						●			●		855
		HM514100-12			120	210		11m/.385						●			●		855
		HM514100-7			70	140	5v–5	11m/.55						●			●		869
		HM514400-8		1,048,576 × 4	80	150	5V	11m/.495						●			●		883
		HM514400-10			100	180		11m/.44						●			●		883
		HM514400-12			120	210		11m/.385						●			●		883
		HM514101-8		4,194,304 × 1	80	150		11m/.495						●			●		883
		HM514101-10			100	180		11m/.44						●			●		883
		HM514101-12			120	210		11m/.385						●			●		883
		HM514102-8			80	150		11m/.495						●			●		883
		HM514102-10			100	180		11m/.44						●			●		883
		HM514102-12			120	210		11m/.385						●			●		883
		HM514410-8		1,048,576 × 4	80	150		11m/.495						●			●		883
		HM514410-10			100	180		11m/.44						●			●		883
		HM514410-12			120	210		11m/.385						●			●		883
DRAM Module		HB561008-12	NMOS	262144 × 8	120	210		0.12/2.42										●	963
		HB561008-15			150	260		0.12/2.42										●	963
		HB561003-12		262144 × 9	120	210		0.135/2.55										●	854
		HB561003-15			150	260		0.135/2.16										●	854
		HB561409-10	CMOS		100	180		60m/1.8										●	958
		HB56A18-10S		1048576 × 8	100	180		20m/1.4										●	831
		HB56A18-12S			120	210												●	831
		HB56A18-10A			100	180												●	831
		HB56A18-12A			120	210												●	831
		HB56A19-10S		1048576 × 9	100	180		20m/1.6										●	843
		HB56A19-12S			120	210												●	843
		HB56A19-10A			100	180												●	843
		HB56A19-12A			120	210												●	843
		HB56C18-10		1048576 × 8	100	190		20m/1.8										●	843
		HB56C18-12			120	220												●	843
		HB56C18AT-8A		1048576 × 9	80	560		88/3.08											837
		HB56C18AT-10A			100	A80		88/2.6A											837
		HB56C18AT-12A			120	400		88/2.20											837
		HB56C19-8			80	630		99/3465											849
		HB56C19-10			100	190		22m/2.0										●	849
		HB56C19-12			120	220												●	849
		HB56C19AT-8A			80	630		99/3465										●	849
		HB56C19AT-10A			100	540		99/2970										●	849
		HB56C19AT-12A			120	450		99/2475										●	849
		HB56D25608A-6H		262,144 × 8	60	180		22/990										●	967
		HB56D25608A-7H			70	160		22/880										●	967
		HB56D25608A-8A			80	132		22/726										●	967
		HB56D25608A-10A			100	110		22/605										●	967
		HB56D25608A-12A			120	94		22/517										●	967
		HB56D25609A-85A		262,144 × 9	85	202		33/1.11										●	979
		HB56D25609A-10A			100	170		33/.94										●	979
		HB56D25609A-12A			120	144		33/.79										●	979

(continued)

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1										Page
									Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	
DRAM Module		HB56D25609B-85A	CMOS	262,144 × 9	85	202		33/1.11	30									●	979
		HB56D25609B-10A			100	176		33/.94										●	979
		HB56D25609B-12A			120	144		33/.79										●	979
		HB56D25636B-85		262,144 × 36	85	160		126/4.24	72									●	991
		HB56D25636B-10			100	190												●	991
		HB56D25636B-12			120	220												●	991
		HB56D51236B-85		524,288 × 36	85	160		252/4.58										●	1003
		HB56D51236B-10			100	190		252/3.91										●	1003
		HB56D51236B-12			120	220		252/3. 36										●	1003
	4M-b	HB56A49-8		4,194,304 × 9	80	160	5V	99m/4.455	30									●	1027
		HB56A49-10			100	190		99m/3.96										●	1027
		HB56A49-12			120	220		99m/4.405										●	1027
		HB56A48-8		4,194,304 × 8	80	160		88m/3.96										●	1015
		HB56A48-10			100	190		88m/3.52										●	1015
		HB56A48-12			120	220		88m/3.08										●	1015
		HB56D136-8		1,045,576 36	80	160		126m/5.25	72									●	1039
		HB56D136-10			100	190		126m/4.62										●	1039
		HB56D136-12			120	220	5V ± 5%	126m/3.99										●	1039
		HB56D236-8		2,097,152 × 36	80	160		252m/5.57										●	1049
		HB56D236-10			100	190		252m/4.94										●	1049
		HB56D236-12			120	220		252m/4.31										●	1049

■ MOS ROM

Program	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1				Page
								Pin No.	G	P	FP	
Mask	256k-b	HN623257	CMOS	32768 × 8	150	5 +	5μ/0.1	28		●	●	1060
		HN623258			200					●	●	1063
	1M-b	HN62331*3		131072 × 8	120					●	●	1069
		HN62321			150					●	●	1066
		HN62321B			200					●	●	1077
		HN62331E*3			120					●	●	1077
		HN62321E			200					●	●	1077
		HN62331A*3			120			32		●	●	1069
		HN62321A			150					●	●	1080
	2M-b	HN62422*3		131072 × 16 or 262144 × 8	150			40/44		●	●	1083
		HN62412			200					●	●	1083
	4M-b	HN62424*3		262144 × 16 or 524288 × 8	150			40/44		●	●	1087
		HN62404			200					●	●	1087
		HN62324B*3		524288 × 8	150			32		●	●	1091
		HN62304B			200					●	●	1091
		HN62414		262144 × 16 or 524288 × 8	200/170			40		●		1101
					200/170			44/48		●	●	1101
		HN62314		512K × 8	200/170			32		●	●	1107
		HN62444		512K × 8	100			40		●	●	1095
				256 × 16	100			44/48			●	1095
	8M-b	HN62408*3		524288 × 16 or 1048576 × 8	200			42/44		●	●	1114

(continued)

■ MOS ROM

Program	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1				Page
								Pin No.	G	P	FP	
Electrically Erasable & Programmable	16M-b	HN62308B	CMOS	1M × 8	200	+5	5μ/0.1	32		●	●	1119
		HN66403P		1M × 8 512K × 16	250			42		●		1123
		HN624016*3		1048576 × 16 or 20978152 × 8	200					●		1127
	64k-b	HN58C65-25		8192 × 8	250		2m/20m	28		●	●	1138
		HN58C66-25			250					●	●	1147
	256k-b	HN58C256-20*4		32768 × 8	200		0.5μ/0.1			●	●	1156
UV Erasable & Electrically Programmable	256k-b	HN27C256A-10*3			100				●			1158
		HN27C256A-12*3			120				●			1158
		HN27C256A-15*3			150				●			1158
		HN27C256H-70			70		0.15		●			1166
		HN27C256H-85			85				●			1166
	512k-b	HN27512-25	NMOS	65536 × 8	250		50m/0.2		●			1176
		HN27512-30			300				●			1176
	1M-b	HN27C1024H-85	CMOS	65536 × 16	85		0.2	40	●			1183
		HN27C1024H-10			100				●			1183
		HN27C101-17		131072 × 8	170		0.5μ/0.1	32	●			1192
		HN27C101-20			200				●			1192
		HN27C101-25			250				●			1192
		HN27C301-17			170				●			1200
		HN27C301-20			200				●			1200
		HN27C301-25			250				●			1200
One Time Electrically Programmable	256k-b	HN27C256-25T	CMOS	32768 × 8	250		0.5μ/50m				●	1209
		HN27C256-30T			300						●	1209
	512k-b	HN27512-25	NMOS	65536 × 8	250		50m/0.2			●		1215
		HN27512-30			300					●		1215
	1M-b	HN27C101-20	CMOS	131072 × 8	200		0.5μ/0.1	32		●	●	1222
		HN27C101-25			250					●	●	1222
		HN27C301-20			200					●	●	1229
		HN27C301-25			250					●	●	1229
		HN27C101-AG		128k × 8	15/12/10				●			1237
					15/12				●	●	●	1237
		HN27C4096		256k × 16	12/12/10			40	●			1247
					12/15			44				1247

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■ ECL RAM

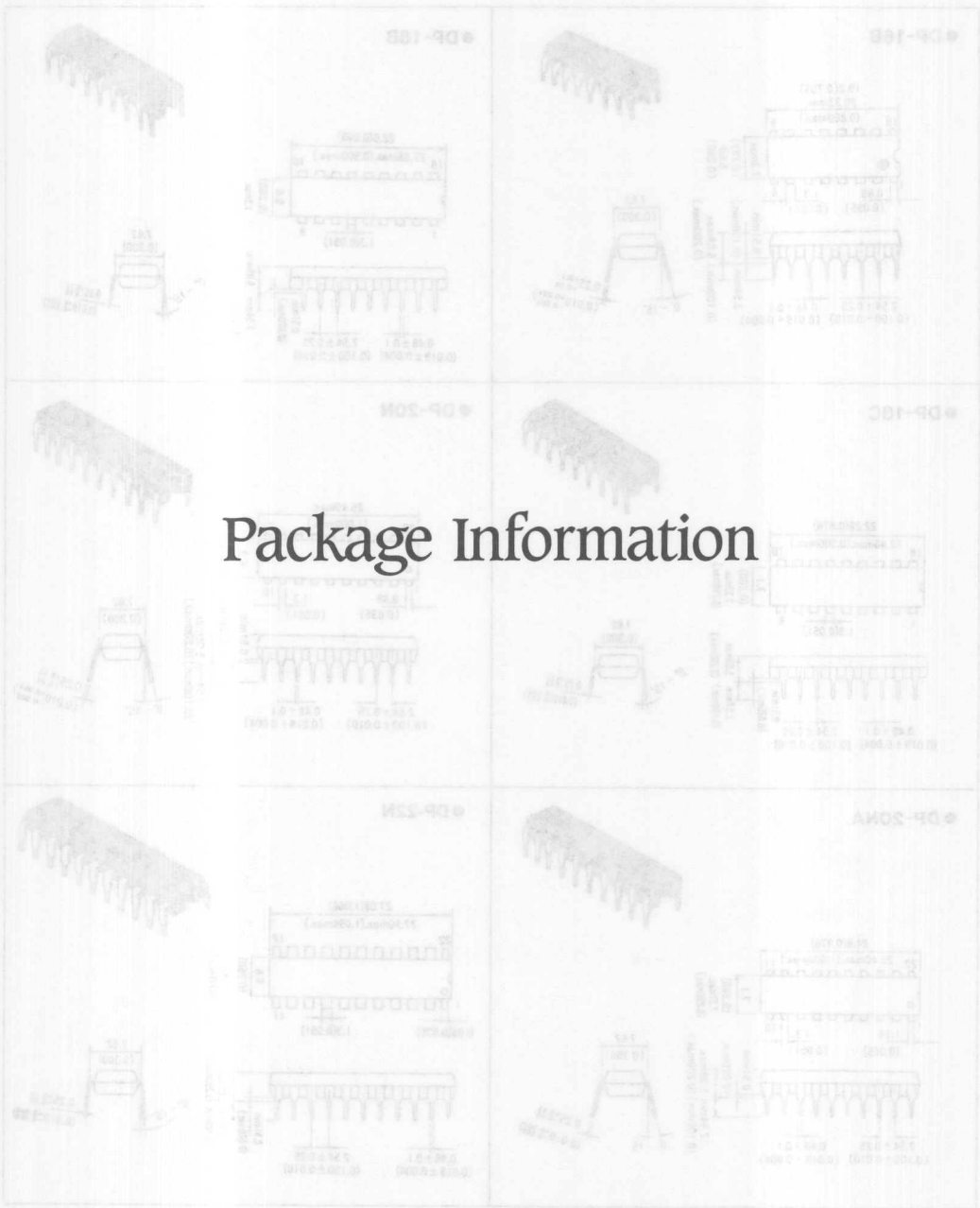
Level	Total Bit	Type No.	Organization (word × bit)	Output	Access Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1					Page
								Pin No.	G	F	CG	JP	
ECL 10K	64k-b	HM10494-10	16384 × 4	Open	10	–5.2	0.8	28	●	●			1258
		HM10494-12			12				●	●			1258
		HM10490-10	65536-1		10		.57	22	●	●			1263
		HM10490-12			12				●	●			1263
	256k-b	HM10504-10	65536 × 4		10		.50	28		●			1267
		HM10504-12			12					●			1267
		HM10500-15*3	262144 × 1	Emitter	15		0.52	24	●				1269
ECL100K	64k-b	HM100494-10*4	16384 × 4		10	–4.5	0.65	28	●	●		●	1273
		HM100494-12*4			12				●	●		●	1273
		HM100490-10	65536 × 1		15		0.57	22	●	●		●	1277
		HM100490-12			20				●	●		●	1277
		HM100490-15							●	●		●	1277
	256k-b	HM100504F-10	65536 × 4		10		.50	28		●			1281
		HM100504F-12			12					●			1281
		HM100500-18*3	262144 × 1		18		0.5	24/28	●	●	●		1282
	64k-b	HM101494-10	16384 × 4		10	–5.2	.75	28	●	●			1285
		HM101494-12			12				●	●			1285
		HM101490-10	65536 × 1		10		.57	22	●	●			1289
		HM101490-12			12				●	●			1289
		HM101504-10			10					●			1293
		HM101504-12			12					●			1293
		HM101500-15*3					.50	24		●			1294

Notes) *1. The package codes of G, F and CG and applied to the package material as follows.
G; cerdip, F; Flat Package, CG; Ceramic Leadless Chip Carrier
*2. Maintenance Only. This device is not available for new application.
*3. Preliminary
*4. Under Development

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Package Information



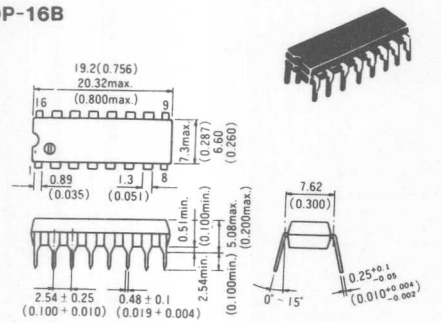
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PACKAGE INFORMATION

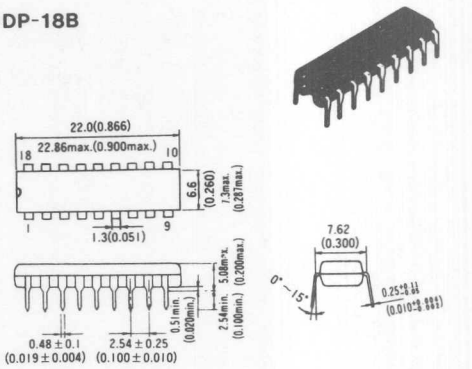
- **Dual-in-line Plastic**

Unit: mm (inch) Scale 1/1

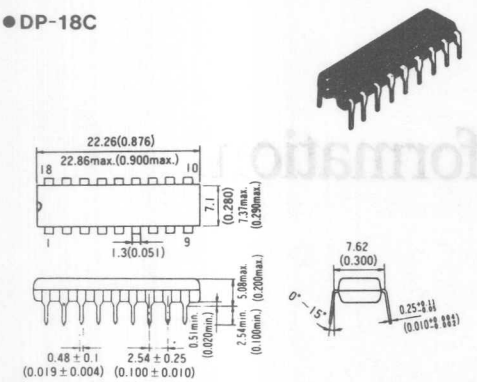
●DP-16B



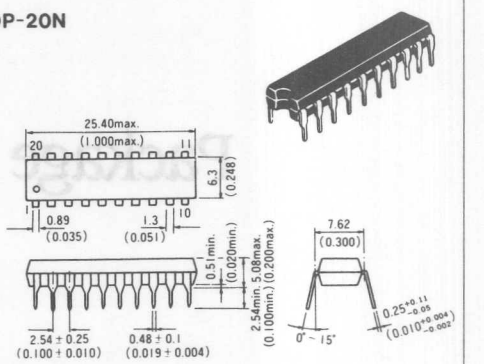
●DP-18B



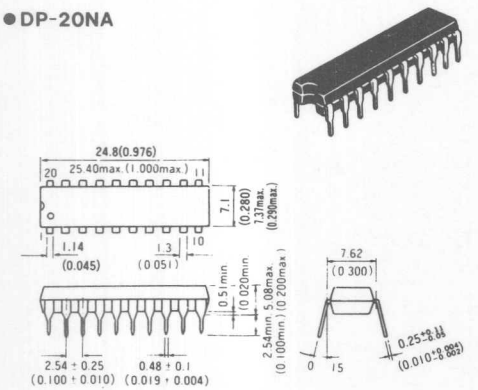
●DP-18C



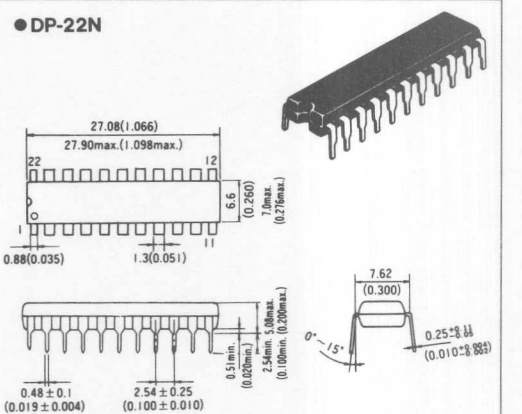
●DP-20N



●DP-20NA



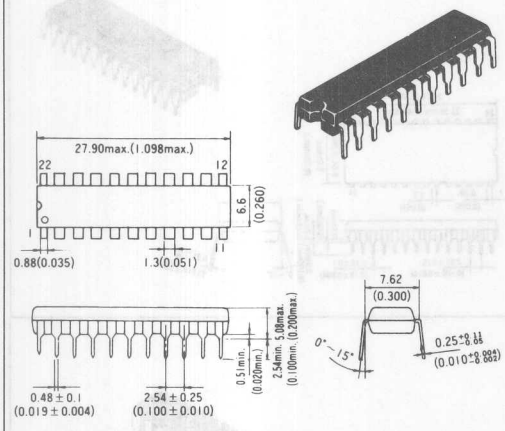
●DP-22N



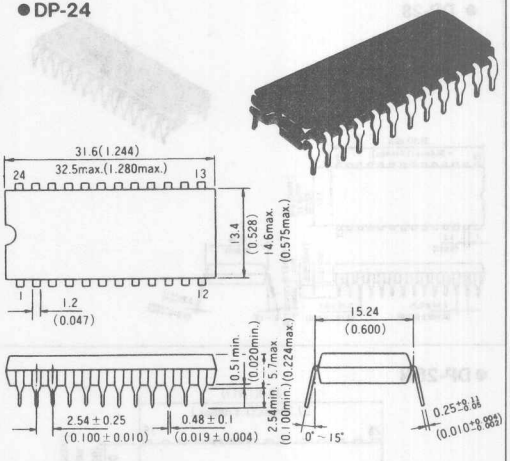
● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

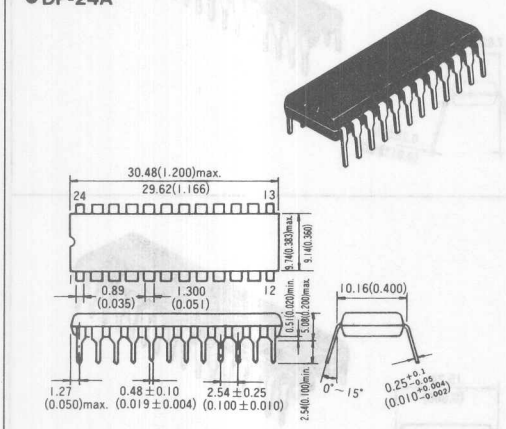
● DP-22NB



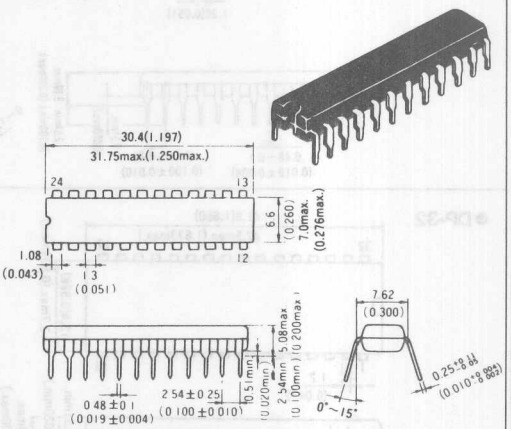
● DP-24



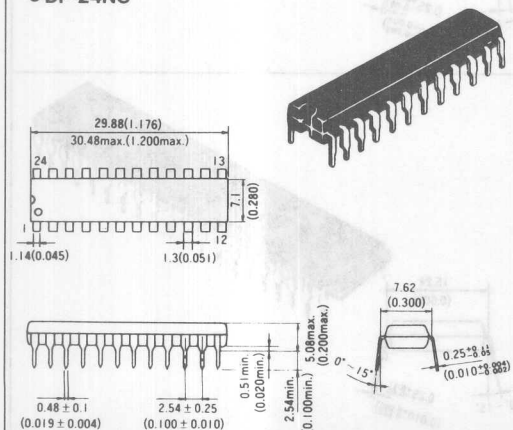
● DP-24A



● DP-24N



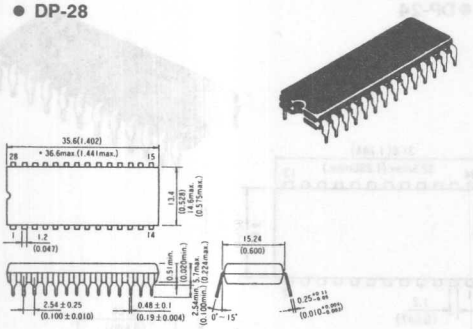
● DP-24NC



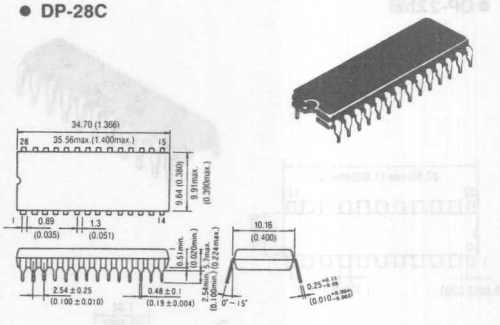
● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

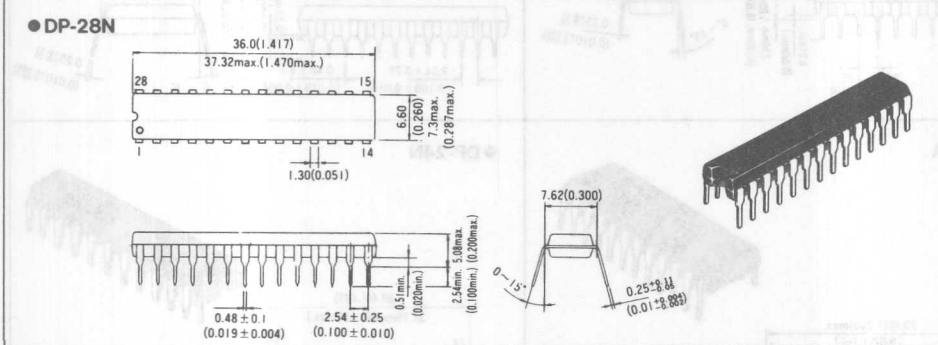
● DP-28



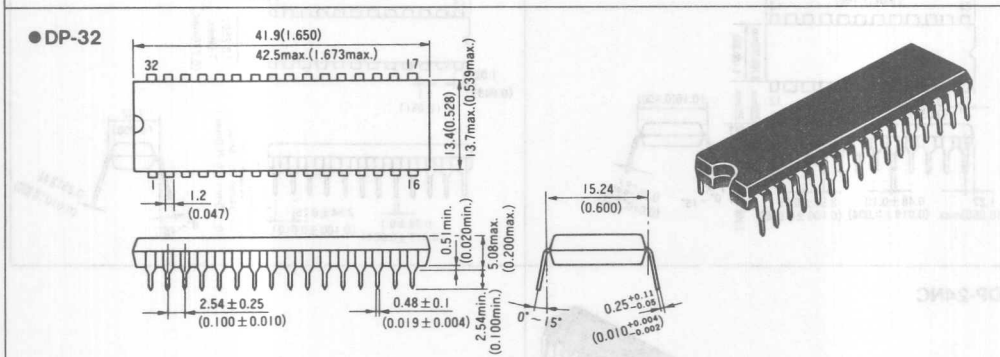
● DP-28C



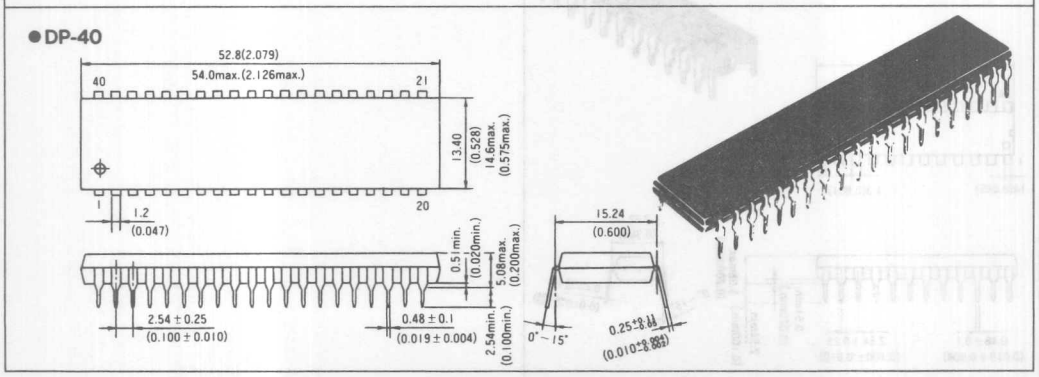
● DP-28N



● DP-32



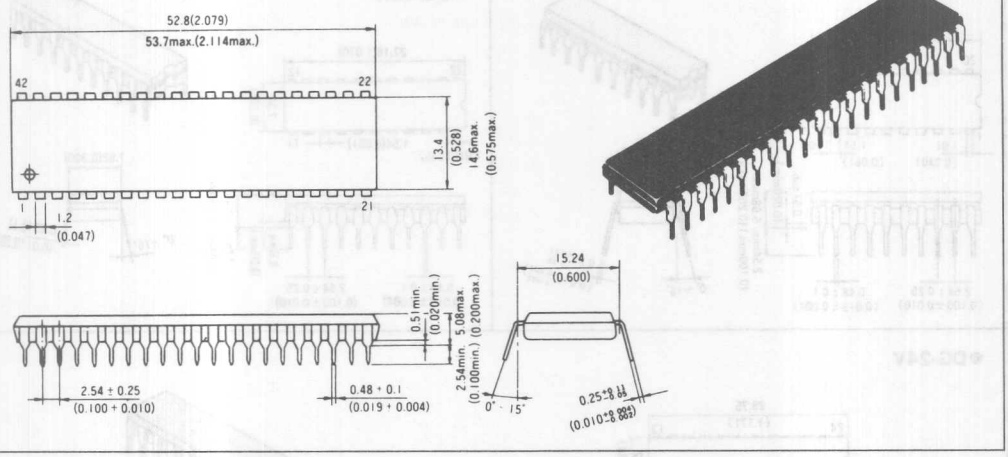
● DP-40



● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

● DP-42



Applicable ICs

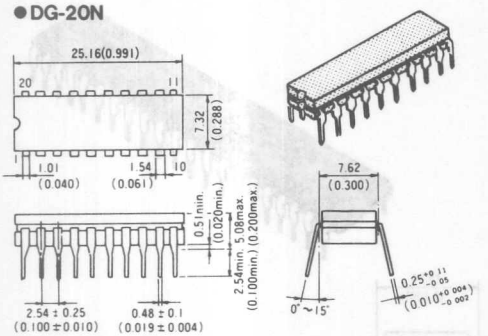
DP-16B	HM50256P Series, HM50257P Series, HM51256P Series, HM51256LP Series, HM51258P Series
DP-18B	HM50464P Series, HM50465P Series
DP-18C	HM53051P, HM511000AP Series, HM511000SP Series, HM511000HP Series, HM511001AP Series, HM511001SP Series, HM511002AP Series, HM511002SP Series
DP-20N	HM6168HP Series, HM6168HLP Series, HM6268P Series, HM6268LP Series, HM6167P Series, HM6167LP Series, HM6167HP Series, HM6167HLP Series, HM6267P Series, HM6267LP Series
DP-20NA	HM514256P Series, HM514256AP Series, HM514256SP Series, HM514256HP Series, HM514258HLP Series, HM514258SP Series
DP-22N	HM6287P Series, HM6287LP Series
DP-22NB	HM6288P Series, HM6288LP Series, HM6788P Series, HM6788HP Series, HM6287HP Series, HM6287HLP Series, HM6787P Series, HM6787HP Series
DP-24	HM6116P Series, HM6116LP Series, HM6116AP Series, HM6116ALP Series
DP-24A	HM53461P Series, HM53462P Series
DP-24N	HM6116ASP Series, HM6116ALSP Series
DP-24NC	HM6716P Series, HM6719P Series, HM6789P Series, HM6789HP Series, HM6208P Series, HM6208LP Series, HM6208HP Series, HM6208HLP Series, HM6708P Series, HM6207P Series, HM6207LP Series, HM6207HP Series, HM6207HLP Series, HM6707P Series
DP-28	HM6264P Series, HM6264LP Series, HM6264LP-L Series, HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM62256LP-L Series, HM65256AP Series, HM65256BP Series, HM65256BLP Series, HN623257P, HN623258P, HN62321P, HN62321BP, HN62331P, HN62321EP, HN62331EP, HN62321AP, HN62331AP, HN58064P, HN58C66P, HN58C256P, HN27128AP, HN27256P, HN27512P
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM65256ASP Series, HM65256BSP Series, HM65256BLSP Series, HM63021P Series
DP-32	HM628128P Series, HM628128LP Series, HM658128DP Series, HM65256ASP Series, HM65256BSP Series, HN27C101P Series, HN27C301P Series
DP-40	HN62412P, HN62422P, HN62404P, HN62424P
DP-42	HN62408P, HN624016P

PACKAGE INFORMATION

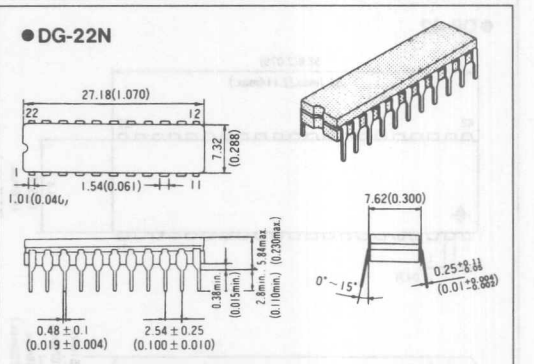
● CERDIP

Unit: mm (inch) Scale 1/1

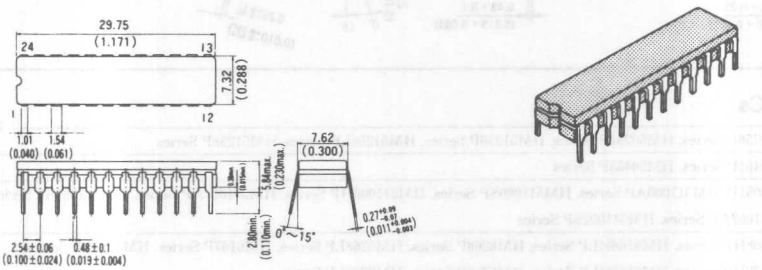
● DG-20N



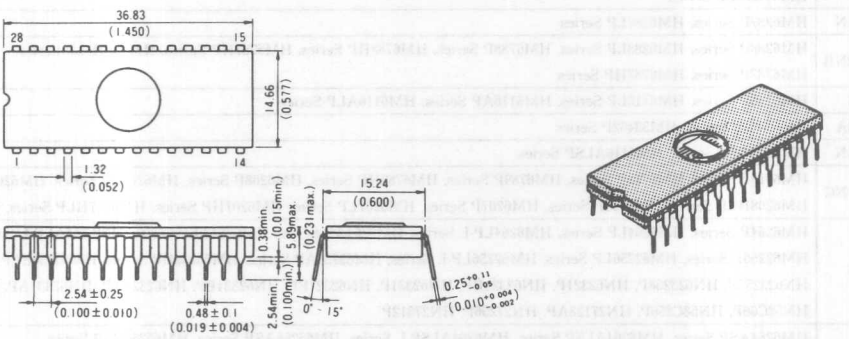
● DG-22N



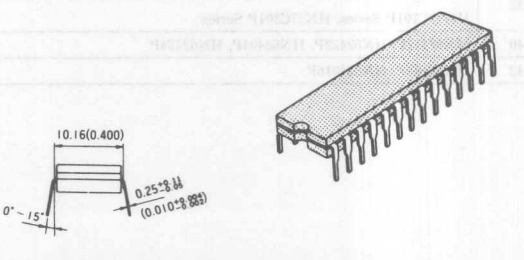
● DG-24V



● DG-28



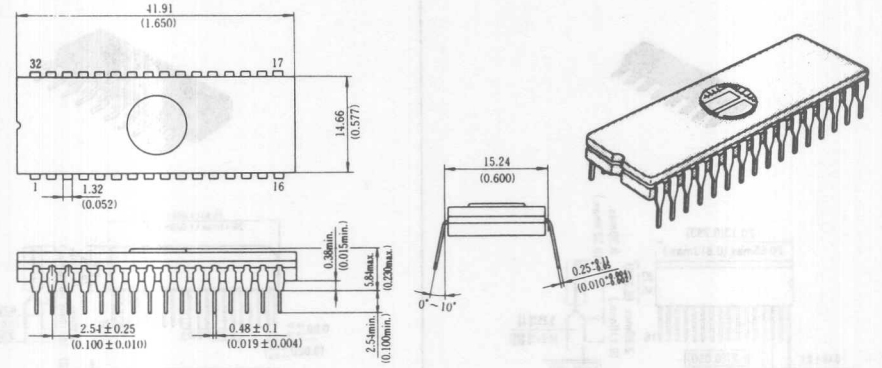
● DG-28N



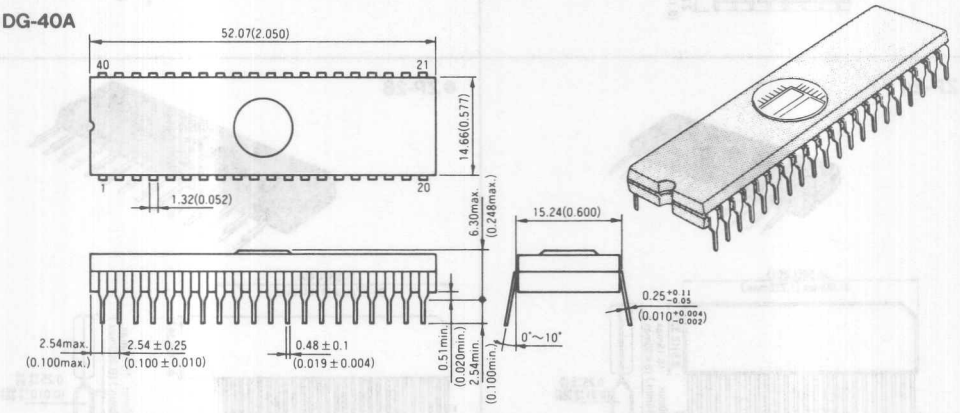
● CERDIP

Unit: mm (inch) Scale 1/1

● DG-32



● DG-40A



Applicable ICs

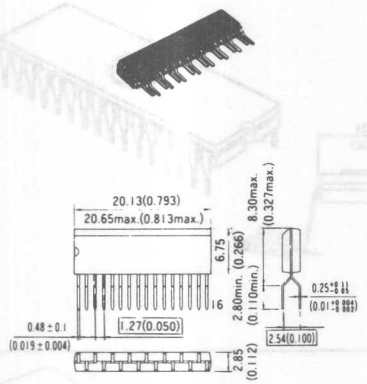
DG-20N	HM10480-15, HM100480-15
DG-22N	HM10490-15, HM100490 Series
DG-24V	HM10500-15
DG-28	HN27128AG Series, HN27256G Series, HN27C256G Series, HN27C256AG Series, HN27C256HG Series, HN27512G Series
DG-28N	HM10494 Series, HM100494 Series
DG-32	HN27C101G Series, HN27C301G Series
DG-40A	HN27C1024HG Series

PACKAGE INFORMATION

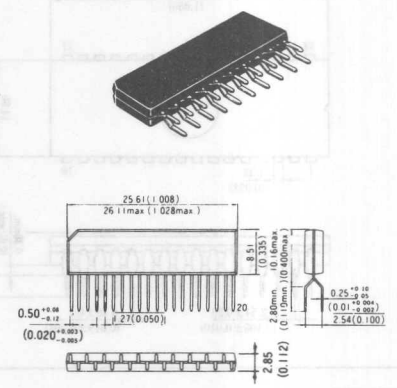
● Zigzag-in-line Plastic

Unit: mm (inch) Scale 1/1

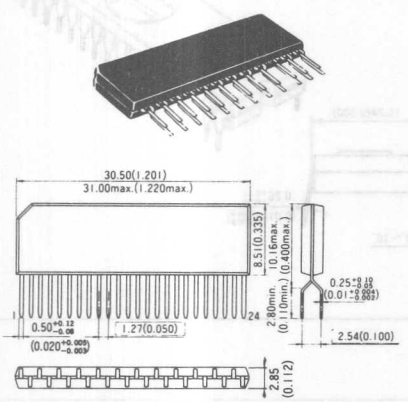
● ZP-16



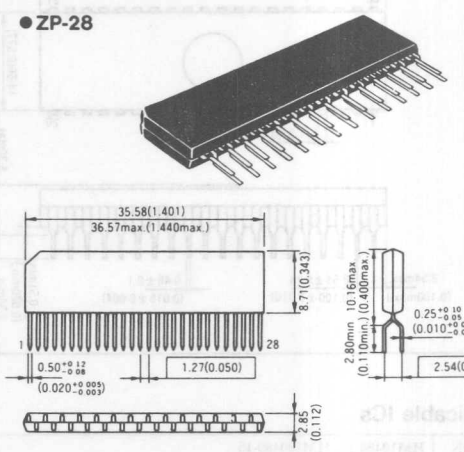
● ZP-20



● ZP-24



● ZP-28



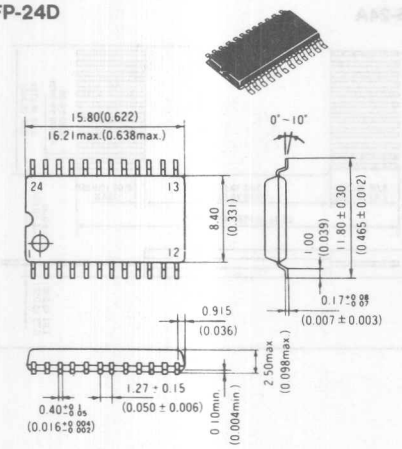
Applicable ICs

ZP-16	HM50256ZP Series, HM50257ZP Series, HM51256ZP Series, HM51256LZP Series
ZP-20	HM514256ZP Series, HM514256AZP Series, HM514256SZP Series, HM514256HZP Series, HM514258AZP Series HM514258SZP Series, HM511000AZP Series, HM511000SZP Series, HM511000HZP Series, HM511001AZP Series, HM511001SZP Series, HM511002AZP Series, HM511002SZP Series
ZP-24	HM53461ZP Series, HM53462ZP Series
ZP-28	HM534251ZP Series, HM534252ZP Series, HM534253ZP Series

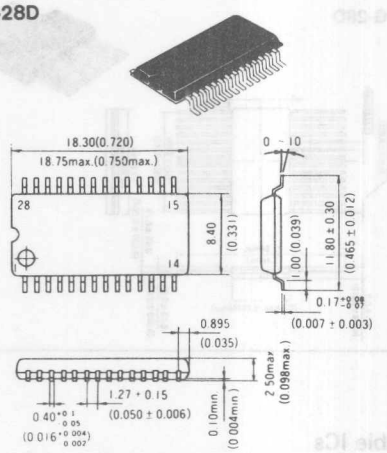
● Flat Package

Unit mm (inch) Scale 1½

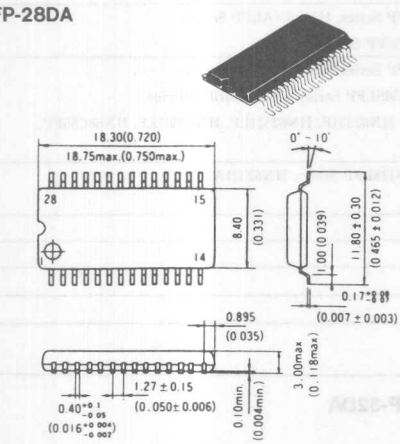
● FP-24D



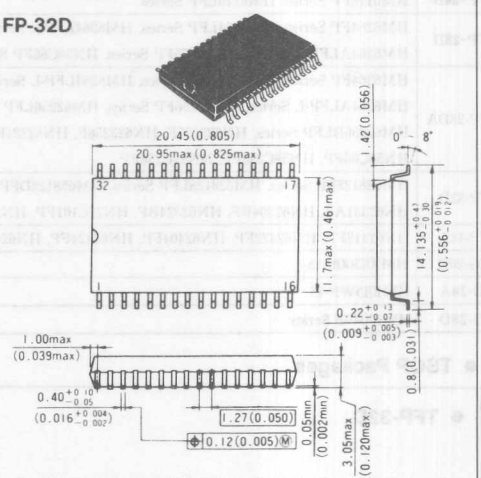
● FP-28D



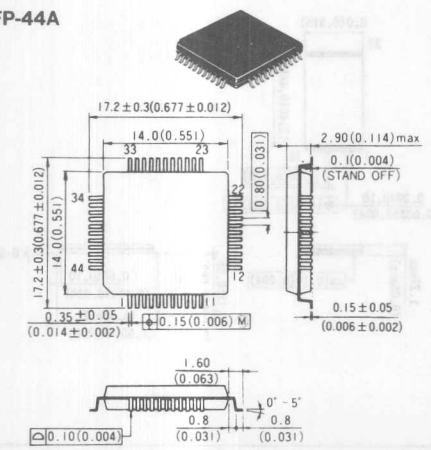
● FP-28DA



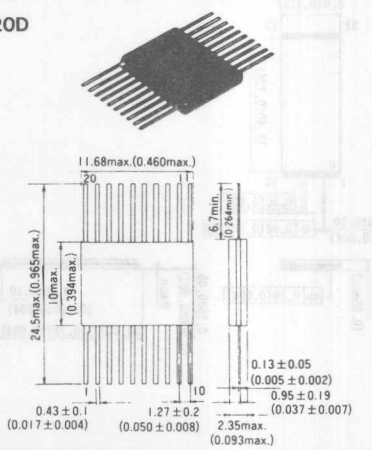
● FP-32D



● FP-44A

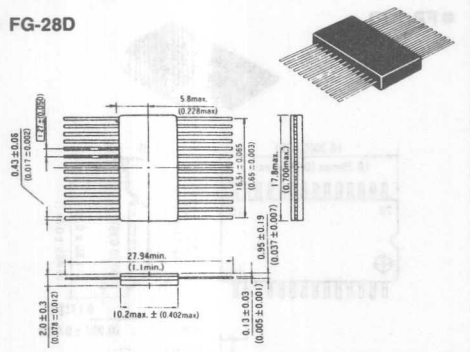


● FG-20D

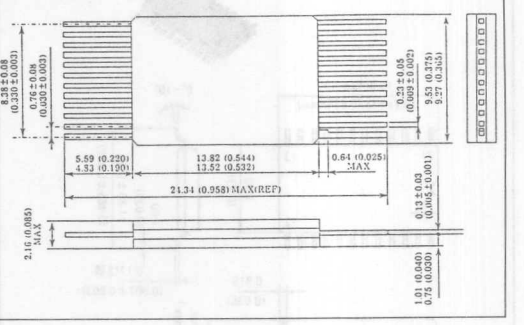


● Flat Packages (continued)

● FG-28D



● FG-24A

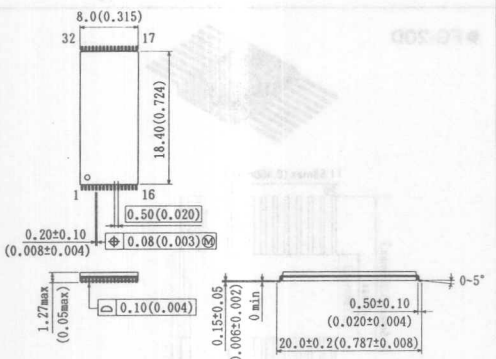


Applicable ICs

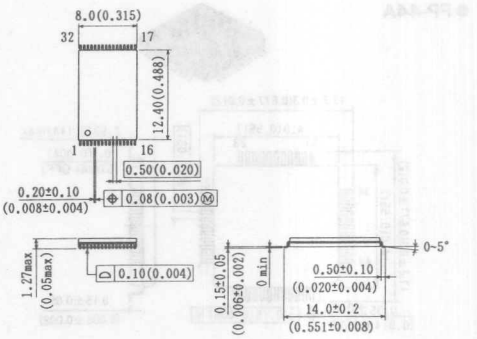
FP-24D	HM6116FP Series, HM6116LFP Series
FP-28D	HM6264FP Series, HM6264LFP Series, HM6264LFP-L Series, HM6264AFP Series, HM6264ALFP Series HM6264ALFP-L Series, HN58C65FP Series, HN58C66FP Series, HN58C256FP Series
FP-28DA	HM6264FP Series, HM6264LFP Series, HM6264LFP-L Series, HM6264AFP Series, HM6264ALFP Series HM6264ALFP-L Series, HM62256FP Series, HM62256LFP Series, HM62256SLFP Series, HM65256BFP Series, HM65256BLFP Series, HN623257F, HN623258F, HN62321F, HN62321BF, HN62331F, HN62321EF, HN62331EF, HN58C65FP, HN58C66FP, HN58C256FP, HN27C256FP
FP-32D	HM628128FP Series, HM628128LFP Series, HM658128DFP Series, HM658128LFP Series, HN62321AF, HN62331AF, HN62304BF, HN62324BF, HN27C101FP, HN27C301FP
FP-44A	HN62412FP, HN62422FP, HN62404FP, HN62424FP, HN62408FP
FG-20D	HM101500F-15
FG-24A	HM1015WF-15
FG-28D	HM10049F Series

● TSOP Packages

● TFP-32D

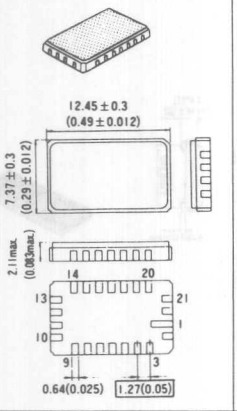


● TFP-32DA

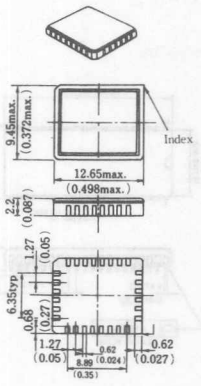


● Leadless Chip Carrier

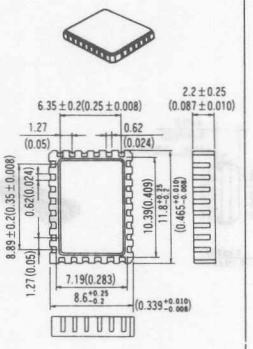
● CG-22A



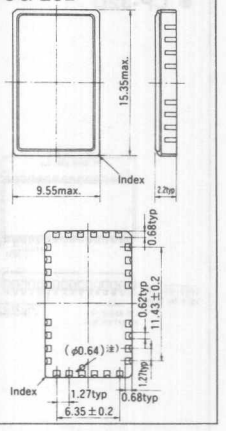
● CG-28



● CG-28A

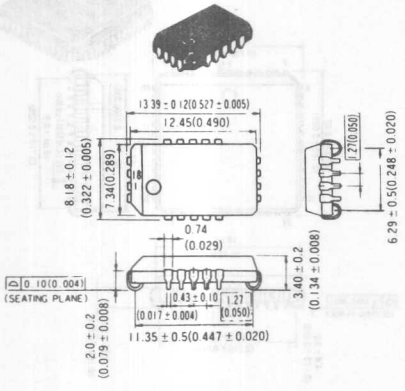


● CG-28B

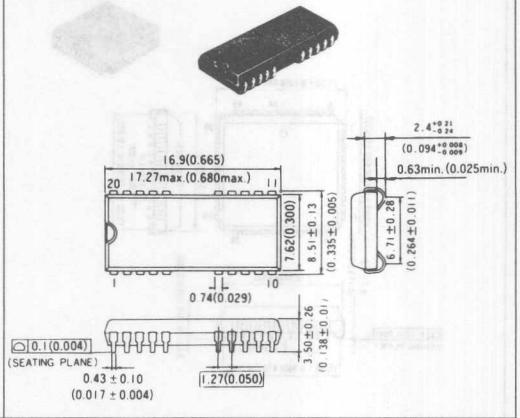


● Flat Package (J-bend Leads)

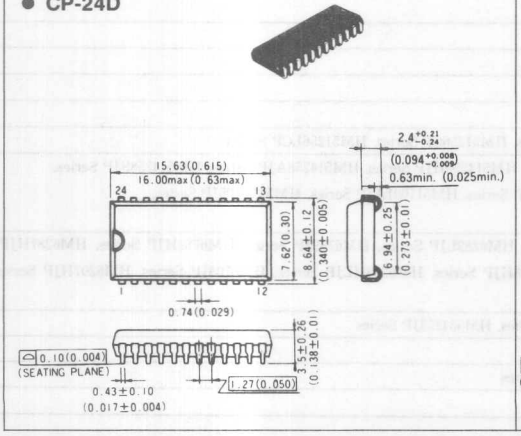
● CP-18



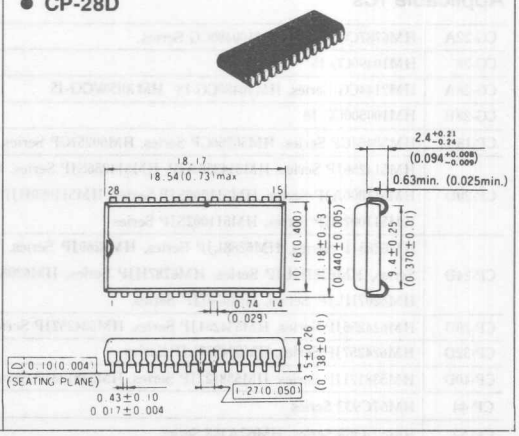
● CP-20D



● CP-24D



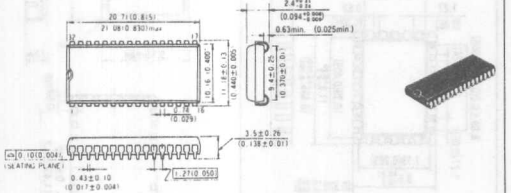
● CP-28D



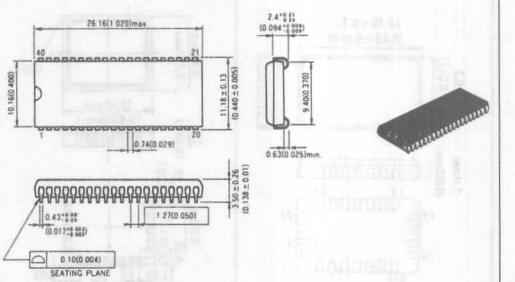
● Flat Packages (J-Bend Leads) (continued)

Unit: mm (inch) Scale 1½

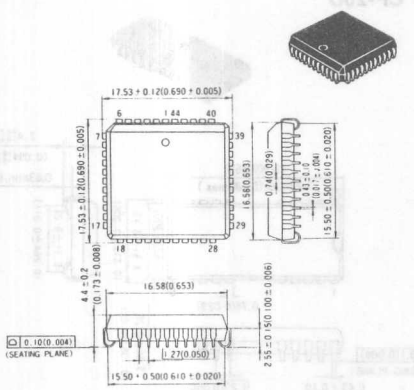
● CP-32D



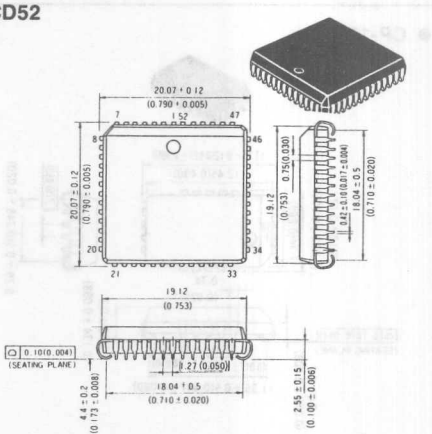
● CP-40D



● CP-44



● CD52



Applicable ICs

CG-22A	HM6787CG Series, HM100490CG Series
CG-28	HM10490CG-15
CG-28A	HM2144CG Series, HM10480CG-13 HM1015WCG-15
CG-28B	HM100500CG-18
CP-18	HM50464CP Series, HM50256CP Series, HM50257CP Series, HM51256CP Series, HM51256LCP Series
CP-20D	HM514256JP Series, HM514256AJP, HM514256SJP Series, HM514256HJP Series, HM514258AJP Series, HM514258SJP Series, HM511000AJP Series, HM511000SJP Series, HM511000HJP Series, HM511001AJP Series, HM511001SJP Series, HM511002AJP Series, HM511002SJP Series
CP-24D	HM6288JP Series, HM6288LJP Series, HM6289JP Series, HM6289LJP Series, HM6789JP Series, HM6789HJP Series, HM6287HJP Series, HM6287HLJP Series, HM6787HJP Series, HM6208HJP Series, HM6208HLJP Series, HM6708JP Series, HM6207HJP Series, HM6207HLJP Series, HM6707JP Series,
CP-28D	HM624256JP Series, HM534251JP Series, HM534252JP Series, HM534253JP Series
CP-32D	HM624257JP Series, HM624257LJP Series
CP-40D	HM538121JP Series, HM538122JP Series, HM538123JP Series
CP-44	HM67C932 Series
CP-52	HM62A168 Series, HM62A188 Series

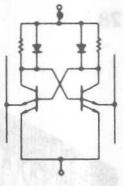
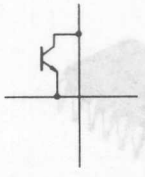
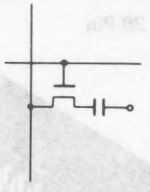
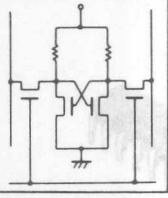
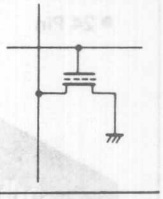
■ RELIABILITY OF HITACHI IC MEMORIES

1. STRUCTURE

IC memories are basically classified into bipolar type and MOS type and utilized effectively by their characteristics. The characteristic of bipolar memories is high speed but small capacity, instead, MOS memories have large capacity. There are also differences in circuit design, layout pattern, degree of integration, and manufacturing process. These memories have been produced with the standardized concept of design and inspection all through the processes of designing, manufacturing and inspection.

IC memories are constituted by the unit patterns called cells, which are integrated in high density. The knowhows based on our experience have been applied in every production stage. In addition, reliability has been ensured using TEG (Test Element Group) evaluation. Examples of cell circuits of bipolar and MOS memories are shown in Table 1.

● **Table 1 Basic Cell Circuit of IC Memories**

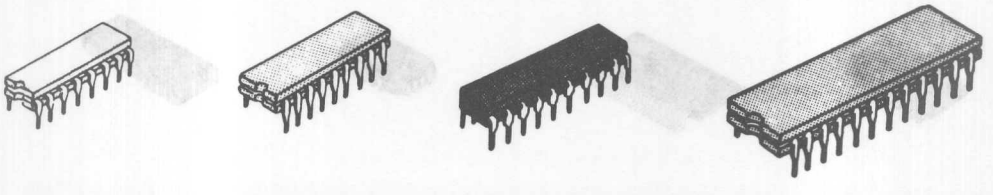
Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

Dies of IC memories are produced in various packages. In this process of packaging, Hitachi has also innovated new techniques and ensured to high level. As packages for IC memories, cerdip (glass-sealed) packages and plastic packages are currently used. Also such packages as LCC (Leadless Chip Carrier) or SOP (Small Outline Package) have been developed for high density packaging. Cerdip packages sealed hermetically are suitable for equipment requiring high reliability. Plastic packages are widely applied to many kinds of equipment. Hitachi plastic packages have been improved the reliability level as highly as that of the hermetically sealed packages. Table 2 shows the outlines of the Hitachi packages.

● **Table 2 IC Memory Package Outline**

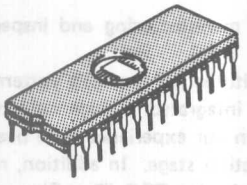
■ Cerdip

● 16 pin ● 18 Pin ● 20 Pin ● 24 Pin

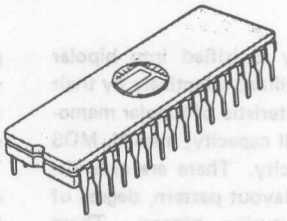


■ Cerdip (continued)

● 28 Pin with Lid

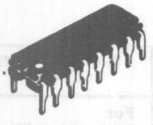


● 32 Pin with Lid

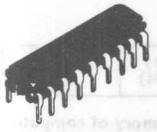


■ Plastic DIP

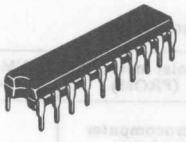
● 16 Pin



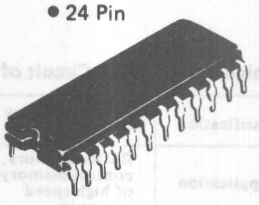
● 18 Pin



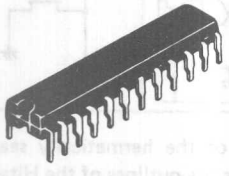
● 20 Pin



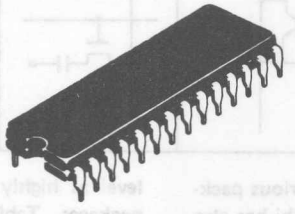
● 24 Pin



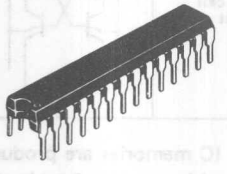
● 24 Pin



● 28 Pin

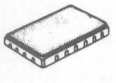


● 28 Pin

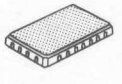


■ Leadless Chip Carrier

● 20 Pin



● 22 Pin



● 24 Pin

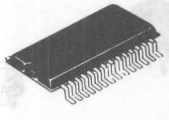


■ SOP

● 24 Pin

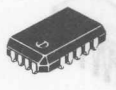


● 28/32 Pin



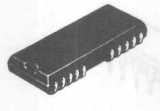
■ PLCC

● 18 Pin



■ SOJ

● 20/26/28/32 Pin



2. RELIABILITY

Results of reliability tests are listed below.

2.1 Reliability Test Data on Bipolar Memories

The reliability test data on the bipolar memories are shown in Table 3 and 4. Since they are manufactured under the standardized design rules and quality control, there is no difference in reliability among the various types. And the larger the capacity is, the higher the reliability per bit becomes.

● Table 3 Results on Bipolar Memory Reliability Test (1)

Test item	HM10480-15					HM2144CG				
	Test condition	Samples	Total component hours	Failures	Failure rate* (1/hr)	Test condition	Samples	Total component hours	Failures	Failure rate* (1/hr)
High-temperature (Operating)	T_a=125°C V_{EE}=–5.2V	340	C.H. 3.4×10^5	0	1/h 2.7×10^{-6}	T_a=125°C V_{EE}=–5.2V	120	C.H. 1.2×10^5	0	1/h 7.7×10^{-6}
High-temp storage	T_a=200°C	351	3.51×10^5	0	2.6×10^{-5}	T_a=200°C	120	1.2×10^5	0	7.7×10^{-6}

* Confidence level 60%

● Table 4 Results on Bipolar Memory Reliability Test (2)

Test item	Test condition	HM10480-15		HM2144CG	
		Samples	Failure	Samples	Failures
Temperature cycling	–55°C to +150°C, 10 cycle	160	0	180	0
Soldering heat	260°C, 10 seconds	35	0	22	0
Thermal shock	0°C to +100°C, 10 cycles	50	0	50	0
Mechanical shock	1500G, 0.5ms, Three times each for X, Y and Z	30	0	22	0
Variable frequency	100 to 200 Hz, 20G, Three times each for X, Y and Z	40	0	22	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	22	0

2.2 Reliability test data on Hi-BiCMOS memory

Hi-BiCMOS memory is newly designed based on the latest fine machining technologies (2m ~ 1m), which features low electric consumption / high integrity by CMOS and high speed / high drivability by bipolar. This device also attains high speed close to ECL and low electric consumption as CMOS. Input and output level supports both ECL and TTL. Reliability test data of HM100490-15 (64k-words x 1-bit) and HM6788P-25 (16k-words x 4-bits) are listed in table 5 and table 6.

The above shows the sufficient reliability of high speed Hi-BiCMOS in the normal use with some limitations considered from its own circuit composition. For further information, see each data sheet. Besides the caution points with CMOS and bipolar device, avoid abnormal use as in deformed or slow wave form which causes malfunction and latch up.

Table 5 Results on Hi-BiCMOS Memory Reliability Test (1)

Test item	HM100490-15 (Cerdip)					Test item	HM6788P-25 (Plastic)					Remarks
	Test condition	Samples	Total test time	Failures	Failure rate		Test condition	Samples	Test test time	Failures	Failure rate	
High-temperature pulse operation	Ta = 125°C V_{EE}=–4.5V	380	C.H. 3.8×10^5	0	1/h 2.4×10^{-6}	High-temperature pulse operation	Ta = 125°C V_{CC} = 5.0V	420	C.H. 4.2×10^5	1*1	1/h 4.8×10^{-6}	*1 foreign matter
						Moisture endurance	85°C 85%RH 5V	210	2.1×10^5	0	4.8×10^{-6}	
High-temp. storage	Ta=200°C	330	3.3×10^5	0	3.0×10^{-6}	Pressure cooker	121°C100%RH	80	0.16×10^5	0	6.3×10^{-5}	

Table 6 Results on Hi-BiCMOS Memory Reliability Test (2)

Test item	Test condition	HM100490-15 (Cerdip)		HM6788P-25 (Plastic)	
		Samples	Failure	Samples	Failure
Temperature cycling	−55°C ~ −150°C 100 cycles	180	0	180	0
Soldering heat	250°C 10 seconds	22	0	22	0
Thermal shock	0°C ~ 100°C 10 cycles	50	0	50	0
Mechanical shock	1500G, 0.5ms Three times each for X, Y and Z	22	0	–	–
Variable frequency	100 ~ 200Hz, 20G Three times each for X, Y and Z	22	0	–	–
Constant acceleration	20000G, 1 minute, each for X, Y and Z	22	0	–	–

2.3 Reliability test data on MOS memories

2.3.1 Reliability test data on MOS DRAM and SRAM

Table 7 and table 8 shows the reliability test data on the representative types of 1M DRAM (HM511000/ HM514256), 256k SRAM (HM62256) 1M SRAM (HM628128FP).

The life test is performed at high temperature and high voltage to evaluate the reliability of products using fewer samples. All failures are caused in manufacturing process, so we feedback the data into manufacturing process to improve the quality and reliability.

- **Table 7 Reliability Data on 1M DRAM**

Test item	Test condition	HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	125°C/5.5V	300	6.00×10^{5}	0	1.53×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	
	125°C/7V	1252	4.50×10^{5}	1*	4.48×10^{-6}	3186	9.34×10^{5}	0	9.85×10^{-7}	
	150°C/7V	200	4.00×10^{5}	0	2.30×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	*1 Oxide film Failure ×1
Moisture endurance	85°C 85% RH 5.5V	420	8.40×10^{5}	0	1.10×10^{-6}	682	1.36×10^{6}	0	6.74×10^{-7}	
Pressure cooker	121°C/100% RH	150	4.50×10^{4}	0	2.04×10^{-5}	200	6.00×10^{4}	0	1.53×10^{-5}	

* Confidence level 60%

- **Table 8. Reliability Data on 256K and 1M SRAM**

Test item	Test condition	HM62256FP (SOP)				HM628128FP (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	125°C/5.5V	3088	3.11×10^{6}	0	8.88×10^{-7}	1038	1.04×10^{6}	0	8.86×10^{-7}	
	125°C/7V	455	4.55×10^{5}	0	2.02×10^{-6}	951	5.33×10^{5}	1*1	3.79×10^{-6}	*1 Foreign x 2
	150°C/7V	103	1.00×10^{5}	1*1	2.02×10^{-5}	80	1.60×10^{5}	0	5.75×10^{-6}	
Moisture endurance	85°C/85% RH 7V	680	6.80×10^{5}	0	1.35×10^{-6}	127	2.54×10^{5}	0	3.62×10^{-6}	*2 Leak x 1
Pressure cooker	121°C/100% RH	320	6.40×10^{4}	1*2	3.16×10^{-5}	90	2.70×10^{4}	0	3.41×10^{-5}	

* Confidence level 60%

2.3.2 Reliability Test Data on EPROM

EPROM has two types; conventional EPROM with transparent window and one time programmable ROM (OTPROM) packaged in plastic package. Table 9 shows reliability test data on the representative EPROM types 512k EPROM (HN27512, HN27512P), 1M EPROM (HN27C101, HN27C301).

● **Table 9. Reliability Data on 512K and 1M EPROM**

Test item	Test condition	HN27512 (Cerdip/Plastic)				HN27C101/HN27C301				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature operation	125°C/5.5V	200	3.72×10^5	0	2.47×10^{-6}	180	3.24×10^5	0	2.84×10^{-6}	*1 Data dissipation x 49
	125°C/7V	530	7.95×10^5	0	1.16×10^{-6}	327	6.54×10^5	0	1.41×10^{-6}	
High-temperature bake	175°C	260	4.91×10^5	0	1.87×10^{-6}	150	7.5×10^5	0	1.23×10^{-6}	
	200°C	240	3.72×10^5	1*1	5.43×10^{-6}	130	6.49×10^5	1*1	3.11×10^{-6}	
	250°C	180	1.89×10^5	7*1	4.44×10^{-5}	110	3.07×10^5	40*1	1.30×40^{-4}	
Moisture endurance	85°C/85% RH 5.5V	290	5.22×10^5	0	1.76×10^{-6}	–	–	–	–	Data of 512K OTPROM
Pressure cooker	121°C/100% RH	50	0.10×10^5	0	9.20×10^{-5}	–	–	–	–	

* Confidence level 60%.

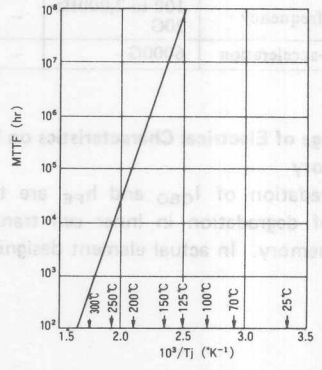
The failure shown in table 9 is due to the data dissipation in memory cells. Getting thermal energy, electrons in memory cells are activated and go through the floating gate. In actual usage, however, it has no problem because this phenomenon dependes on temperature (about 1.0eV of activated energy) greatly. The moisture resistance of OTPROM is also satisfactory.

Table 10 shows the example of PROM derating. When derating, the parameter is generally only the temperature because other operating conditions are specified. Especially to lower the junction temperature during mounting is important for stabilizing the operation relative to access time, refresh time and other characteristics.

● **Table 10 Example of HN27C101/HN27C301 Derating**

Factor	Temperature
Failure criteria	Electrical Characteristics, Function Test
Failure mechanism	Increase of leak current and others

Results:
The result from high temperature baking of PROM is shown in the right figure.



Note: Decreasing junction temperature shown in the figure will promise the higher reliability. The junction temperature can be calculated by a formula : $T_j = T_a + \theta_{ja} \cdot P_d$ θ_{ja} in about 100°C/W with no air flow and about 60 to 70°C/W with 2.5 m/s air flow.

2.3.3 Reliability Data on MASK ROM

Table 9 shows the reliability test data on 2M and 4M bit MASK ROM. MASK ROM is patterned according to ROM information in manufacturing process, so data dissipation isn't occurred in high temperature like EPROM and EEPROM.

● **Table 11. Reliability Data on 2M and 4M MASK ROM**

Test item	Test condition	HN62412P (Plastic)				HN62404P (Plastic)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temp. pulse operaton	125°C/5.5V	–	–	–	–	200	4.0×10^{5}	0	2.3×10^{-6}	
	125°C/7V	120	1.2×10^{5}	0	7.67×10^{-6}	300	3.0×10^{5}	0	3.0×10^{-6}	
Moisture endurance	85°C/85% RH 5.5V	120	1.2×10^{5}	0	7.67×10^{-6}	120	1.20×10^{5}	0	7.67×10^{-6}	
Pressure cooker	121°C/ 100% RH	45	2.3×10^{4}	0	4.1×10^{-5}	45	2.3×10^{4}	0	4.1×10^{-5}	

* Confidence level 60%.

2.3.4 Reliability Data on MOS Memory (The result of environment test)

Table 12 shows examples of each environment test data. They show good results without any failure even in severe environment.

V_{TH} of MOS transistor is one of the basic process parameters in MOS memory, which has almost no change using surface stabilization technology and clean process. Figure 4 shows the examples of time changes for 1M DRAM; V_{DD} min. (V_{min}) and access time (t_{RAC}) in high temperature pulse test.

● **Table 12 Reliability Data on MOS Memories**

Test item	Test condition	HM511000P (DIP)		HM511000JP (SOJ)		HM62256FP (SOP)		HM628128FP (SOP)		EPROM (Cerdip)		Remarks
		Samples	Failure	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	–55°C to 150°C 10 cycle	3755	0	2786	0	3328	0	710	0	2790	0	
Temperature cycling	–55°C to 150°C 500 cycle	150	0	200	0	482	0	105	0	450	0	
Thermal shock	–65°C to 150°C 15 cycle	77	0	100	0	76	0	77	0	80	0	
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	22	0	22	0	
Mechanical shock	1,500G, 0.5ms	–	–	–	–	–	–	–	–	38	0	
Variable frequency	100 to 2,000Hz 20G	–	–	–	–	–	–	–	–	38	0	
Constant-acceleration	6000G	–	–	–	–	–	–	–	–	38	0	*6,000G

2.4 Change of Electrical Characteristics on IC Memory

The degradation of I_{CBO} and h_{FE} are the main factors of degradation in inner cell transistor of bipolar memory. In actual element designing, however, it is designed to operate in the range at which no degradation happen. Therefore no change of characteristics including access time are observed. Time dependence in access time for HM10470 are shown in Fig. 1.

Figure 1 Time change in access time for bipolar memory

Example	
Device name	HM10480-15
Test condition	Ta = 125°C, V_{EE} = –5.2V
Failure criteria	t_{AA} = 15ns
Failure mechanism	Surface degration

Results:
Access time is stabilized.

Example of time change in access time for Bipolar memory

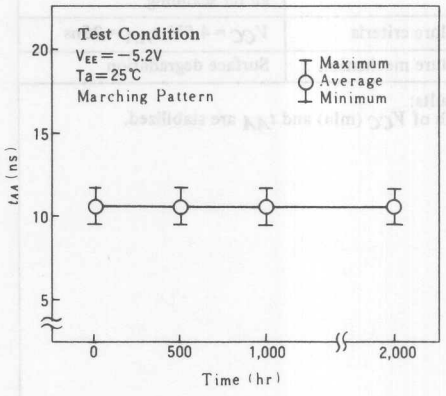


Figure 2 Time change in access time for Hi-BiCMOS memory

Example	
Device name	HM100490
Test condition	Ta = 125°C, V_{EE} = –4.5V all bit scanning
Failure criteria	t_{AA} = 15ns
Failure mechanism	Surface degradation

Results:
Access time is stabilized.

Example of time change in access time for Hi-Bi CMOS memory

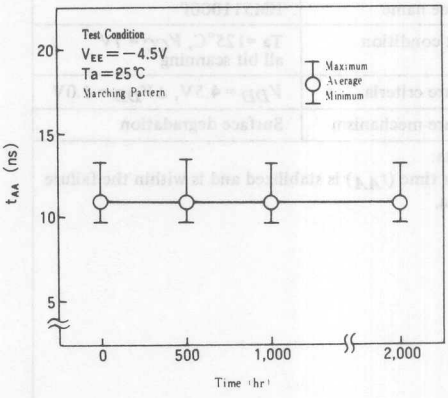
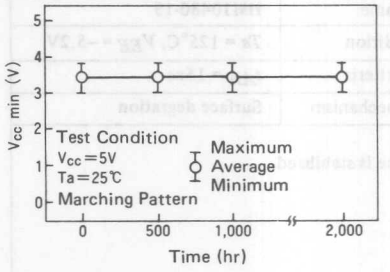


Figure 3 Time change in V_{CC} min and t_{AA} for Hi-BiCMOS memory

Example	
Device name	HM6788P-25
Test condition	Ta = 125°C, V_{CC} = 5.0V all bit scanning
Failure criteria	V_{CC} = 4.5V, t_{AA} = 25ns
Failure mechanism	Surface degradation

Results:
Both of V_{CC} (min) and t_{AA} are stabilized.

Examples of time change in V_{CC} min and t_{AA} for Hi-Bi CMOS memory



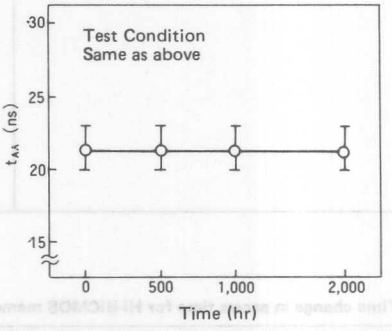


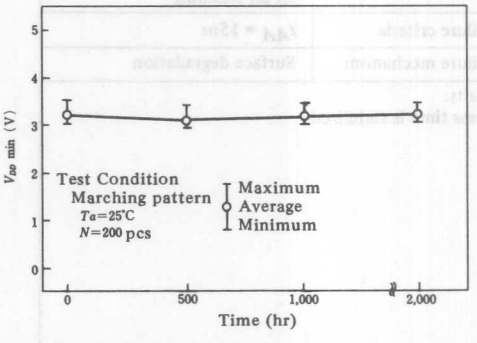
Figure 4 Time change in V_{DD} min and t_{RAC} for MOS memory

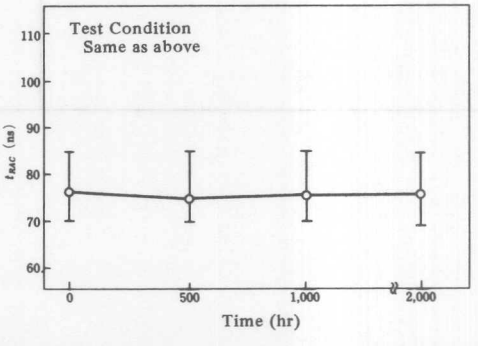
Example	
Device name	HM511000P
Test condition	Ta =125°C, V_{CC} = 7V all bit scanning
Failure criteria	V_{DD} = 4.5V, ΔV_{DD} = 1.0V
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Note: Test accuracy is 0.2V, 2ns.

Example of time change in V_{DD} min and t_{RAC} for MOS memory





2.5 Failure Mode Rate

Figure 5 and 6 show examples of failure mode happened in users' application. Since IC memories require the finest pattern process technology, the percentage of failures, such as pinholes, defects on photoresist and foreign materials, tends to increase. To eliminate the defects in the manufacturing process, Hitachi has improved the process and performed 100% burn in screening under high temperature. Hitachi has been collecting and checking customers' process-data and marketing data for higher reliability of our products. To analyze them is very helpful for the improvement of designing and manufacturing.

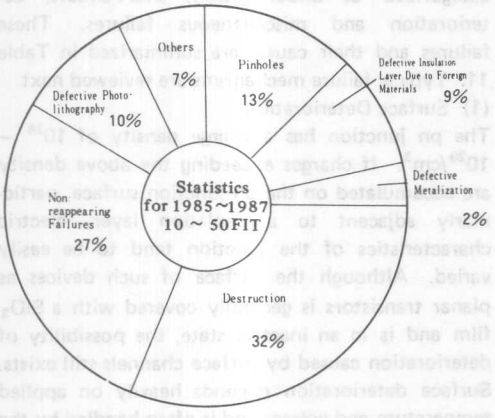


Figure 5 Failure Mode Rate of Bipolar Memory

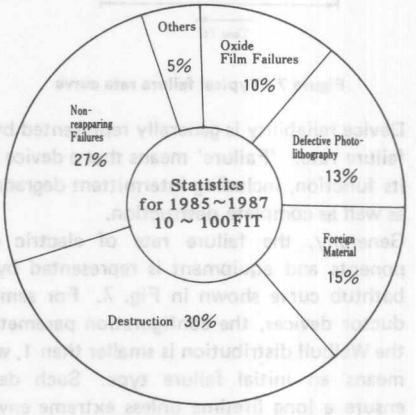


Figure 6 Failure Mode Rate of MOS Memory

3. Reliability of Semiconductor Devices

3.1. Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along proper environmental conditions. This section describes reliability characteristics, failure types and their mechanisms in terms of devices. First, semiconductor device characteristics are examined in light of their reliability.

(1) Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.

(2) Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

(3) Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.

(4) Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data cannot be used in some cases.

(5) Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.

(6) Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should be also reviewed when electrode and package materials are not suited for particular environmental conditions.

(7) Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

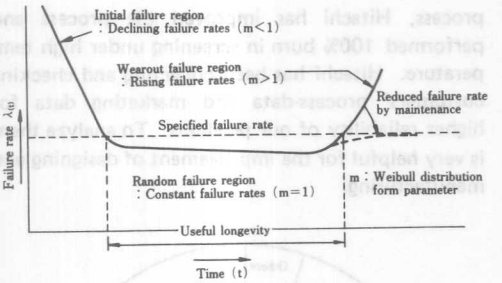


Figure 7 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Fig. 7. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering". It is used to examine the physical mechanism of failures in terms of atoms and molecules to improve device reliability. This physical approach was introduced to the reliability field with the demand for minimized development cost and period, as technology rapidly developed and system performance increased, requiring more complex and higher levels of reliability. These conditions derived from the development of solid state physics (semiconductor physics) after World War II and associated device development.

Failure physics have been employed to:

1) Detect failed devices as soon as possible
2) Establish models and equation used for failure prediction
3) Evaluate reliability in short periods by accelerated life test

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage and usage by adding physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure types and their mechanism

Device failures are physically discussed in this section. Semiconductor device failures are basically categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These failures and their causes are summarized in Table 11. Typical failure mechanisms are reviewed next.

(1) Surface Deterioration

The pn junction has a charge density of 10^{14} – $10^{20}/cm^3$. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electric characteristics of the junction tend to be easily varied. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model.

One example of recent failures is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS} by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 2 μm to 0.8 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have employed improved design and process techniques to prevent these problems. However, as process becomes finer, surface deterioration may possibly become a serious problem.

(2) Electrode-related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticeable failures include electromigration and Al wiring corrosion in plastic sealed packages.

① Electromigration

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with current of about scattering electrons, an 'electron wind' is produced. This wind moves the

metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

② Multi-metal line related failures

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

③ Al line corrosion and disconnection

When Plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Fig. 8). Under high-temperature and high-humidity, corrosions are randomly

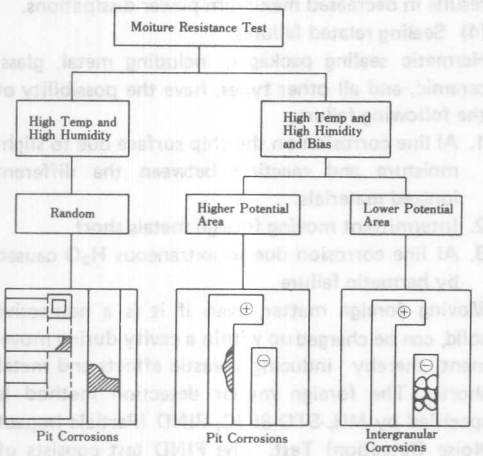


Figure 8 Categorized Al corrosion mode

generated over the element surface. However, after an extended period of time, the corrosions have not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-appllied, high-temperature, high-humidity condition, on the other hand, corrosions are generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Fig. 9.

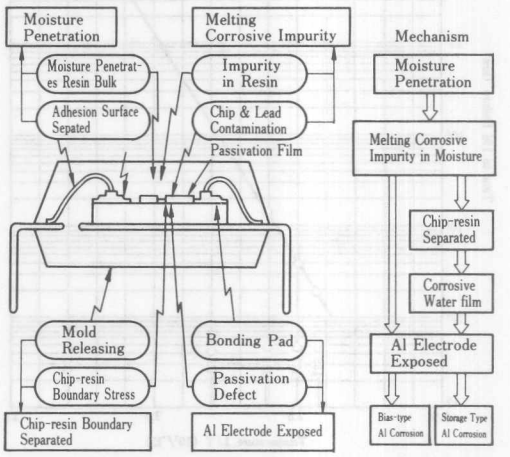


Figure 9 Plastic package cross section and Al corrosion mechanism

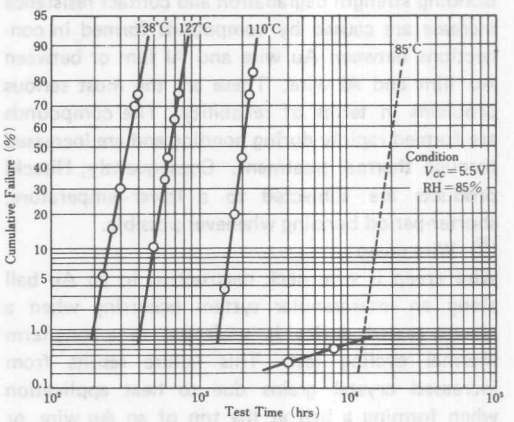


Figure 10 An Example of Moisture Resistance by High temp. and High humidity and bias

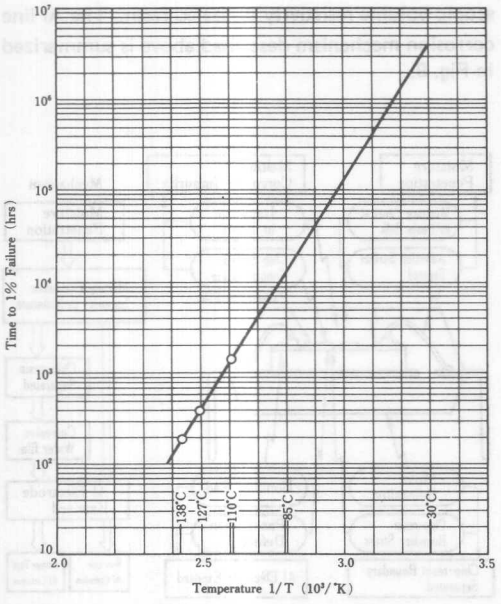


Figure 11 Relationship between temperature and Time to 1% failure (RH = 85%)

(3) Bonding related failures

① Degradation caused by intermetallic formation

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

② Wire creep

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

③ Chip crack

With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

④ Reduced maximum power dissipations

For power devices, heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance. This results in decreased maximum power dissipations.

(4) Sealing related failures

Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short
3. Al line corrosion due to extraneous H_2O caused by hermetic failure

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying.

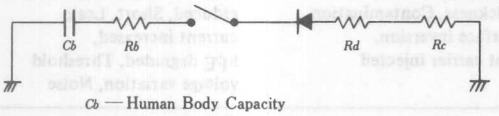
(5) Disturbance

①Electrostatic discharge destruction

Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure; the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 10. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged

with 2000V, the dissipated energy is obtained as follows: With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.



C_b — Human Body Capacity
R_b — Human Body Resistance
R_d — Device Resistance
R_c — Resistance Between Device and Ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$$

Figure 12 Equivalent circuit of human body model

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Fig. 13. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction. 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

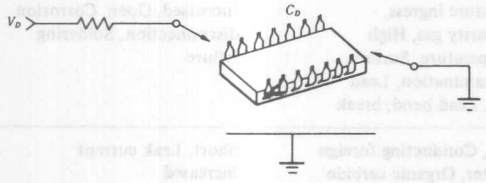


Figure 13 Equivalent circuit of charging model

② Latch up

Latch up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply and noise is applied, or when a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parasitic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is off or the flowing current is forced to be reduced to a certain level. Once latch up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch up. Latch up triggering input or output currents start to flow under the following conditions.

Vin <Vcc or Vin < GND for input level

Vout > Vcc or Vout < GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

③ Soft errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating nodes, causing temporary soft errors. This phenomenon is shown in Fig. 14. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, organic material, PIQ, is applied to the surface of the device.

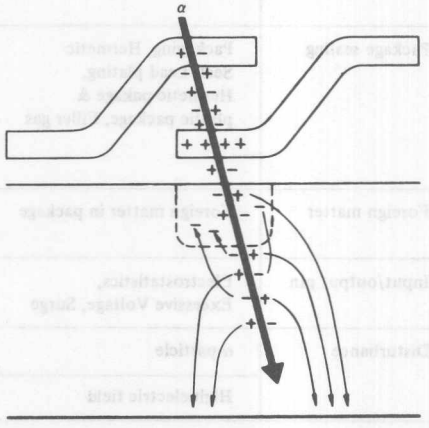


Figure 14 Soft error caused by α particles in dynamic memory

Table 13. Failure causes and mechanism

Failure related causes		Failure mechanisms	Failure modes
Passivation	Surface oxide film, Insulating film between wires	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Withstanding voltage reduced, Short, Leak current increased, h_{FE} degraded, Threshold voltage variation, Noise
Metallization	Interconnection, Contact, Through hole	Flaw, Void, Mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improper thickness, Electromigration, Corrosion	Open, Short, Resistance increased
Connection	Wire bonding, Ball bonding	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Open, Short Resistance increased
Wire lead	Internal connection	Disconnection, Sagging, Short	Open, Short
Diffusion, Junction	Junction diffusion, Isolation	Crystal defect, Crystallized impurity, Photo resist mismatching	Withstanding voltage reduced, Short
Die bonding	Connection between die and package	Peeling chip, Crack	Open, Short, Unstable operation, Thermal resistance increased
Package sealing	Packaging, Hermetic Seal, Lead plating, Hermetic pakage & plastic package, Filler gas	Integrity, moisture ingress, Impurity gas, High temperature, Surface contamination, Lead rust, Lead bend, break	Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure
Foreign matter	Foreign matter in package	Dirt, Conducting foreign matter, Organic carbide	Short, Leak current increased
Input/output pin	Electrostatistics, Excessive Voltage, Surge	Electron destroyed	Short, Open, Fusing
Disturbance	α particle	Electron hole generated	Soft error
	High electric field	Surface inversion	Leak current increased

(6) Fine geometry related problems

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 3 μm → 2 μm → 1.3 μm → 0.8 μm.

However power supply has not been scaled down used for 5V, only line dimensions have been fined increasingly. Problems associated with finer geometry are shown in Table 14.

Table 14. Finer geometry related problems

Item	Problems	Countermeasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

■ QUALITY ASSURANCE OF IC MEMORY

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and their required quality level and also to maintain the satisfied level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the followings;

(1) Establish the reliability in design at the stage of new product development.
(2) Establish the quality at all steps in manufacturing process.
(3) Intensify the inspection and the assurance of reliability of products.
(4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.

With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishment of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate under single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve the reliability based on reliability targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

(1) Design Standardization
Design standardization needs establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability, with the exception of special requirement on function.

(2) Device Design
It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we study the technology prior to development of the device in detail.

(3) Reliability Test by Test Site
Test site is sometimes called Test Pattern. It is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode;
   - Analysis of relation between failure mode and manufacturing process condition.
   - Analysis of failure mechanism.
   - Establishment of QC point in manufacturing.
2. Effects of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.

In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.

The followings are the items to consider at design review.

(1) Describe the products based on specified design documents.
(2) Considering the documents from the standpoint of each participant, plan and execute the subprogram such as calculation, experiments and

investigation if unclear matter is found.

(3) Determine the contents and methods of reliability test based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Arrange the preparation for production.

(6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.

(7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi;

(1) Problems is solved in each process so that even the potential failure factors will be removed at final stage of production.

(2) Feedback of information is made to insure satisfied level of process ability.

As the result, we assure the reliability.

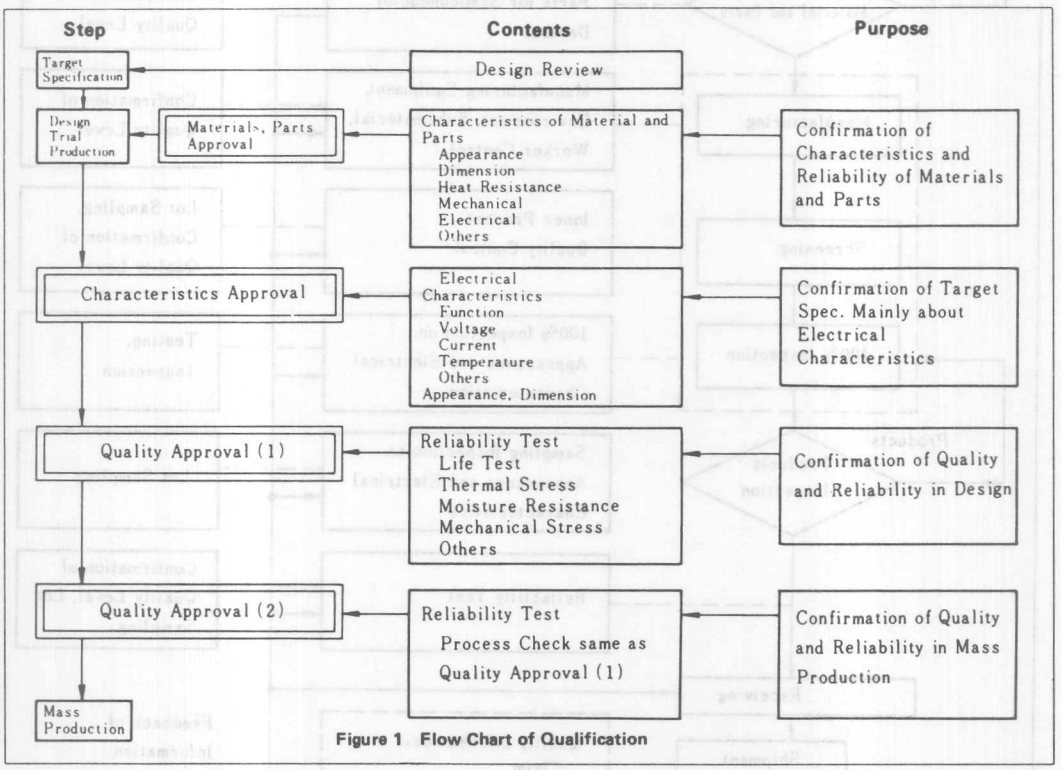


Figure 1 Flow Chart of Qualification

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described in section 2.

The followings are the views on qualification in Hitachi:

(1) From the standpoint of customers, qualify the products objectively by a third party.
(2) Consider the failure experiences and data from customers.
(3) Qualify every change in design and work.
(4) Qualify intensively on parts and materials and process.
(5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Considering the views mentioned above, qualification shown in Fig. 1 is done.

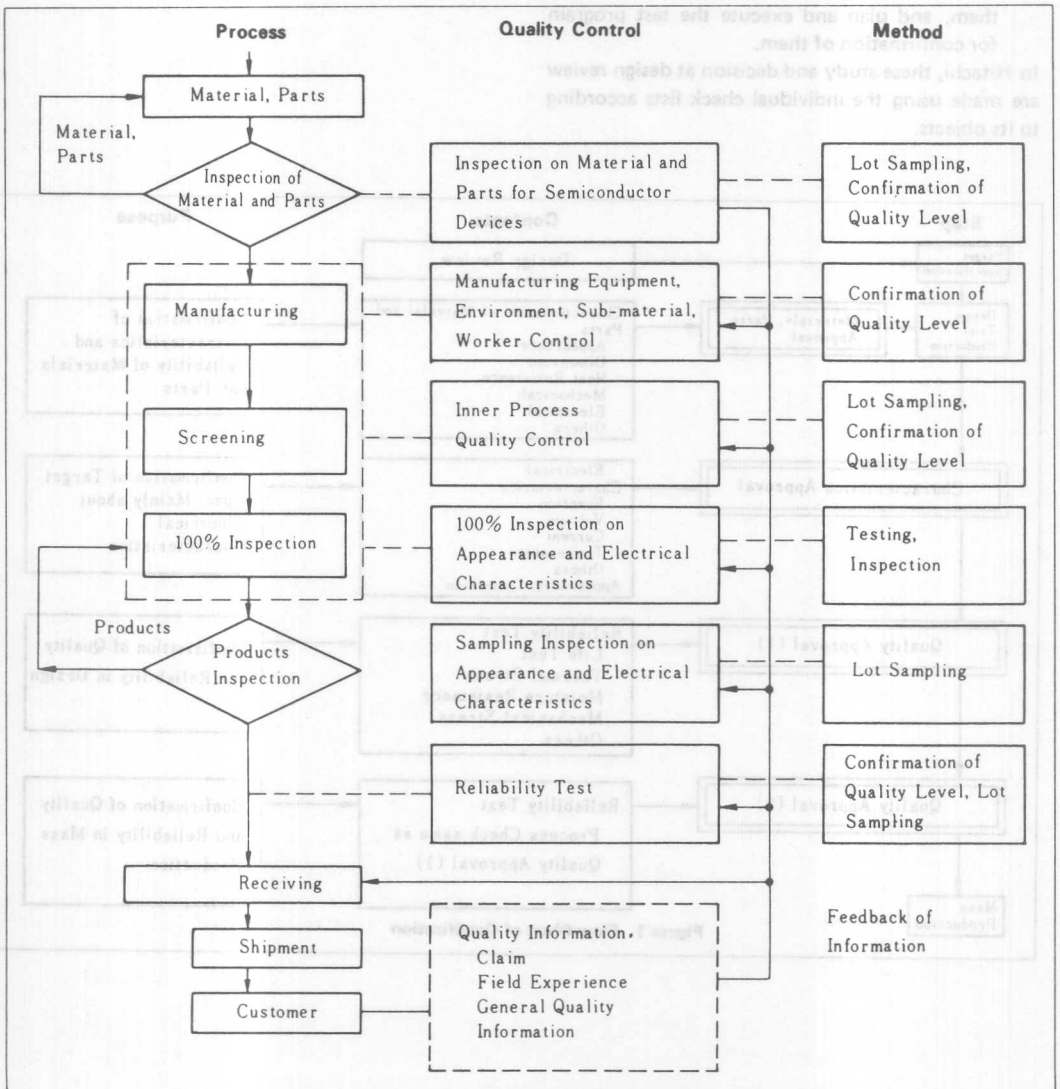


Figure 2 Flow Chart of Quality Control in Manufacturing Process

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3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Fig. 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The items such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D.

The other activities for quality assurance are as follows.

- **Table 1. Quality Control Check Points of Parts and Material (example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

(1) Technology Meeting with Vendors
(2) Approval and Guidance of Vendors
(3) Analysis and tests of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Fig. 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling. Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted produsts.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed with the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-material.

Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

Process	Control Point		Purpose of Control
▽Purchase of Material			
Wafer			
○Surface Oxidation	Oxidation		Assurance of Resistance
○Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
○Photo Resist	Photo Resist		
○Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇PQC Level Check			Check of Photo Resist
○Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
○Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc)
◇PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
○Evaporation	Evapo-ration	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
○Inspection on Evaporation			
◇PQC Level Check			
○Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
○Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
○Chip Scribe		Appearance of Chip	
○Inspection on Chip Appearance			
◇PQC Lot Judgement			
Frame			
○Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
		Appearance after Wire Bonding	Quality Check of Wire Bonding
◇PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
○Inspection after Assembling		Appearance after Assembling	
◇PQC Lot Judgement			
Package			
○Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇PQC Level Check	Marking	Marking Strength	
○Final Electrical Inspection			
◇Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
○Appearance Inspection			
△Sampling Inspection on Products			
○Receiving			
Shipment			

Figure 3 Example of Inner Process Quality Control

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3.3.3 Final Tests and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake.

The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

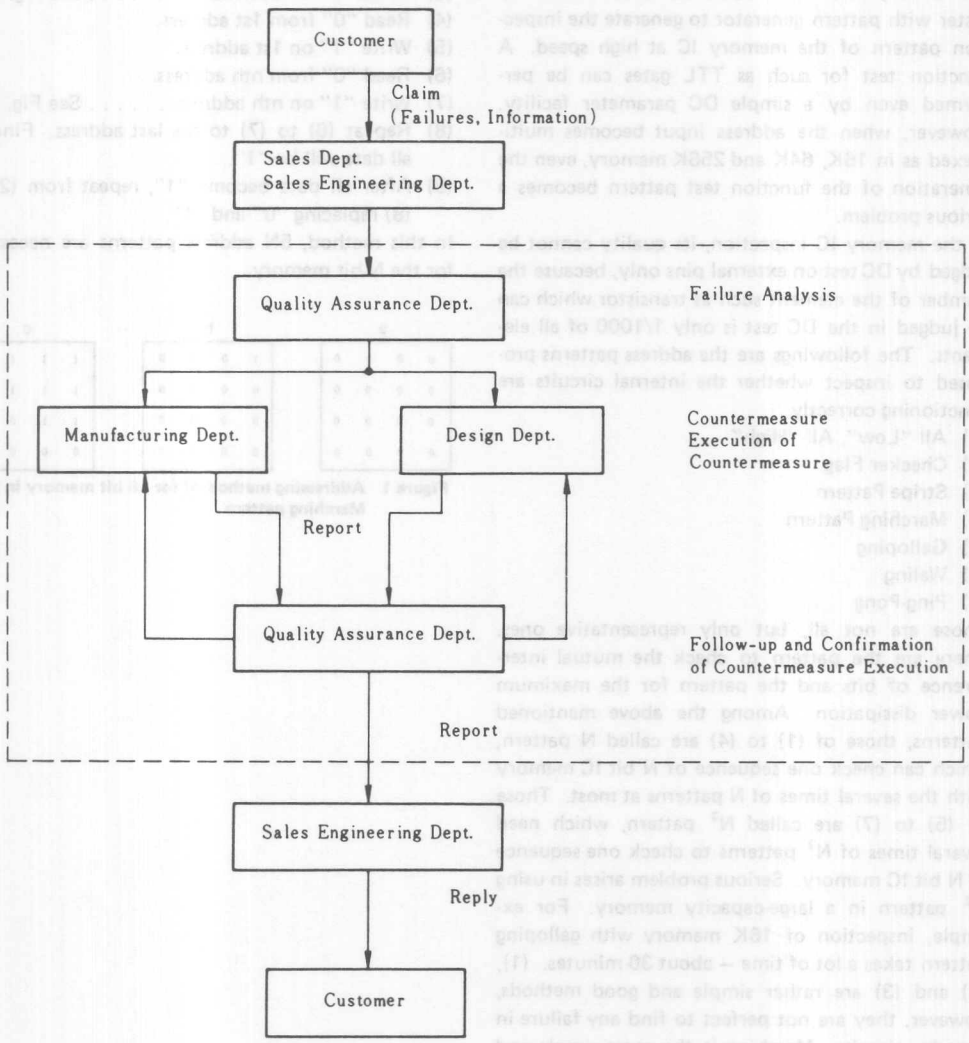


Figure 4 Process Flow Chart of Coping with Failure to a Customer

■ OUTLINE OF TESTING METHOD

1. INSPECTION METHOD

Compared to conventional core memories, IC memories contain all peripheral circuits, such as the decoder circuit, write circuit and read circuit. As a result, assembly and electrical inspection of ICs are all performed by IC manufacturers. Consequently, as the electrical inspection of IC memories are becoming more systematic, conventional IC inspection facilities are becoming useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a simple DC parameter facility. However, when the address input becomes multiplexed as in 16K, 64K and 256K memory, even the generation of the function test pattern becomes a serious problem.

In the memory IC inspection, its quality cannot be judged by DC test on external pins only, because the number of the element such as transistor which can be judged in the DC test is only 1/1000 of all elements. The followings are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

(1) All "Low", All "High"
(2) Checker Flag
(3) Stripe Pattern
(4) Marching Pattern
(5) Galloping
(6) Waling
(7) Ping-Pong

Those are not all, but only representative ones. There are the pattern to check the mutual interference of bits and the pattern for the maximum power dissipation. Among the above mentioned patterns, those of (1) to (4) are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Those of (5) to (7) are called N^2 pattern, which need several times of N^2 patterns to check one sequence of N bit IC memory. Serious problem arises in using N^2 pattern in a large-capacity memory. For example, inspection of 16K memory with galloping pattern takes a lot of time – about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16 bit memory is described below.

(1) Clear all bits . . . . . See Fig. 1 (a)
(2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
(3) Write "1" on 0th address. . . . . See Fig. 1(b)
(4) Read "0" from 1st address.
(5) Write "1" on 1st address.
(6) Read "0" from nth address.
(7) Write "1" on nth address . . . . . See Fig. 1(c)
(8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
(9) After all data become "1", repeat from (2) to (8) replacing "0" and "1".

In this method, 5N address patterns are necessary for the N-bit memory.

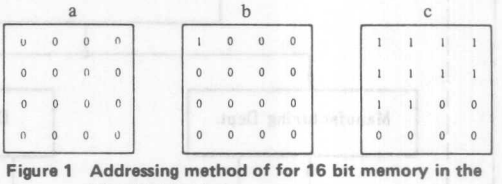


Figure 1 Addressing method of for 16 bit memory in the Marching pattern

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■ APPLICATION

1. Static RAM

1.1. Static RAM Memory Cell

The static RAM memory cell consists of flip-flops organized as 4 NMOS transistors and 2 load resistors as shown in figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

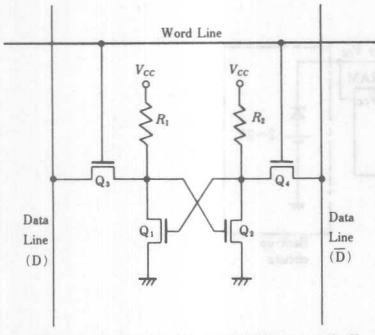


Figure 1-1. Static RAM Memory Cell

1.2. Data Retention Mode and Battery Back-up System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. So, it enables a battery back-up system to retain data during power failure.

Data Retention Mode: The important point in designing a battery back-up system is the timing relation between the memory power supply during the change (ordinal source → battery) and the chip select signal. If the timing for the change is missed, the data in memory might be destroyed.

Figure 1-2. shows the timing for switching the power supply. The following explains the technical terms related to the data retention mode.

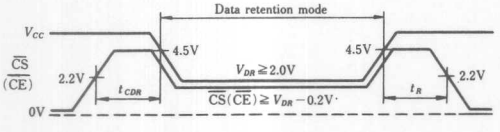


Figure 1-2. Timing for Battery Back-up Application

Data retention mode: The period that the power supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS} = V_{DR} - 0.2V$).

t_{CDR} (time for chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (Operation recovery time): The minimum time needed to change from data retention mode to operating mode. Normally, it is the same as the cycle time of the memory.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally, the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in data retention mode. It depends on memory power supply voltage and ambient temperature. It is specified at supply voltage (V_{DR}) = 3.0 V.

Battery Back-up System: battery back-up sequence is described in the following:

1. External circuit detects failure of system power supply.
2. External circuit changes RAM to standby mode.
3. External circuit separates RAM from system power supply.
4. External circuit switches to Back-up power supply.

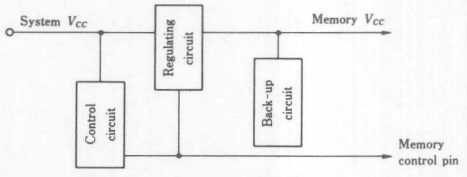


Figure 1-3. Example of Battery Back-up System

The control circuit detects the power failure and cuts off the power after switching memories to standby mode. On recovery, it confirms power supply and after some delay, returns memories to operating mode. The memory control signals depend on the types of memories used in the system.

* Using memory with only one $\overline{CS}$. NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. As the level of $\overline{CS}$ in data retention mode must be higher than V_{DR} − 0.2V, the power supply for this NAND gate must either be shared with the memory power supply, or be pulled up to the memory power supply.
* Using memory with two $\overline{CS}$. Basically, the signals are the same as mentioned above. In general use, two pins should be used for the control signal and the chip select signal respec-

tively. $\overline{CS}$, which can intercept current path of other pins in the input buffers, is for control signal input of data retention mode.

* Using memory with $\overline{CS}$ and CS. As CS selects the chips at high level, it is better to use CS than $\overline{CS}$ as control signal input for data retention mode. As soon as power down is detected, signals should be brought to low level. So a pull-up to the memory power supply level is not needed and circuit organization is simplified.

Figure 1-4 shows an example of a battery back-up system circuit. Hitachi recommends using CMOS logic for gate G_1 in control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch regulating circuit from system power supply to back-up power supply.

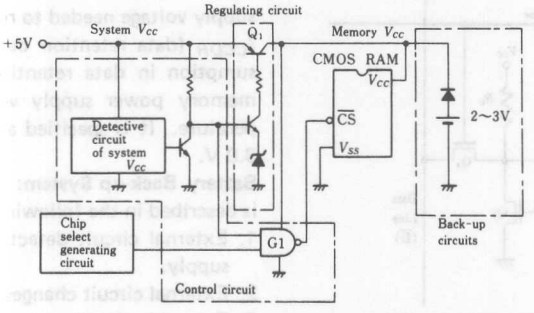


Figure 1-4. Example of Battery Back-up System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

A new type of memory, pseudo-static RAM has been developed providing the advantages of dynamic RAM (low cost, high density), and static RAM (easy usage). IC memory consists of memory cells for data storage, and input/output circuits for interfacing to the external circuits. PSRAM provides the memory cell and peripheral circuits of DRAM and the external control circuits, which includes a part of the refresh control circuits not provided by dynamic RAM, and interface circuits similar to that of static RAM, on a chip, as shown in table 2-1. Address input is not multiplexed and data input/output is byte-wide like standard static RAM. With PSRAM x 8 organization, medium density memory system can be designed easily. PSRAM provides address refresh, automatic refresh and self refresh.

Figure 2-1 shows examples of system design using PSRAM and DRAM. Using PSRAM, the circuits interfacing CPU to DRAM can be drastically reduced.

Figure 2-2 shows block diagram of pseudo static RAM.

Table 2-1. PSRAM Features

	SRAM	PSRAM	DRAM
Memory Cell	4 Tr + 2 R	1 Tr + 1 C	
Organization	x1, x4, x8	x8	x1, x4
Address	Single Address		Multiplexed Address
Refresh	Nor Necessary	Necessary	
External Circuits	Simple ⟺ Complexed		

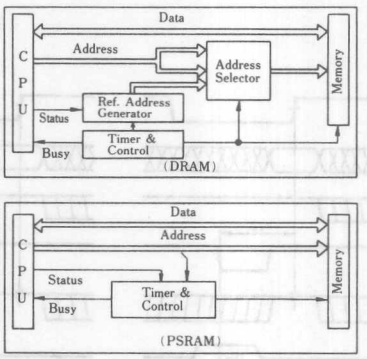


Figure 2-1. System Organization

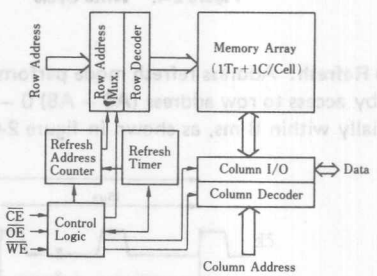


Figure 2-2. Block Diagram (PSRAM)

2.2. 1 Mbit Pseudo-Static RAM Function

Read/Write Cycle: Figure 2-3 and figure 2-4 show the timing chart for the read/write cycle of 1 Mbit pseudo-static RAM HM658128. The HM658128 can perform 2 types of access in a read cycle, $\overline{CE}$ access (Figure 2-3 (a)) and $\overline{OE}$ access figure 2-3 (b)). It writes the data at the rising edge of $\overline{WE}$ (figure 2-4 (a)) or at the rising edge of $\overline{CE}$ (figure 2-4 (b)). The $\overline{CS}$ pin should be brought high when the address is latched at the falling edge of $\overline{CE}$ in the read/write cycle. The HM658128 has no $\overline{OE}$ specification at the falling edge of $\overline{CE}$ as it provides both $\overline{OE}$ pin and $\overline{RFSH}$ pin.

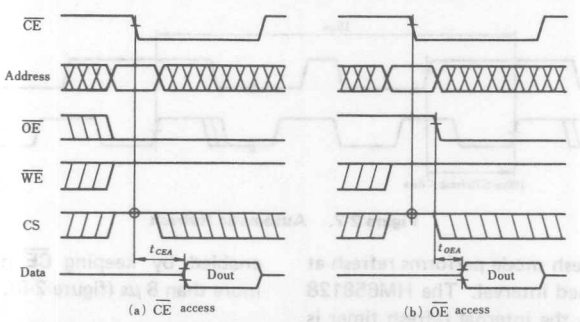


Figure 2-3. Read Cycle

CS Standby Mode: The HM658128 enters CS standby mode for one cycle if CS turns to low at the falling edge of $\overline{CE}$ (figure 2-5).

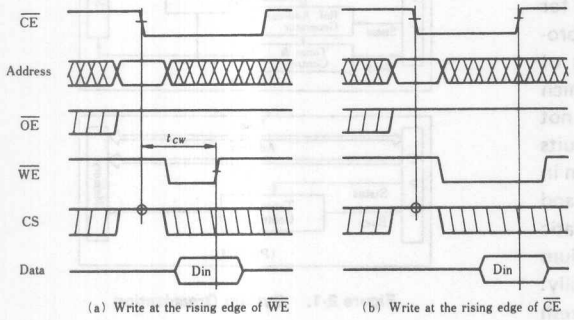


Figure 2-4. Write Cycle

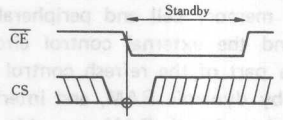


Figure 2-5. CS Standby Mode

Address Refresh: Address refresh mode performs refresh by access to row address (A0 – A8) 0 – 511 sequentially within 8 ms, as shown in figure 2-6 (in distributed mode). In this mode, CS should be high at falling edge of $\overline{CE}$.

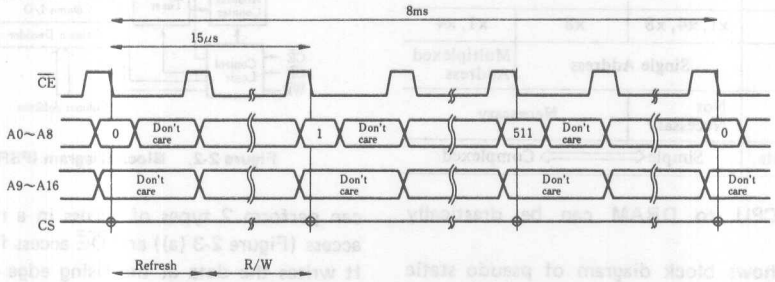


Figure 2-6. Address Refresh

Automatic Refresh: The HM658128 goes to automatic refresh mode if $\overline{RFSH}$ falls while $\overline{CE}$ is high and it is kept low for more than 180 ns.
It is not required to input the refresh address from address pins A0 – A8, as it is generated internally. Figure 2-7 shows the timing chart for distributed refresh. In automatic refresh mode, the timing for only $\overline{CE}$ and $\overline{RFSH}$ are specified.

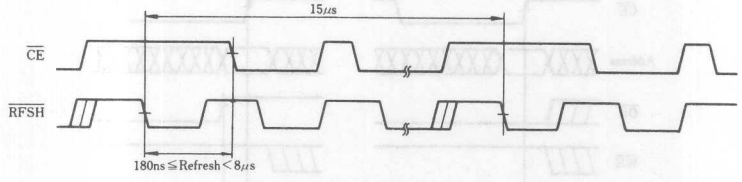


Figure 2-7. Automatic Refresh

Self Refresh: Self refresh mode performs refresh at the internally determined interval. The HM658128 enters the mode when the internal refresh timer is enabled by keeping $\overline{CE}$ high and $\overline{RFSH}$ low for more than 8 μs (figure 2-8).

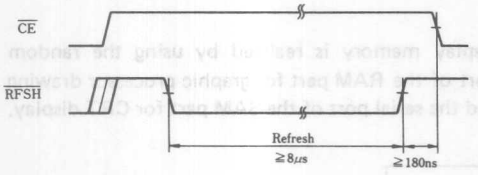


Figure 2-8. Self Refresh

Considerations on Using HM658128: The following should be considered when using the HM658128.

- Data retention. The HM658128 can retain the data with a battery (but not for long time). The HM658128L, low power version, offers typical self-refresh or standby current of 100μA.
  A 1-Mbyte system (using eight HM658128Ls) can retain the data for about 1.5 months with battery of 100 mAh current. V_{CC} = 5 V ± 10% must be maintained for data retention.
- Power on. Start HM658128 operation by executing more than eight initial cycles (dummy cycles) more than 100 μs after power voltage reaches 4.5 V – 5.5 V after power on.
- Bypass capacitor. Hitachi recommends inserting 1 bypass capacitor per RAM.

2.3 Pseudo-Static RAM Data Retention

PSRAM with self refresh retains data $\overline{CE}$ and $\overline{OE}$ are fixed for more than defined period. The following explains considerations for PSRAM data retention.

First, PSRAM cannot retain the data at low supply voltage.

They employ 1 MOS type memory cell as shown in figure 2-9. The charge is stored on the capacitor C as memory data. The data 1, written at low supply

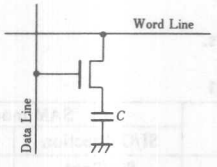


Figure 2-9. Memory Cell of PSRAM

voltage, cannot be read as 1 at high supply voltage.

Figure 2-10 indicates the operation voltage for self refresh and subsequent read of PSRAM. If the data is read out at more than 5 V of V_{CC}, for example, after self refresh is performed at V_{CC} = 3.7 V, it is destroyed.

PSRAM must be used at supply voltage from 4.5V to 5.5V.

Second self refresh current increases at low supply voltage.

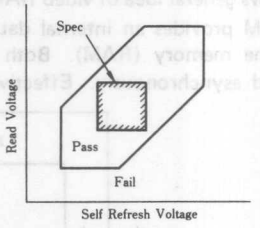


Figure 2-10. PSRAM Operating Voltage

PSRAM provides the voltage level detector circuit to reduce self refresh current. However, it should be noted that the circuit increases the current with low supply voltage in self refresh (figure 2-11). Self refresh current also increases at low temperature (figure 2-12).

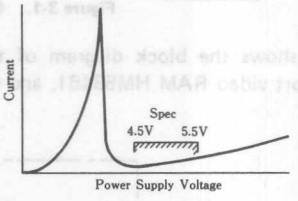


Figure 2-11. Self Refresh Current vs. Voltage

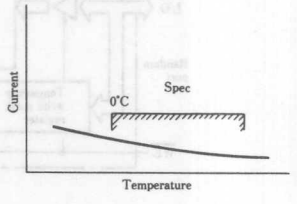


Figure 2-12. Self-Refresh Current vs Temperature

Please use PSRAM within the recommended operation range (V_{CC} more than 4.5 V, temperature more than 0°C) for data retention, especially using a battery.

3. Video RAM

3.1. Multiport Video RAM

Figure 3-1 shows general idea of video RAM. Multiport video RAM provides an internal data register (SAM) with the memory (RAM). Both of them can be accessed asynchronously. Effective graphic display memory is realized by using the random port of the RAM part for graphic processor drawing and the serial port of the SAM part for CRT display.

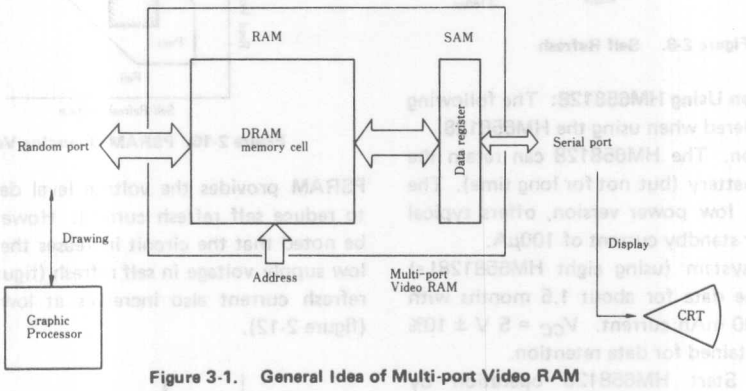


Figure 3-1. General Idea of Multi-port Video RAM

Figure 3-2 shows the block diagram of the 256-kbit multiport video RAM HM53461, and table 3-1 shows the operation modes of the HM53461.

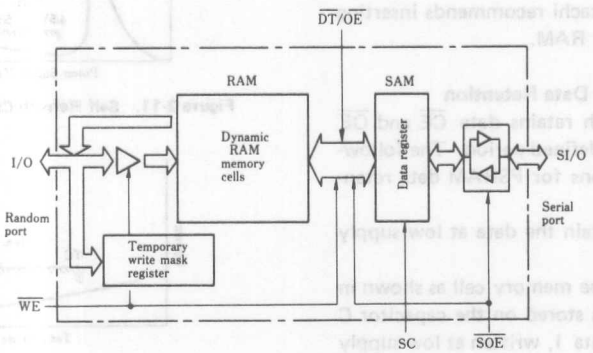


Figure 3-2. Block Diagram of HM53461

The operation modes shown in table 3-1 are described as follows.

Table 3-1. Operation Modes of HM53461

At the falling edge of RAS				RAM modes	SAM modes	
CAS	DT/OE	WE	SOE		SI/O direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary write mask data program	Sin/Sout	1, 2, 3
H	L	H	X	Read transfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	CBR refresh	Sin/Sout	1,2

H: High
L: Low
X: Don't Care

Notes: 1. Transfer cycle executed previously defines SI/O direction.
2. SI/O is in high impedance state with SOE high, even if the direction is Sout.
3. The HM53461 starts write operation if WE is low at the falling edge of CAS or become low between the falling edge of CAS and the rising edge of RAS.

Read/Write Operation: Read/write is performed on the random port in the same sequence as for a dynamic RAM (figure 3-3). The HM53461 starts the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

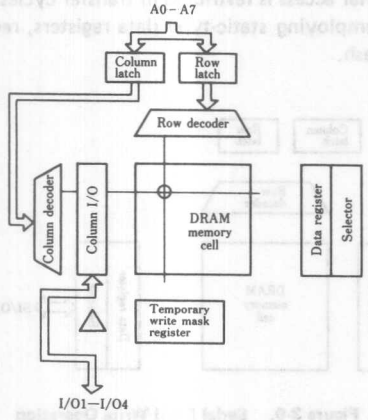


Figure 3-3. Read/Write Operation

Temporary Write Mask Set and Temporary Masked Write Operation: The HM53461 provides temporary masked write operation which inhibits to write data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. Temporary write mask set function defines the bits to be inhibited (figure 3-4). This operation puts the data on I/O1 – I/O4 into the internal temporary write mask register. When 0 is programmed to the register, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

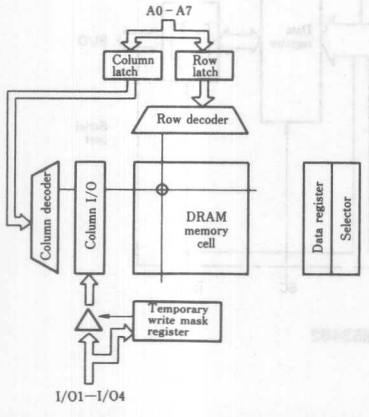


Figure 3-4. Temporary Masked Write Operation

Read Transfer Operation: In this cycle, the HM53461 transfers the data of one row in RAM (1024 bits), which address is specified at the falling edge of $\overline{RAS}$, to SAM (figure 3-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port turns to serial read mode at the rising edge of $\overline{DT/OE}$.

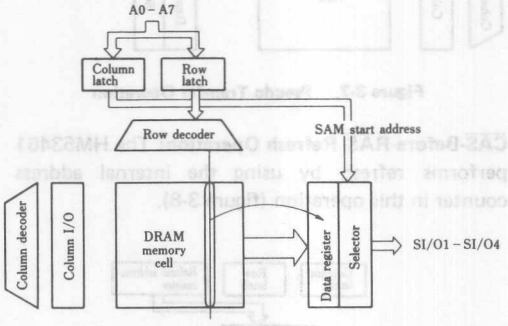


Figure 3-5. Read Transfer Operation

Write Transfer Operation: In this cycle, the HM53461 transfers the data in the SAM data register (1024 bits) to one row in RAM, which address is specified at the falling edge of $\overline{RAS}$ (figure 3-6). The start address in SAM can be programmed in this cycle. After data transfer, serial port turns to serial write mode.

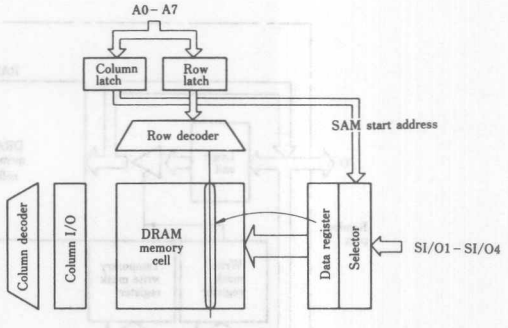


Figure 3-6. Write Transfer Operation

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (figure 3-7). It does not perform data transfer between RAM and SAM. SAM start address can be programmed in this cycle.

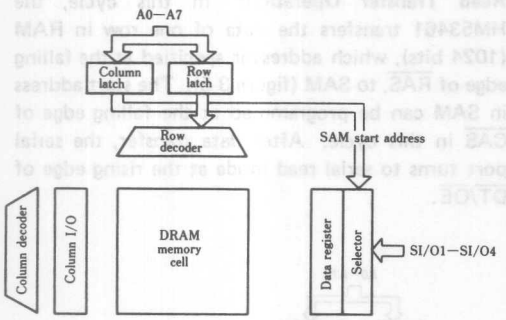


Figure 3-7. Pseudo Transfer Operation

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Operation: The HM53461 performs refresh by using the internal address counter in this operation (figure 3-8).

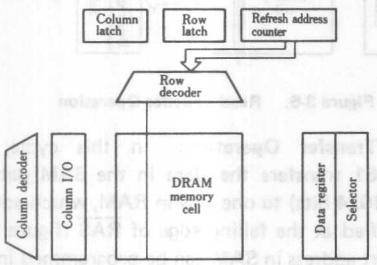


Figure 3-8. $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

Serial Read/Write Operation: The HM53461 reads/writes the contents of the SAM data register in serial at the rising edge of SC (serial clock input) (figure 3-9). The address for serial access is generated by the internal address pointer, independently of random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

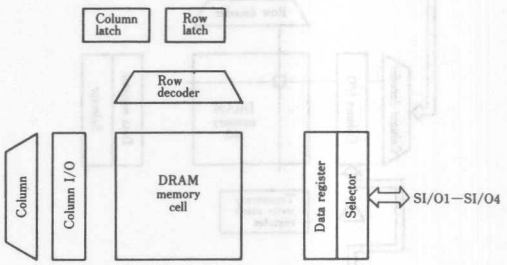


Figure 3-9. Serial Read/Write Operation

The HM53462 is a multiport video RAM, adding logic operation capability to the advantages of HM53461.

Figure 3-10 shows the block diagram. Table 3-2 describes the operation modes.

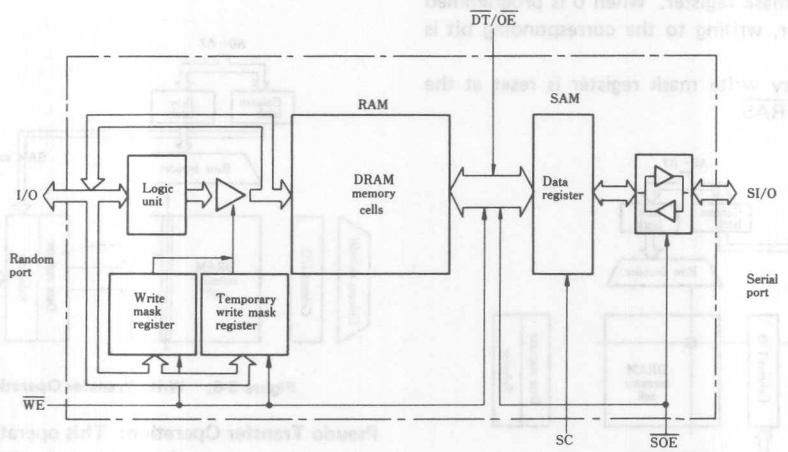


Figure 3-10. Block Diagram of HM53462

Table 3-2. Operation Modes of HM53462

At the falling edge of $\overline{RAS}$				RAM modes	SAM modes	
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SOE}$		SI/O direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary masked write	Sin/Sout	1, 2, 3
H	L	H	X	Read transfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	$\overline{CAS}$-before-$\overline{RAS}$ refresh	Sin/Sout	1,2
L	X	L	X	Logic operation program (CBR Refresh)	Sin/Sout	1,2

H: High L: Low X: Don't Care

Notes: 1. Transfer cycle previously executed defines SI/O direction.
2. SI/O is in high impedance with $\overline{SOE}$ high, even if SI/O direction is Sout.
3. HM53462 writes if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of RAS.

Logic Operation Programming: This function programs a logic operation (figure 3-11). The logic operation is available until re-programmed or reset. In logic operation mode, HM53462 performs read-modify-write internally when data is written into random port. The result of the logic operation between memory data and written data is put into the address from which the memory data is transferred.

In the logic operation programming cycle, the mask register, which differs from the temporary mask register, is also programmed. It is available until re-programmed.

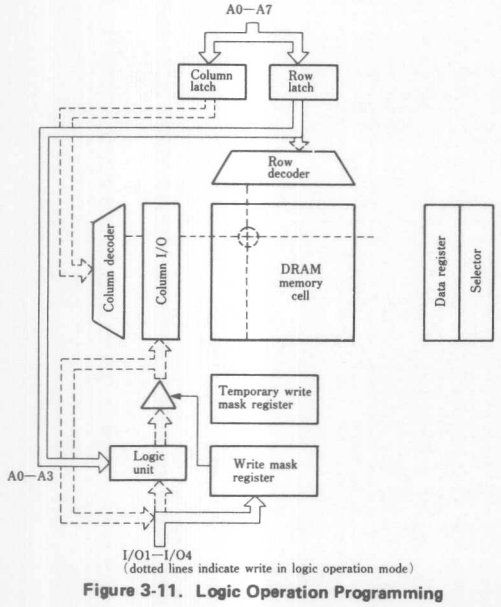


Figure 3-11. Logic Operation Programming

Notes: Notes on using HM53461/HM53462 are as follows.

- Dummy $\overline{RAS}$ cycle. Devices should be initialized by 8 dummy $\overline{RAS}$ cycles (minimum) before access to random port. Refresh cycle can be inserted for initialization. It is recommended that the system be initialized by dummy $\overline{RAS}$ cycle in the automatic reset time of the processor.
- Bypass capacitor. One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.
- Negative voltage input. Negative polarity input level to input pin or I/O pin should be under −1 V. In this range, it has no effect on device characteristics or RAM/SAM data retention.
- Initialization of logic operation mode (HM53462). The logic operation programming cycle should be executed before access to the random port to initialize logic operation mode after power on. At this time, the operation codes (0101) and all 1 write mask data are recommended.

3.2. Line Memory

Hitachi has produced a line memory for line buffers with simple circuits, providing specific functions as described below.

The line buffer can improve picture quality by storing 1 horizontal line data. It has following features.

- Capacity to store 1 horizontal line data
- High-speed operation matching the sampling speed of PAL TV signal (4 fsc/8 fsc) or NTSC TV signal (4 fsc/8 fsc).

- Separate data inputs/outputs and capability of serial data inputs and outputs.

The conventional line buffer composed of high speed static RAMs requires separate input/output for double buffer organization. It also requires interleaving for high speed operation, matching 4 fsc/8 fsc, where fsc is the subcarrier frequency. In addition, external circuits are needed for serial address scan.

The line memory provides all of these functions. Figure 3-12 shows the standard organization of a conventional memory buffer and figure 3-13 shows the block diagram of line memory.

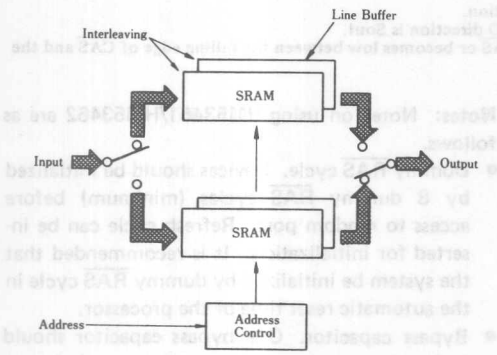


Figure 3-12. Standard Organization of Conventional Line Buffer

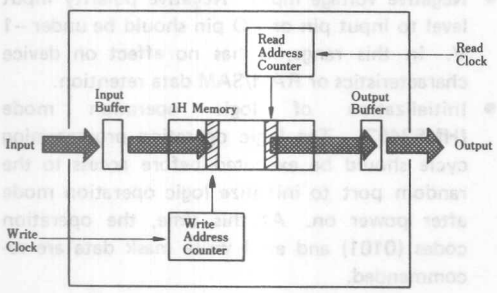


Figure 3-13. Block Diagram of Line Memory

The Hitachi HM63021 is a 2048-word x 8-bit line memory storing 2 horizontal lines of data.

It has five different modes for various video graphic system applications. It realizes high speed operations for PAL and NTSC TV signals, and dissipates little power employing 1.3 μm CMOS technology and static-type memory cells.

The features of the HM63021 are described as follows:

- Five modes for various video graphic system applications
  - Delay line mode
  - Alternate 1H/2H delay mode
  - TBC (Time-Base Corrector) mode
  - Double speed conversion mode
  - Time-base compression/expansion mode
- High speed cycle time
  - HM63021-34: 34 ns min (corresponds to 8 fsc of NTSC TV signal)
  - HM63021-28: 28 ns min (corresponds to 8 fsc of PAL TV signal).

Line memory in the system using digital signal processing technologies offers following applications:

1. comb filter
2. double-speed conversion (non-interlace)
3. compression/expansion of graphics (picture-in-picture)
4. dropout canceller
5. time-base corrector
6. noise reducer

4. Dynamic RAM

4.1. Dynamic RAM Memory Cell

The dynamic RAM memory cell consists of 1 MOS transistor and 1 capacitor, as shown in figure 4-1. It detects the data in the cell (1 or 0) by the charge stored in capacitor. Dynamic RAM offers higher density than that of static RAM because of fewer components per chip.

However, Dynamic RAM must rewrite data, called refresh, in a defined cycle because the charge stored in the capacitor leaks.

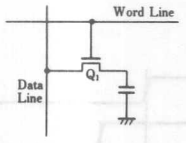


Figure 4-1. Memory Cell of Dynamic RAM

4.2. Power On Procedure

After turning on power, to set the internal memory circuitry, hold for more than 100 μs, then apply eight or more dummy cycles before operation. The dummy cycle may be either a normal read/write cycle or a refresh cycle. When using an internal refresh counter, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required as dummy cycles.

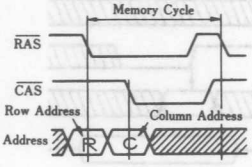
A0 – A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 – A8	Refresh Address Inputs

(a) Pin Arrangement

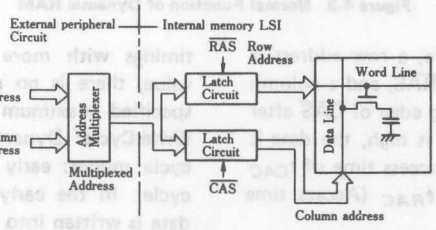
4.3 Address Multiplexing

Dynamic RAMs are used to increase capacity because of their smaller cell area. In using dynamic RAMs in systems, however, it is desirable to increase the memory density by using smaller packages. To reduce the number of pins and the package size, address multiplexing is used.

Using a 1-Mbit dynamic RAM, 20-address signals are necessary to select one of 1,048,576 memory cells. Address multiplexing allows address signals to be applied to each address pin. Thus only 10-address input pins are required to select one of 1048,576 addresses. Multiplexed address inputs are latched as follows: $\overline{RAS}$ (Row Address Strobe) selects one of word lines according to the row address signal, and one of column decoders is selected by $\overline{CAS}$ (column address strobe) following column address signal. Although two extra signals, $\overline{RAS}$ and $\overline{CAS}$, are required, the number of address pins is reduced to half. Figure 4-2 shows the pin arrangement, address latch waveform, and the block diagram of address-multiplexed 1-Mbit dynamic RAM. Systems need an address multiplexer in order to latch the multiplexed address signals into the device.



(b) Address Latch

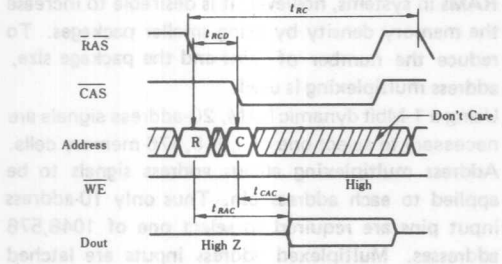


(c) Block diagram of Address Multiplexing

Figure 4-2 Address Multiplexing of Dynamic RAMs

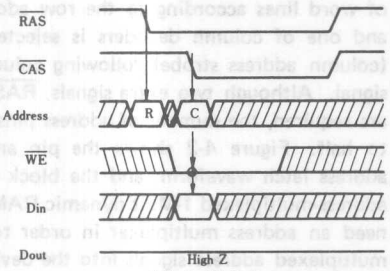
4.4. Dynamic RAM Function

Figure 4-3 shows the normal function of Dynamic RAM.



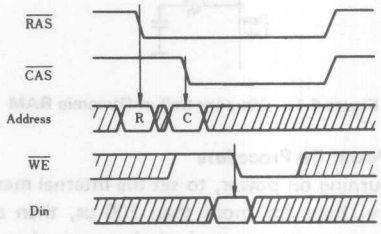
(a) Read Cycle

t_{RC}: Random Read or Write Cycle Time
t_{RCD}: RAS to CAS Delay Time
t_{RAC}: Access Time from RAS
t_{CAC}: Access Time from CAS
R: Row Address
C: Column Address

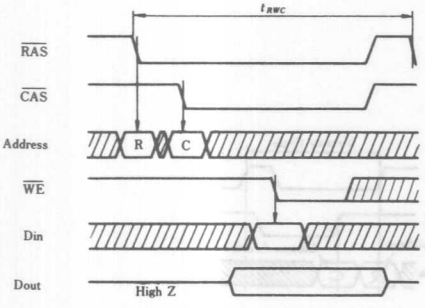


(Early Write)

(b) Write Cycle



(Delayed Write)



(c) Read-Modify-Write Cycle

t_{RWC}: Read-Write Cycle Time

Figure 4-3 Normal Function of Dynamic RAM

Read Cycle: In the read cycle, a row address is latched at the falling edge of $\overline{RAS}$, and a column address is latched at the falling edge of $\overline{CAS}$ after the $\overline{RAS}$ falling edge. If $\overline{WE}$ is high, the data is read out from Dout with the access time of t_{CAC} (Access time from $\overline{CAS}$) or t_{RAC} (Access time from $\overline{RAS}$).

The t_{RCD} maximum ($\overline{RAS}$ to $\overline{CAS}$ delay time) is specified only to guarantee the specified minimum values of other timings such as the cycle time, $\overline{RAS}$/$\overline{CAS}$ pulse width. Therefore, when using these timings with more than the specified minimum value, there is no need to limit the t_{RCD} to the specified maximum value.

Write Cycle: Dynamic RAM provides two write cycle modes: early write cycle and delayed write cycle. In the early write cycle, when $\overline{WE}$ is low, data is written into Din at the falling edge of $\overline{CAS}$. In delayed write cycle, when $\overline{WE}$ is high, data is written into Din at the falling edge of $\overline{WE}$ after $\overline{CAS}$ falling.

Read-Modify-Write Cycle: The read-modify-write

cycle is initiated by taking $\overline{WE}$ high. Data is read out from Dout at the falling edge of $\overline{CAS}$ with $\overline{WE}$ high. Then, when $\overline{WE}$ goes low, data is written into the same address from Din in the same cycle.

The cycle time in the read-modify-write mode (t_{RWC}) is longer than the cycle time in read/write mode (t_{RC}).

4.5 High Speed Access Mode

Dynamic RAM access time is typically longer than that of static RAMs. To realize higher speed operation, they have high speed access modes.

The read operation in dynamic RAM is performed as follows:

When a word line is selected by row address, all data in the memory cells connected to the selected word line is transferred to sense amplifiers. One of these sense amplifiers is selected by the column address, and its contents are output.

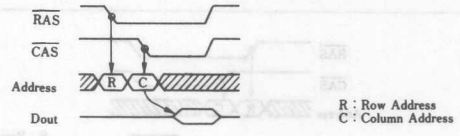
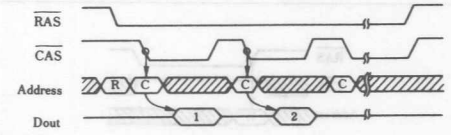
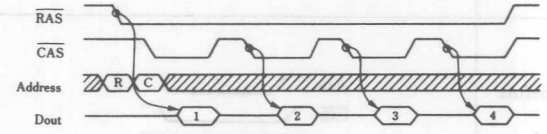
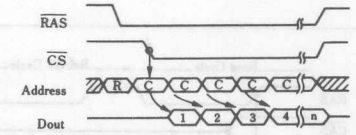
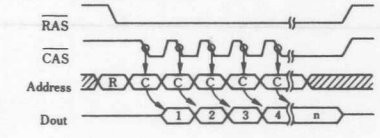
The output of data from other sense amplifiers is controlled only by the column address.

Access controlled only by column address with the row address fixed is called high speed access mode. Table 4-1 compares each mode.

Page Mode: This is the most typical access mode in dynamic RAM. The column address is switched synchronized with $\overline{CAS}$ falling.

Nibble Mode: In a nibble mode dynamic RAM,

Table 4-1. Comparison of Dynamic RAM High Speed Access Modes

Normal Mode	
Page Mode	
Nibble Mode	
Static Column Mode	
High-Speed Page Mode	

data from 4 sequential addresses is stored in the 4-bit output latch circuits. Output is provided by the $\overline{CAS}$ signal, which controls the latch circuits. When 4 addresses are accessed sequentially, the row addresses on and after second bit need not be selected. Therefore, it facilitates the timing design. In nibble mode, the operation is limited to 4 addresses, however, it enables faster access (t_{NAC}) than that in page mode.

Static Column Mode: In static column mode, the column address is switched without the synchronized signal by high-speed static RAM technology in the peripheral circuits.

High Speed Page Mode: This mode is the advanced mode of static column mode, with $\overline{CAS}$ providing the address latch function.

4.6 Refresh

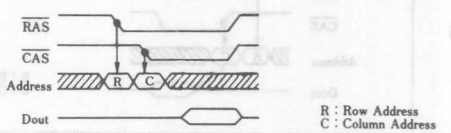
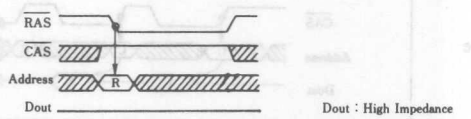
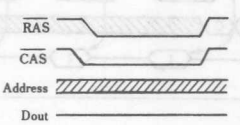
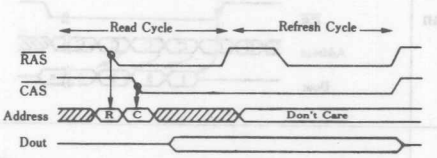
Refresh operation is performed by accessing every word line within the specified time (refresh cycle). Table 4-2 compares the following refresh modes in dynamic RAM.

$\overline{RAS}$ Only Refresh: In $\overline{RAS}$ only refresh mode, refresh can be completed by selecting only row addresses synchronized with $\overline{RAS}$.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh: This mode refreshes by the $\overline{CAS}$ falling edge before $\overline{RAS}$ in the period defined by the internal refresh address generator. This mode simplifies the external address multiplexer.

Hidden Refresh: In hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh is performed while output data is valid.

Table 4-2. Comparison of Dynamic RAM Refresh Modes

Read	
$\overline{RAS}$ Only Refresh	
$\overline{CAS}$ before $\overline{RAS}$ Refresh	
Hidden Refresh	

▨: Don't care

5. EEPROM

5.1. EEPROM Memory Cell

EEPROM is electrically erasable and programmable ROM, which can be erased or written remotely while the system is in operation.

The Hitachi EEPROM memory cell is MNOS (Metal Nitride Oxide Semiconductor) type, as shown in figure 5-1.

An MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of oxide film is about 20 Å and that of nitride film is 300 to 500 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. Electrons move by the tunneling phenomenon between the substrate and traps.

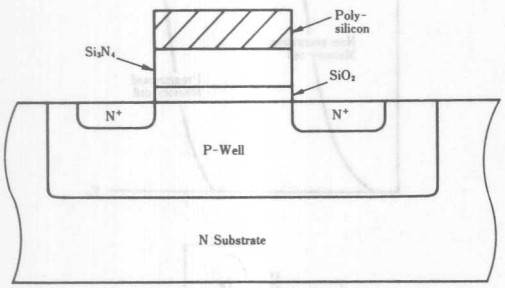


Figure 5-1. MNOS Type Memory Transistor

5.2. 64-kbit CMOS EEPROM Function

Page Write Function: The 64-kbit HN58C65 can latch 32 bytes (max) and write them in one write cycle. Writer cycle time is specified as 10 ms (max.). The effective byte write speed of HN58C65 in page write mode is:

10 ms/32 bytes = 0.31 ms/byte

Thus it takes only 2.56 seconds to write the whole HN58C65. Figure 5.2 shows internal operation. The following describes operation sequence:

1. 32-byte memory cell data at the row address selected by address pins A5 – A12 is latched.
2. Latched data at the column address specified by address pins A0 – A4 is altered with write data, which is put into Din buffer from I/O pins I/O0 – I/O7.

   The 32 bytes (max) of latched data are altered by repeating this operation 32 times.
3. 32-bytes memory cell data in the selected row (1) are erased (All 1).
4. Latched data is written into the selected row (3).
5. CPU acknowledges the completion of write cycle by the internal timer. The HN58C65 provides RDY/$\overline{\text{BUSY}}$ and $\overline{\text{Data}}$ polling to indicate the write completion.

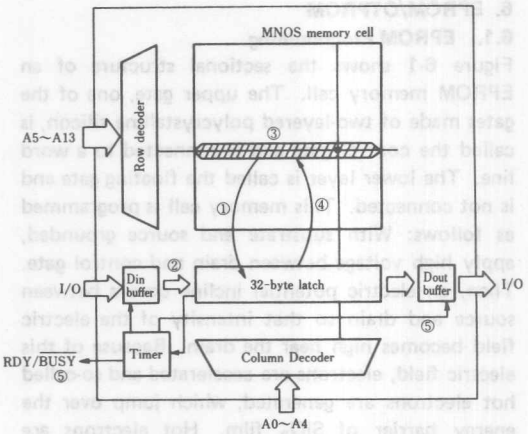


Figure 5-2. HN58C65 Page Write

Internal Timer: The HN58C65 indicates the completion of data write to the CPU by using the internal timer. The HN58C65 enters next cycle as soon as detecting the completion of write. This function offers high system throughput as the CPU can access other devices during write cycle. The HN58C65 has two functions, RDY/$\overline{\text{Busy}}$ and $\overline{\text{Data}}$ polling, to indicate the completion of data write.

The RDY/$\overline{\text{Busy}}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C65 is in data write operation ($\overline{\text{Busy}}$) and turns to high impedance state at the end of data write (RDY). RDY/$\overline{\text{Busy}}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{\text{Busy}}$ pins can be wired-OR when using several HN58C65s.

The $\overline{\text{Data}}$ polling approach, implemented by software, indicates the completion of data write through pin 19 (I/O7). While the data write is not completed, I/O7 shows the inverted data of what was written in the last cycle. In using this approach, RDY/$\overline{\text{Busy}}$ pin should be opened or grounded. The $\overline{\text{Data}}$ polling approach can acknowledge the completion of data write in an individual HN58C65, even if several HN58C65s are used in the system.

Data Protection: EEPROM performs data write with a higher voltage (V_{PP}) than power supply voltage (V_{CC}). The HN58C65 internally generates V_{PP} by a high voltage generator with the combination of control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$). It supports the following functions to avoid accidental data write (data protection).

1. Data protection against the noise on the control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during operation.
2. Data protection against the noise at power-on/power-off.

6. EPROM/OTPROM

6.1. EPROM Programming

Figure 6-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows: With substrate and source grounded, apply high voltage between drain and control gate. Then, an electric potential incline occurs between source and drain so that intensity of the electric field becomes high near the drain. Because of this electric field, electrons are accelerated and so-called hot electrons are generated, which jump over the energy barrier of SiO_2 film. Hot electrons are pulled by the electric potential of the control gate and pour into the floating gate. Electrons stored in the floating gate remain stable, as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

Figure 6-2. shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1V, the current in a programmed transistor does not flow until V_G rises to 7 V – 10 V. Therefore, if the voltage of word line applied to the control gate is about 5 V in readout, the non-programmed memory transistor will be on, and the programmed one will be off. This means that the data can be read out by means of the same structure as NOR-type mask ROM.

6.2. Erasing EPROM

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erase). Changing the logic 1 to logic 0 through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{pw}, the more electrons can be programmed in, as shown in Figure 6-3. If V_{PP} exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce the yield voltage.

Hitachi's EPROMs can usually be written and erased more than 100 times.

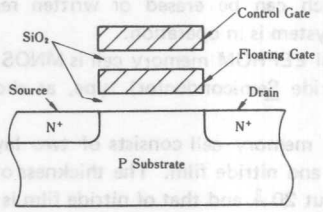


Figure 6-1. Cross Section of EPROM Memory Cell

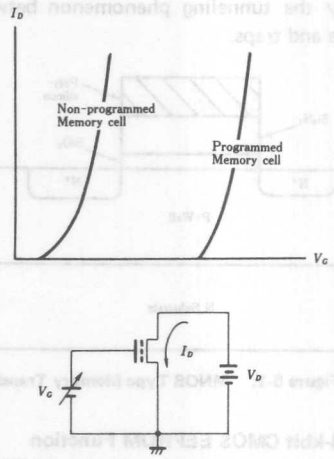


Figure 6-2. Fundamental Characteristic of EPROM Memory Cell

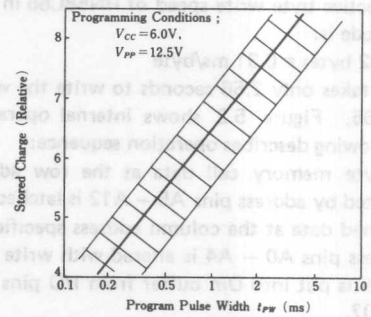


Figure 6-3. Standard Programming Characteristics of EPROMs

EPROMs are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2

film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as $E = h\nu$. E means the energy of light, h is Planck's constant, ν is light frequency. Erasure isn't caused by light over certain wavelengths, and under certain wavelengths, erasure does occur. However, erasure time depends upon the quantity of photons, therefore erasure time cannot be shortened by shorter wavelength. Figure 6-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å, and is saturated at about 3000Å.

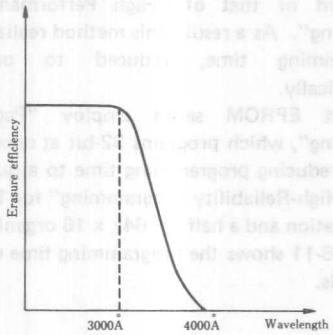


Figure 6-4. Erasure Efficiency of EPROM

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2,537Å and 15 $W \cdot s/cm^2$ respectively. These conditions can be met by placing the device 2 – 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. Contamination or foreign materials should be removed with a solvent such as alcohol that does not damage the package.

Figure 6-5 shows EPROM standard erasure characteristics.

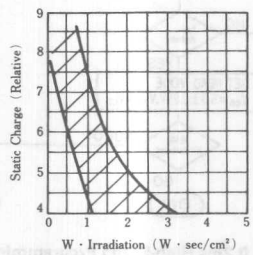


Figure 6-5. Standard Erasure Characteristics

6.3. EPROM Data Retention Characteristic

About 2 to 20×10^{-14} coulomb of electrons are accumulated in the floating gate when programmed. However, these electrons dissipate with time. Then the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 6-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

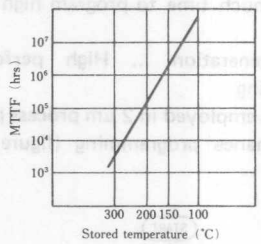


Figure 6-6. EPROM's Data Rentention Characteristic

Data Dissipation by Ultraviolet Light: Ultraviolet rays at a wavelength of not greater than 3,000 – 4000Å is capable of releasing the electric charge at

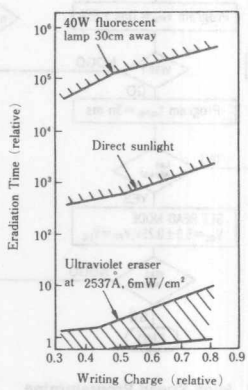


Figure 6-7. EPROM's Data Retention Time

floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 6-7 shows the standard, data retention time under an ultraviolet eraser, sunlight and fluorescent lighting.

6.4 Optimized High-Speed Programming

With the increase of EPROM density, the time for programming becomes more important. The method for high speed programming has been developed and put into practical use according to each EPROM generation.

Following explains three methods for High-Speed programming.

(1) First generation ... conventional programming.

This method is employed in the 3 μm and 5 μm process products. Programming is performed with a uniform pulse of 50 ms per byte. Although it is the advantage that it applies enough pulse to all bits, it takes much time to program high density devices.

(2) Second generation ... High performance programming

This method is employed in 2 μm process product. "High Performance programming (figure 6-8) is performed with a base pulse of 1 ms width. It repeats programming and reading (verifying) until the data is programmed enough. There are two good points in this programming.

First, the programming itself is performed with optimum program time depending on the capability of each memory cell.

Second, after verification, the data is programmed using three times as long a pulse and assures high-reliability data retention.

(3) Third generation ... Fast High Reliability Programming

This method is employed in the 1.3 μm process products. "Fast High-Reliability Programming" (figure 6-9) is performed with a base pulse of 0.2 ms. It also shortenes a supplement pulse width to one-third of that of "High Performance Programming". As a result, this method realizes short programming time, reduced to one-tenth theoretically.

1M bit EPROM series employ "Page Programming", which programs 32-bit at once (figure 6-10), reducing programming time to a quarter of "Fast High-Reliability Programming" for 128k x 8 organization and a half for 64k x 16 organization.

Figure 6-11 shows the programming time of above methods.

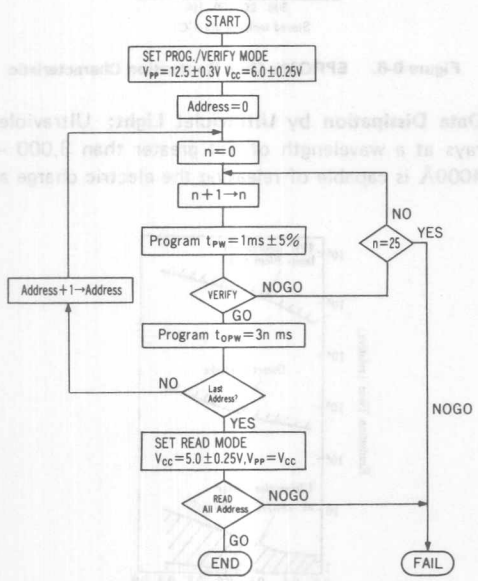


Figure 6-8. High-Speed Programming (High Performance Programming)

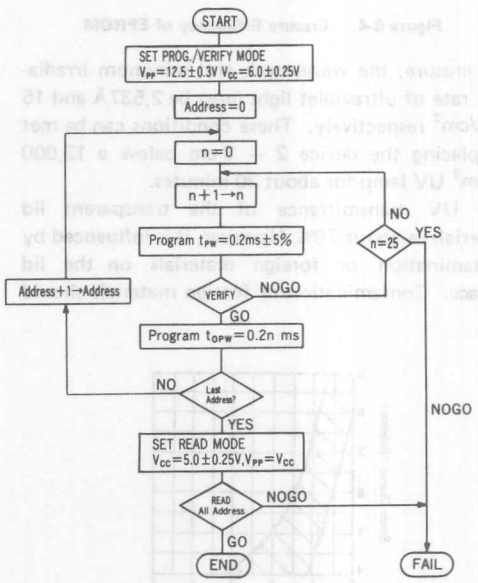


Figure 6-9. 0.2ms High-Speed Programming (Fast High-Reliability Programming)

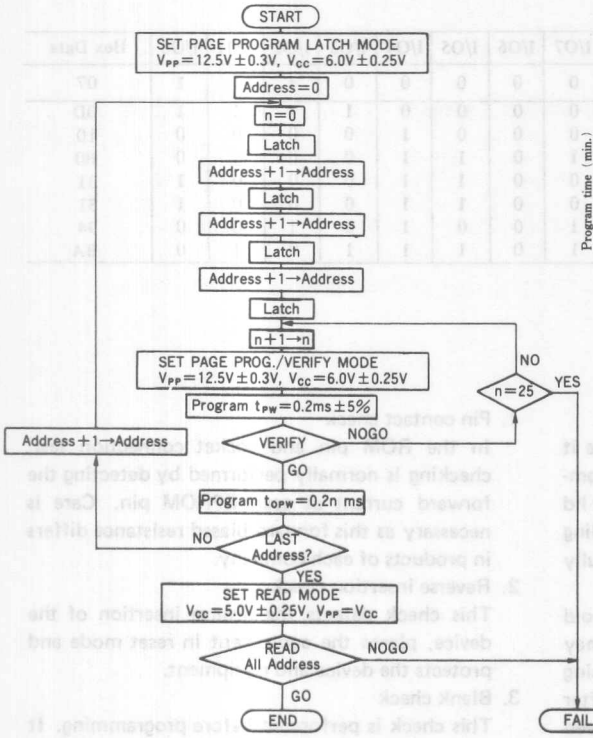
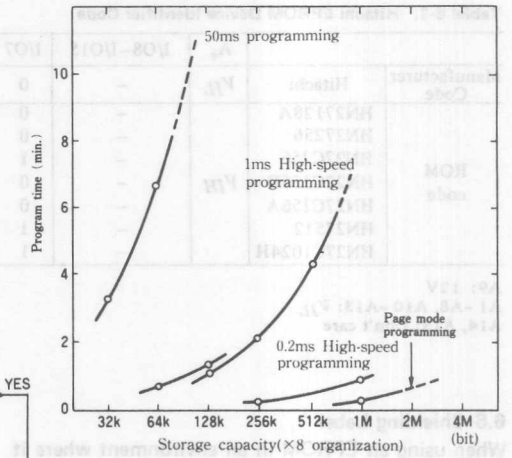


Figure 6-10. Page-Mode Programming (Page Programming)



(Note) Actual program time differs according to the programmer.

Figure 6-11. Shortened Program Time by High-Speed Programming.

6.5 Device Indentifier Code

EPROM programming conditions depend on EPROM manufacturers and device types, confusion may cause miss operation. As a countermeasure some EPROMs provide device identifier code including such information as manufacture and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows: (1) program voltage, (2) program timing, (3) high-performance programming algorithm, (4) pin configuration. The Hitachi EPROM has a device identifier code area besides the memory access area, as shown in figure 6-12.

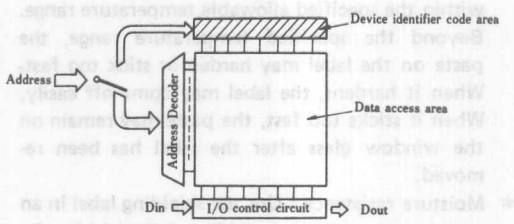


Figure 6-12. Device Identifier Code

Table 6-1 describes how to use the device identifier code. Setting A9 at 12 V and A1 – A8, A10 – A13 at V_{IL} access the device identifier code area and I/O0 – I/O7 output the programming condition code with V_{IL} or V_{IH} of A0.

Tablel 6-1. Hitachi EPROM Device Identifier Code

		A_0	I/O8–I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
Manufacturer Code	Hitachi	V_{IL}	–	0	0	0	0	0	1	1	1	07
ROM code	HN27128A	V_{IH}	–	0	0	0	0	1	1	1	1	0D
	HN27256		–	0	0	0	1	0	0	0	0	10
	HN27C256		–	1	0	1	1	0	0	0	0	B0
	HN27C256H		–	0	0	1	1	0	0	0	1	31
	HN27C256A		–	0	0	1	1	0	0	0	1	31
	HN27512		–	1	0	0	1	0	1	0	0	94
	HN27C1024H		–	1	0	1	1	1	0	1	0	BA

A9: 12V
A1 -A8, A10 -A13: V_{IL}
A14, A15: Don't care

6.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends putting a shielding label on its transparent lid to absorb ultraviolet light. In choosing a shielding label, the following points should be carefully checked.

★ Adhesiveness (mechanical strength). Avoid repeated attaching or exposure to dust that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on over the old one since peeling may create a static charge.)

★ Allowable temperature range. Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may come off easily. When it sticks too fast, the paste may remain on the window glass after the label has been removed.

★ Moisture resistance. Use the shielding label in an environment whose humidity falls within the specified allowable humidity range.

6.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, 3 functions at least are necessary: blank check function prior to programming, programming function, and the verify function after programming. Figure 6-13 shows the programming flow chart. Some programmers check for pin contact failure or the reverse insertion before the blank check.

The outline of each block is as follows.

1. Pin contact check
   In the ROM pin and socket connection test, checking is normally performed by detecting the forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.
2. Reverse insertion check
   This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.
3. Blank check
   This check is performed before programming. It checks whether the device is an erased EPROM, or it preventing EPROM reprogramming. Since the output data in the erased condition are 1 (high level), check whether or not data in EPROM are all 1. It will fail-stop even when one bit is 0 (low level). Normally, it is designed to provide warning with a lamp or buzzer.
4. Programming
   The function of programming the data in the internal RAM of the programmer into EPROM will fail-stop when programming cannot be done. The normal flow is as shown in figure 6-14. The EPROM data will be read out prior to programming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, the data will be read out again and compared with the programming data, and if they coincide, the programmer will progress to the next address.
5. Verify
   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It performs fail-stop when they do not coincide. Normally, when it fails, it lights the fail lamp and displays

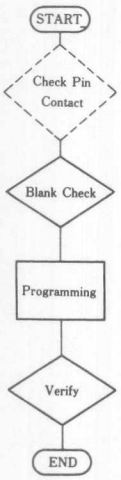


Figure 6-13. Programming Flow Chart of EPROM Programmer (1)

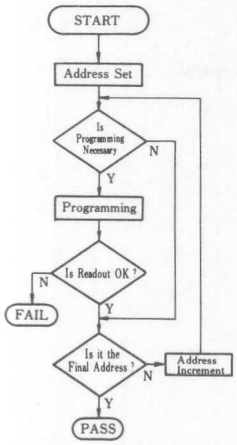


Figure 6-14. Programming Flow Chart of EPROM Programmer (2)

the address and data.

6. How to input the program
   Table 6-2 shows several methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are prefered options.

Table 6-2. EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch on the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction, and list preparation of the program can be made.

6.8 Handling EPROMs

Touched with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it reduces the electric charges in the floating gate, too. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM. Avoid using things such as gloves that may generate static electricity.
2. Refrain from rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which contain some ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute established charge.

6.9 Ensuring OTPROM Reliability

One time electrically programmable ROM (OTPROM) has two kinds of packages: standard dual in-line package (DIP) and small outline package (SOP). It is one time only programmable because it has no window for ultraviolet light exposure; testing by programming and erasure cannot be performed after it is assembled.

So, Hitachi performs screening test for programming, access time, and data retention on wafers at proving test.

However, rare defects may occur in the assembly process cannot be completely removed in final test screening which is only a reading test.

Therefore, Hitachi recommends that users perform high temperature baking after programming devices to ensure high reliability.

Detailed conditions and procedures for screening are shown in figure 6-15. First, program and verify devices. Then, leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check read-out function and remove the chips with data retention failures.

From the results of devices in which the recommended screening test is properly performed, we confirm that the data retention characteristics of OTPROMs are equal to general EPROMs.

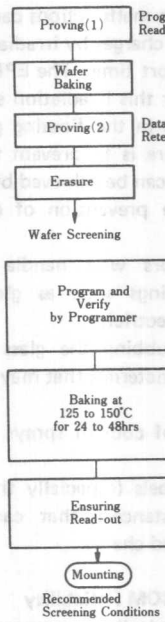


Figure 6-15. Screening Flow Chart of OTPROM

7. MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into mask ROMs is performed by the CAD system on a large-sized computer. ROM code data should conform to specifications given below, using either paper tape, EPROM, or magnetic tape. Additional instructions, such as chip select and customers' part number, should be given in the "ROM Specification Identification Sheet"

7.1 Specification of EPROM

1. Submit the three sets of the EPROM-stored data. Specify the address of the EPROM in the case of two or four EPROMs.
2. The ROM code data is input from the start address to Final Address in the EPROM.
3. Type of EPROM
   HN482764 (8-kword x 8-bit, 2764 Compatible)
   HN4827128 (16-kword x 8-bit, 27128 Compatible)
   HN27256 (32-kword x 8-bit, 27256 Compatible)
   HN27C256 (32-kword x 8-bit, 27C256 Compatible)

7.2 Specification of Magnetic Tape

1. Use the following type of magnetic tape which can be used by a magnetic tape device compatible with the IBM magnetic tape device.
   Length . . . . . 2,400 feet, 1,200 feet or 600 feet
   Width . . . . . 1/2 inch
   Channel . . . . . 9 channels
   Bit density . . . . 800 BPI or 1,600 BPI (Clearly state which it is in the "ROM Specification Indetification Sheet".)
2. Use EBCDIC as the use code.
3. Follow the format of the magnetic tape as described below
   No leading tape mark
   No label
   Record size . . . . . 80 byte/1 record
   Block size . . . . . 10 records/1 block
   The end of the file should be indicated by 2 successive tape marks (TM) (figure 7-1).
4. HMCS6800 load module data mode. This mode is the object mode output from the assembler HMCS6800.
   Divide the 8-bit code into the upper and lower 4-bit codes, and convert each into hexadecimal notation.
   Example: The code 1100 0110 is as follows under binary notation.

(Upper 4-bits)				(Low 4-bits)				Bit weight
D7	D6	D5	D4	D3	D2	D1	D0	(ROM output
1	1	0	0	0	1	1	0	equivalence)

   The actual load module mode is shown in figure 7-2.

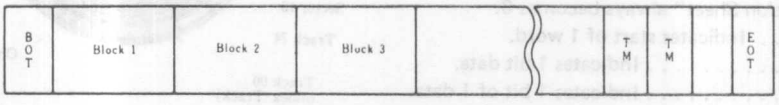


Figure 7-1. Magnetic Tape Format

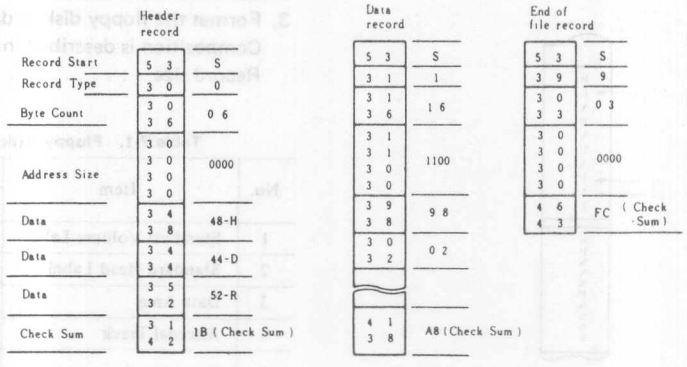


Figure 7-2. HMCS68000 Load Module Data Format

S0 indicates the head of the file and S9 indicates the end of the file. The actual data starts following S1. This means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. The printed example of the HMCS6800 load module mode is as shown in figure 7-3.

```
Header Record  →S00B000058204558414D504CB5
Data Record    →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record    →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record    →S9030000FC
```

Figure 7-3. HMCS6800 Load Module Example

If an address is skipped, enter the skipped address into the "ROM Specification Identification Sheet" and the data (00 or FF) entered into the skipped address.

5. BNPF mode
   One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.
   The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.
   (Example) The code of AA (hexadecimal) is symbolized as shown in figure 7-4.
   It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specification Identification Sheet" always becomes 0.
   B . . . . . Indicates start of 1 word.
   N . . . . . Indicates 1 bit data.
   P . . . . . Indicates 1 bit of 1 data.
   F . . . . . Indicates end of 1 word.

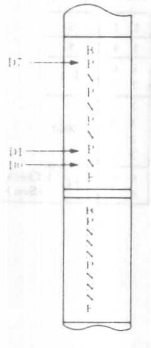


Figure 7-4. BNPF Mode Example

7.3 Specification of Floppy Disk

1. Use the following type of floppy disk (figure 7-5):
   Type. . . . 8 Inch Single Sided and Single Density
   Number of Sectors 26
   Number of Tracks 77

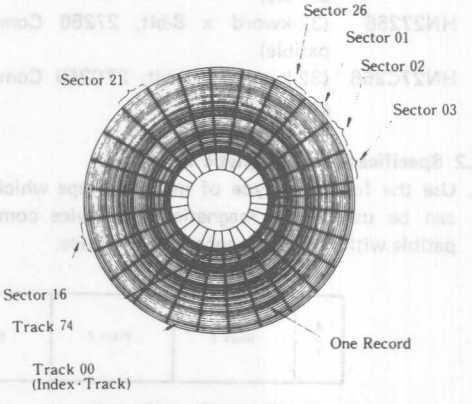


Figure 7-5. Floppy Disk Format

2. Use EBCDIC as the use code.
3. Format the floppy disk as described below.
   Composition is described in table 7-1.
   Record size . . . . . 80 byte/1 record

Table 7-1. Floppy Disk Composition

No.	Item	Location	
		Track	Sector
1	Standard Volume Label	00	07
2	Standard Head Label	00	08 – 26
3	Data Area	01 – 73	01 – 26
4	Alternal Track	75, 76	01 – 26
5	Spare Track	00 74	01 – 06 01 – 26

Use the sectors as in figure 7-6. Use one sector for one record, that is, 80 bytes out of 128 bytes used for one record.

4. Data Mode. See data mode for magnetic tape.

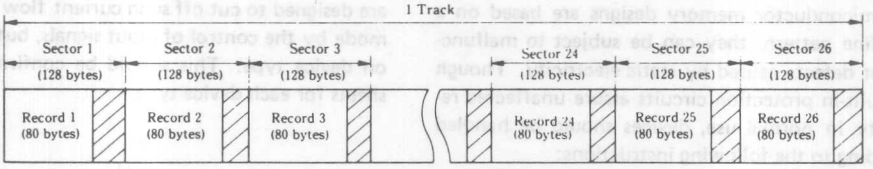


Figure 7-6. Floppy Disk Sector Format

: unused

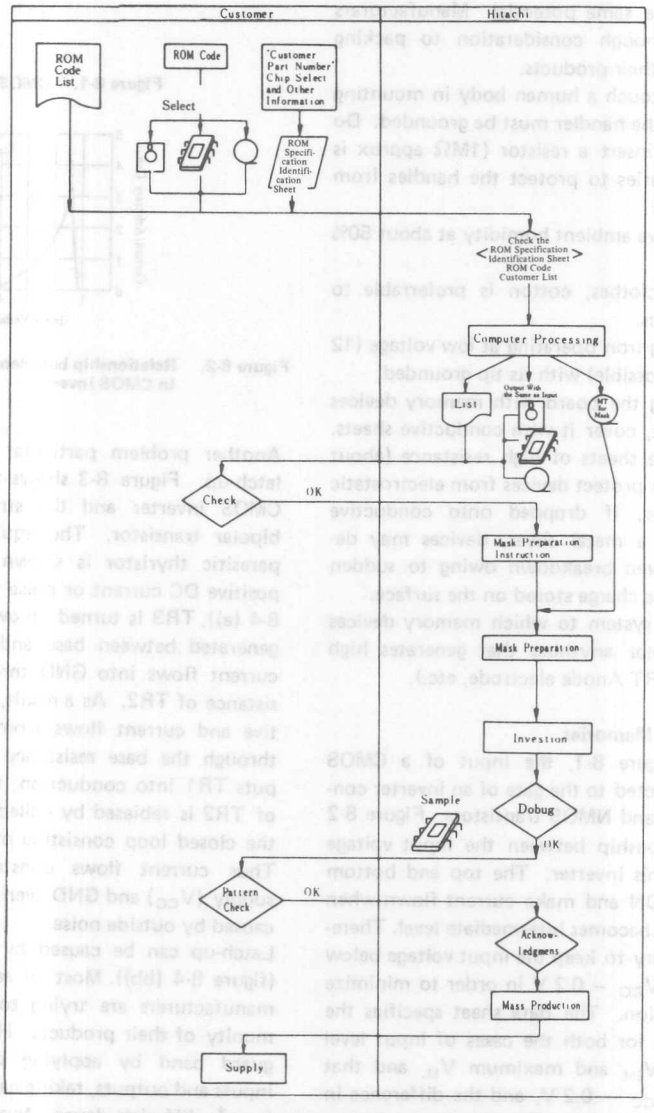


Figure 7-7. Mask ROM Development Flowchart

8. INSTRUCTIONS FOR USING MEMORY DEVICES

8.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled according to the following instructions:

1. In transporting and storing memory devices, put them in conductive magazine or put all pins of each device into a conductive mat so that they are kept at the same potential. Manufacturers should give enough consideration to packing when shipping their products.
2. When devices touch a human body in mounting or inspection, the handler must be grounded. Do not forget to insert a resistor (1MΩ approx is desirable) in series to protect the handles from electrical shock.
3. Keep the relative ambient humidity at about 50% in process.
4. For working clothes, cotton is preferrable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. In transporting the board with memory devices mounted on it, cover it with conductive sheets.
7. Use conductive sheets of high resistance (about 10^9 ohm/□) to protect devices from electrostatic discharge. For, if dropped onto conductive materials like a metal sheet, devices may deteriorate or even breakdown owing to sudden discharge of the charge stored on the surface.
8. Never set the system to which memory devices are applied near anything that generates high voltage (e.g. CRT Anode electrode, etc.).

8.2 Using CMOS Memories

As shown in figure 8-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 8-2 shows the relationship between the input voltage and current in this inverter. The top and bottom transistors turn ON and make current flown when the input voltage becomes intermediate level. Therefore, it is necessary to keep the input voltage below 0.2 V or above V_{CC} − 0.2 V in order to minimize power consumption. The data sheet specifies the stand-by current for both the cases of input level with minimum V_{IH} and maximum V_{IL} and that with 0.2 V or V_{CC} − 0.2 V, and the difference in value is remarkably great. Some memory devices are designed to cut off such current flow in standby mode by the control of input signals, but it depends on device type. This should be confirmed in data sheets for each device type.

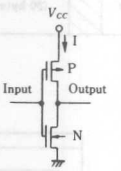


Figure 8-1. CMOS Inverter

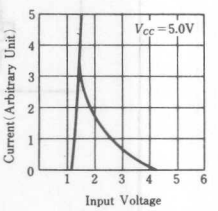


Figure 8-2. Relationship between Input Voltage & Current In CMOS Inverter

Another problem particular to CMOS devices is latch-up. Figure 8-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in figure 8-4. When positive DC current or pulse noise is applied (figure 8-4 (a)), TR3 is turned on owing to the bias voltage generated between base and emitter. And trigger current flows into GND through R_P, the base resistance of TR2. As a result, TR2 becomes conductive and current flows from power supply (V_{CC}) through the base resistance of TR1 (R_N), which puts TR1 into conduction, too. Then, as the base of TR2 is rebiased by collector current from TR1, the closed loop consisting of TR1 and TR2 reacts. Thus current flows constantly between power supply (V_{CC}) and GND even without trigger current caused by outside noise.

Latch-up can be caused by a negative pulse, too (figure 8-4 (bb)). Most of semiconductor memory manufacturers are trying to improve latch-up immunity of their products. Hitachi provides enough guard band by applying diffusion layer around inputs and outputs, taking care not to connect input to p^+ diffusion layer. Input voltage for 64 kbit

static RAM HM6264A, for example, is specified as follows:

V_{IH} max 6.0 V (not depending on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
−0.3 V (DC level)

Thus almost no consideration for latch-up is required in system design.

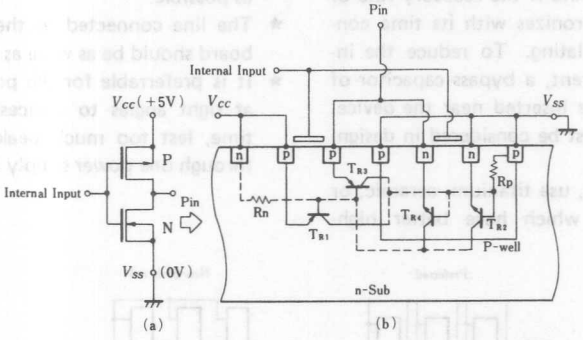


Figure 8-3. Cross Section Structure of CMOS Inverter

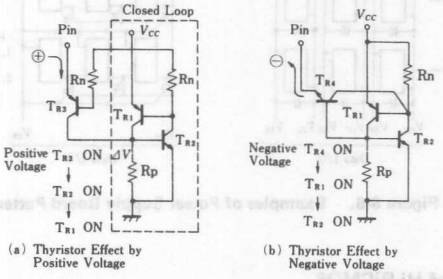


Figure 8-4. Equivalent Circuit of Parasitic Thyristor

8.3 Noise Prevention

Noise in semiconductor memories is roughly classified into input signal noise and power supply noise.

8.3.1 Input Signal Noise

Input signal noise is caused by overshoot and undershoot. If either of them is out of recommended DC operating conditions, normal operation is hindered, and voltage over absolute maximum rating will break the device. In operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohm into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because it is often caused by unstable reference voltage (GND level).

8.3.2 Power Supply Noise

The power source noise can be classed as low-frequency noise and high-frequency noise as shown in figure 8-5. To assure stable memory operation, the peak-to-peak power supply voltage in the presence of low-or high-frequency noise should be held below 10 percent of its standard level.

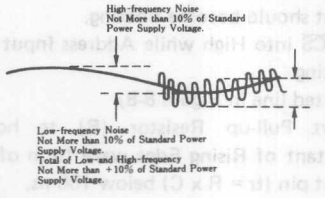


Figure 8-5. Power Source Noise

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1 – 0.01 μF should be inserted near the device. The following points must be considered in designing pattern of the board:

★ For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.

★ Bypass capacitors must be applied as near to the power supply pin of memory devices as possible, and inductance in the path from V_{CC} pin to V_{SS} pin through the bypass capacitor must be as little as possible.

★ The line connected to the power supply on the board should be as wide as possible.

★ It is preferrable for the power supply line to be at right angles to devices selected at the same time, lest too much peak current should flow through one power supply line at a time.

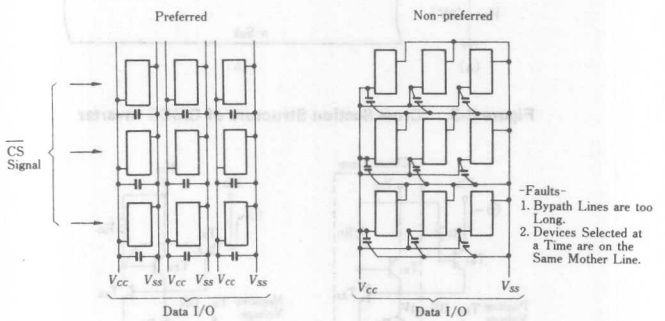


Figure 8-6. Examples of Power Supply Board Pattern

8.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destructed in case that Address Input of the HM6716, HM6719, HM6787, HM6788 and HM6789 series becomes floating and sticks at and around threshold voltage. (e.g. CPU does Address Bus to off state in Figure 1.) Consequently, the following three methods are recommended so as to preserve malfunction of memory device.

A: Insert latch as shown in Figure 8-7 lest Address Input should become floating.

B: Put $\overline{CS}$ into High while Address Input becomes floating.
(Dotted line in Figure 8-8)

C: Insert Pull-up Resistor (R) to hold time constant of Rising Edge wave form of Address Input pin (tr = R x C) below 150 ns.

Stable operation can be assured if you have already adopted the above three method (A, B, C), while if you have any problem, please contact our sales offices.

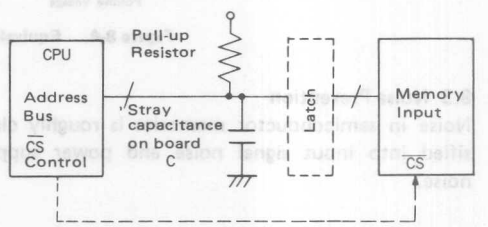


Figure 8-7

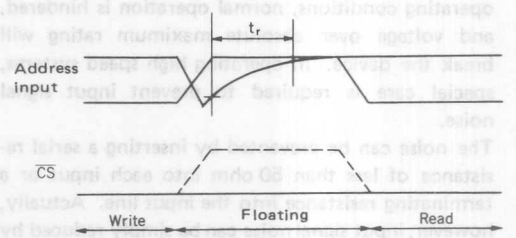


Figure 8-8

1



Section 1
MOS Static RAM

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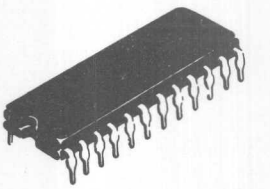
HM6116 Series — Maintenance Only

2048-word x 8-bit High Speed CMOS Static RAM

■FEATURES

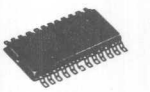
- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
  - 10μW (typ.) (L-version)
  - Operation: 200mW (typ.)
  - 175mW (typ.) (L-version)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116P Series



(DP-24)

HM6116FP Series

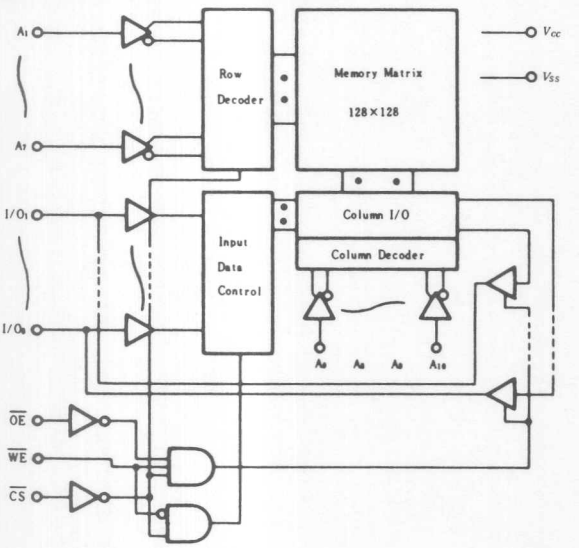


(FP-24D)

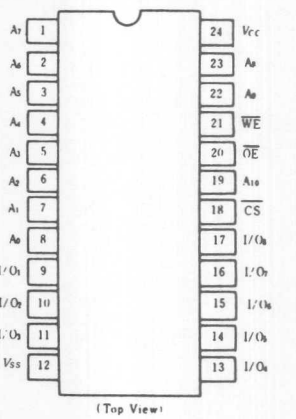
■ORDERING INFORMATION

Type No.	Access Time	Package
HM6116P-2 HM6116P-3 HM6116P-4	120ns 150ns 200ns	600mil 24pin Plastic DIP
HM6116LP-2 HM6116LP-3 HM6116LP-4	120ns 150ns 200ns	
HM6116FP-2 HM6116FP-3 HM6114FP-4	120ns 150ns 200ns	24pin Plastic SOP
HM6116LFP-2 HM6116LFP-3 HM6116LFP-4	120ns 150ns 200ns	

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

Note) This device is not available for new application.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. 3.5V for pulse width≤50ns

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−0.3*1	—	0.8	V

Note) *1. −3.0V for pulse width≤50ns.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116-2			HM6116-3/-4			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	—	—	10	—	—	10	μA
			—	—	2*3	—	—	2*3	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	—	—	10	—	—	10	μA
			—	—	2*3	—	—	2*3	
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
			—	35*3	70*3	—	30*3	60*3	
	I_{CC1}*2	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
			—	30*3	—	—	25*3	—	
Average Operating Current	I_{CC2}	Min. cycle, duty=100% $I_{I/O}$=0mA	—	40	80	—	35	70	mA
			—	35*3	70*3	—	30*3	60*3	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	5	15	—	5	15	mA
			—	4*3	12*3	—	4*3	12*3	
	I_{SB1}	$\overline{CS}$≥V_{CC}−0.2V, 0V≤V_{IN}≤0.2V or V_{CC}−0.2V≤V_{IN}	—	0.02	2	—	0.02	2	μA
			—	2*3	50*3	—	2*3	50*3	
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

Notes) *1. V_{CC}=5V, Ta=25°C
*2. Reference Only
*3. This characteristics are guaranteed only for L-version.

■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

●READ CYCLE

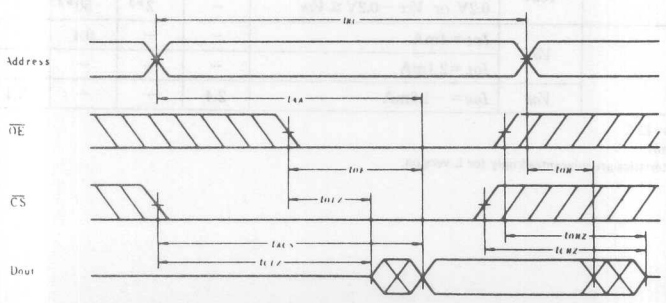
Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

●WRITE CYCLE

Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

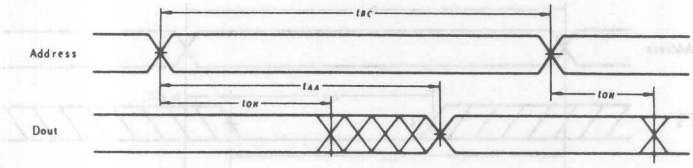
■TIMING WAVEFORM

●READ CYCLE (1)[1]

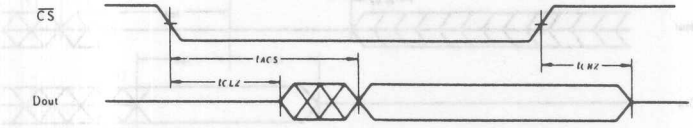


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● READ CYCLE (2)[1][2][4]

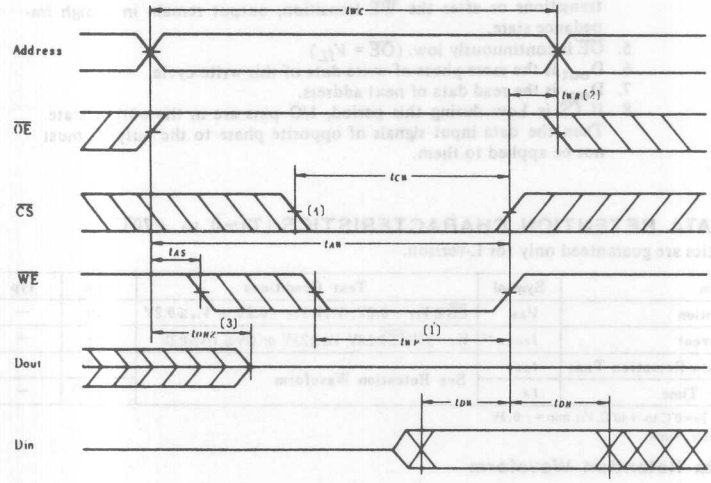


● READ CYCLE (3)[1][3][4]

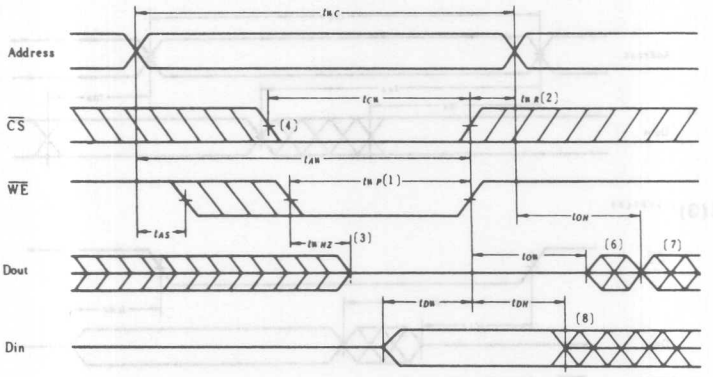


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE (1)



● WRITE CYCLE (2)[5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

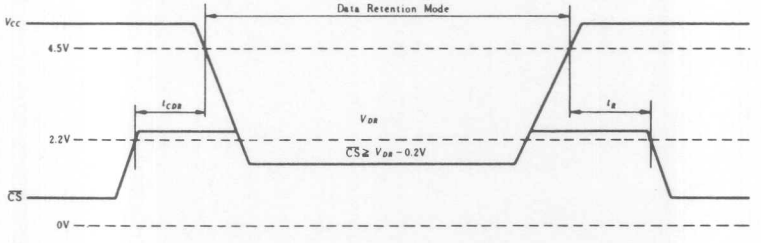
■ LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics are guaranteed only for L-version.

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*1	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $V_{IH} \geq 2.8V$ or $0V \leq V_{IN} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*2	—	—	ns

Notes) *1. 10μA max at $Ta = 0°C$ to $+40°C$, V_{IL} min $= -0.3V$
*2. t_{RC} = Read Cycle Time.

● Low Vcc Data Retention Waveform



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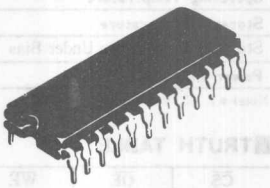
HM6116A Series — Maintenance Only

2048-word × 8-bit High Speed Static CMOS RAM

■ FURTURES

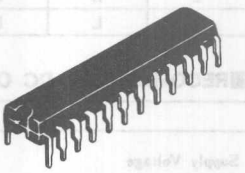
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
    5μW (typ.) (L-version)
  - Operation: 15mW (typ.) (f = 1 MHz)
    10 mW (typ.) (L-version)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116AP Series



(DP-24)

HM6116ASP Series

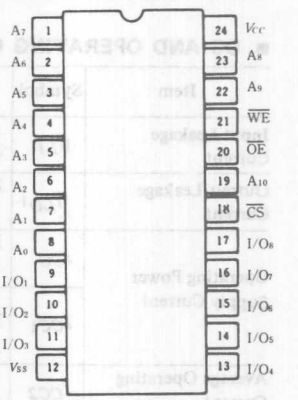


(DP-24N)

■ORDERING INFORMATION

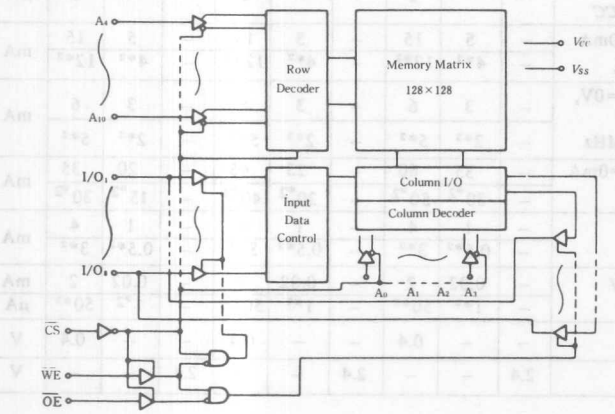
Type No.	Access Time	Package
HM6116AP-12	120ns	600mil 24pin Plastic DIP
HM6116AP-15	150ns	
HM6116AP-20	200ns	
HM6116ALP-12	120ns	
HM6116ALP-15	150ns	
HM6116ALP-20	200ns	
HM6116ASP-12	120ns	300mil 24pin Plastic DIP
HM6116ASP-15	150ns	
HM6116ASP-20	200ns	
HM6116ALSP-12	120ns	
HM6116ALSP-15	150ns	
HM6116ALSP-20	200ns	

■PIN ARRANGEMENT



(Top View)

■FUNCTIONAL BLOCK DIAGRAM



Note) This device is not available for new application.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.5V for pulse width≦50ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−0.3*1	—	0.8	V

Note) *1. −3.0V for pulse width≦50ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116A-12			HM6116A-15			HM6116A-20			Unit
			min	typ*1	max	min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=V_{SS} to V_{CC}	–	–	2	–	–	2	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2	–	–	2	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	5	15	–	5	15	–	5	15	mA
		V_{in}=V_{IH} or V_{IL}	–	4*2	12*2	–	4*2	12*2	–	4*2	12*2	
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V, $\overline{CS}$=V_{IL},	–	3	6	–	3	6	–	3	6	mA
		$I_{I/O}$=0mA, f=1MHz	–	2*2	5*2	–	2*2	5*2	–	2*2	5*2	
Average Operating Current	I_{CC2}	min. cycle, $I_{I/O}$=0mA	–	35	60	–	25	45	–	20	35	mA
		duty = 100%	–	30*2	50*2	–	20*2	40*2	–	15*2	30*2	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	1	4	–	1	4	–	1	4	mA
			–	0.5*2	3*2	–	0.5*2	3*2	–	0.5*2	3*2	
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} − 0.2V	–	0.02	2	–	0.02	2	–	0.02	2	mA
		0V ≦ Vin	–	1*2	50*2	–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	–	–	0.4	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	2.4	–	–	2.4	–	–	V

Notes) *1. V_{CC}=5V, T_a=25°C
*2. This characteristics is guaranteed only for L-version.

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■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

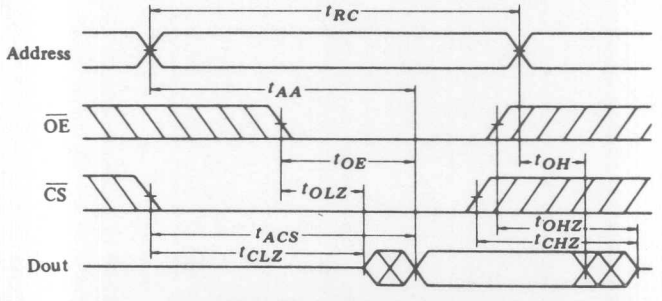
Item	Symbol	HM6116A-12		HM6116A-15		HM6116A-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Select Access Time	t_{ACS}	–	120	–	150	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output Valid	t_{OE}	–	55	–	60	–	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	20	–	ns

● WRITE CYCLE

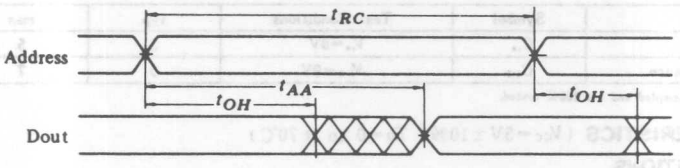
Item	Symbol	HM6116A-12		HM6116A-15		HM6116A-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

■TIMING WAVEFORM

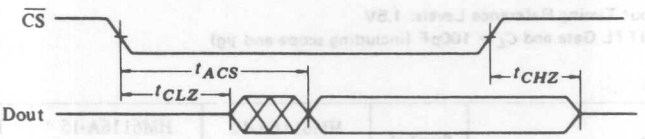
●READ CYCLE (1)[1]



● READ CYCLE (2) [1][2][4]

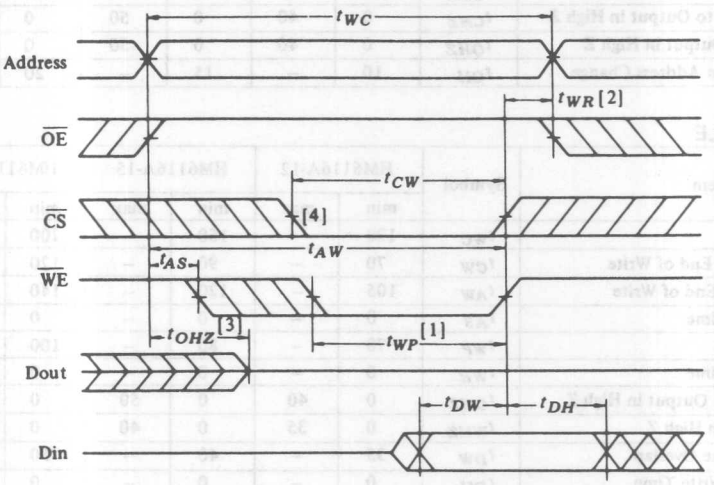


● READ CYCLE (3) [1][3][4]



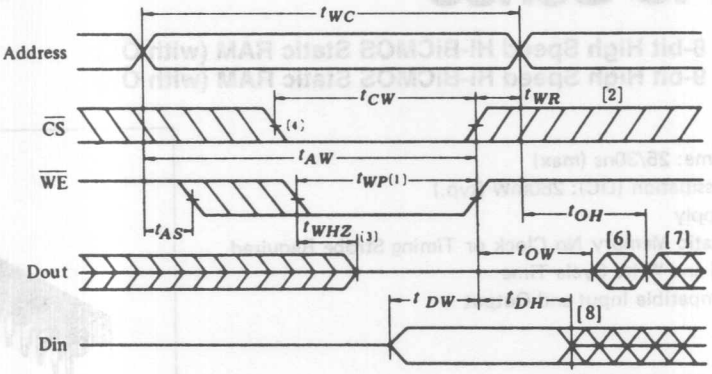
NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE(1)



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● WRITE CYCLE (2)[3]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

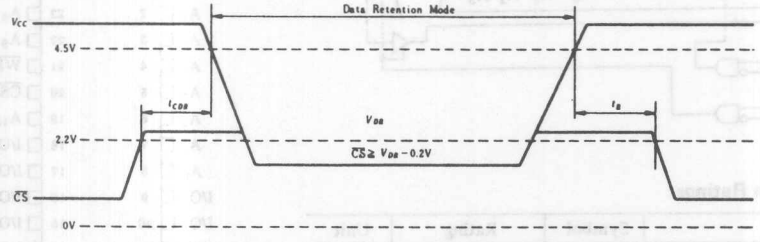
■ LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics is guaranteed only for L-version.

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*1	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $0V \leq V_{IN}$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*2	—	—	ns

Notes) *1. 10μA max at $Ta = 0°C$ to $+40°C$, V_{IL} min $= -0.3V$
*2. t_{RC} = Read Cycle Time.

● Low Vcc Data Retention Waveform

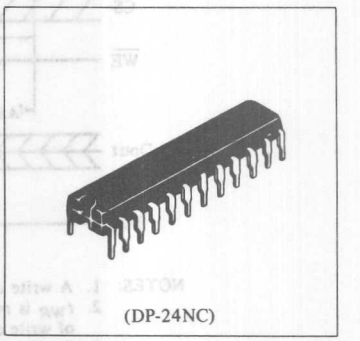


HM6716 Series
HM6719 Series

Maintenance Only

2048-word × 8-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)
2048-word × 9-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

- **Features**
- Fast Access Time: 25/30ns (max)
- Low Power Dissipation (DC): 280mW (typ.)
- +5V Single Supply
- Completely Static Memory No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

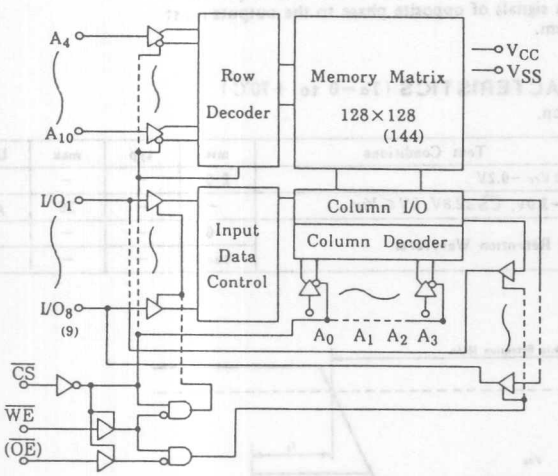


(DP-24NC)

■ ORDERING INFORMATION

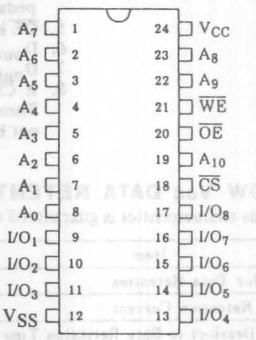
Type No.	Access Time	Package
HM6716P-25	25ns	300 mil 24 Pin Plastic DIP
HM6716P-30	30ns	
HM6719P-25	25ns	
HM6719P-30	30ns	

■ Block Diagram



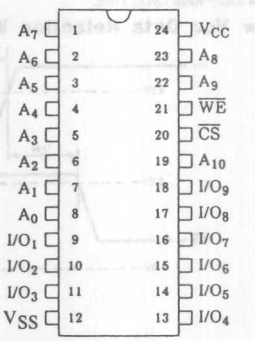
■ PIN ARRANGEMENT

● **HM6716**



(Top View)

● **HM6719**



(Top View)

■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ Truth Table

• HM6716

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–

• HM6719

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (2) (3)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

■ Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}*)	−3.0	–	0.8	V

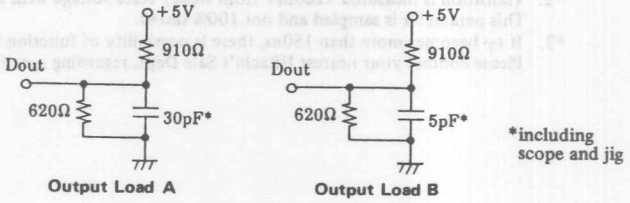
*) Pulse Width: 20ns, DC: −0.5V

■ DC and Operating Characteristics (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{IN}= V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	–	120	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}$=0mA	–	–	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}$−0.2V $V_{IN} \leqq$ 0.2V or $V_{IN} \geqq V_{CC}$−0.2V	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA	2.4	–	–	V

■ AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input and Output reference levels: 1.5V
Input rise and fall time: 4ns
Output Load: See Figure



(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW}, t_{OLZ}, t_{OHZ})

■ Capacitance (T_a = 25°C, f = 1.0 MHz)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	–	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	8	pF

Note) This parameter is sampled and not 100%, tested.

■ AC Characteristics (V_{CC} 5V ± 10%, T_a = 0 to +70°C, unless otherwise noted.)

● Read Cycle

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	–
Address Access Time	t_{AA}	–	25	–	30	ns	–
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	–
Chip Selection to Output in Low Z	t_{CLZ}	0	–	0	–	ns	*2
Output Enable to Output Valid	t_{OE}	0	20	0	20	ns	*1
Output Enable to Output in Low Z	t_{OLZ}	0	–	0	–	ns	*1, *2
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	*2
Chip Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	*3

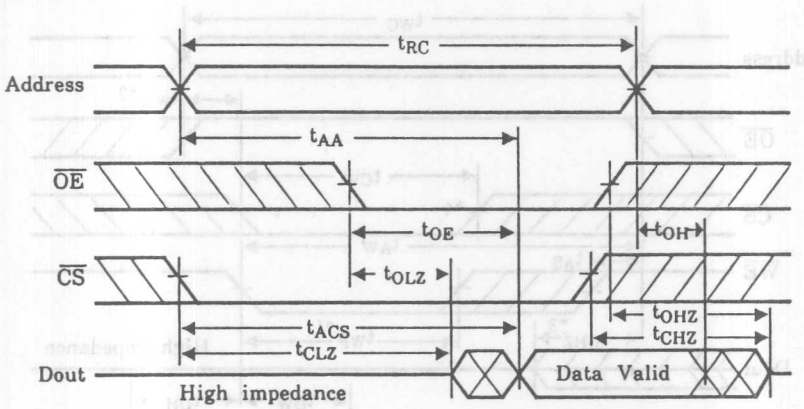
● Write Cycle

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	25	–	30	–	ns	–
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	–
Write Pulse Width	t_{WP}	20	–	25	–	ns	–
Write Recovery Time	t_{WR}	0	–	0	–	ns	–
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns	*2
Data Valid to End of Write	t_{DW}	15	–	15	–	ns	–
Data Hold Time	t_{DH}	5	–	5	–	ns	–
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*2

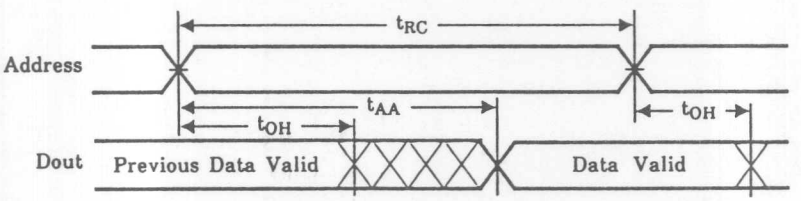
Notes) *1. These parameters are for HM6716.
*2. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
*3. If t_T becomes more than 150ns, there is possibility of function fail. Please contact your nearest Hitachi's Sale Dept. regarding specification.

■ Timing Waveforms

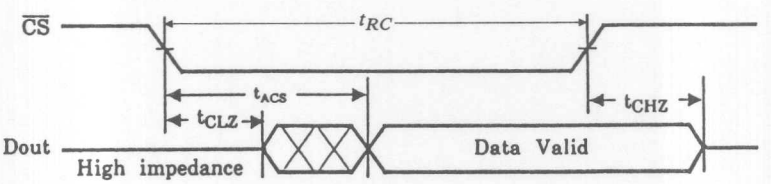
● Read Cycle (1)*1



● Read Cycle (2)*1,*2,*4

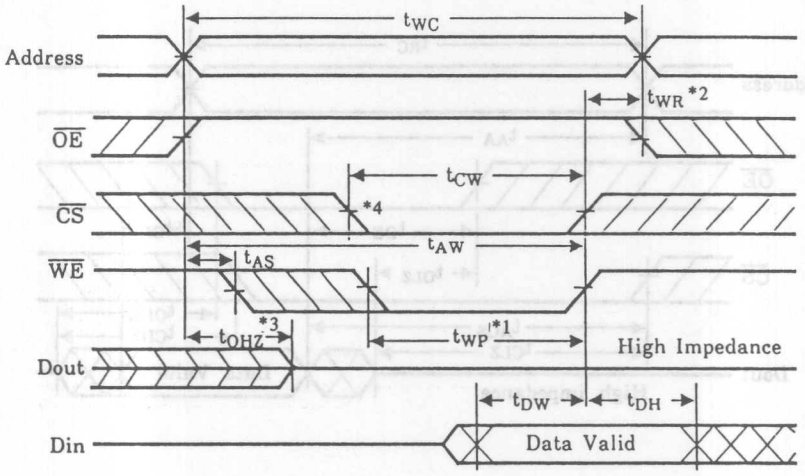


● Read Cycle (3)*1,*3,*4

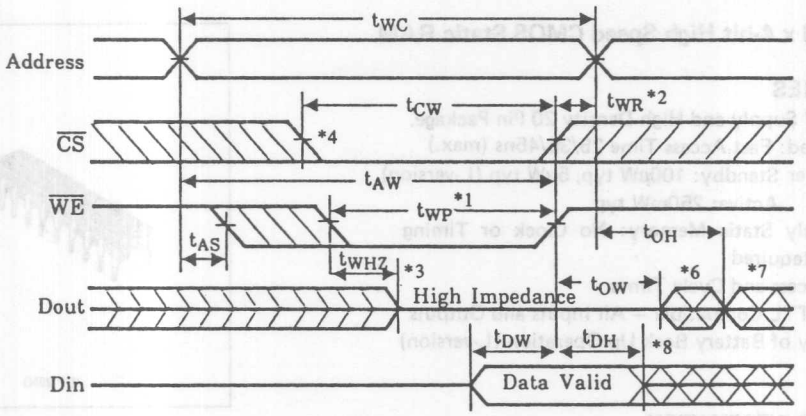


Notes) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}=V_{IL}$.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
*4. $\overline{OE}=V_{IL}$.

- **Write Cycle (1)**



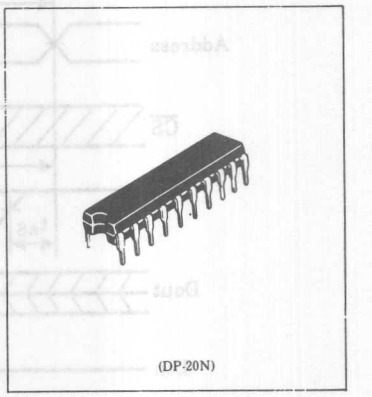
- **Write Cycle (2)**[*5]



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL}).
*6. Dout is the same phase of write data of this write cycle.
*7. Dout is the read data of next address.
*8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6268 Series

4096-word x 4-bit High Speed CMOS Static RAM



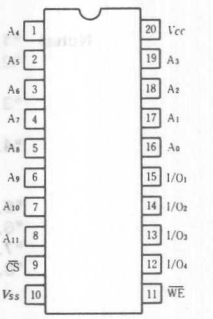
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35/45ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

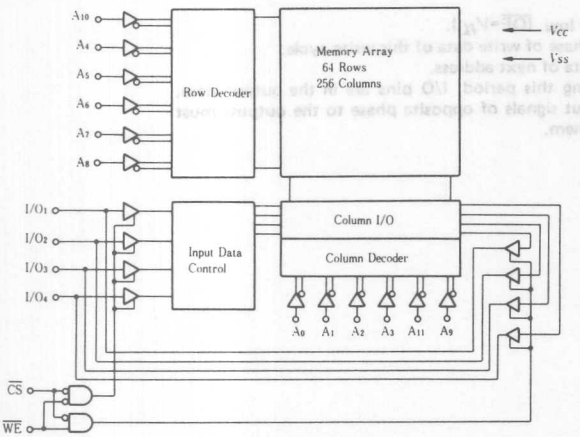
Type No.	Access Time	Package
HM6268P-25	25ns	300mil 20pin Plastic DIP
HM6268P-35	35ns	
HM6268P-45	45ns	
HM6268LP-25	25ns	
HM6268LP-35	35ns	
HM6268LP-45	45ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≦10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta=0 to +70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C

Parameter	Symbol	Test Condition	Min.	Typ.*1	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, min. cycle	–	50*3	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≥ V_{CC} −0.2V,	–	0.02	2.0	mA
		0V ≤ V_{IN} ≤ 0.2V or V_{CC} − 0.2V ≤ V_{IN}	–	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, Ta= +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. 40mA typ. for 45ns version.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

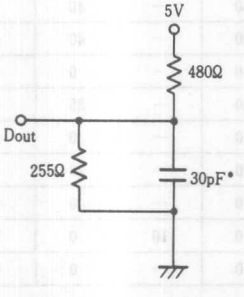
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	9	pF

Note: This parameter is sampled and not 100% tested.

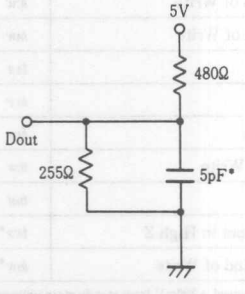
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃, unless otherwise noted.)

- **AC Test Conditions**
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



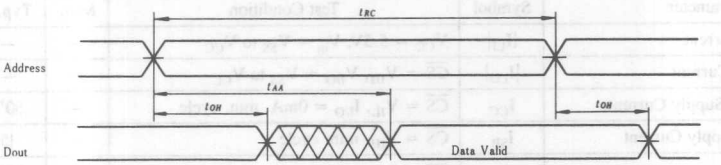
*Including scope and jig.

● READ CYCLE

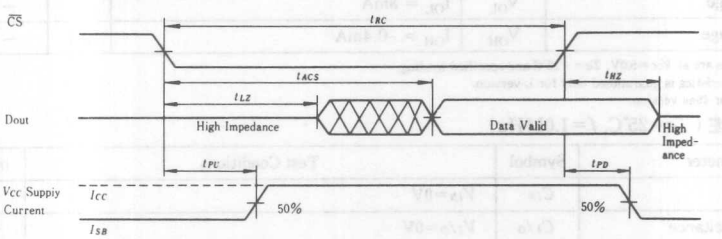
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*1	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	—	30	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1 (1),(2)



● Timing Waveform of Read Cycle No. 2 (1),(3)



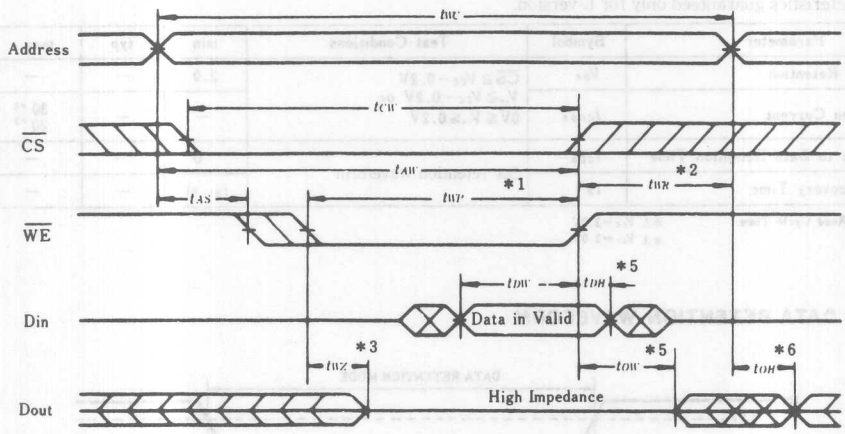
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

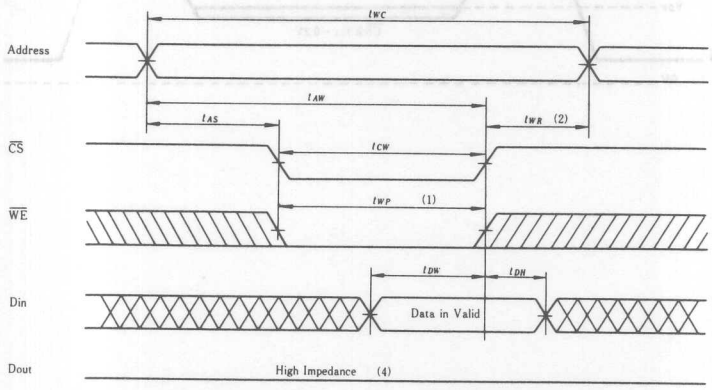
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}*1	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*1	0	—	0	—	0	—	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

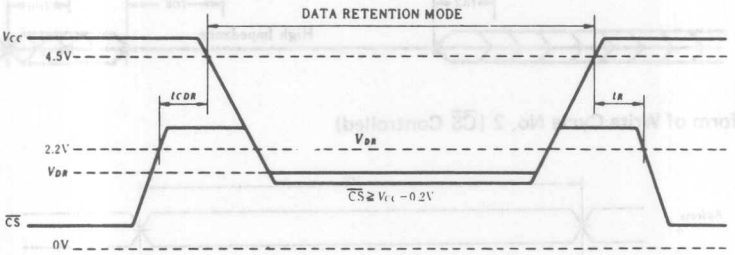
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leq Ta \leq 70°C$)

This characteristics guaranteed only for L-version.

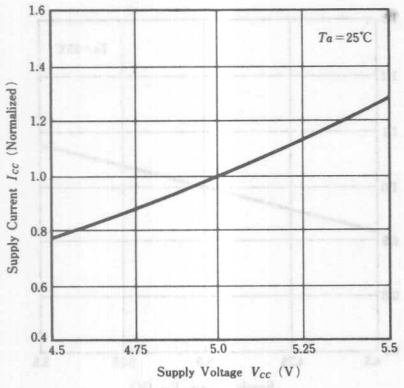
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V *3. V_{CC} = 2.0V

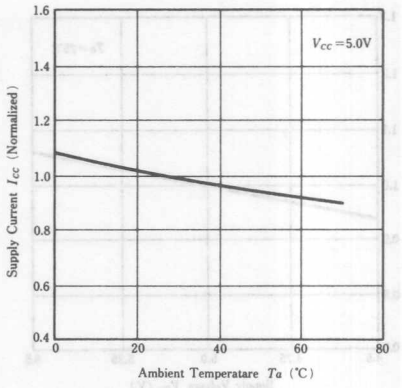
●LOW V_{CC} DATA RETENTION WAVEFORM



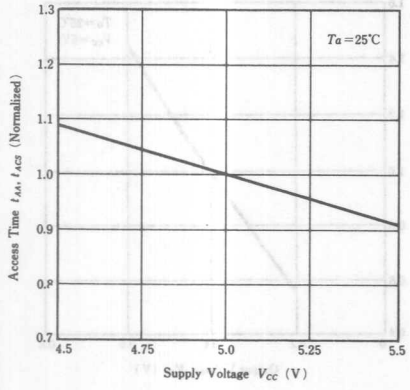
SUPPLY CURRENT VS. SUPPLY VOLTAGE



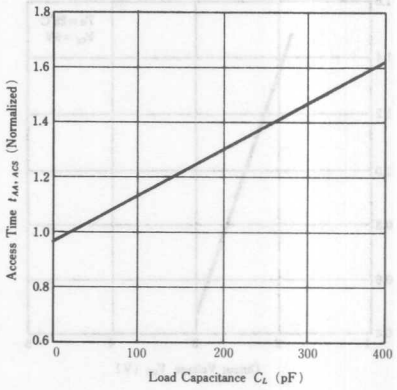
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



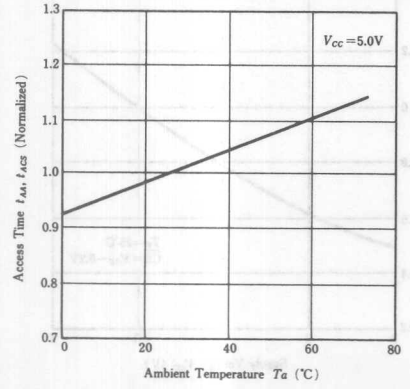
ACCESS TIME VS. SUPPLY VOLTAGE



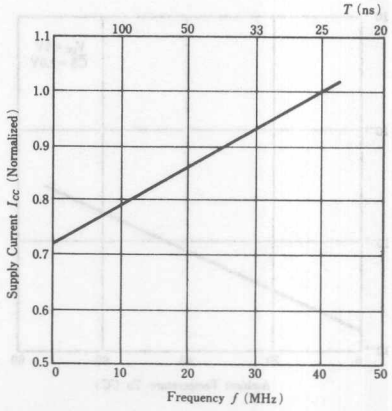
ACCESS TIME VS. LOAD CAPACITANCE



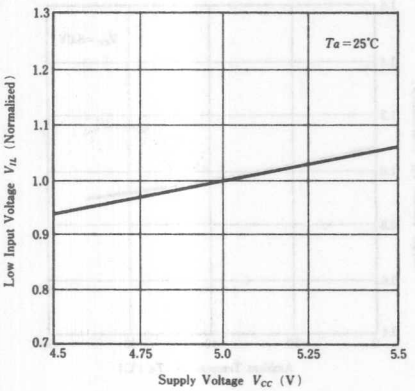
ACCESS TIME VS. AMBIENT TEMPERATURE



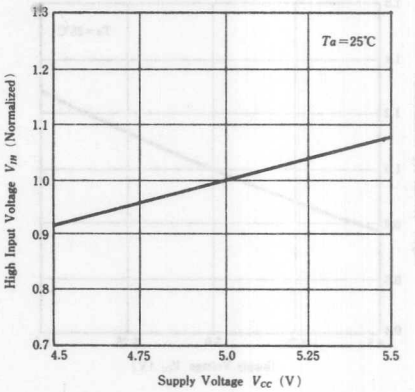
SUPPLY CURRENT VS. FREQUENCY



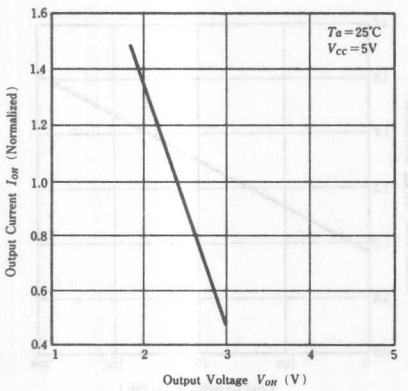
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



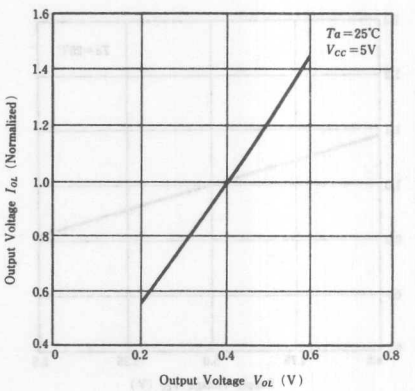
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



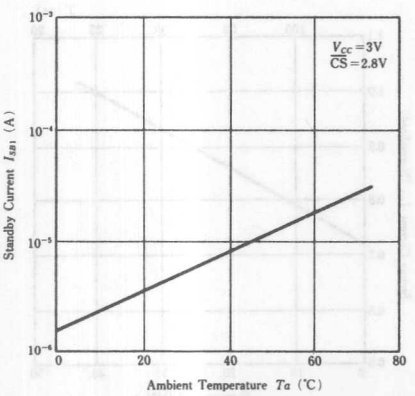
OUTPUT CURRENT VS. OUTPUT VOLTAGE



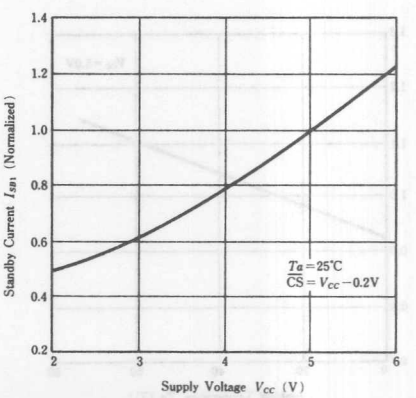
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE

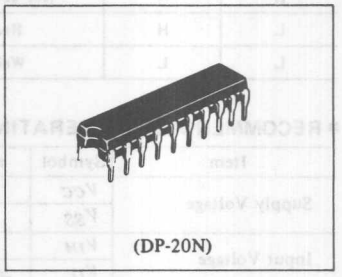


HM6267 Series

16384-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

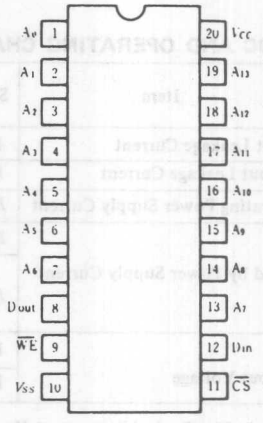


(DP-20N)

■ ORDERING INFORMATION

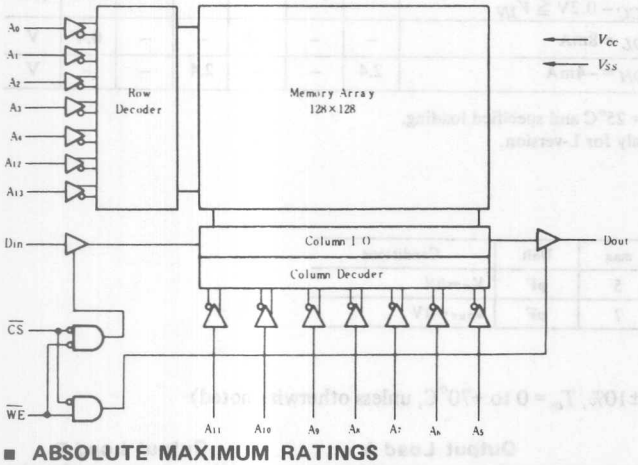
Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plactic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	
HM6267LP-55	55ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	V_T	-0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

Notes) *1. With respect ot V_{SS}.
*2. -3.5V for pulse width ≦ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA, min. cycle	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, min cycle	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} − 0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{IN}	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = −4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

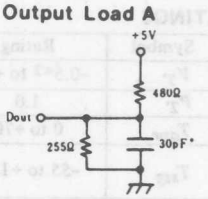
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

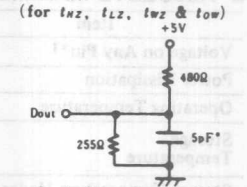
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

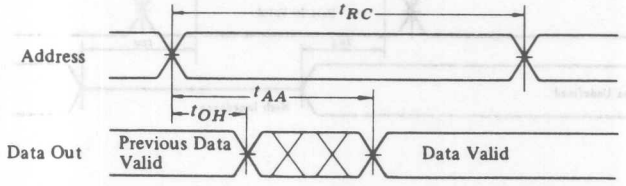


* Including scope and jig.

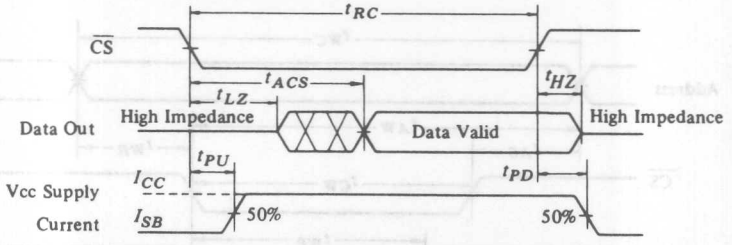
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	-	45	–	55	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	-	55	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2,3,7
Chip Deselectio to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	–	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

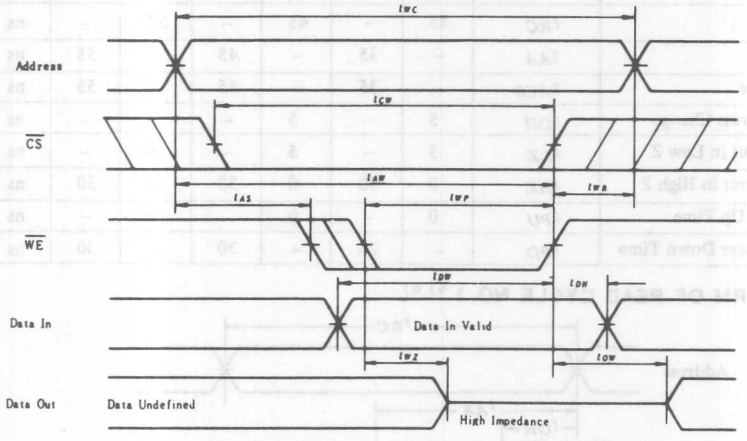


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

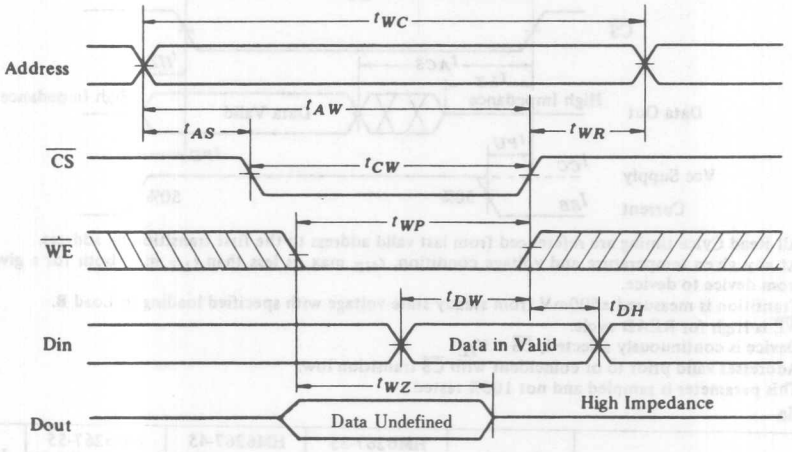
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	55	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3,4

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

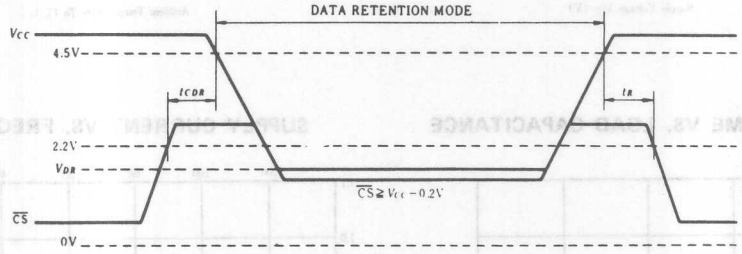
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

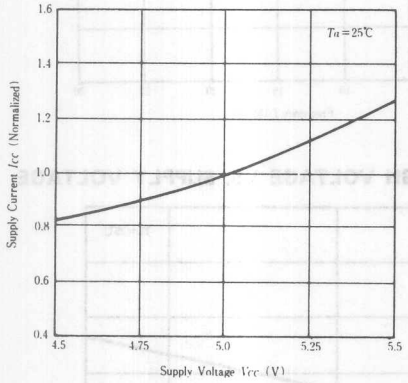
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}	see retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V *3. V_{CC} = 2.0V

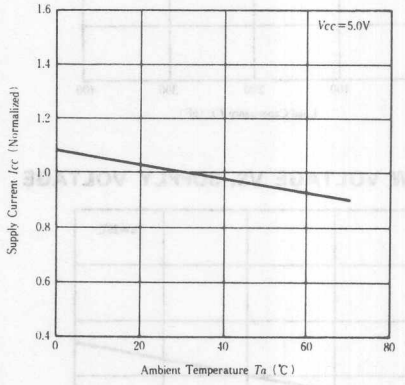
●LOW V_{CC} DATA RETENTION WAVEFORM



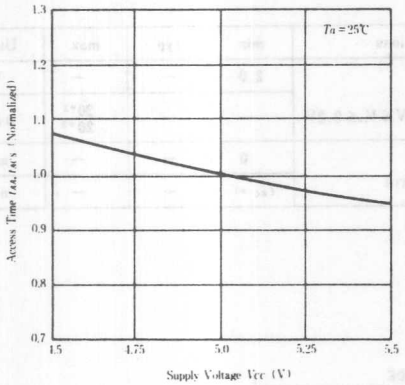
SUPPLY CURRENT VS. SUPPLY VOLTAGE



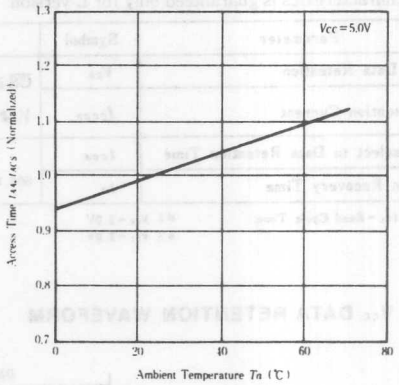
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



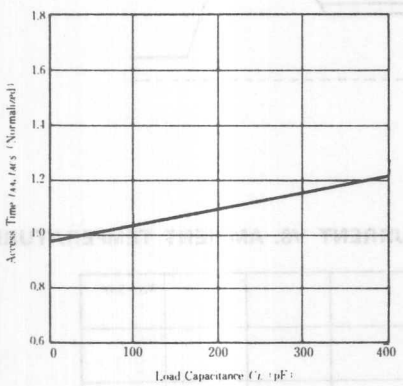
ACCESS TIME VS. SUPPLY VOLTAGE



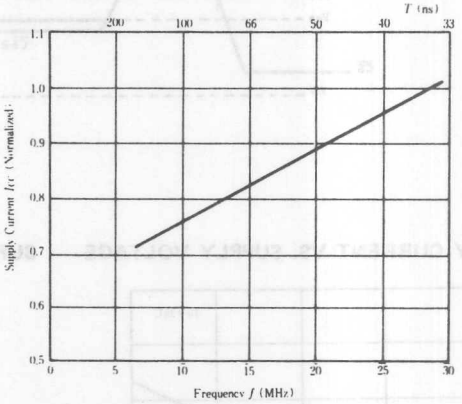
ACCESS TIME VS. AMBIENT TEMPERATURE



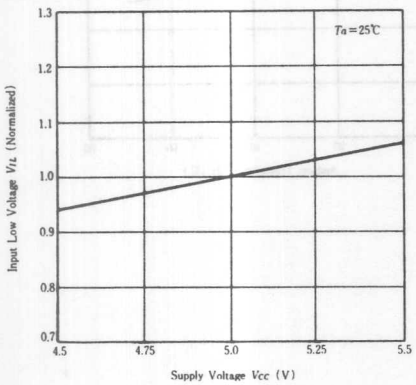
ACCESS TIME VS. LOAD CAPACITANCE



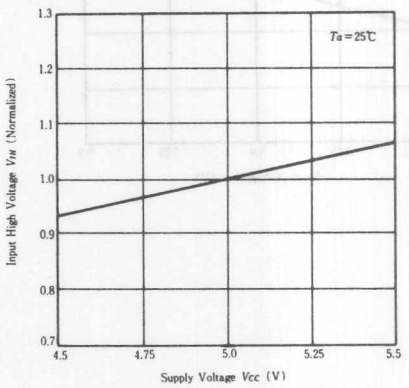
SUPPLY CURRENT VS. FREQUENCY



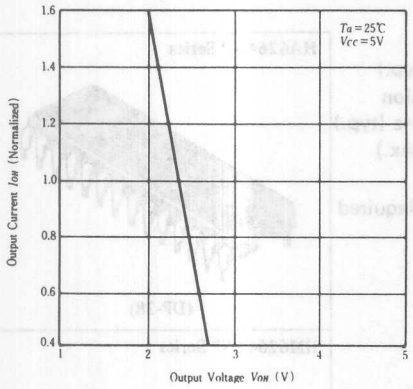
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



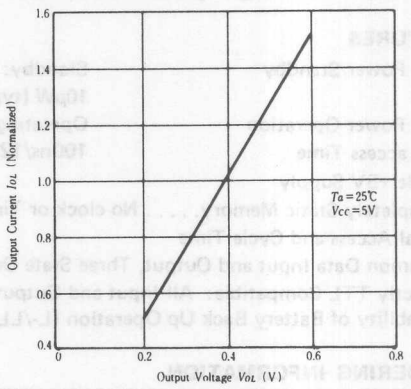
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



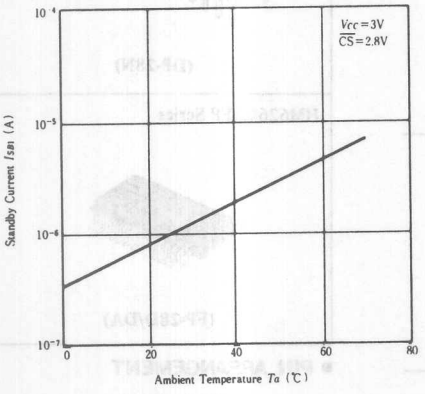
OUTPUT CURRENT VS. OUTPUT VOLTAGE



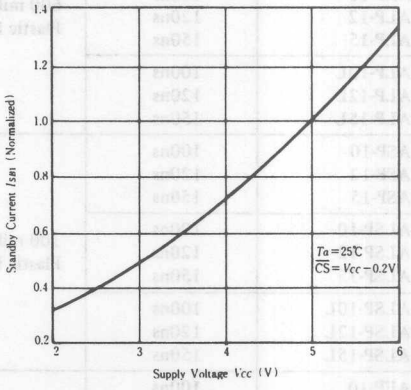
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



HM6264A Series — Maintenance Only

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

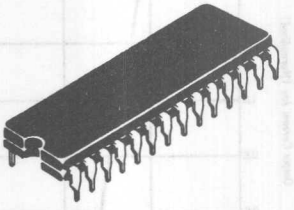
- Low Power Standby — Standby: 0.1mW (typ.) / 10μW (typ.) L-/LL-version
- Low Power Operation — Operating: 15mW/MHz (typ.)
- Fast access Time — 100ns/120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/LL-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6264AP-10	100ns	600 mil 28 pin Plastic DIP
HM6264AP-12	120ns	
HM6264AP-15	150ns	
HM6264ALP-10	100ns	
HM6264ALP-12	120ns	
HM6264ALP-15	150ns	
HM6264ALP-10L	100ns	
HM6264ALP-12L	120ns	
HM6264ALP-15L	150ns	
HM6264ASP-10	100ns	300 mil 28 pin Plastic DIP
HM6264ASP-12	120ns	
HM6264ASP-15	150ns	
HM6264ALSP-10	100ns	
HM6264ALSP-12	120ns	
HM6264ALSP-15	150ns	
HM6264ALSP-10L	100ns	
HM6264ALSP-12L	120ns	
HM6264ALSP-15L	150ns	
HM6264AFP-10	100ns	28 pin Plastic SOP (Note)
HM6264AFP-12	120ns	
HM6264AFP-15	150ns	
HM6264ALFP-10	100ns	
HM6264ALFP-12	120ns	
HM6264ALFP-15	150ns	
HM6264ALFP-10L	100ns	
HM6264ALFP-12L	120ns	
HM6264ALFP-15L	150ns	

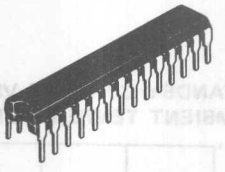
Note) T is added to the end of the type no. for a SOP of 3.00 mm (max.) thickness.

HA6264AP Series



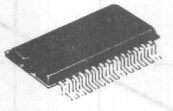
(DP-28)

HM6264ASP Series



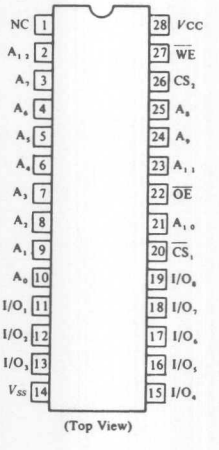
(DP-28N)

HM6264AFP Series



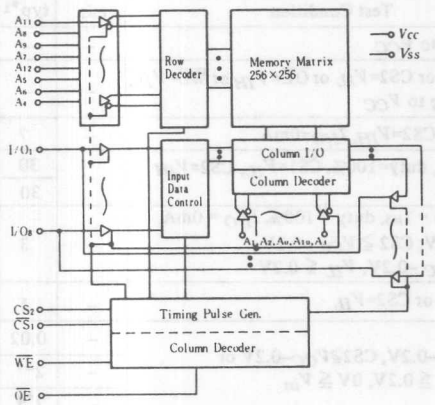
(FP-28D/DA)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage*1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}.
*2. −3.0V for pulse width ≦ 50ns

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB},I_{SB1}	
X	X	L	X		High Z	I_{SB},I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read Cycle
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	--	6.0	V
	V_{IL}	−0.3*1	--	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{in}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}=V_{IL}$, CS2=V_{IH} $I_{I/O}$=0mA	–	30	45*5	mA
				30	55*6	
	I_{CC2}	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0mA, $\overline{CS1} \leqq 0.2V$, CS2 $\geqq V_{CC}-0.2V$ $V_{IH} \geqq V_{CC}-0.2V$, $V_{IL} \leqq 0.2V$	–	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1} \geqq V_{CC}-0.2V$, CS2$\geqq V_{CC}-0.2V$ or $0V \leqq OS2 \leqq 0.2V$, $0V \leqq V_{in}$	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=–0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This characteristics is guaranteed only for LL-version.
*5. For 120ns/150ns version.
*6. For 100ns version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• **AC TEST CONDITIONS**

Input Pulse Levels: 0.8V/2.4V
Input Rise and Fall Time: 10ns
Input Timing Reference Level: 1.5V
Output Timing Reference Level: 0.8V/2.0V
Output Timing Reference Level: HM6264A-10 1.5V
HM6264A-12/15 0.8V/2.0V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

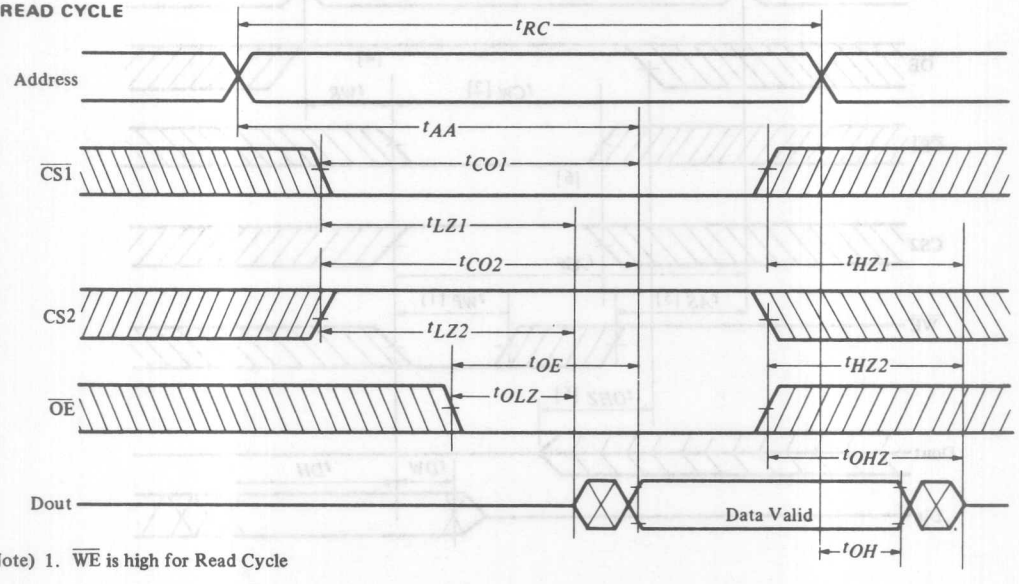
HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

• READ CYCLE

Item		Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	10	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from d device to device.

• READ CYCLE

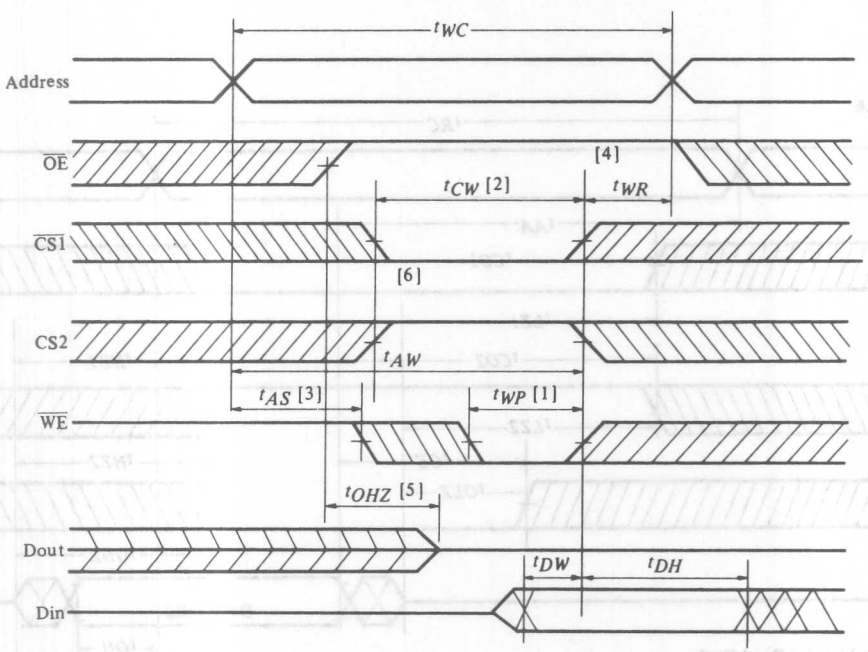


Note) 1. $\overline{WE}$ is high for Read Cycle

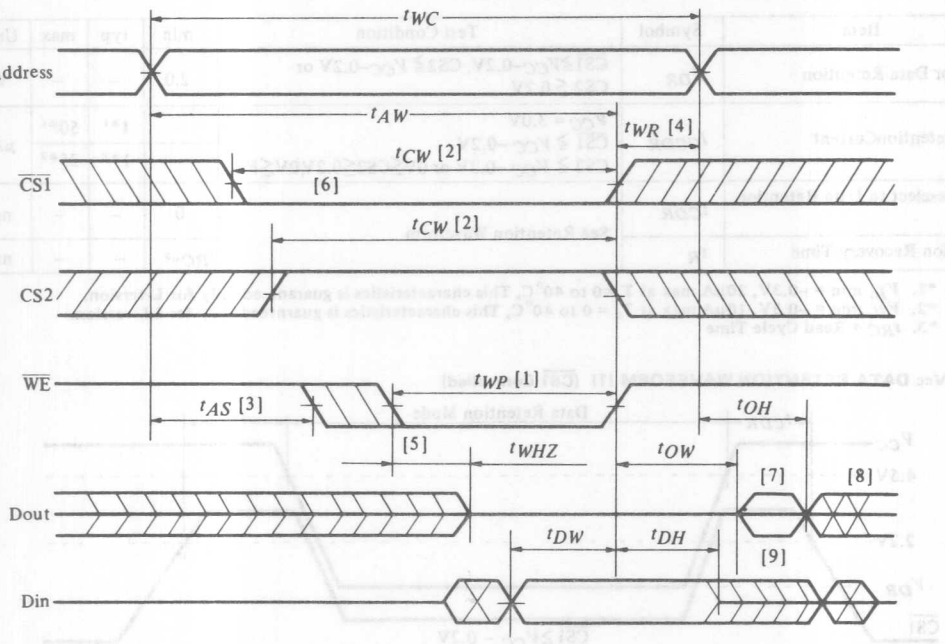
• WRITE CYCLE

Item	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	80	–	85	–	100	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width	t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Enable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

• WRITE CYCLE (1) ($\overline{OE}$ clock)



• WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES:
1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

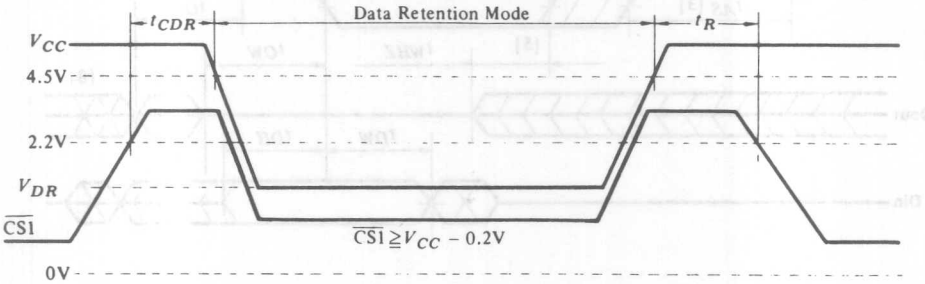
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

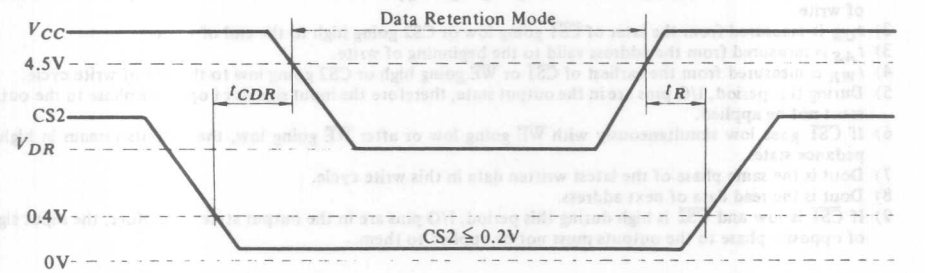
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
Data RetentionCurrent	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $0V \leqq CS2 \leqq 0.2V, 0V \leqq V_{in}$	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = −0.3V, 20μA max at T_a=0 to 40°C, This characteristics is guaranteed only for L-version.
*2. V_{IL} min = −0.3V, 10μA max at T_a = 0 to 40°C, This characteristics is guarnteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

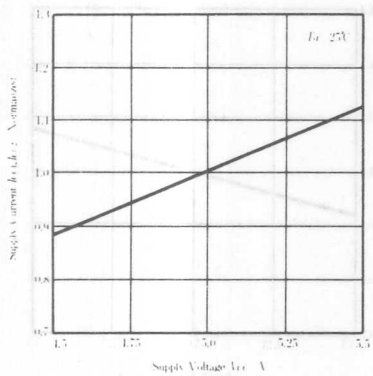


• LOW V_{CC} DATA RETENTION WAVEFORM (2) (CS2 Controlled)

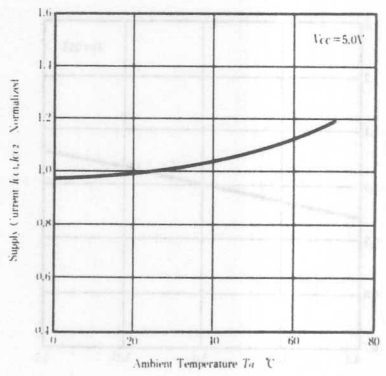


Note) In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

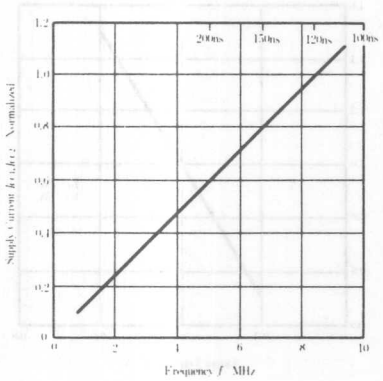
SUPPLY CURRENT VS. SUPPLY VOLTAGE



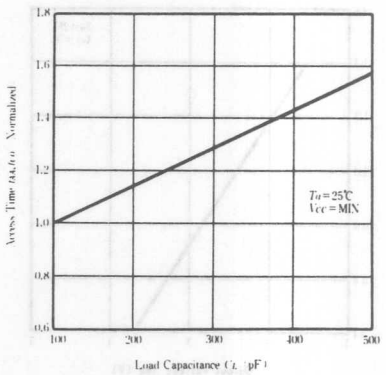
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



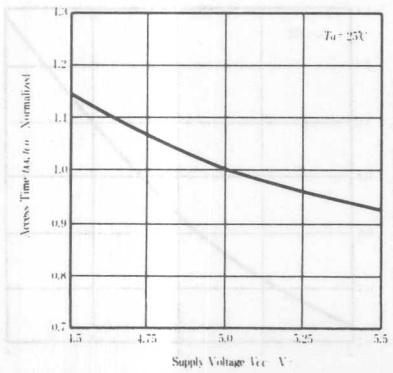
SUPPLY CURRENT VS. FREQUENCY



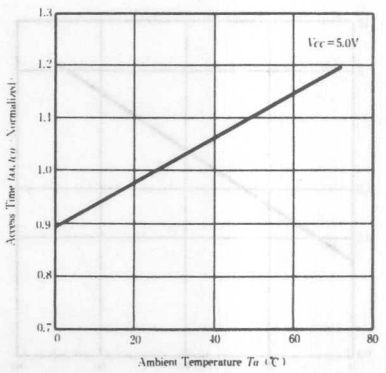
ACCESS TIME VS. LOAD CAPACITANCE



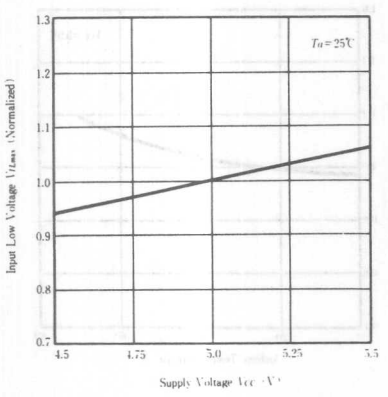
ACCESS TIME VS. SUPPLY VOLTAGE



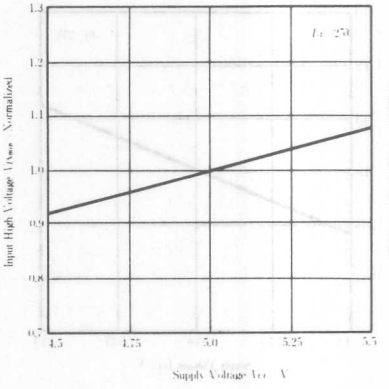
ACCESS TIME VS. AMBIENT TEMPERATURE



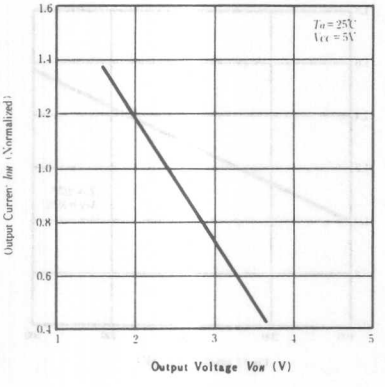
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



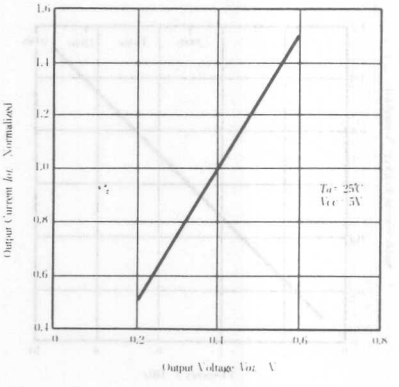
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



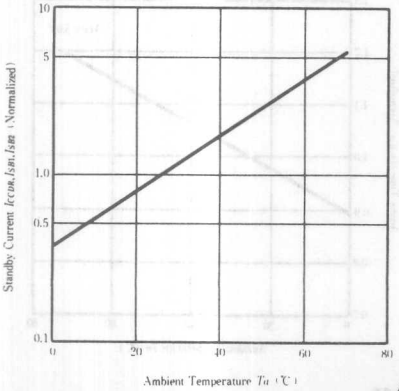
OUTPUT CURRENT VS. OUTPUT VOLTAGE



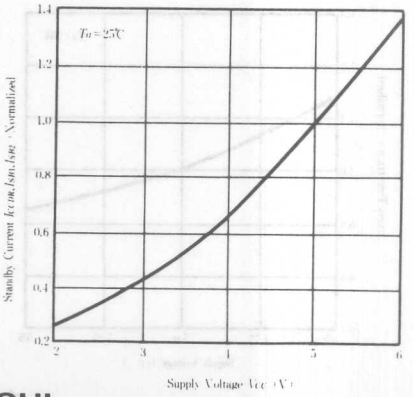
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



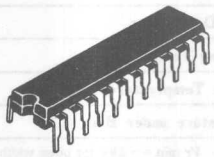
HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6288, packaged in a 300 mil plastic DIP and SOJ, is available for high density mounting. Low power version retains the data with battery back up.



(DP-22NB)



(CP-24D)

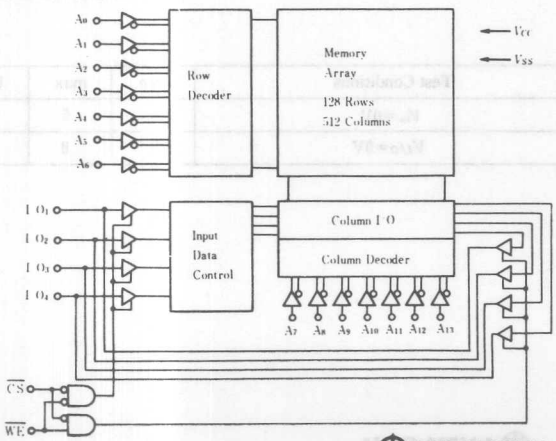
■FEATURES

- Single 5V Supply and High Density Plastic Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active mode 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

■ ORDERING INFORMATION

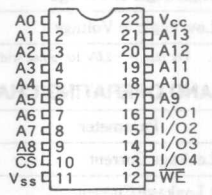
Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25ns 35ns	300 mil 22-pin Plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25ns 35ns	
HM6288JP-25 HM6288JP-35	25ns 35ns	300 mil 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25ns 35ns	

■BLOCK DIAGRAM



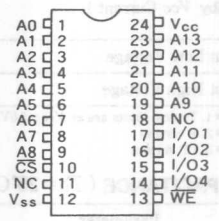
■PIN ARRANGEMENT

- HM6288P Series



(Top View)

- HM6288JP Series



(Top View)

■Pin Description

Pin Name	Function
A0 – A13	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

HITACHI

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: *1. V_T min.= −2.0V for pulse width≦10ns

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	-
L	H	Read	I_{CC}	Dout	Read'Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	–	0.8	V

Note: *1. V_{IL} min.= −2.0V for pulse width≦10ns

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=MAX. $V_{IN}=V_{SS}$ to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA, min. cycle	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS}=V_{IH}$, min. cycle	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS}\geqq V_{CC}-0.2V$	–	0.02	2.0	mA
	I_{SB1}*3	$0V\leqq V_{IN}\leqq 0.2V$ or $V_{CC}-0.2V\leqq V_{IN}$	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}= −4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. P version
*3. LP version

■CAPACITANCE (Ta=25°C, f=1.0MHz)

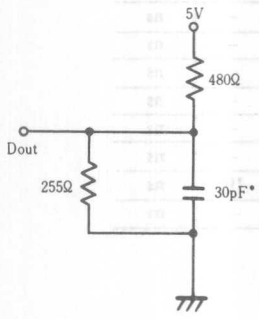
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameter is sampled and not 100% tested

■AC CHARACTERISTICS

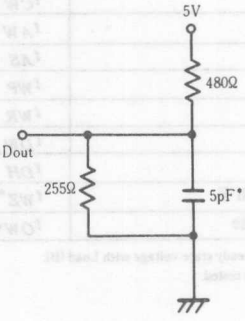
- AC Test Conditions

Input pulse levels: 0V to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure



Output Load (A)

*Including scope & jig.



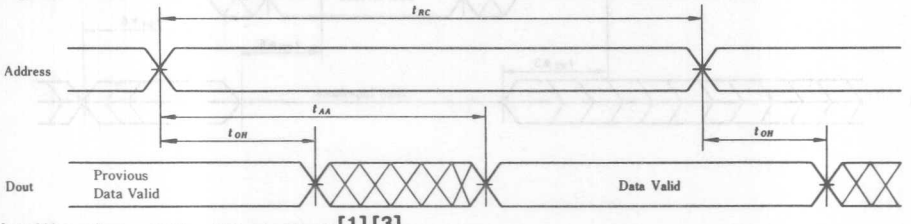
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

■ READ CYCLE

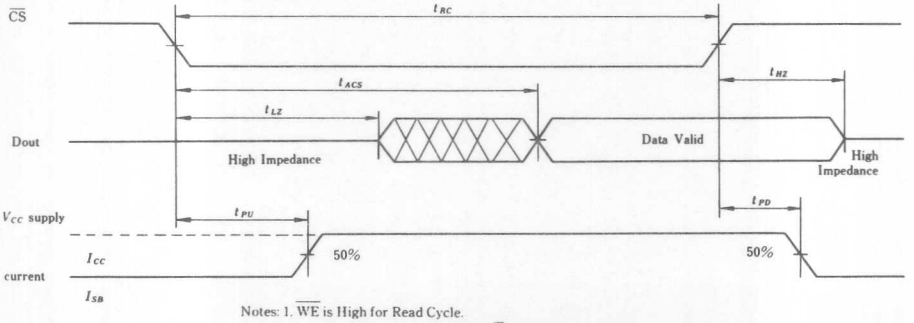
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load(B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



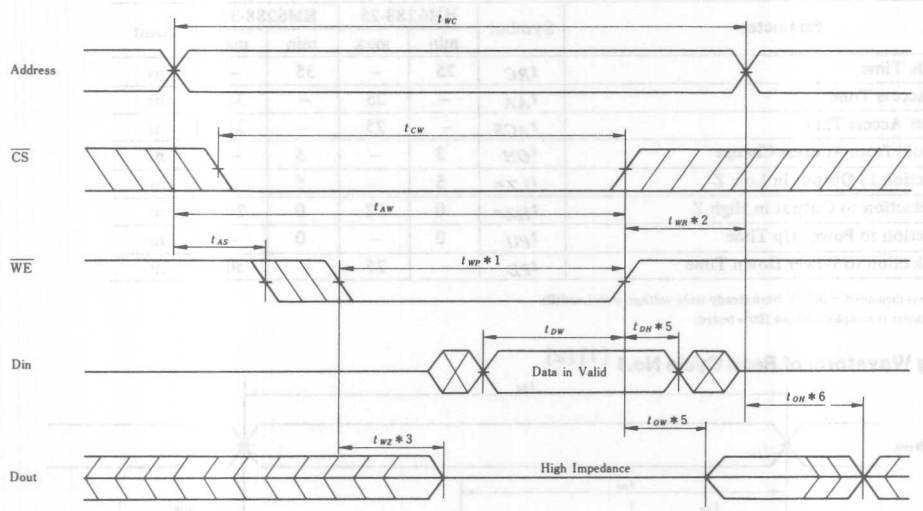
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

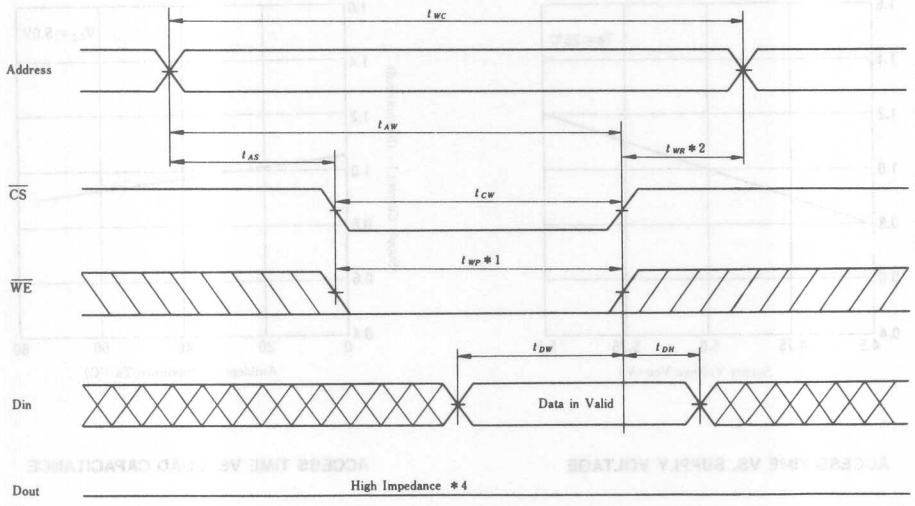
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ}*	0	8	0	10	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

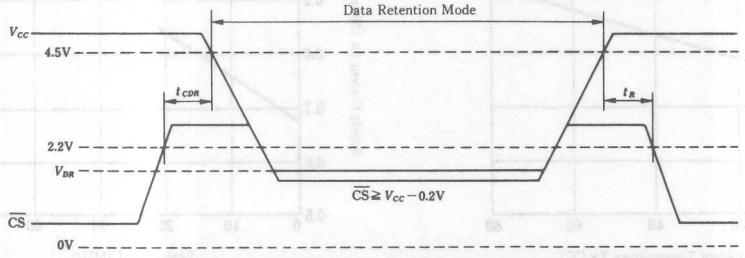
● Low *Vcc* Data Retention Characteristics ($Ta = 0$ to $+70°C$)

(This Characteristics is guaranteed only for L-version.)

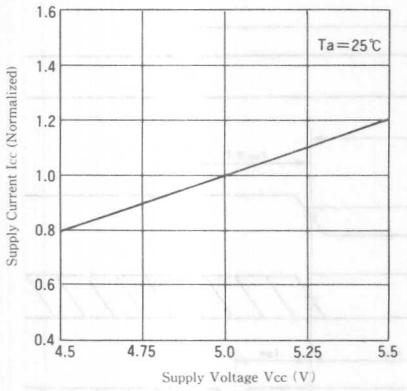
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data retention current	I_{CCDR}	–	–	50[2] 35[3]	μA	
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[1]	–	–	ns	

NOTE : 1. t_{RC} = Read cycle time
2. $V_{CC} = 3.0V$
3. $V_{CC} = 2.0V$

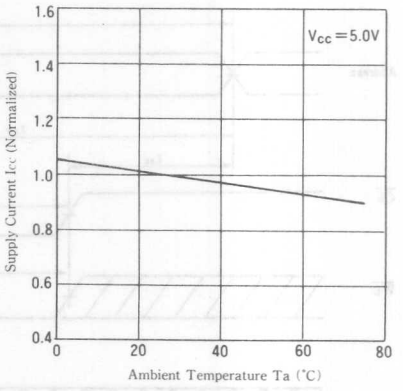
Low *Vcc* Data Retention Waveform



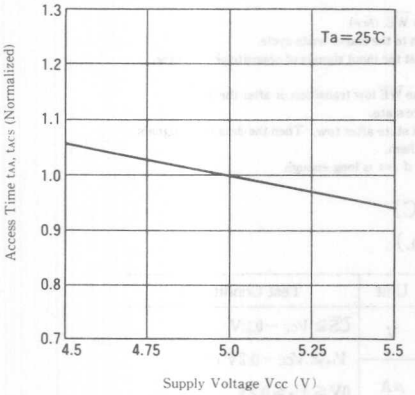
SUPPLY CURRENT VS. SUPPLY VOLTAGE



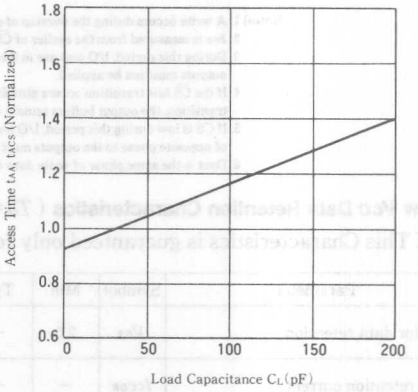
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



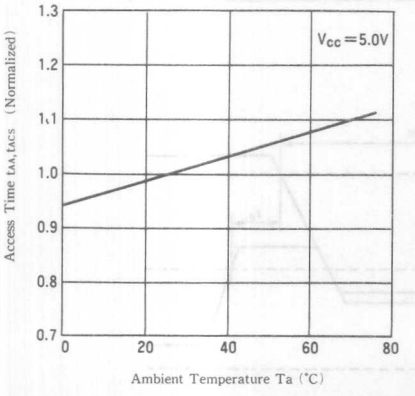
ACCESS TIME VS. SUPPLY VOLTAGE



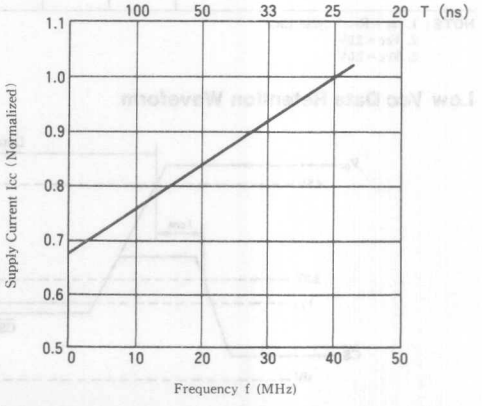
ACCESS TIME VS. LOAD CAPACITANCE



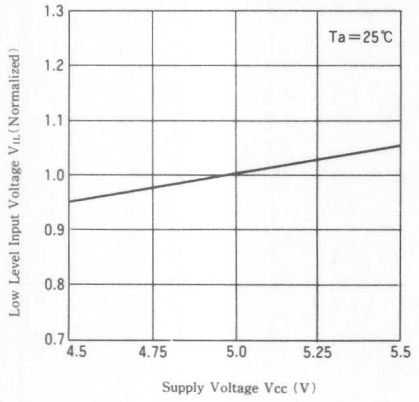
ACCESS TIME VS. AMBIENT TEMPERATURE



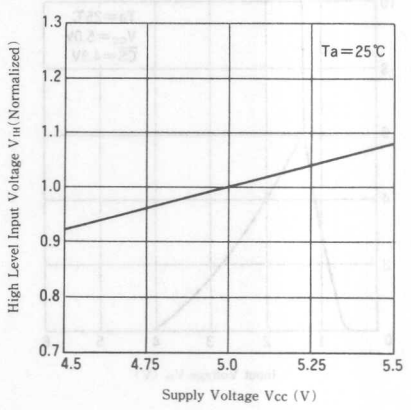
SUPPLY CURRENT VS. FREQUENCY



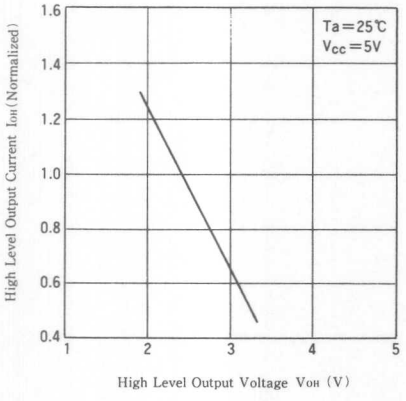
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



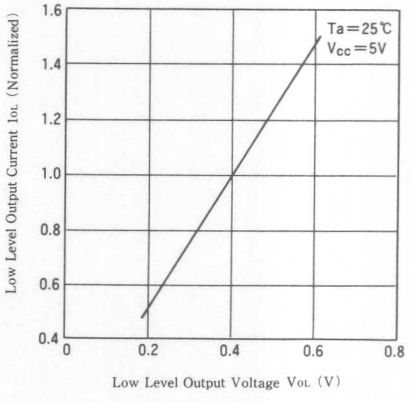
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



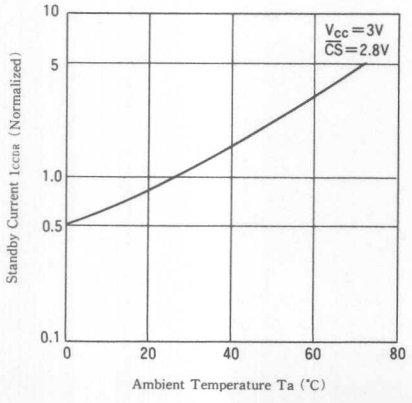
OUTPUT CURRENT VS. OUTPUT VOLTAGE(1)



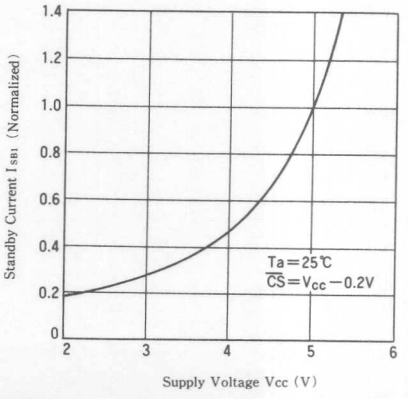
OUTPUT CURRENT VS. OUTPUT VOLTAGE(2)



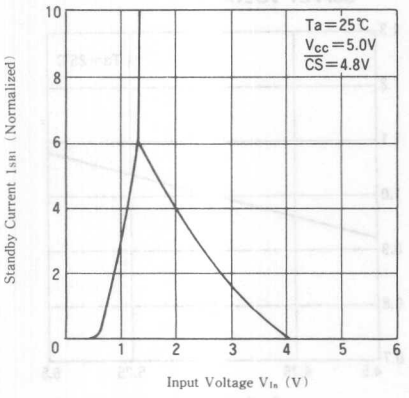
STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE

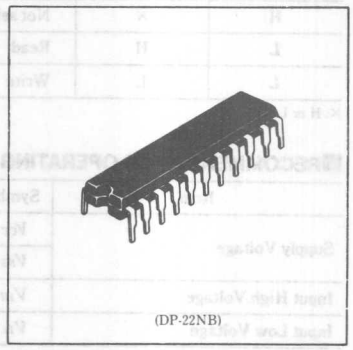


HM6788 Series — Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

■FEATURES

- Super Fast Access Time : 25/30ns (max.)
- Low power Operation
  Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory —
  No Clock or Timing Strobe required
- Balanced Read and Write Cycle Time
- Fully TTL compatible Input and Output

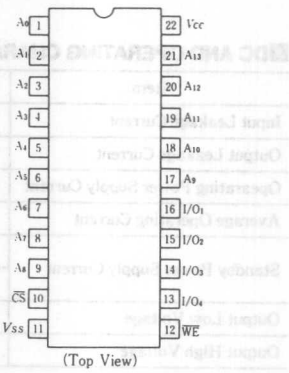


(DP-22NB)

■ ORDERING INFORMATION

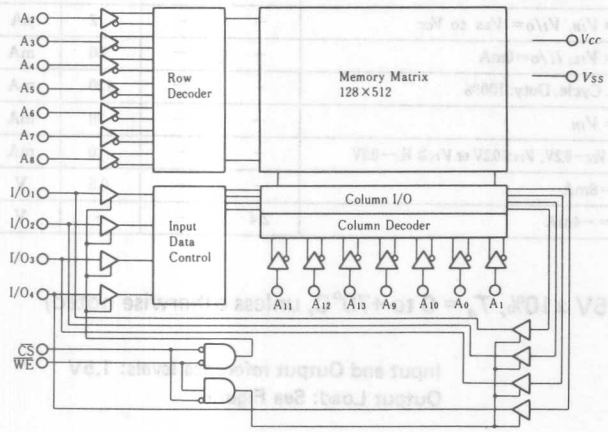
Type No.	Access Time	Package
HM6788P-25	25ns	300 mil 22 pin Plastic DIP
HM6788P-30	30ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

×: H or L

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 20ns pulse width.

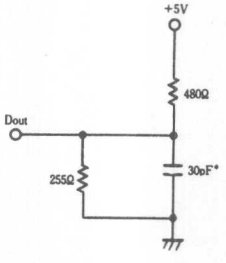
■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.5	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

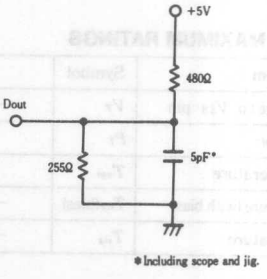
■AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

Input pulse levels: V_{SS} to 3.0V
Input rise and fall time: 4ns
Input and Output reference levels: 1.5V
Output Load: See Figure



Output Load A



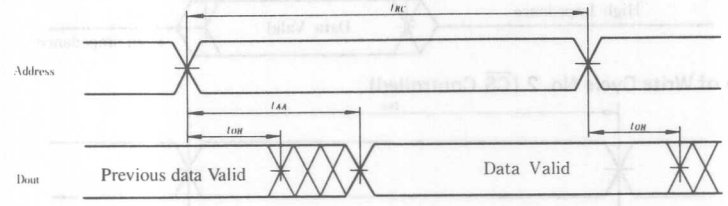
Output Load B
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW})

● READ CYCLE

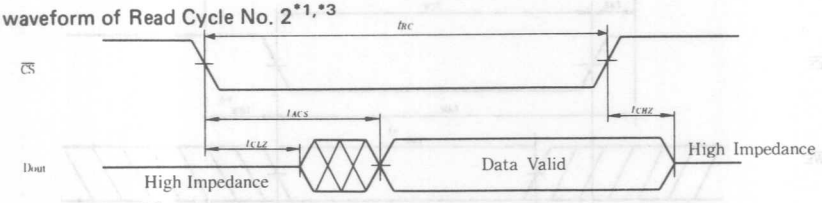
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Address Access Time	t_{AA}	—	25	—	30	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ} *2	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ} *2	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time*1	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time*1	t_{PD}	—	20	—	30	ns
Input Voltage Rise/Fall Time*3	t_r	—	150	—	150	ns

Notes) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV form steady state voltage with Load (B). This parameter is sampled and not 100% tested
*3. If tr becomes more than 150ns, there is possibility of function fail.
please contact your nearest Hitachi Sales Dept. regarding specification.

● Timing waveform of Read Cycle No. 1 *1,*2



● Timing waveform of Read Cycle No. 2 *1,*3



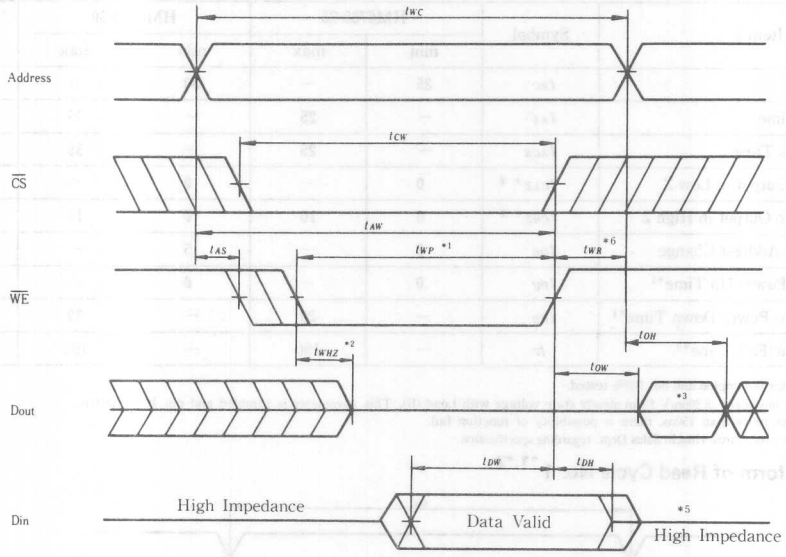
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

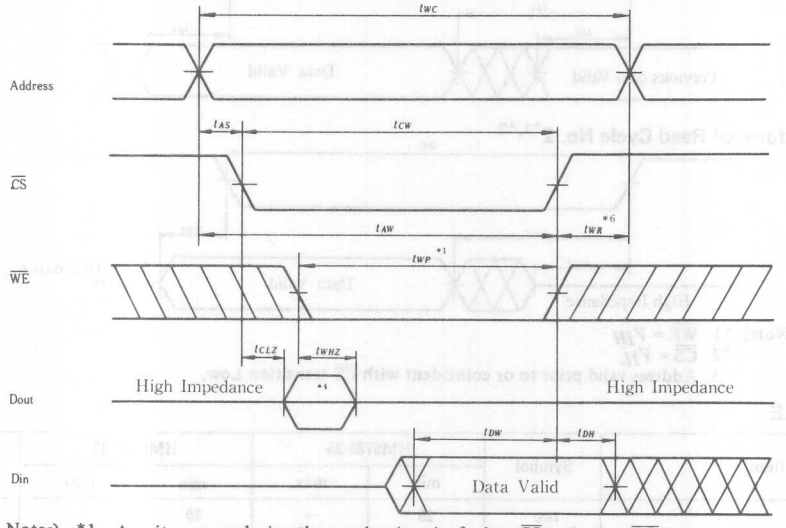
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	ns
Write Pulse Width	t_{WP}	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ} *1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	15	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Output Active from End of Write	t_{OW} *1	0	—	0	—	ns

*1. Transition is measured ±200mV from steady state voltage with Lood(B).
This parameter is sampled and not 100% tested.

- Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Dout is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	8.0	V_{OUT}=0V

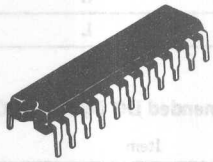
Note) This parameter is sampled and not 100% tested.

HM6788H Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 15/20ns (max.)
- Low power Operation
  Operating: 280mW (typ)
- +5V Single Supply
- Completely Static Memory —
  No Clock or Timing Strobe required
- Equal Access and Cycle Times
- Fully TTL compatible Input and Output

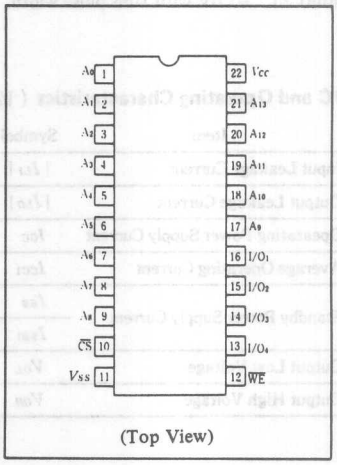


(DP-22NB)

Ordering Information

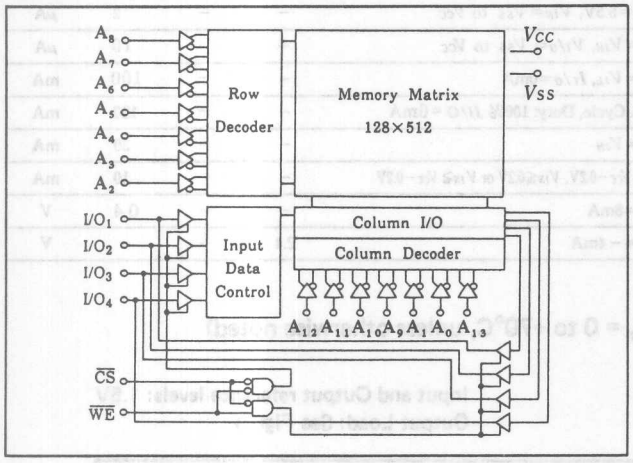
Type No.	Access Time	Package
HM6788HP-15	15ns	300 mil 22 pin Plastic DIP
HM6788HP-20	20ns	

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

×: H or L

Recommended DC Operating Conditions ($0°C \leq Ta \leq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. –3.0V with 10ns pulse width.

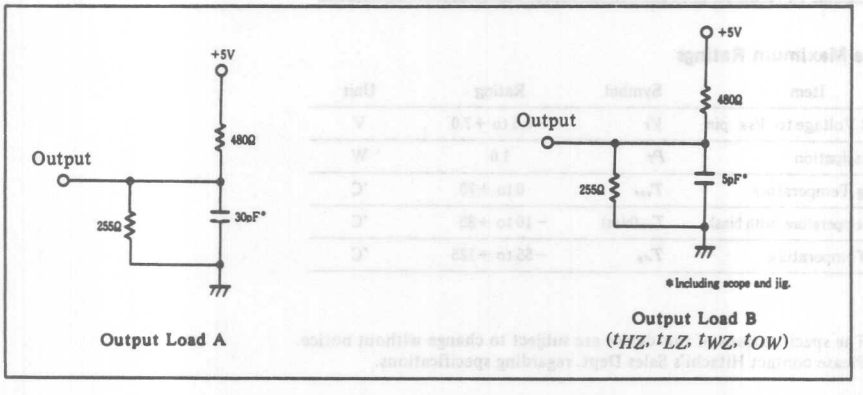
DC and Operating Characteristics ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	10	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}=0mA$	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

AC Characteristics (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall time: 4ns
  Input and Output reference levels: 1.5V
  Output Load: See Figure



Output Load A

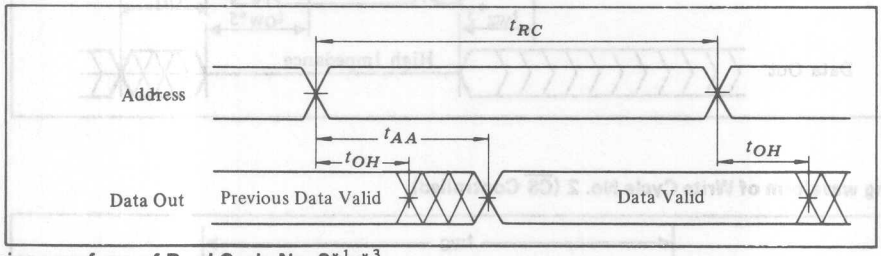
Output Load B
(t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

Read Cycle

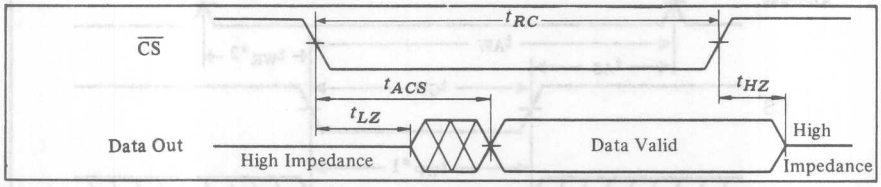
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	

Note) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

- **Timing waveform of Read Cycle No. 1*1,*2**



- **Timing waveform of Read Cycle No. 2*1,*3**



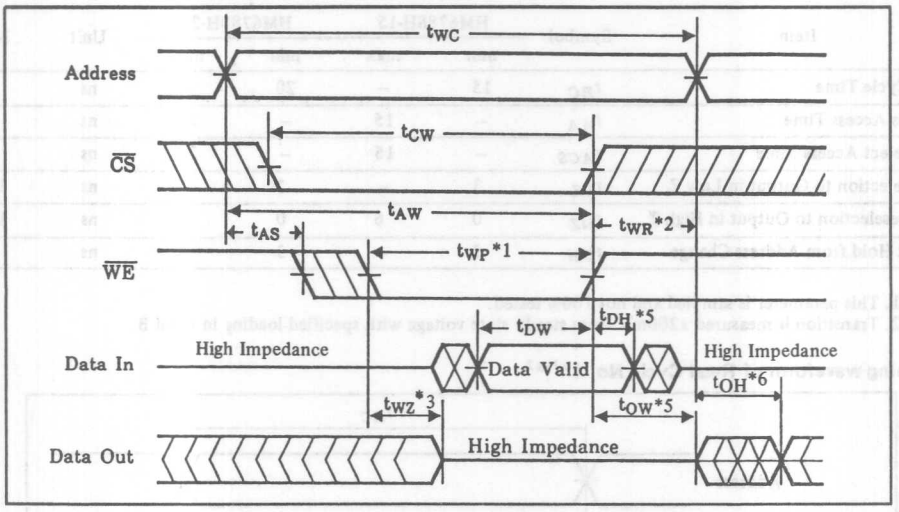
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

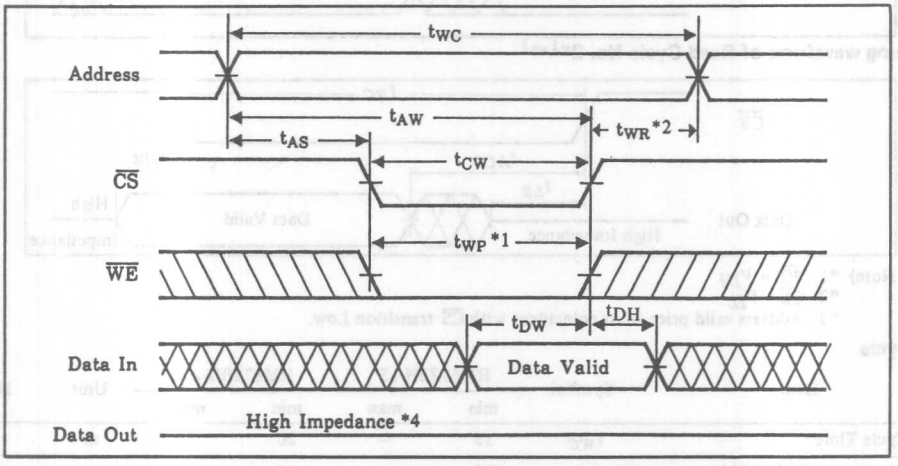
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	1	–	1	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Data Valid to End of Write	t_{DW}	9	–	10	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

- **Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)**



- **Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)**



Note)*1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

*6. Data Out is the same phase of write data of this write cycle.

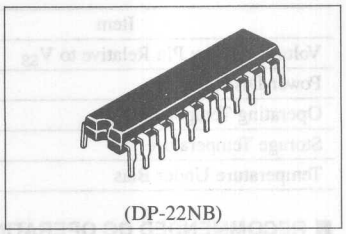
Capacitance (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	$V_{I/O}$=0V

Note) This parameter is sampled and not 100% tested.

HM6788HA Series — Preliminary

16384-Word × 4-Bit High Speed Static RAM



(DP-22NB)

■ FEATURES

- Super Fast
  Access Time. . . . . .12/15/20ns (max.)
- +5V Single Supply
- Low Power Dissipation
  (DC) Operating . . . . . .300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible—All Inputs and Outputs

■ ORDERING INFORMATION

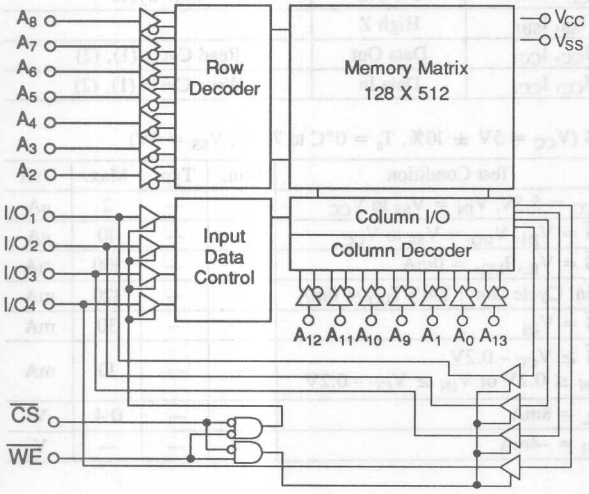
Type No.	Access Time	Package
HM6788HAP-12	12ns	300 mil 22 pin
HM6788HAP-15	15ns	Plastic DIP
HM6788HAP-20	20ns	(DP-22NB)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width ≤ 10ns, DC: −0.5V

■ TRUTH TABLE

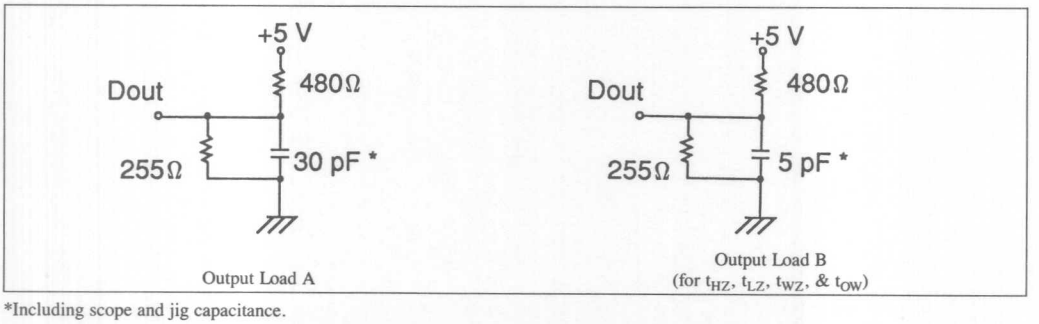
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$, $V_{SS} = 0V$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O}$, = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle Duty: 100% $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	30	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Load: See Figure
- Input Rise and Fall Times: 4ns
- Output Reference Levels: 1.5V



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ}, & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6788HA-12		HM6788HA-15		HM6788HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6788HA-12		HM6788HA-15		HM6788HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	6	—	7	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	3, 4

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

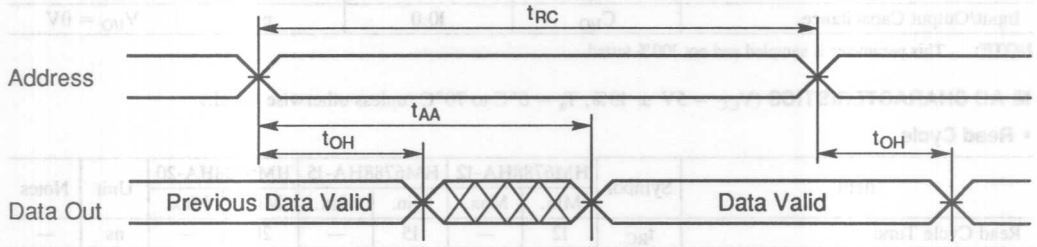
2. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

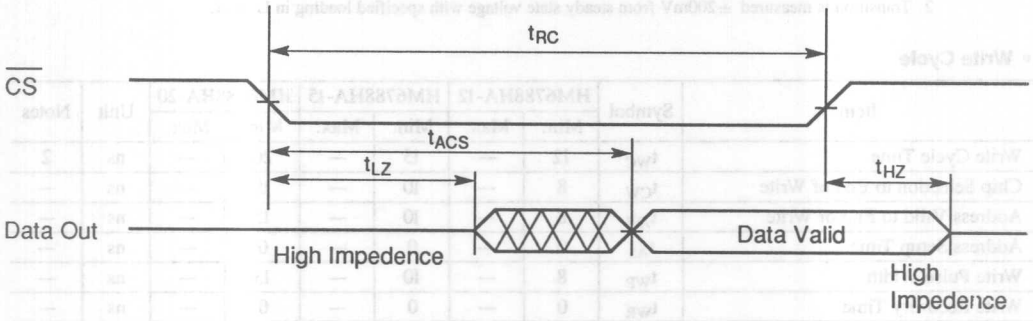
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1) (2)

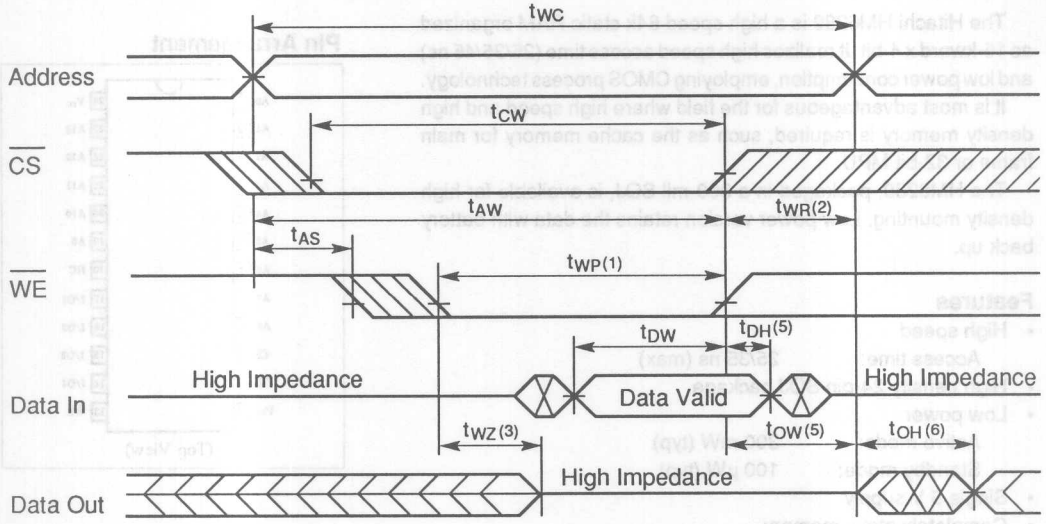


• **Read Cycle (2)** (1) (3)

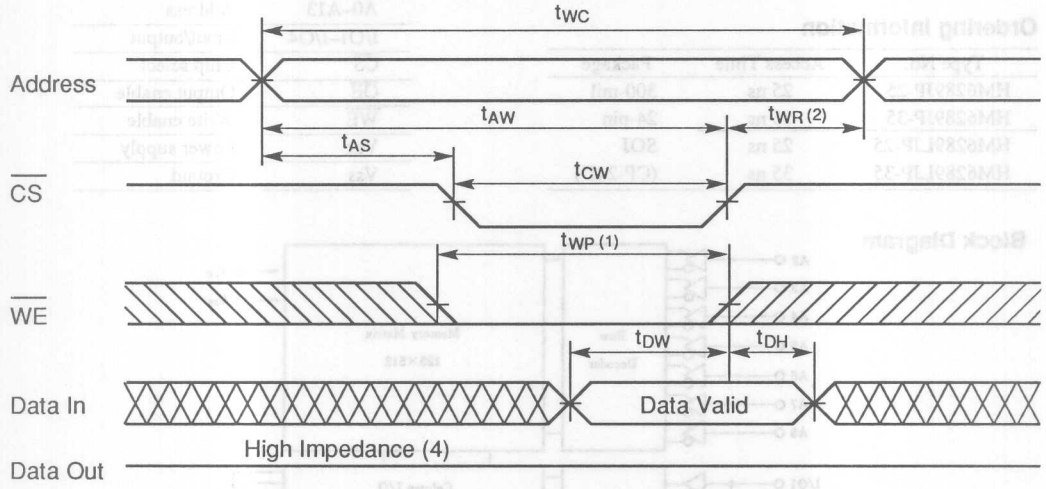


NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle.

HM6289 Series

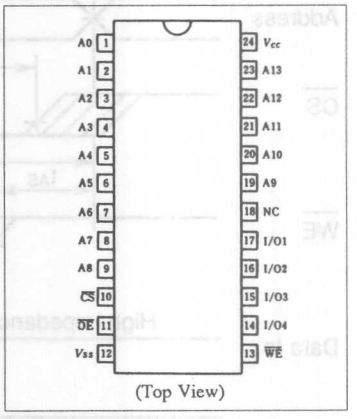
16384-Word × 4-Bit High Speed CMOS Static RAM (with $\overline{OE}$)

The Hitachi HM6289 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. Low power version retains the data with battery back up.

Pin Arrangement



(Top View)

Features

- High speed
  - Access time: 25/35 ns (max)
- High density 24-pin SOJ package
- Low power
  - Active mode: 300 mW (typ)
  - Standby mode: 100 μW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

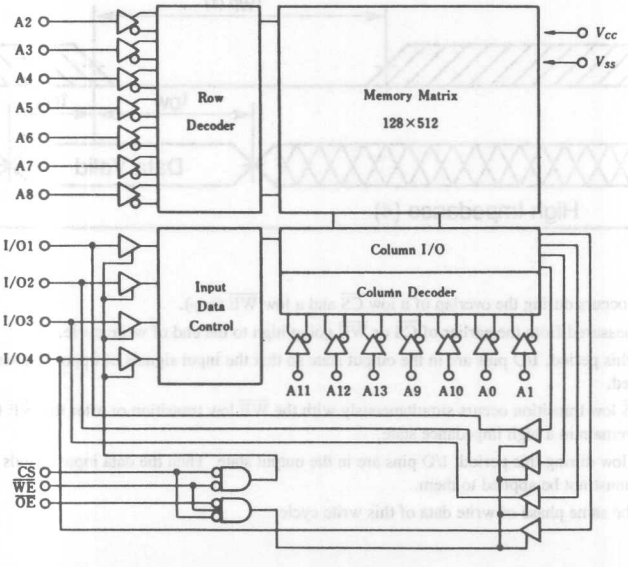
Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mil
HM6289JP-35	35 ns	24-pin
HM6289LJP-25	25 ns	SOJ
HM6289LJP-35	35 ns	(CP-24D)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1)–(3)
L	H	L	Write	Icc	Din	Write cycle (1)–(2)
L	L	L	Write	Icc	Din	Write cycle (3)–(6)

Note: ×; H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{in}	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	–55 to +125	°C
Storage temperature range under bias	T_{bias}	–10 to +85	°C

Note: *1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = 0V to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0 V to Vcc
Operating Vcc current	Icc	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. cycle
Standby Vcc current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V
	I_{SB1}*3	—	0.02	0.1	mA	0V ≤ Vin ≤ 0.2 V or Vcc – 0.2 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. P-version
*3. LP-version

Capacitance (Ta = 25°C, f = 1MHz)

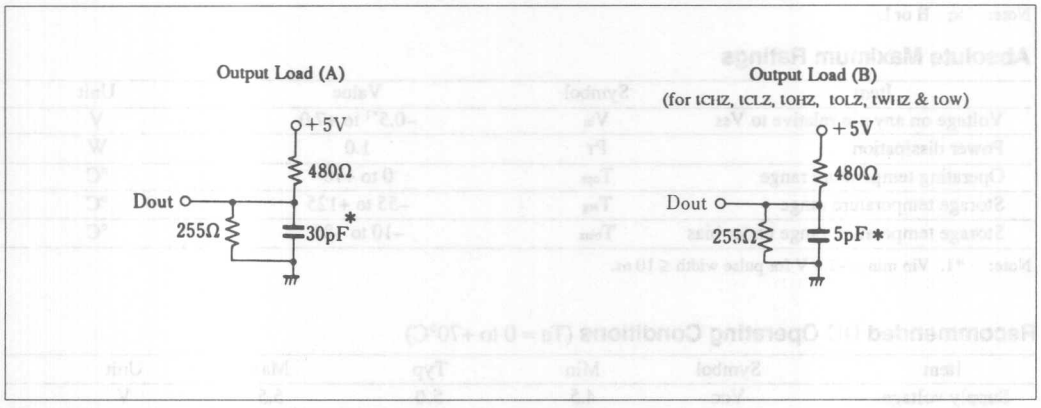
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	V I/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



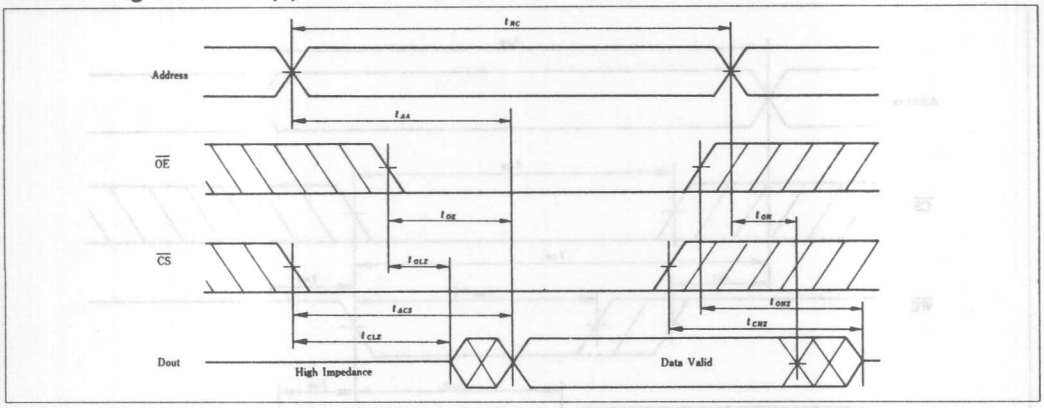
Note: * Including scope & jig.

Read Cycle

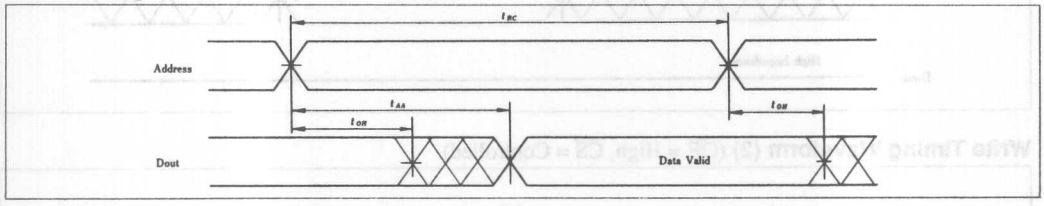
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chis disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: *1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

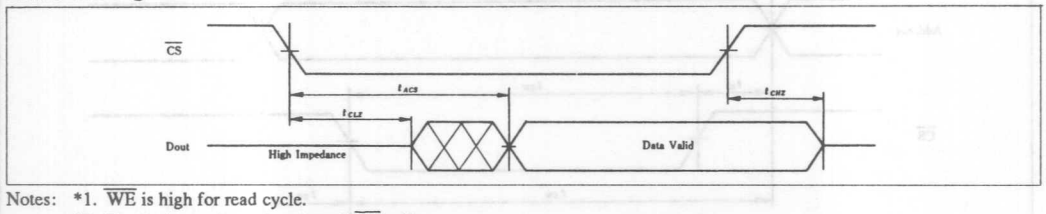
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1,*2,*4



Read Timing Waveform (3) *1,*3,*4



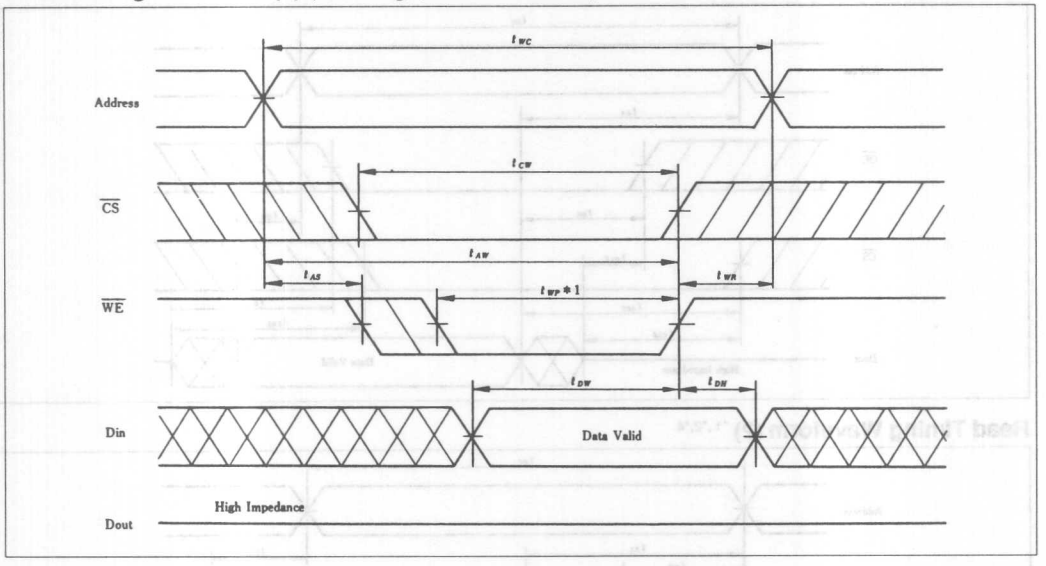
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

Write Cycle

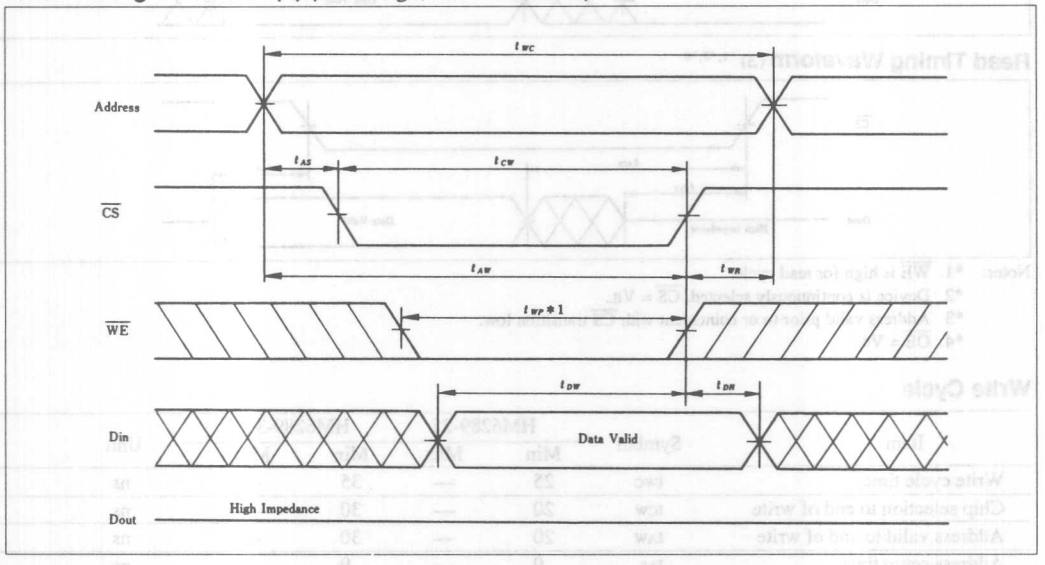
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	10	0	10	ns
Write to output in high-Z*1	t_{WHZ}	0	8	0	10	ns
Data to write time overlap	t_{DW}	12	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write*1	t_{OW}	5	—	5	—	ns

Note: *1. Output transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

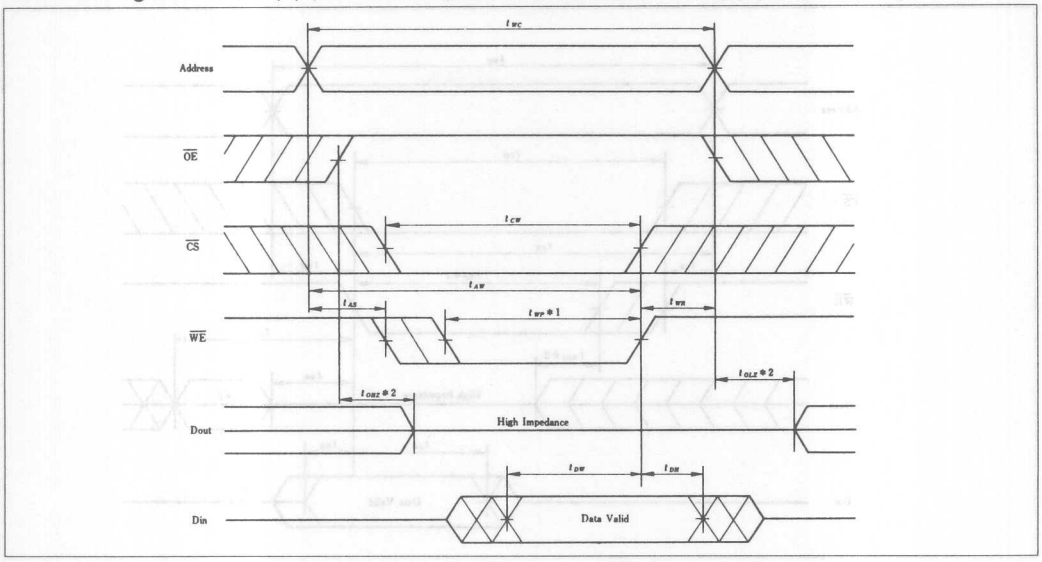
Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



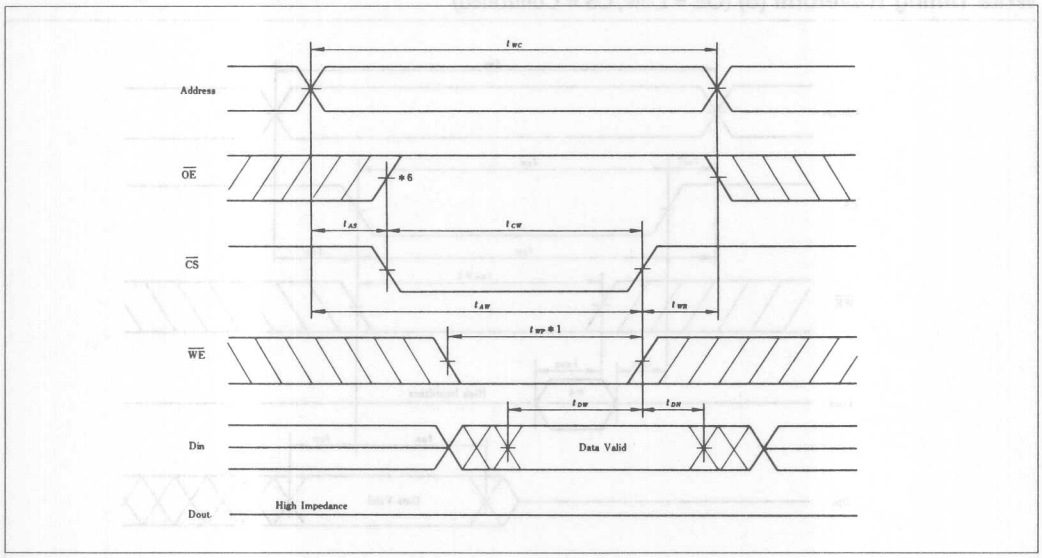
Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



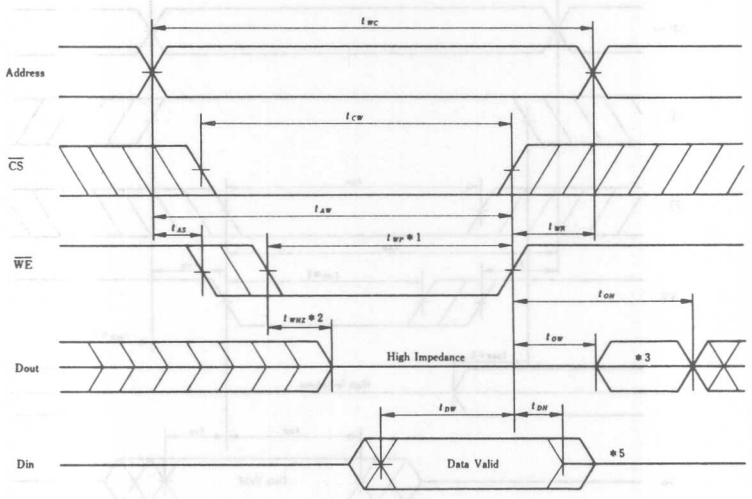
Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



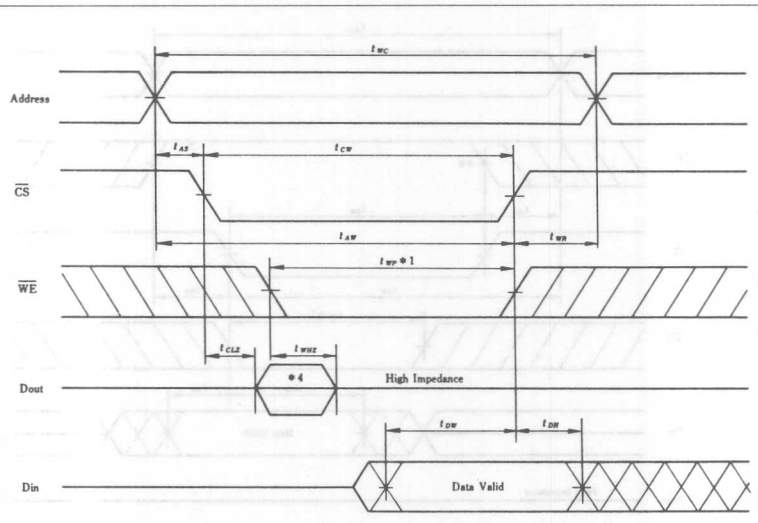
Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes: *1 A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)
*2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tOW. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle, if tWR is long enough.
*7. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

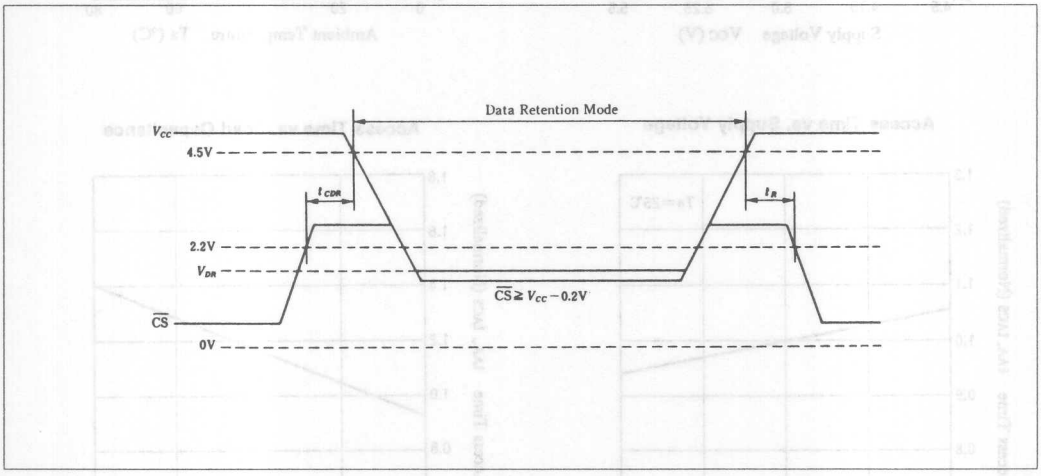
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

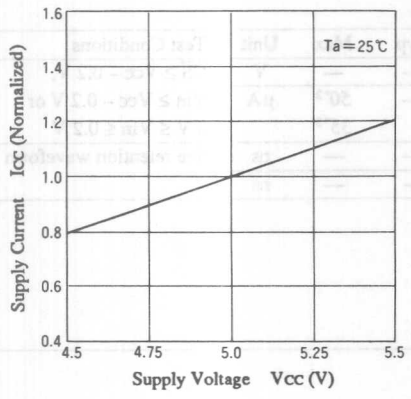
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V,
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Note: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

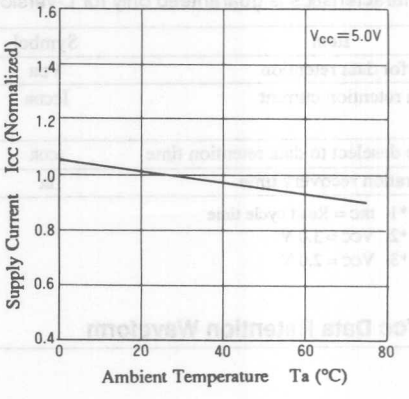
Low Vcc Data Retention Waveform



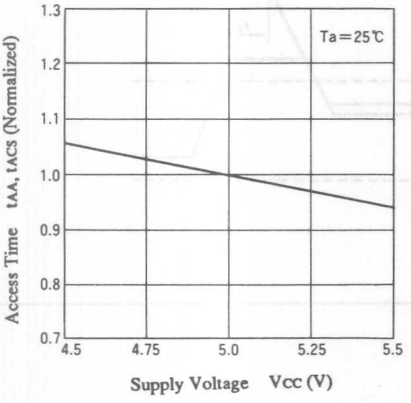
Supply Current vs. Supply Voltage



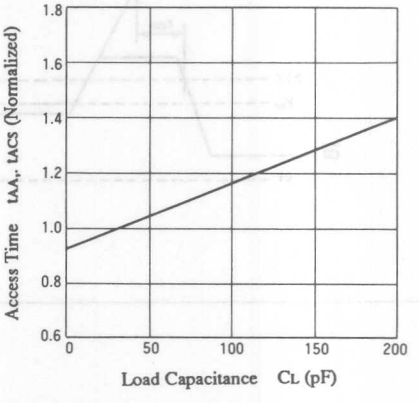
Supply Current vs. Ambient Temperature



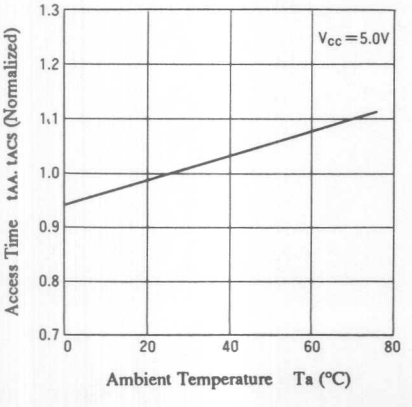
Access Time vs. Supply Voltage



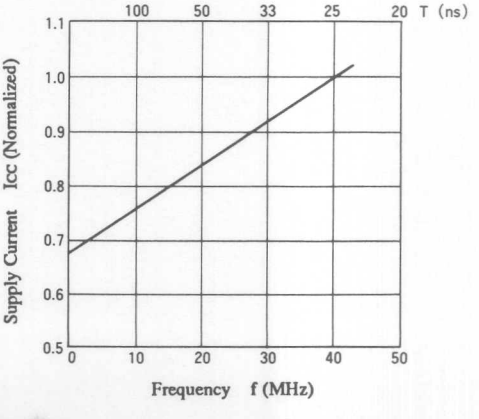
Access Time vs. Load Capacitance



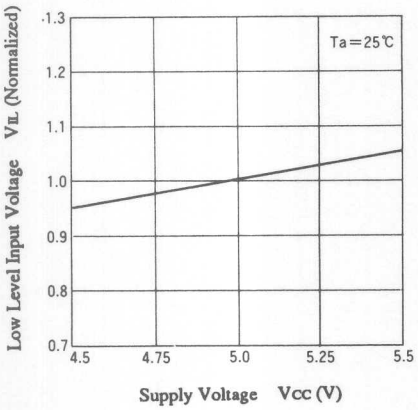
Access Time vs. Ambient Temperature



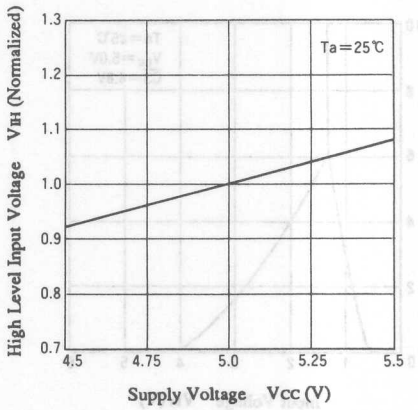
Supply Current vs. Frequency



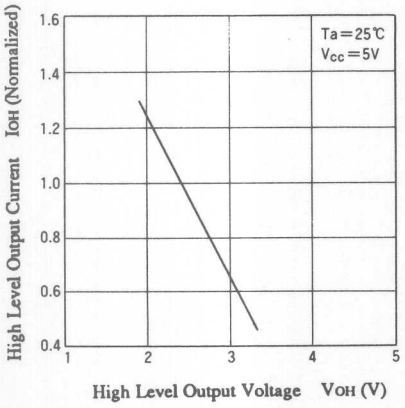
Low Level Input Voltage vs. Supply Voltage



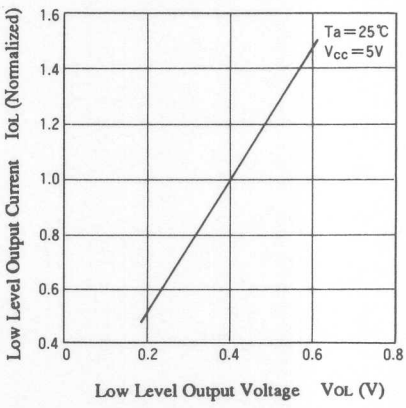
High Level Input Voltage vs. Supply Voltage



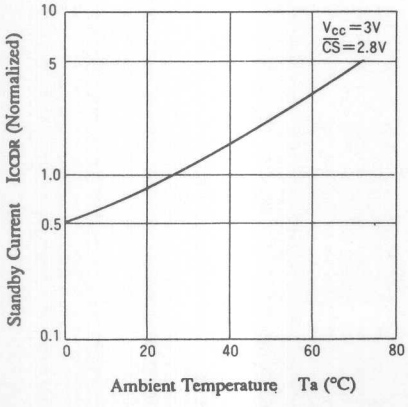
Output Current vs. Output Voltage (1)



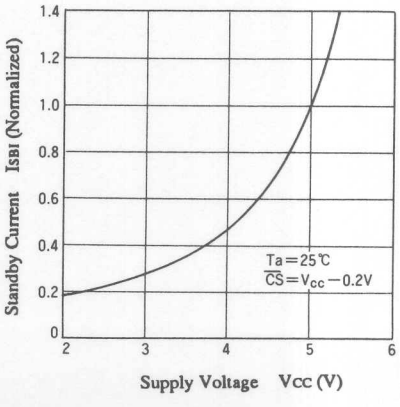
Output Current vs. Output Voltage (2)



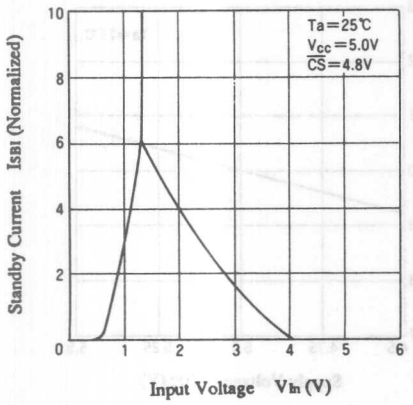
Standby Current vs. Ambient Temperature



Standby Current vs. Supply Voltage



Standby Current vs. Input Voltage



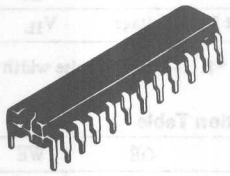
HM6789 Series — Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- Super Fast Access Time: . . . . . 25/30 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 230 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789P Series



(DP-24NC)

HM6789JP Series

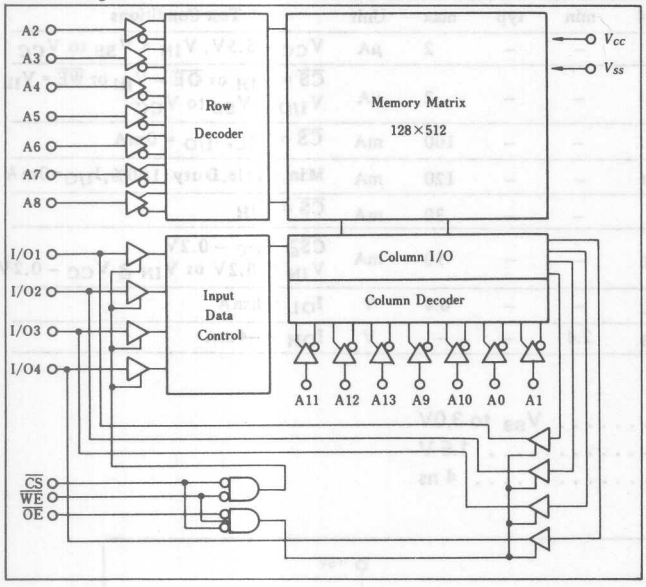


(CP-24D)

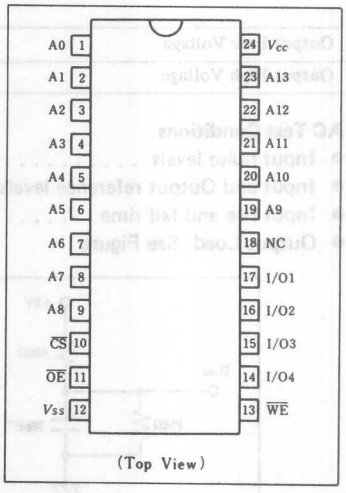
Ordering Information

Type No.	Access Time	Package
HM6789P-25	25ns	300 mil 24 pin
HM6789P-30	30ns	plastic DIP
HM6789JP-25	25ns	300 mil 24 pin
HM6789JP-30	30ns	Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns.

Function Table

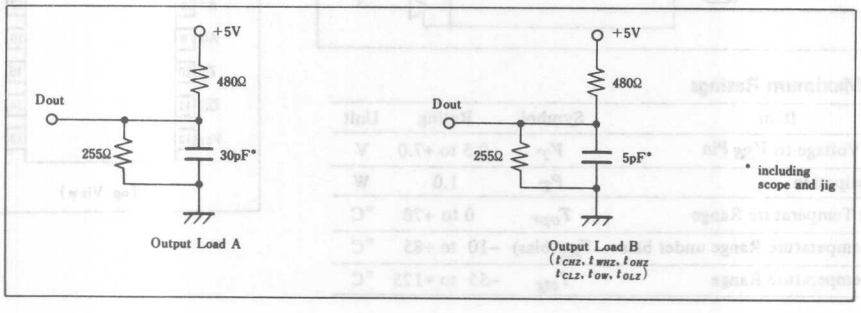
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Din	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} – 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	0	–	0	–	ns
Output Enable to Output Valid	t_{OE}	0	15	0	15	ns
Output Enable to Output in Low Z	t_{OLZ}*1	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Input Voltage Rise/Fall Time	t_T*2	–	150	–	150	ns

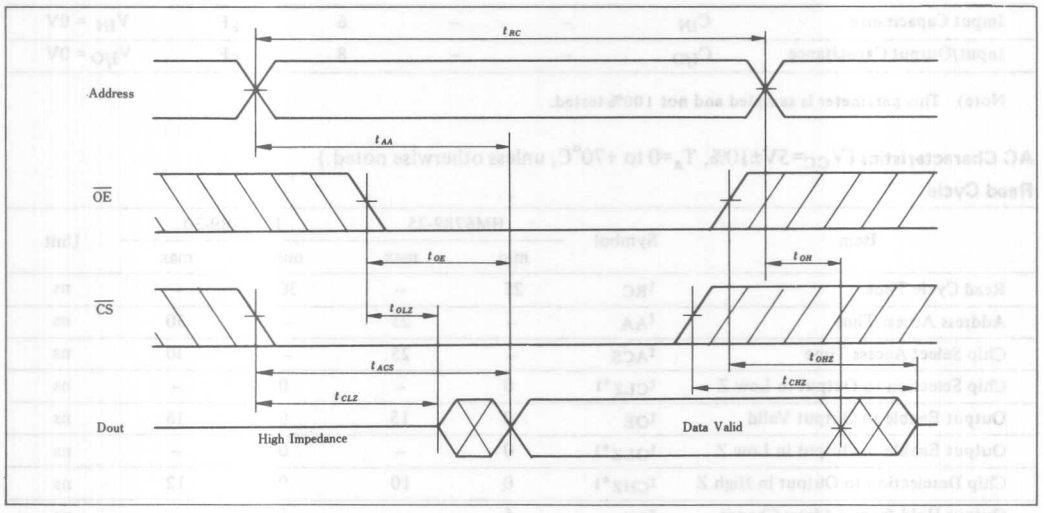
Write Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	30	–	ns
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	20	–	25	–	ns
Write Pulse Width	t_{WP}	20	–	25	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}*1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	–	20	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Output Disable to Output in Hihg Z	t_{OHZ}*1	0	10	0	10	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

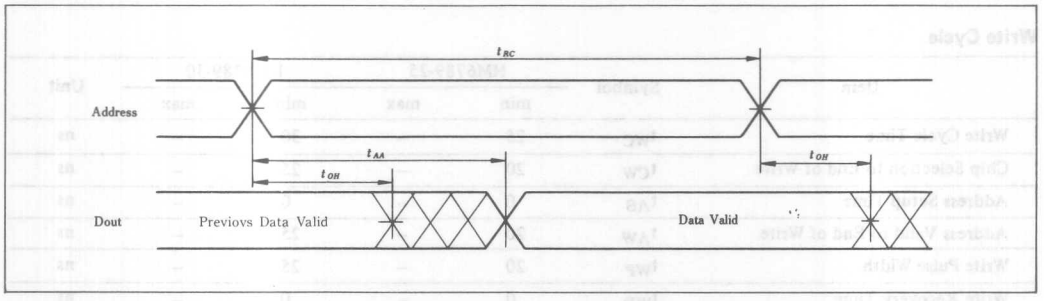
Notes) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.
*2. If t_T becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi Sales Dept. regarding specification.

Timing Waveform

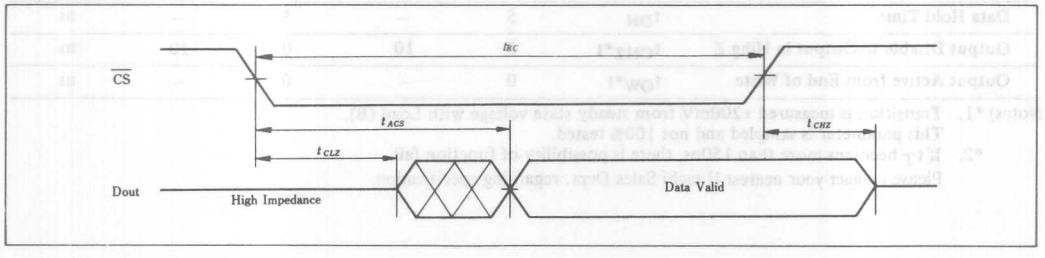
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

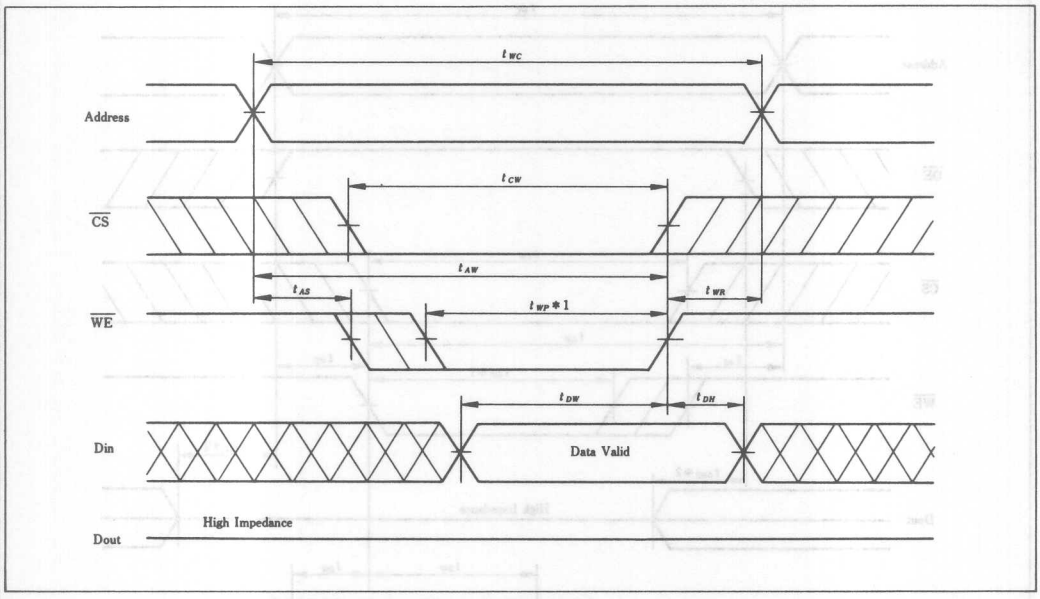


Read Cycle (3) *1, *3, *4

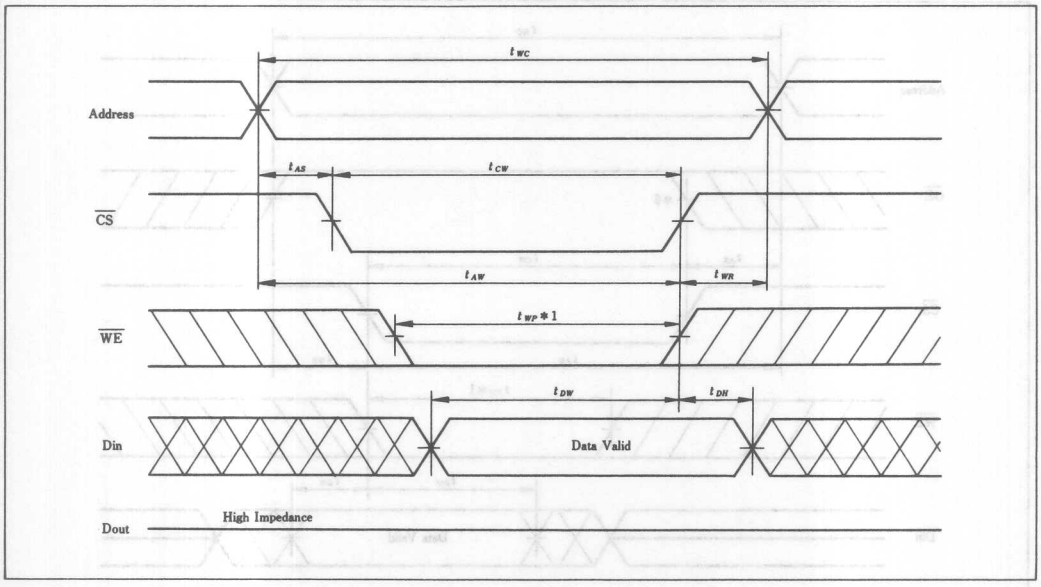


Notes) *1. $\overline{WE}$ = V_{IH}
*2. $\overline{CS}$ = V_{IL}
*3. $\overline{OE}$ = V_{IL}
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

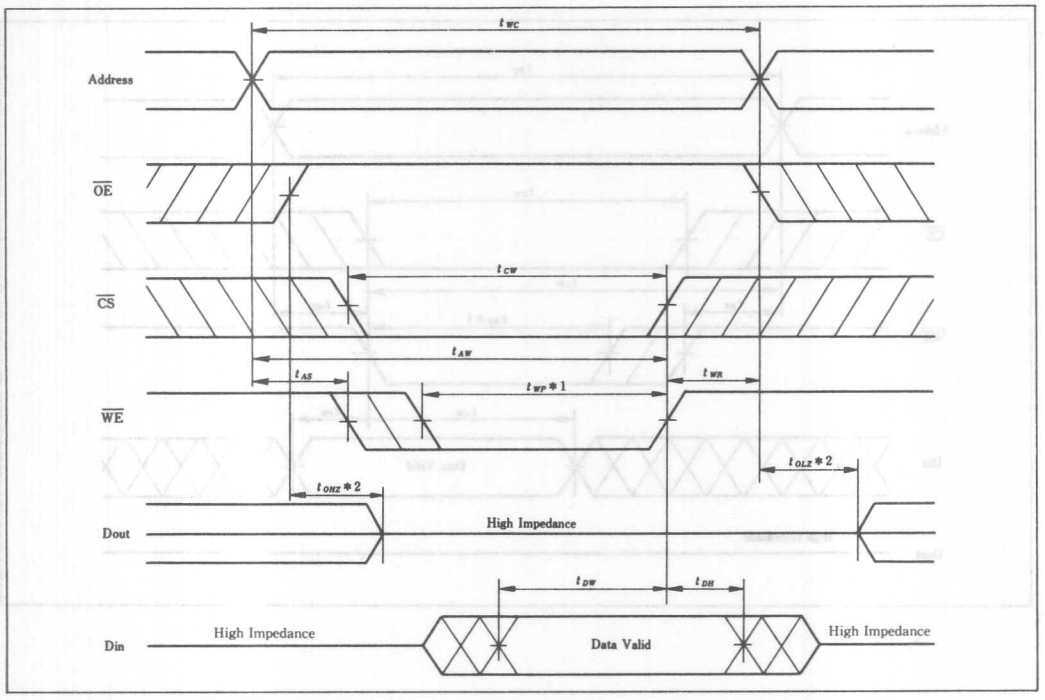
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



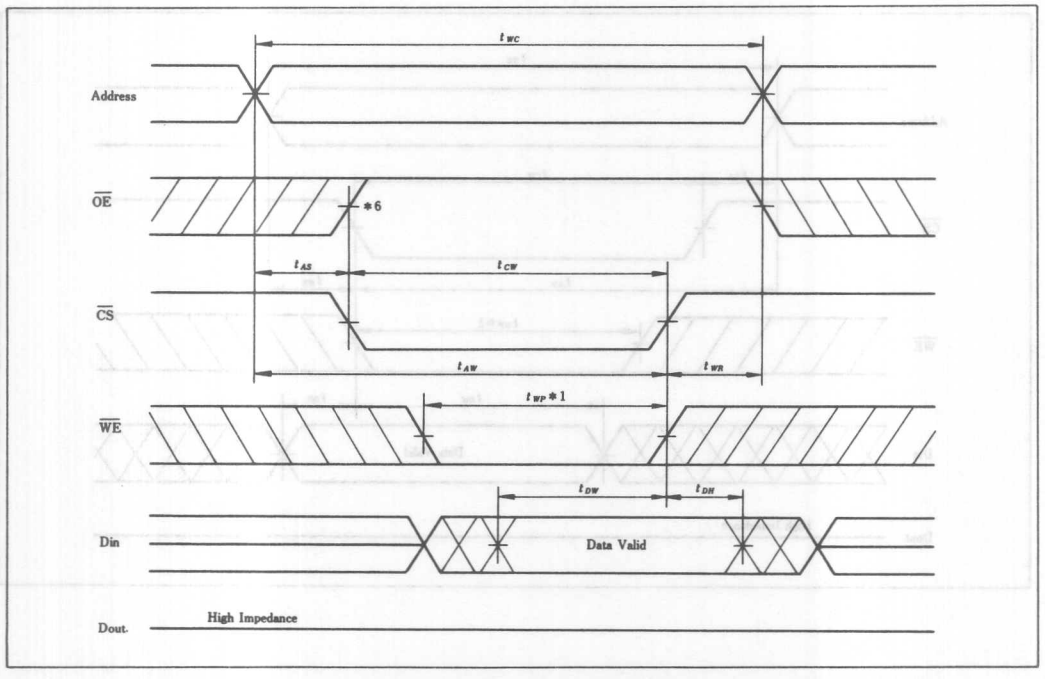
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)

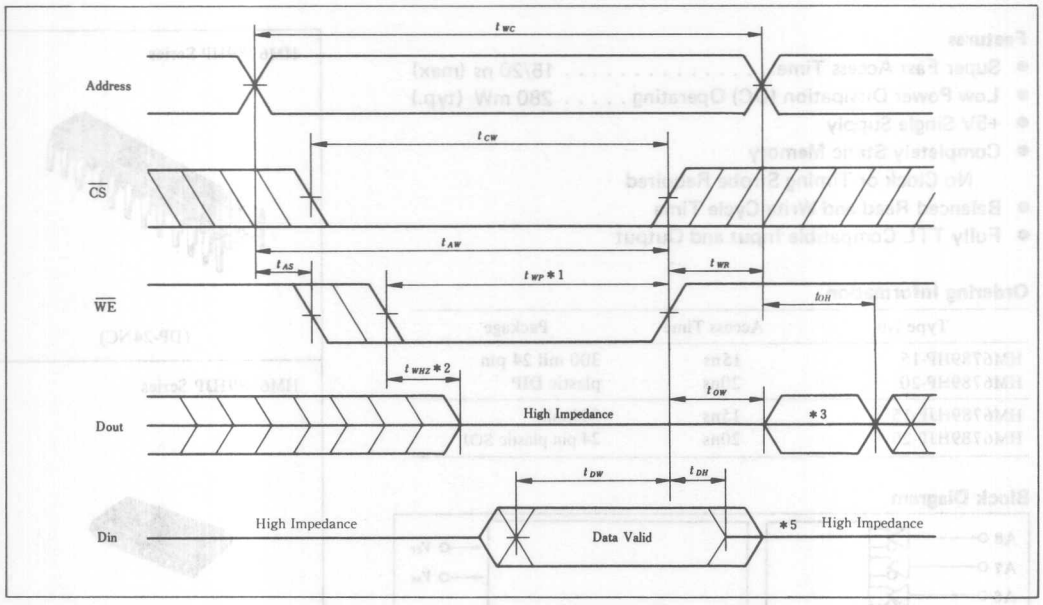


Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)

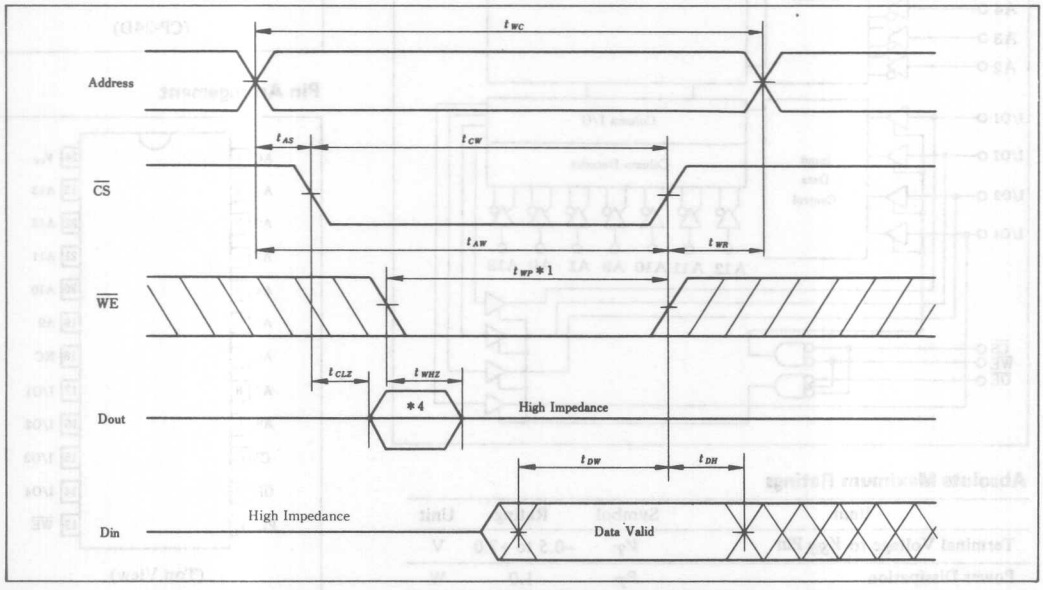


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Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Dout is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

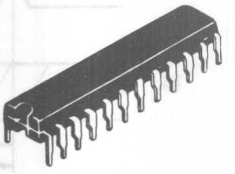
HM6789H Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- Super Fast Access Time: . . . . . 15/20 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 280 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789HP Series



(DP-24NC)

HM6789HJP Series

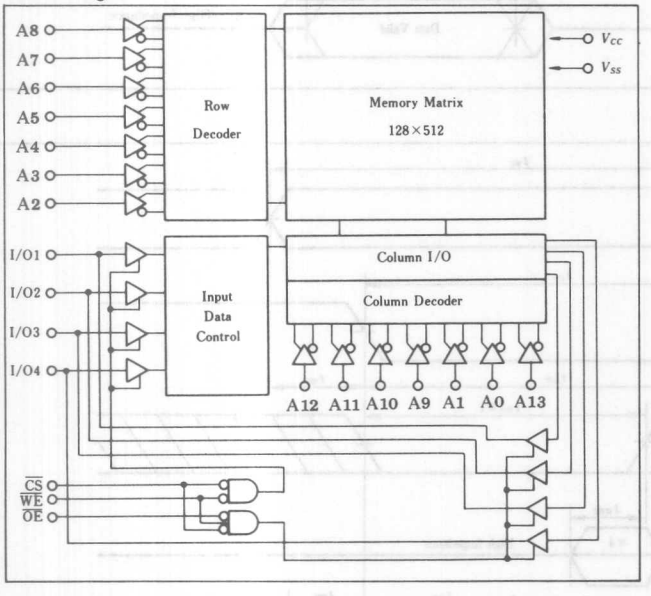


(CP-24D)

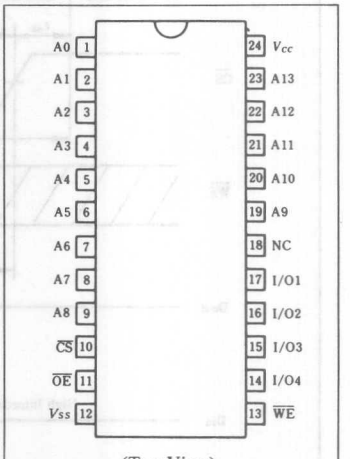
Ordering Information

Type No.	Access Time	Package
HM6789HP-15	15ns	300 mil 24 pin
HM6789HP-20	20ns	plastic DIP
HM6789HJP-15	15ns	300 mil
HM6789HJP-20	20ns	24 pin plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 10ns.

Function Table

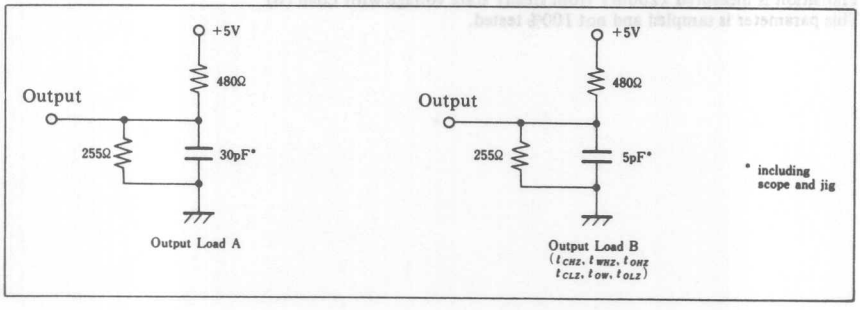
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data Out	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} – 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

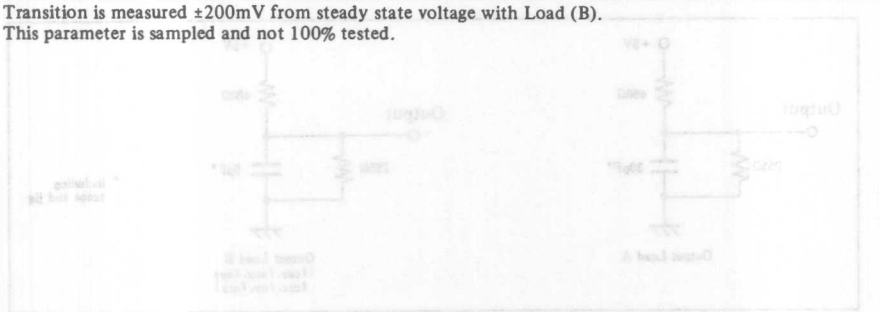
Read Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	15	–	20	–	ns
Address Access Time	t_{AA}	–	15	–	20	ns
Chip Select Access Time	t_{ACS}	–	15	–	20	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	3	–	3	–	ns
Output Enable to Output Valid	t_{OE}	0	12	0	12	ns
Output Enable to Output in Low Z	t_{OLZ}*1	3	–	3	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	6	0	8	ns
Output Hold from Address Change	t_{OH}	3	–	3	–	ns

Write Cycle

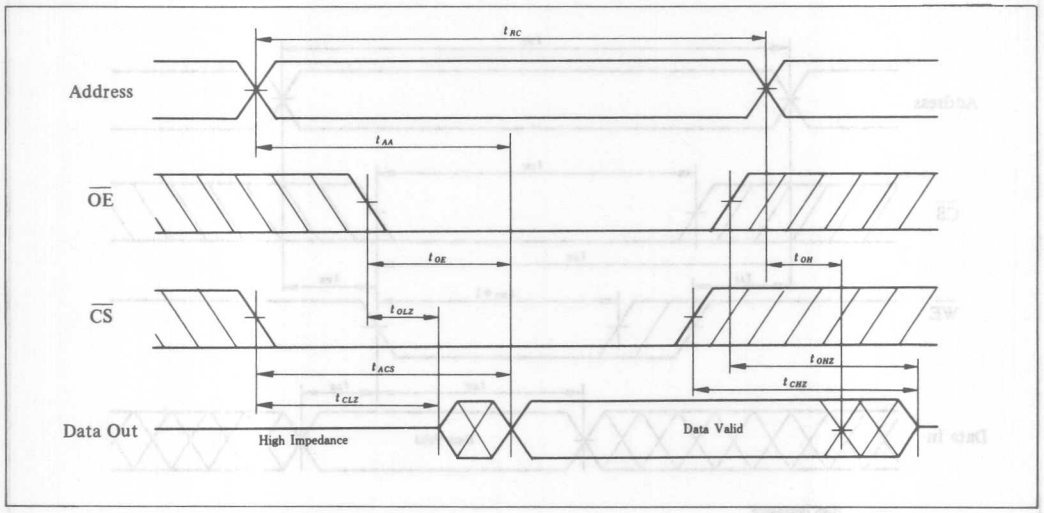
Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	15	–	20	–	ns
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	10	–	15	–	ns
Write Pulse Width	t_{WP}	10	–	15	–	ns
Write Recovery Time	t_{WR}	1	–	1	–	ns
Write to Output in High Z	t_{WHZ}*1	0	6	0	8	ns
Data Valid to End of Write	t_{DW}	9	–	10	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}*1	0	6	0	8	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

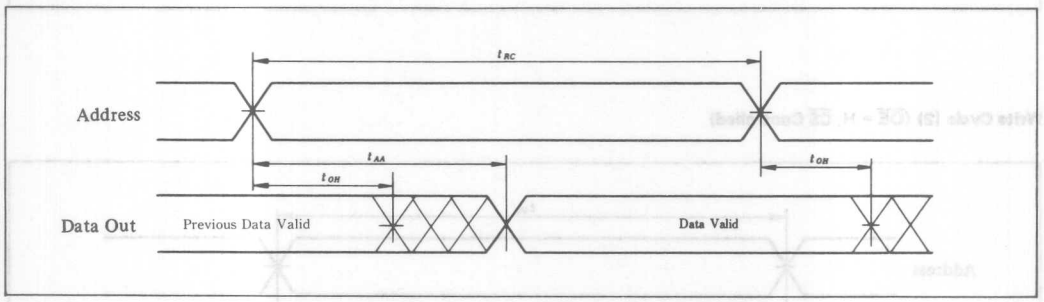


Timing Waveform

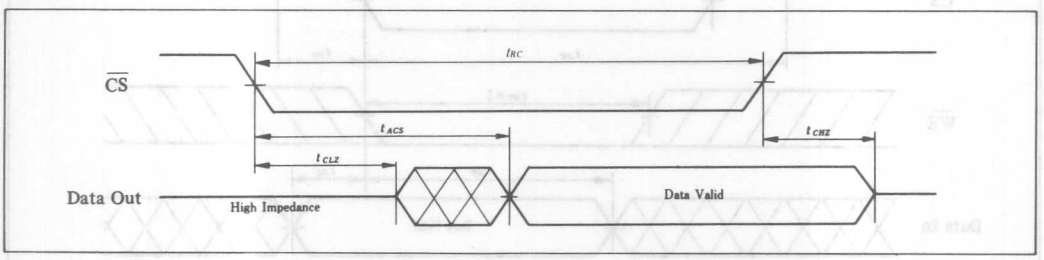
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

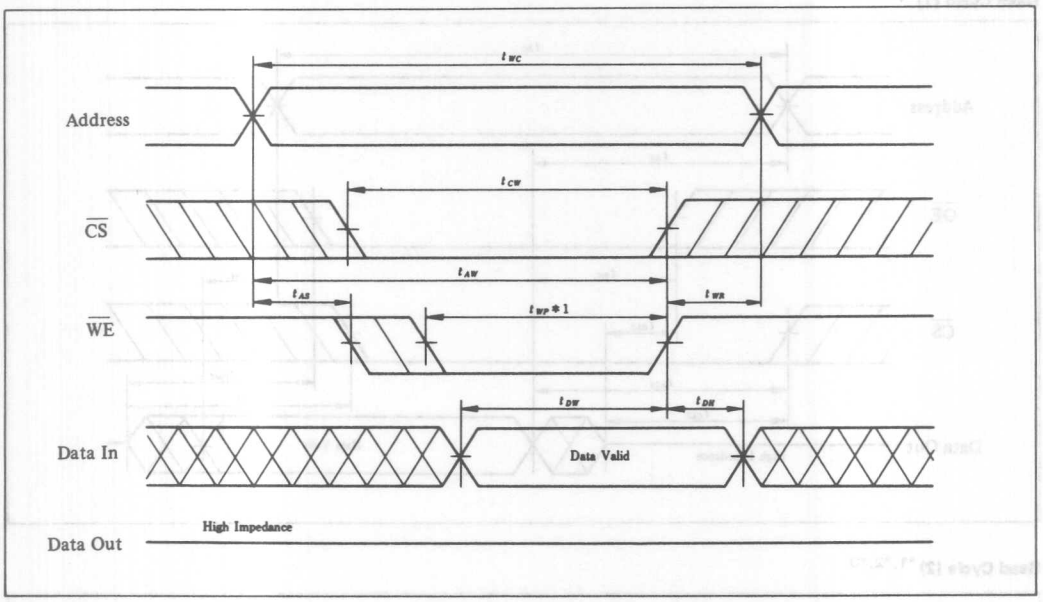


Read Cycle (3) *1, *3, *4

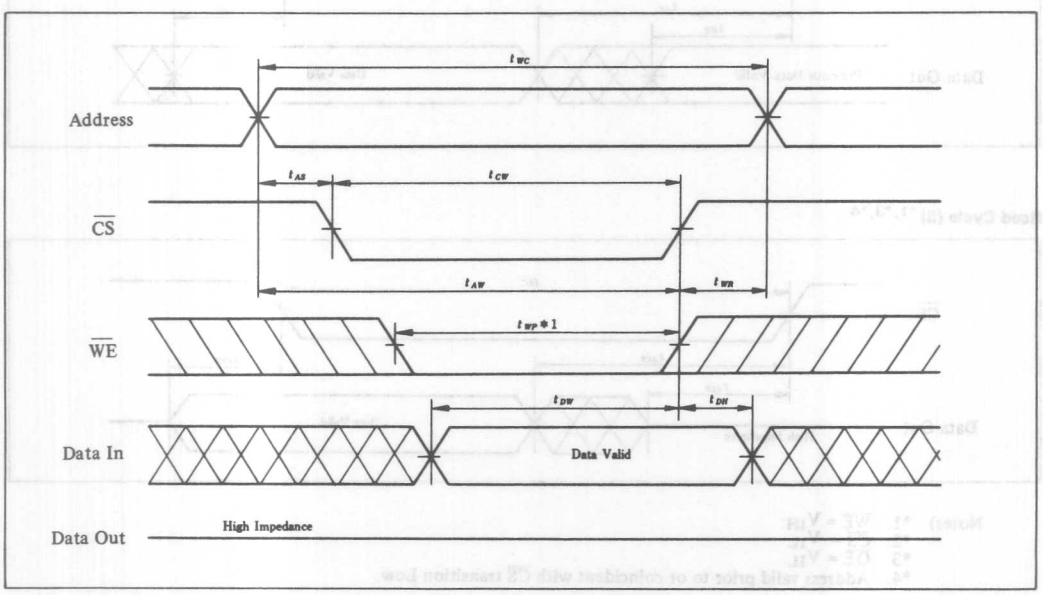


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)

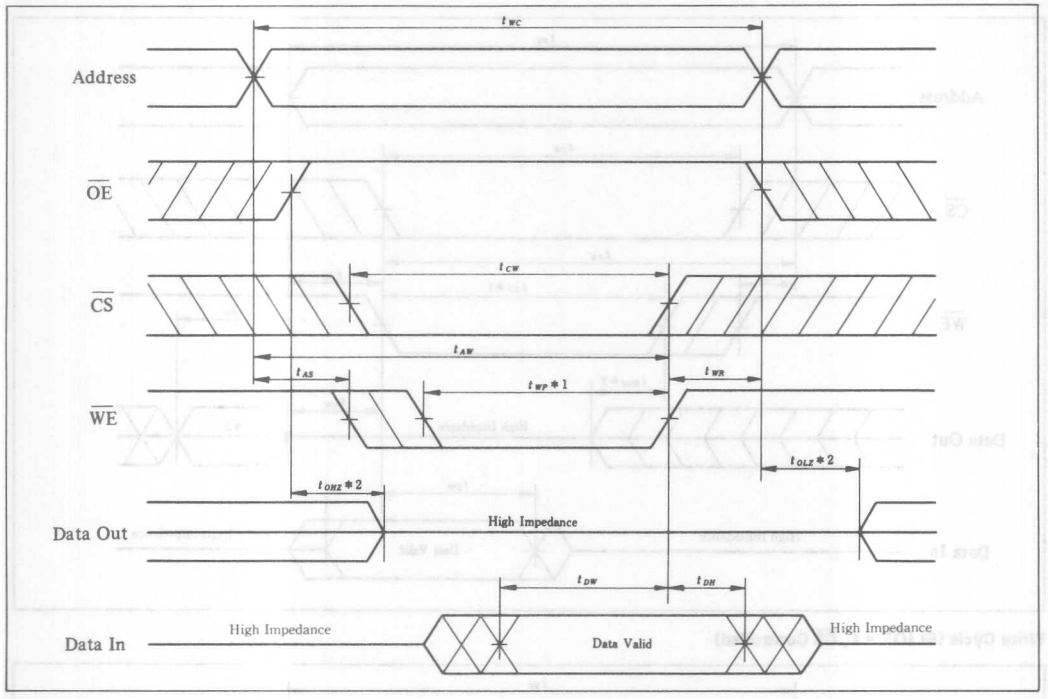


Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)

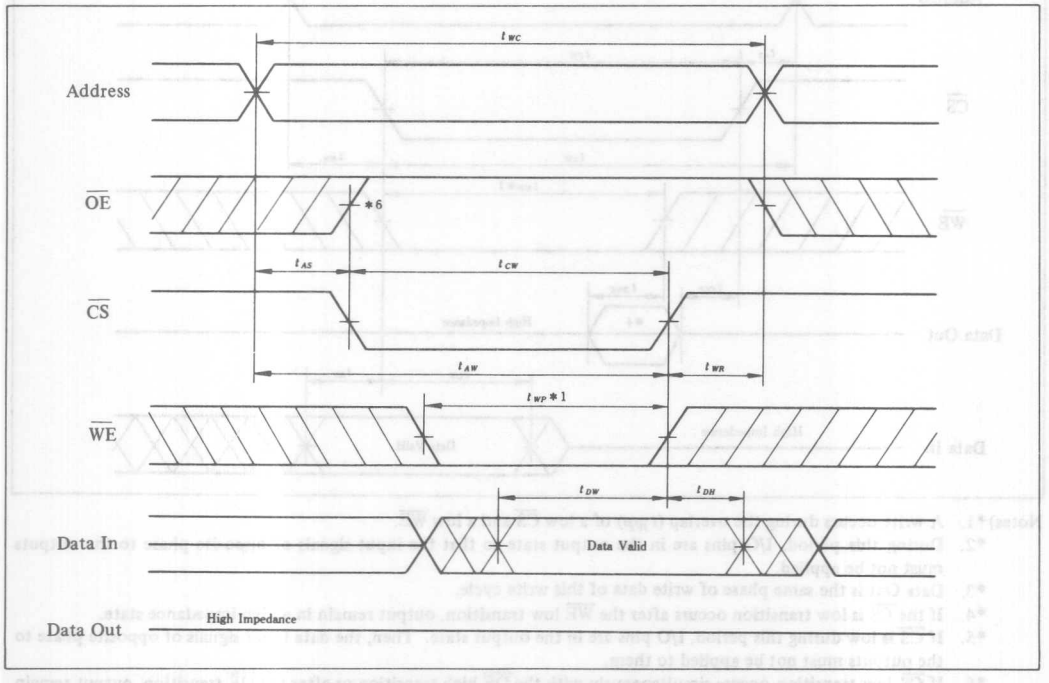


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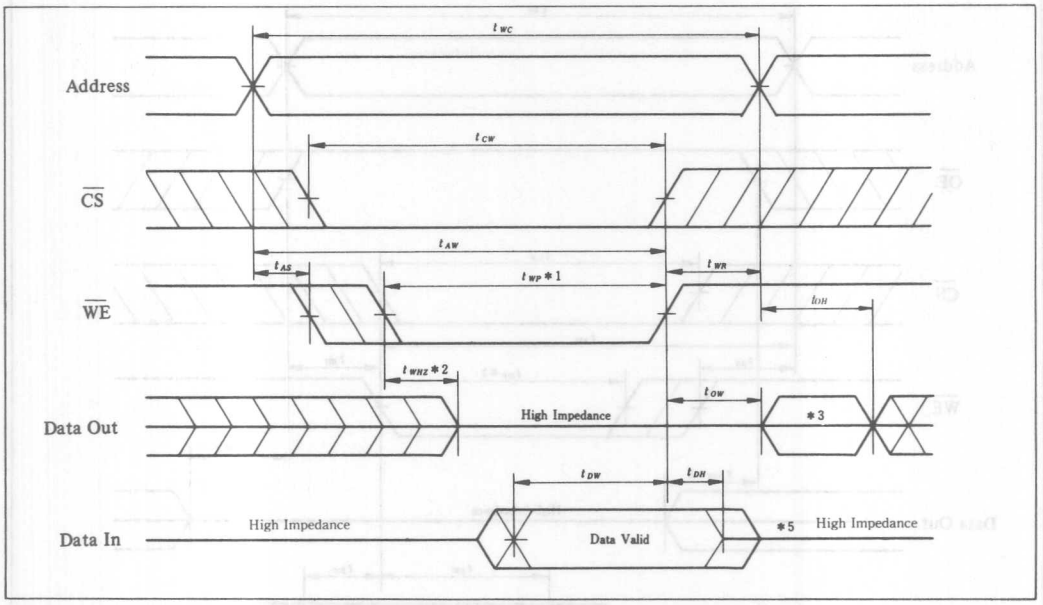
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



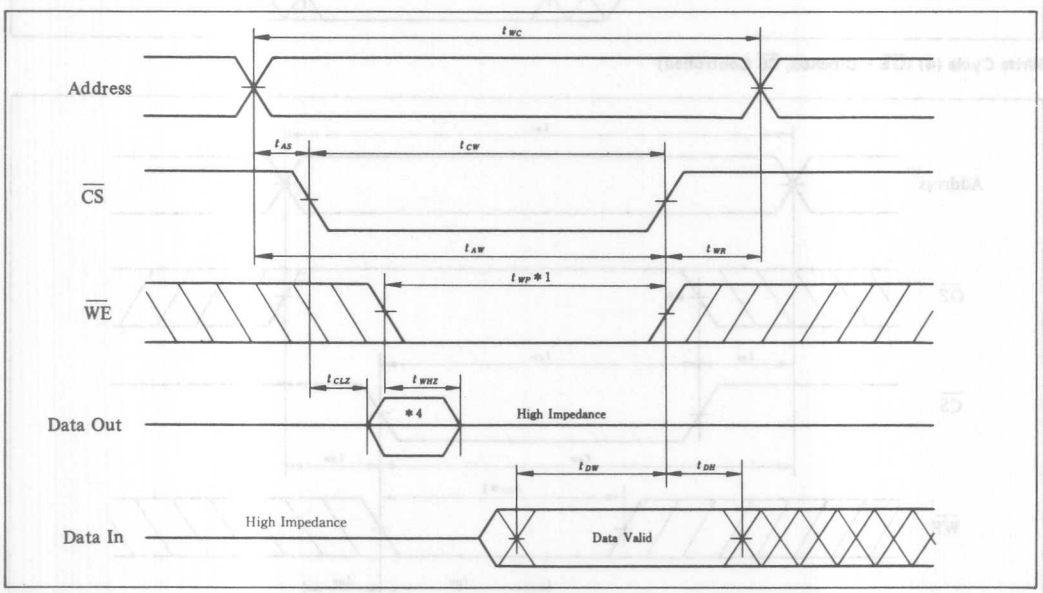
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Data Out is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

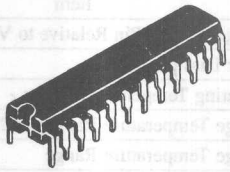
HM6789HA Series

— Preliminary

16384-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

- Super Fast
  Access Time . . . . . .Add. 12/15/20ns (max.)
  $\overline{OE}$ 6/7/8ns (max.)
- Low Power Dissipation
  (DC) Operating . . . . . .300mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



(DP-24NC)

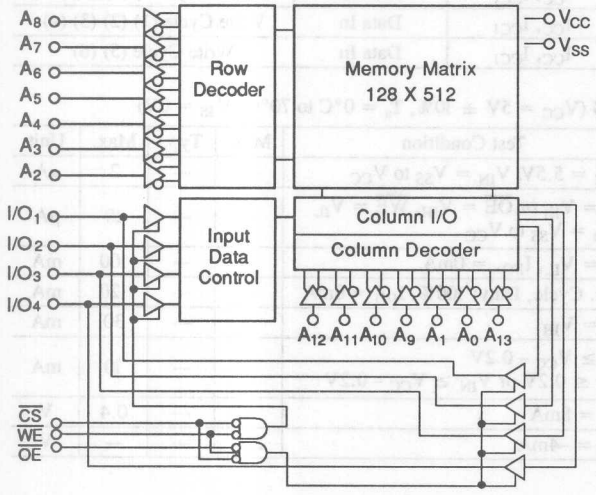


(CP-24D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6789HAP-12	12ns	300 mil 24 pin
HM6789HAP-15	15ns	Plastic DIP
HM6789HAP-20	20ns	(DP-24NC)
HM6789HAJP-12	12ns	300 mil 24 pin
HM6789HAJP-15	15ns	Plastic SOJ
HM6789HAJP-20	20ns	(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	−3.0	—	0.8	V

*Pulse width ≤ 10ns, DC: −0.5V

■ TRUTH TABLE

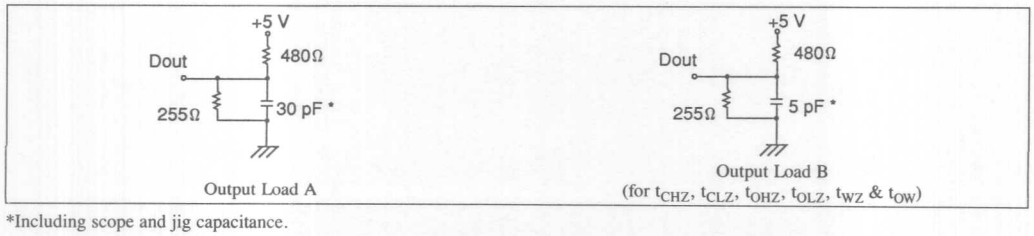
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$, = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V ± 200mV from steady level (Output Load B)
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



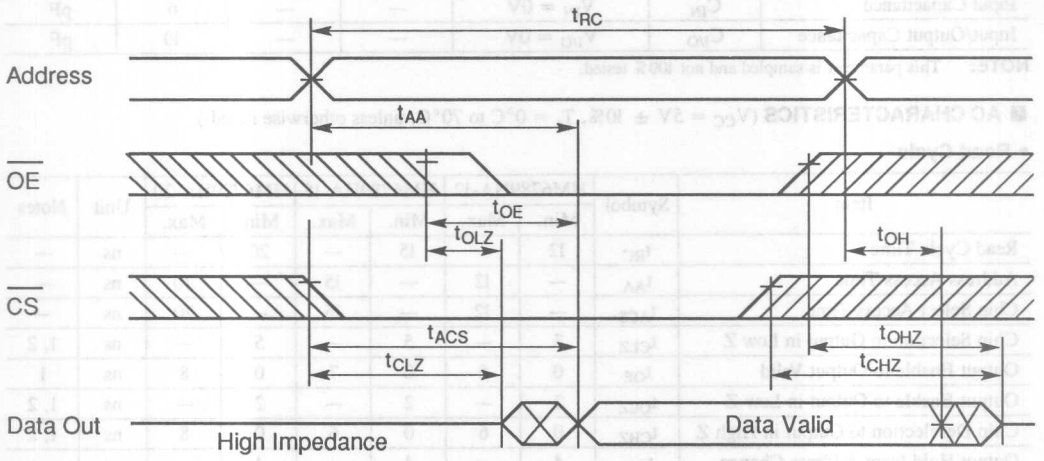
Output Load A

Output Load B
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

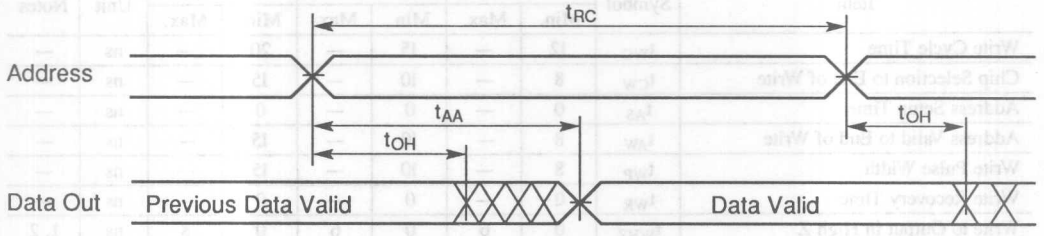
*Including scope and jig capacitance.

■ TIMING WAVEFORM

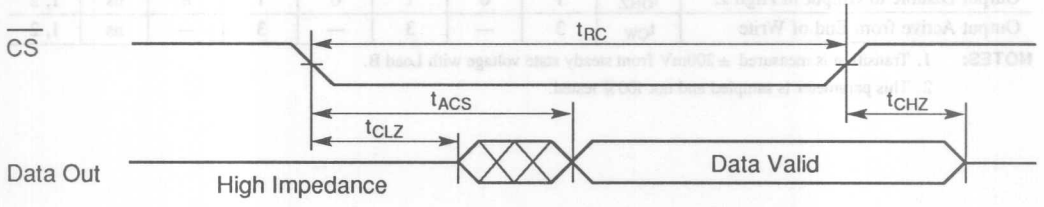
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)



• **Read Cycle (3)** (1) (3) (4)



NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

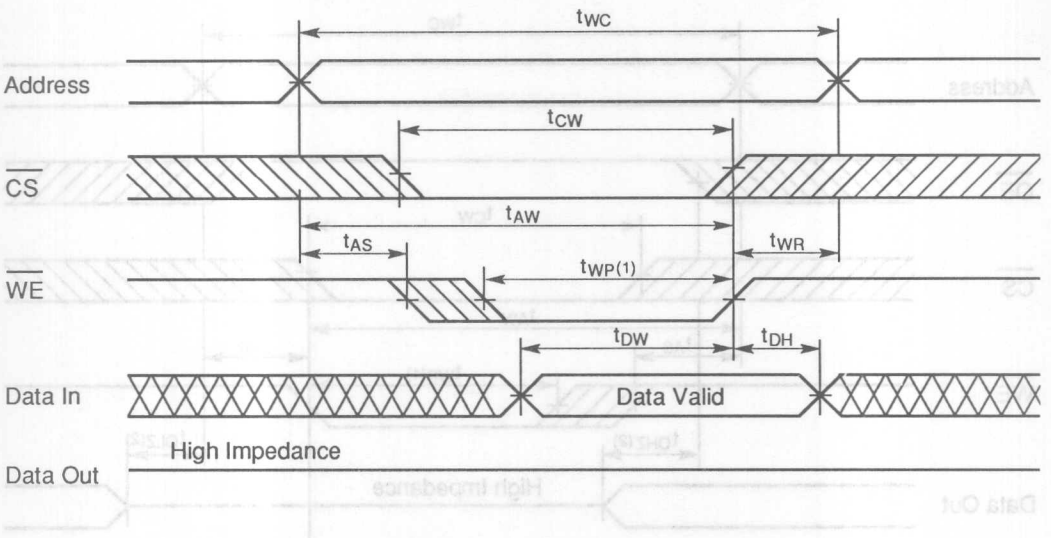
Item	Symbol	HM6789HA-12		HM6789HA-15		HM6789HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Chip Selection to Output in Low Z	t_{CLZ}	3	—	5	—	5	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	6	0	7	0	8	ns	1
Output Enable to Output in Low Z	t_{OLZ}	2	—	2	—	2	—	ns	1, 2
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—

• Write Cycle

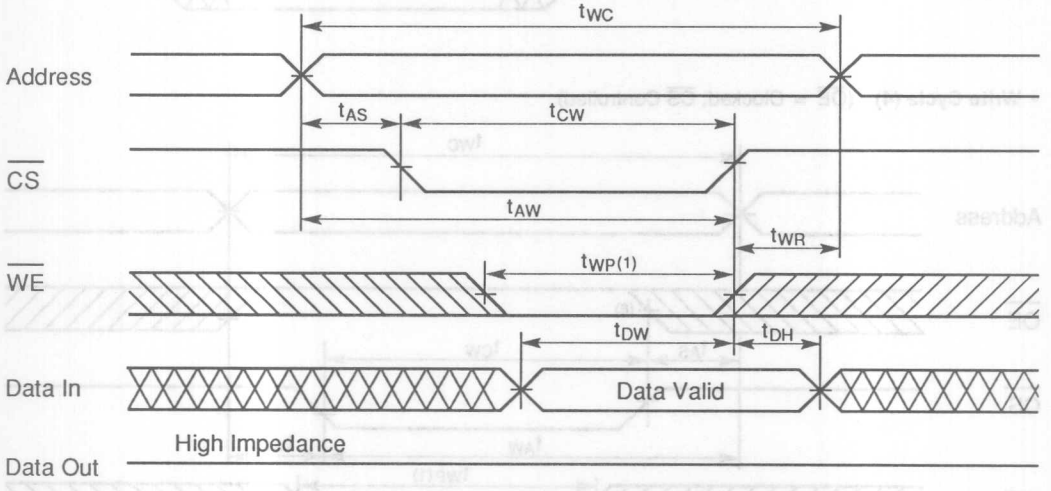
Item	Symbol	HM6789HA-12		HM6789HA-15		HM6789HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	—
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Write to Output in High Z	t_{WHZ}	0	6	0	6	0	8	ns	1, 2
Data Valid to End of Write	t_{DW}	6	—	7	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	1	6	1	6	1	8	ns	1, 2
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	1, 2

NOTES: 1. Transition is measured ±200mV from steady state voltage with Load B.
2. This parameter is sampled and not 100% tested.

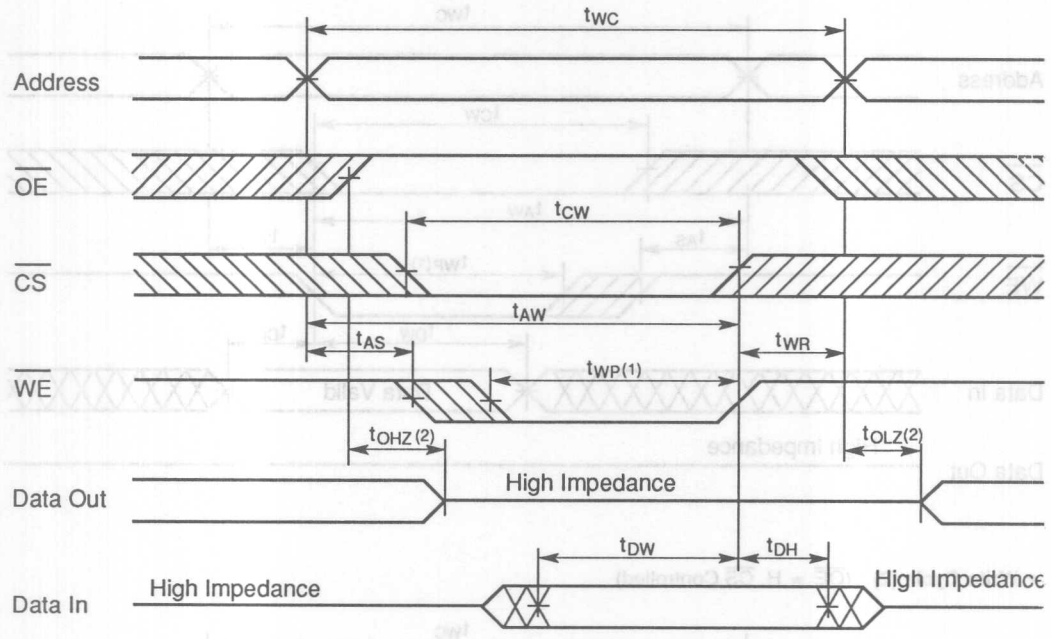
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



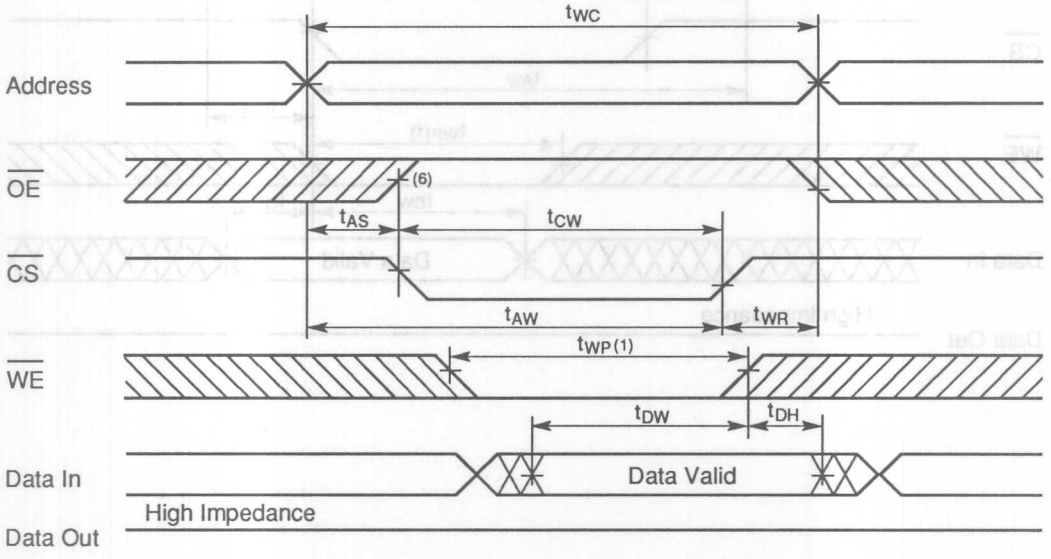
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)

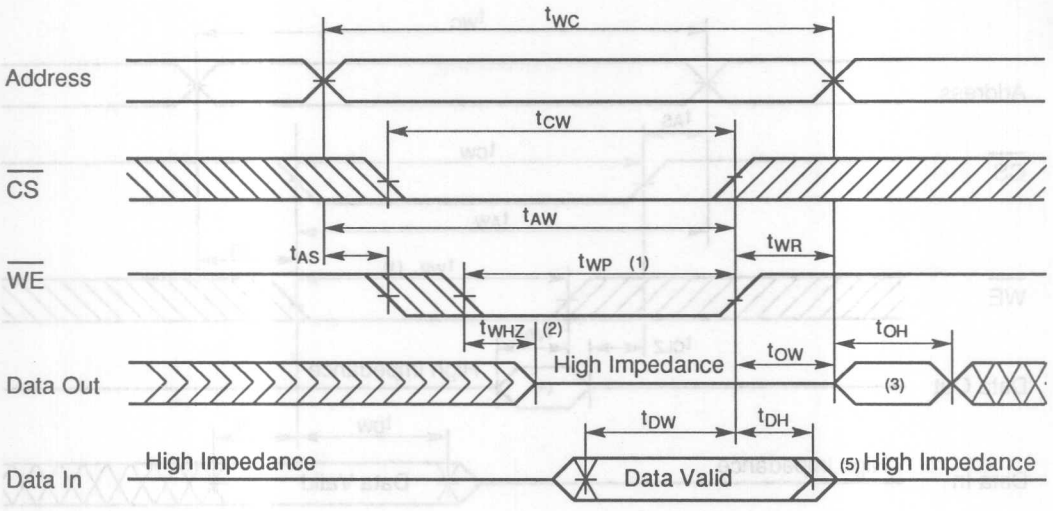


• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)

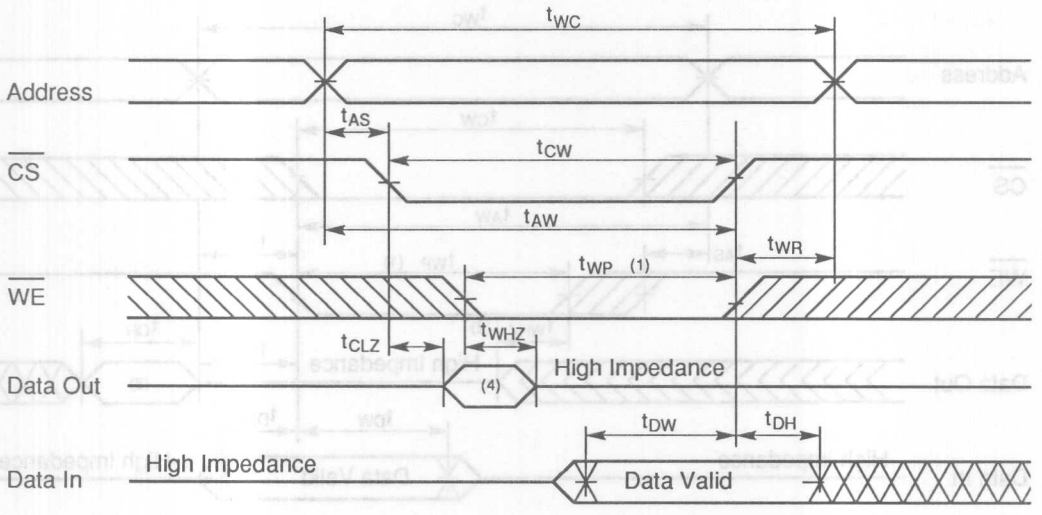


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• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{out} is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

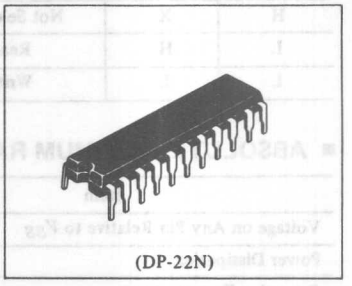
HM6287 Series

Maintenance Only

65536-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
  Standby: 100μW (typ.)/10μW (typ.) (L-version)
  Operation: 300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output
- Capability of Battery Back Up Operation (L-version)

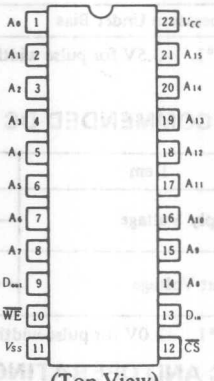


(DP-22N)

■ ORDERING INFORMATION

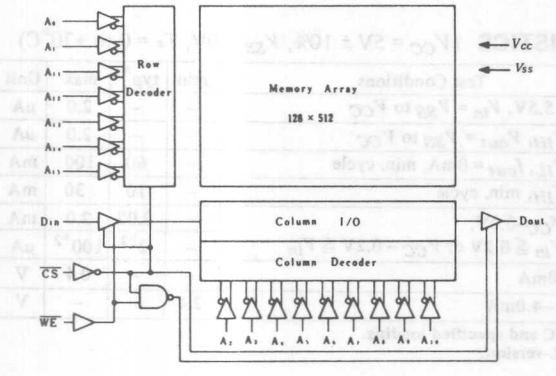
Type No.	Access Time	Package
HM6287P-45	45ns	300 mil 22 pin Plastic DIP
HM6287P-55	55ns	
HM6287P-70	70ns	
HM6287LP-45	45ns	
HM6287LP-55	55ns	
HM6287LP-70	70ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



NOTE: Not for new designs.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{out} = 0mA, min. cycle	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	10	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V,	–	0.02	2.0	mA
		0V ≦ V_{in} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{in}	–	2*2	100*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	5	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	7.5	pF

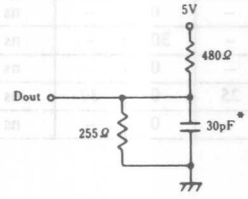
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

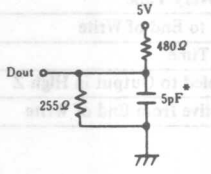
Input Pulse Levels: V_{SS} to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

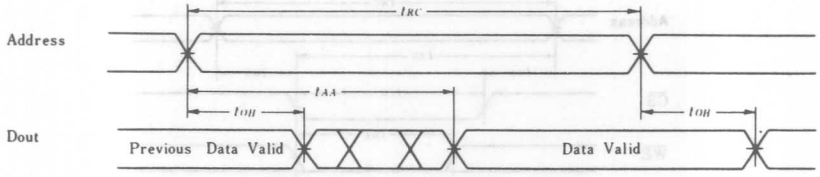


*Including scope & jig capacitance

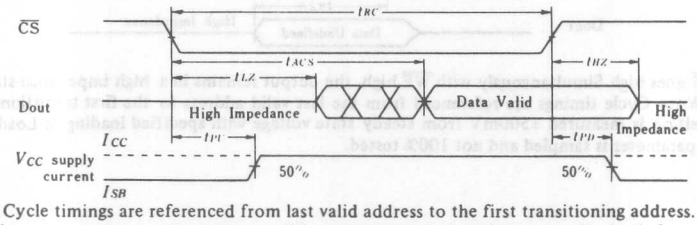
• READ CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns	1
Address Access Time	t_{AA}	–	45	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	7
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	–	40	ns	7

• Timing Waveform of Read Cycle No. 1 (4)(5)



• Timing Waveform of Read Cycle No. 2 (4)(6)

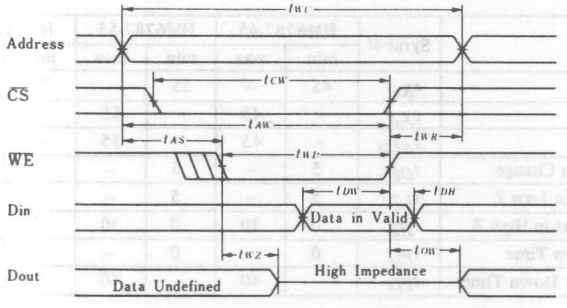


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

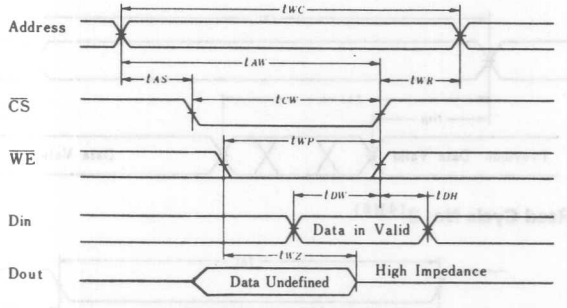
• WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns	2
Chip Selection to End of Write	t_{CW}	40	–	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3, 4

• Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



• Timing Waveform of Write Cycle No. 1 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high Simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

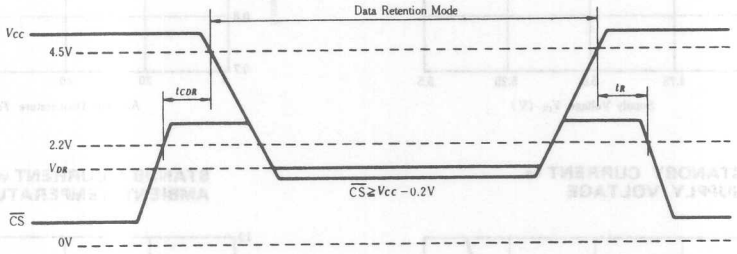
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

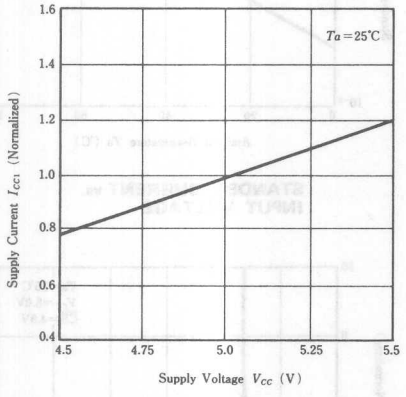
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}		–	1	50*2	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

Note) *1. t_{RC} = Read Cycle Time
*2. V_{CC} = 3.0V

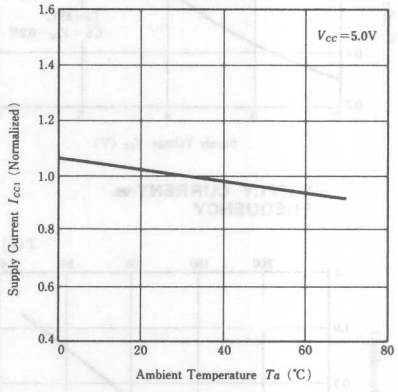
● LOW V_{CC} DATA RETENTION WAVEFORM



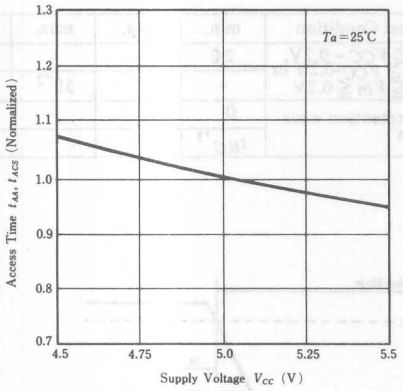
SUPPLY CURRENT vs. SUPPLY VOLTAGE



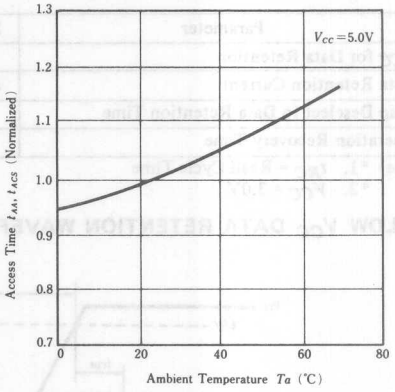
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



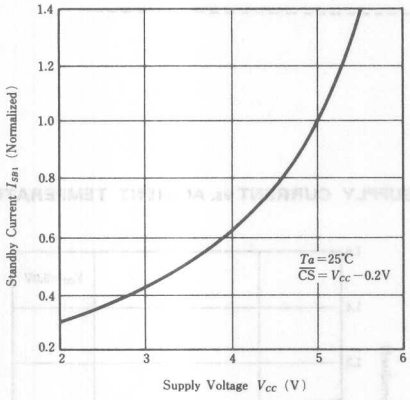
ACCESS TIME vs. SUPPLY VOLTAGE



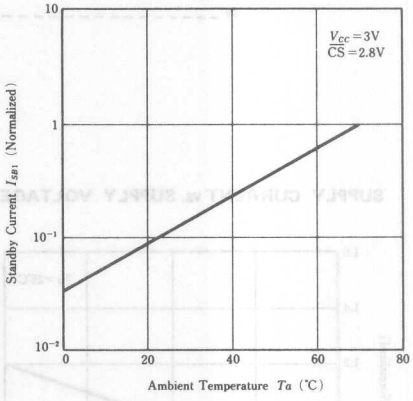
ACCESS TIME vs. AMBIENT TEMPERATURE



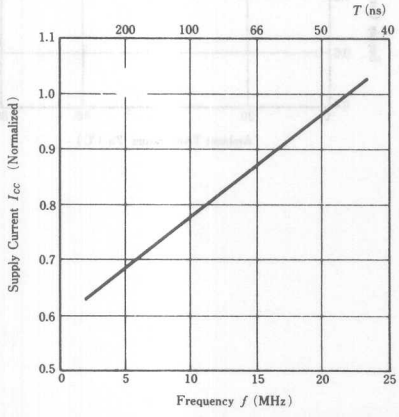
STANDBY CURRENT vs. SUPPLY VOLTAGE



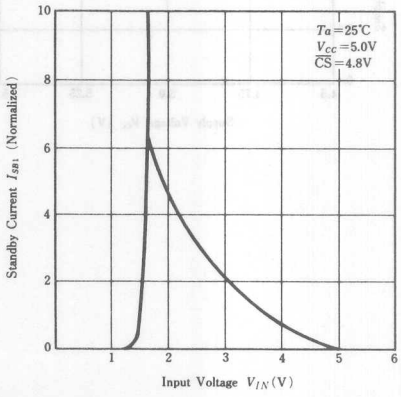
STANDBY CURRENT vs. AMBIENT TEMPERATURE



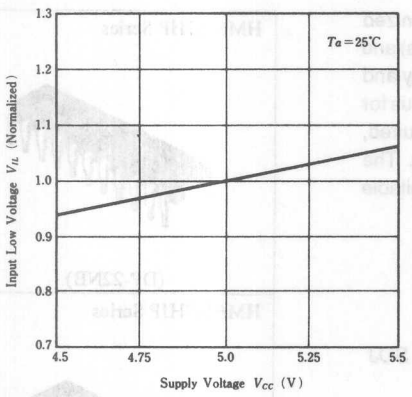
SUPPLY CURRENT vs. FREQUENCY



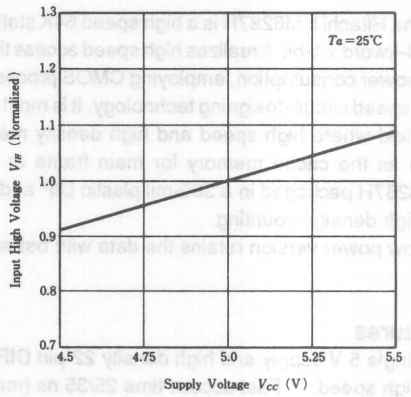
STANDBY CURRENT vs. INPUT VOLTAGE



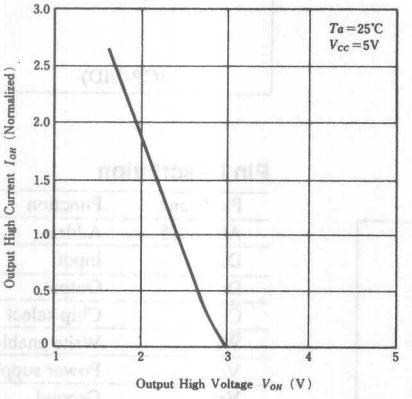
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



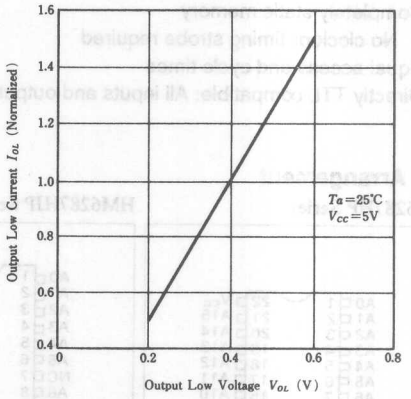
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



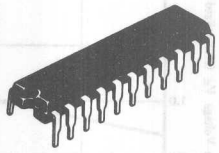
HM6287H Series

65536-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6287H is a high speed 64K static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6287H packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting.

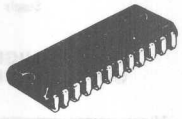
Low power version retains the data with battery back up.

HM6287HP Series



(DP-22NB)

HM6287HJP Series



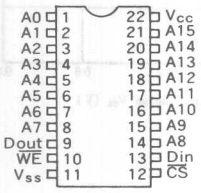
(CP-24D)

Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

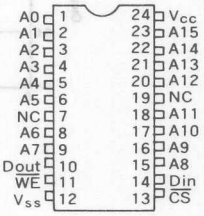
Pin Arrangement

HM6287HP Series



(Top View)

HM6287HJP Series



(Top View)

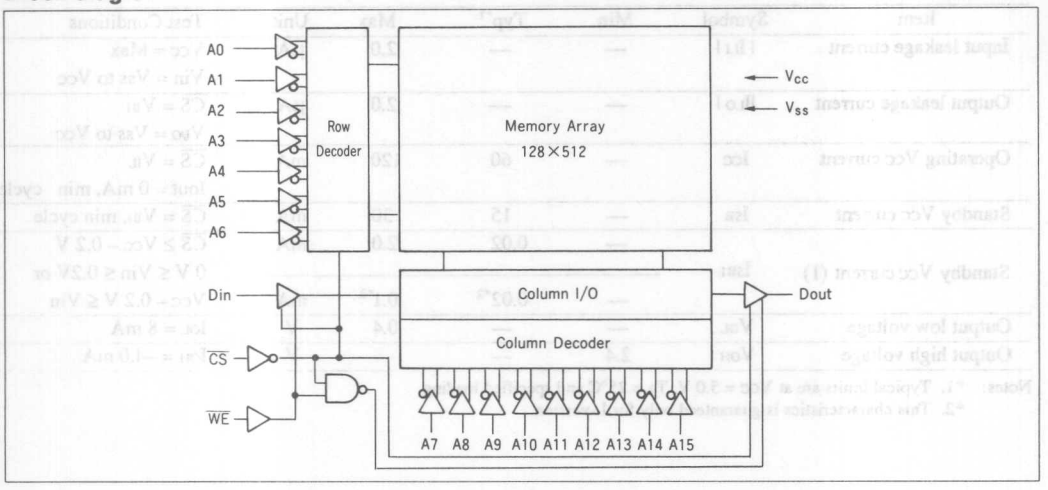
Pin Description

Pin Name	Function
A0 – A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM6287HP-25	25 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

Block diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	D_{out} Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	D_{out}	Read cycle 1, 2
L	L	Write	Icc	High-Z	Write cycle 1, 2

Note: ×: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: *1. V_T min = –2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = Vss to Vcc
Operating Vcc current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL} Iout = 0 mA, min cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby Vcc current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V 0 V ≤ Vin ≤ 0.2V or
		—	0.02*2	0.1*2	mA	Vcc – 0.2 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	8	pF	Vout = 0 V

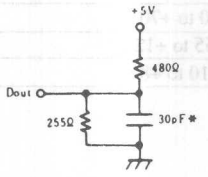
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

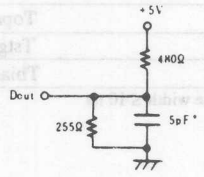
Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

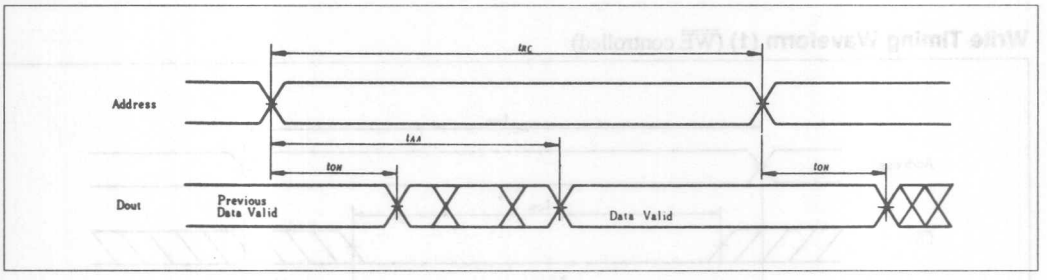


Note: Including scope & jig

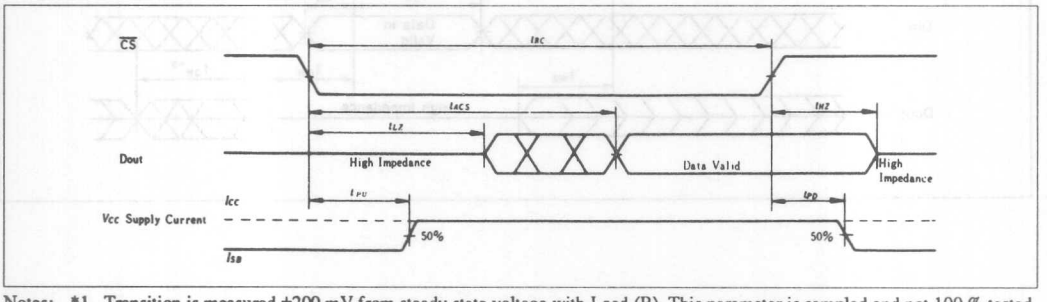
Read Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Read Timing Waveform (1) *2, *3, *5



Read Timing Waveform (2) *2, *4

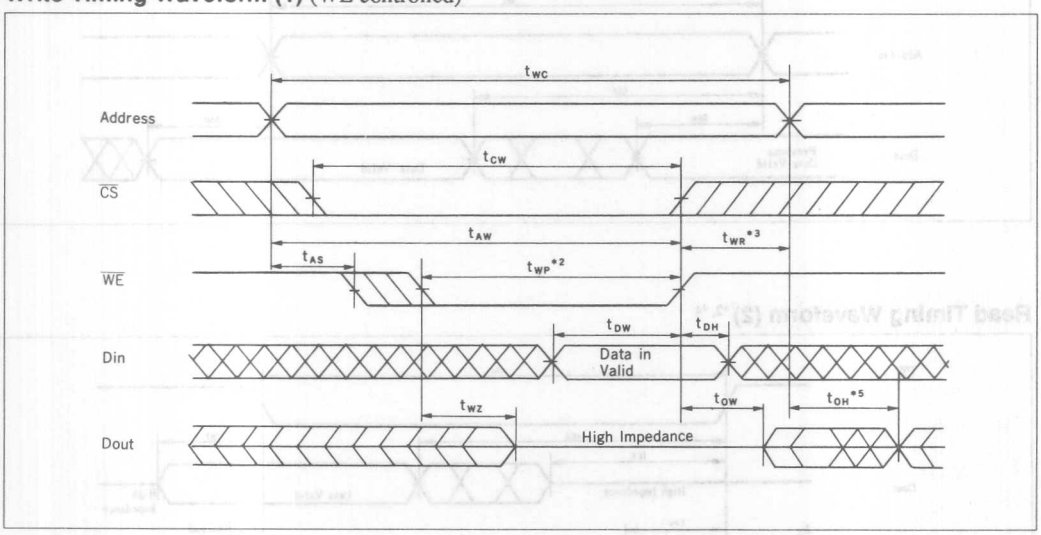


Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100 % tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. All read cycle timing are referenced from last valid address to the first transitioning address.

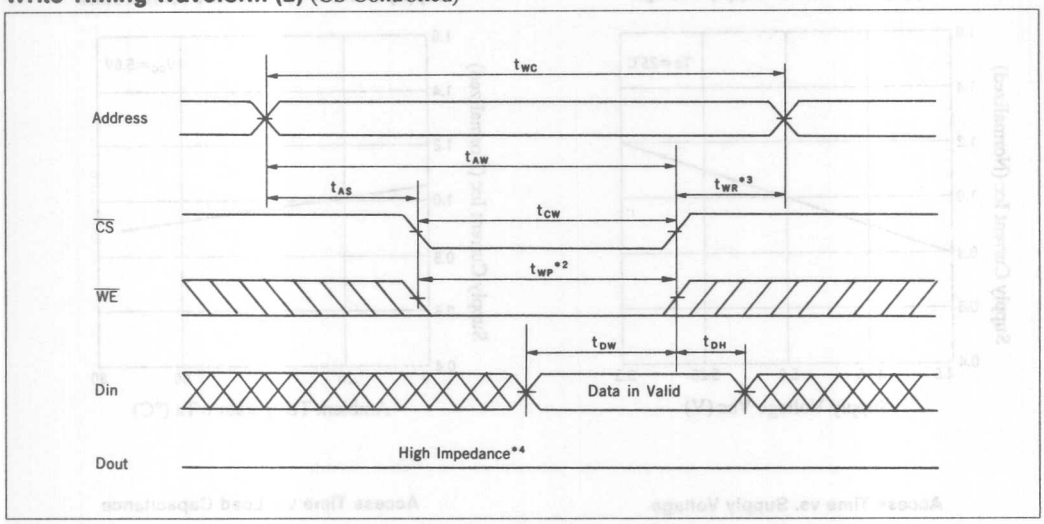
Write Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	8	0	10	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{WE}$ controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

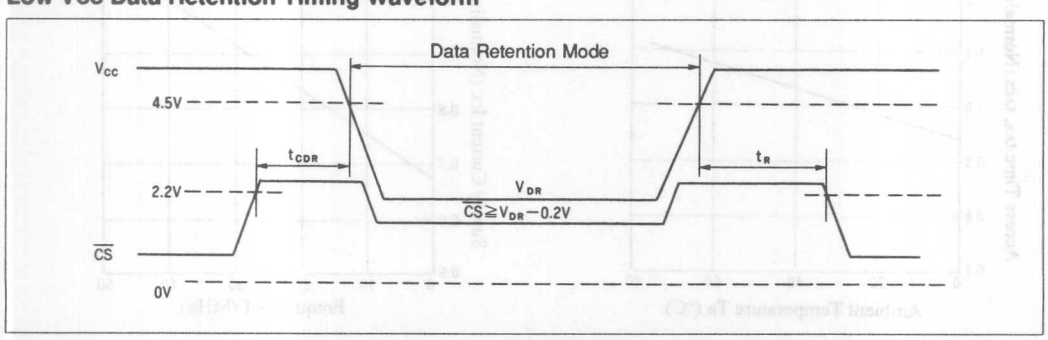
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

(This specification is guaranteed only for L-version.)

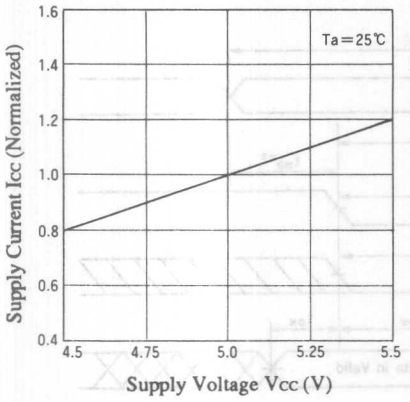
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V
Data retention current	I_{CCDR}	—	—	50*2 35*3	µA	Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

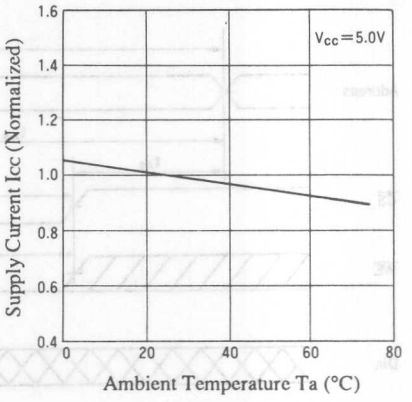
Low Vcc Data Retention Timing Waveform



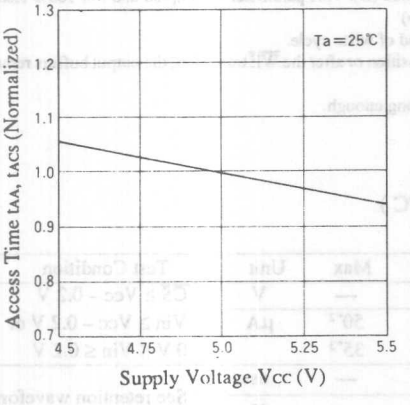
Supply Current vs. Supply Voltage



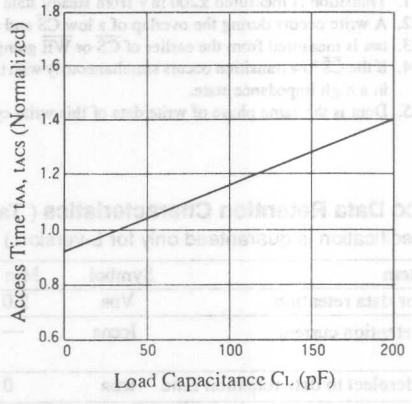
Supply Current vs. Ambient Temperature



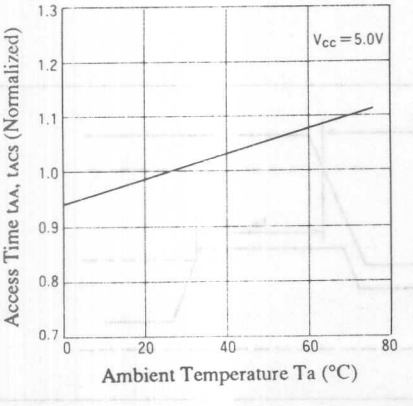
Access Time vs. Supply Voltage



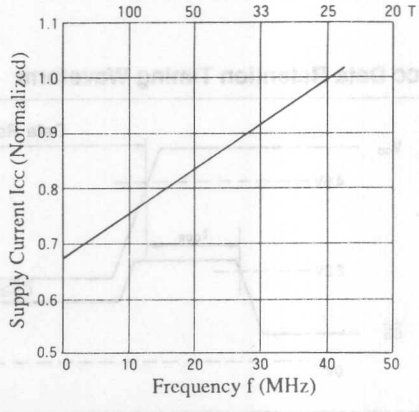
Access Time vs. Load Capacitance



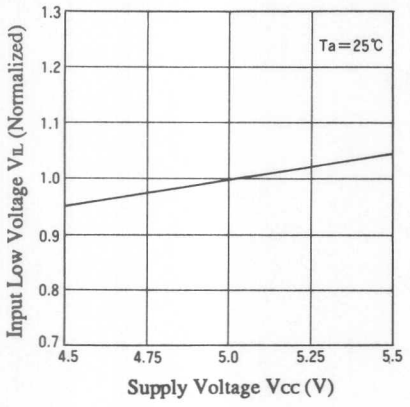
Access Time vs. Ambient Temperature



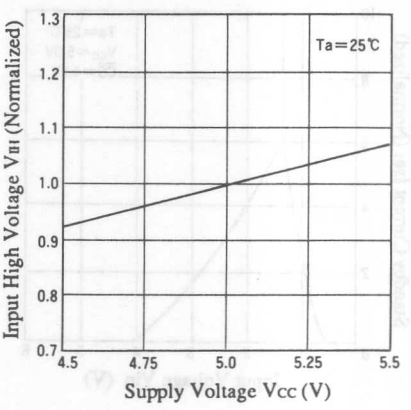
Supply Current vs. Frequency



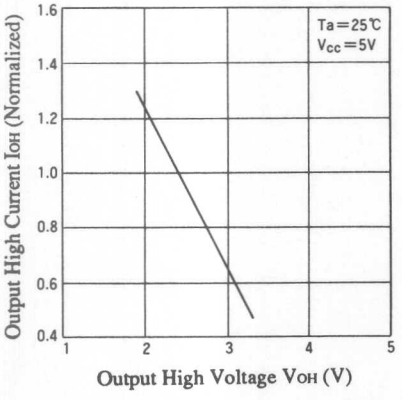
Input Low Voltage vs. Supply Voltage



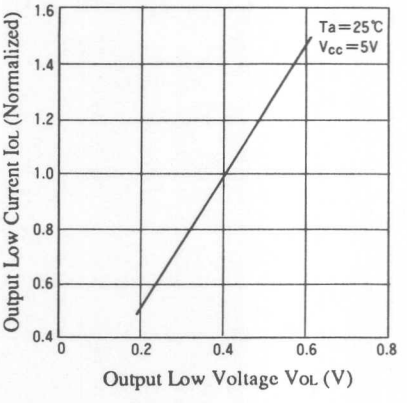
Input High Voltage vs. Supply Voltage



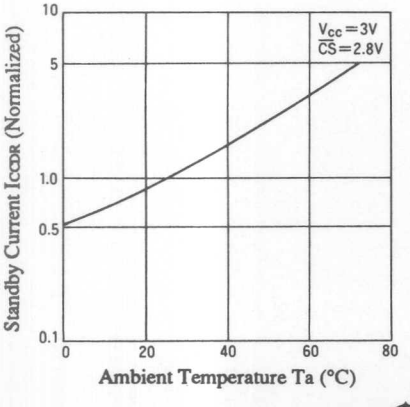
Output Current vs. Output Voltage (1)



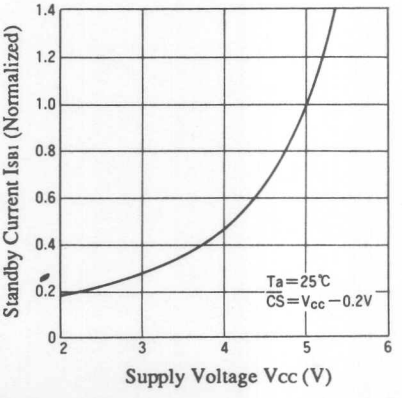
Output Current vs. Output Voltage (2)



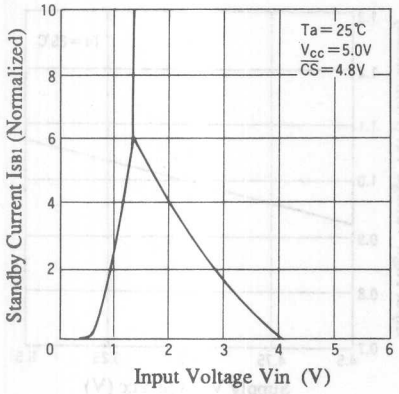
Standby Current vs. Ambient Temperature



Standby Current vs. Supply Voltage



Standby Current vs. Input Voltage



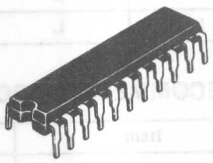
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HM6787 Series

Maintenance Only

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

HM6787P Series



(DP-22NB)

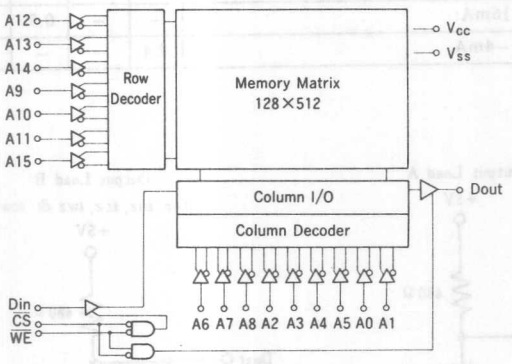
■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
  Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 22-pin Plastic Dip (300 mil) and 22-pin Chip Carrier

■ ORDERING INFORMATION

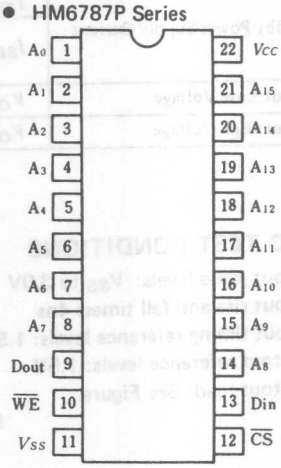
Type No.	Access Time	Package
HM6787P-25	25ns	300 mil 22 pin
HM6787P-30	30ns	Plastic DIP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

- HM6787P Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

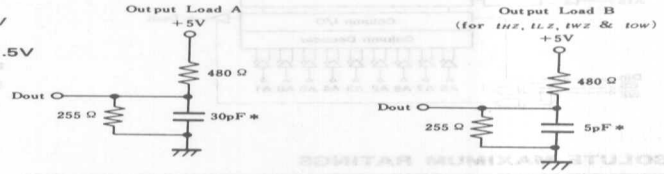
Note) *1. −3.0V for pulse width ≦ 20ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT}=0mA	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	–	40	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$	–	–	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 16mA	–	–	0.5	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	–	–	V

■ AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



* Including scope and jig.

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■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	7.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

• READ CYCLE

Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	
Address Access Time	t_{AA}	–	25	–	30	ns	
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	2
Chip Deselection to Power Down Time	t_{PD}	–	25	–	30	ns	2
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	3

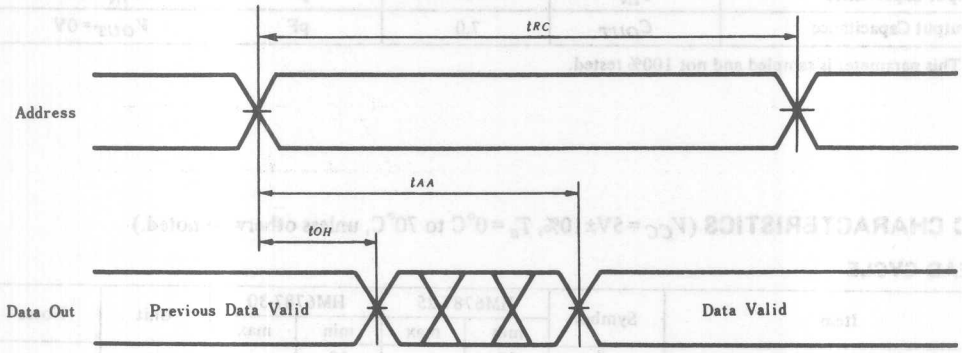
Notes) 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
2. This parameter is sampled and not 100% tested.
3. If t_T becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi's Sale Dept. regarding specification.

• WRITE CYCLE

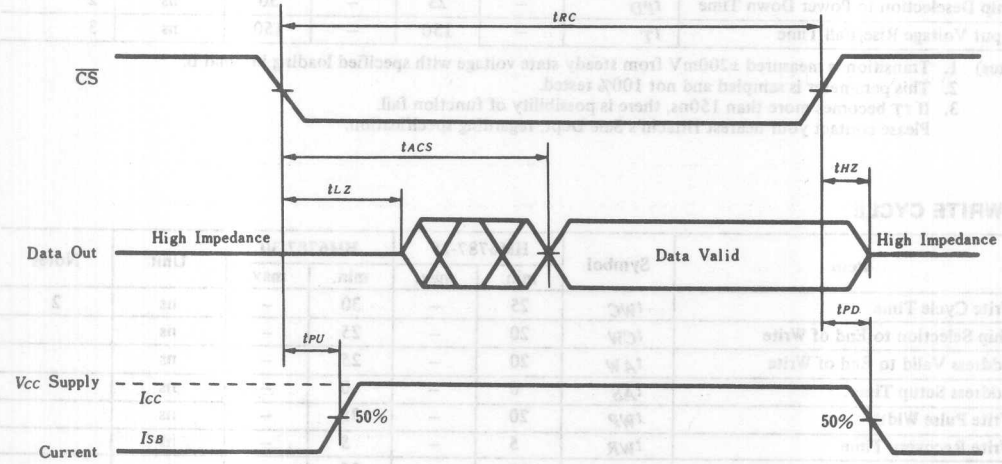
Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	–	30	–	ns	2
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	5	–	5	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[1), 2)]

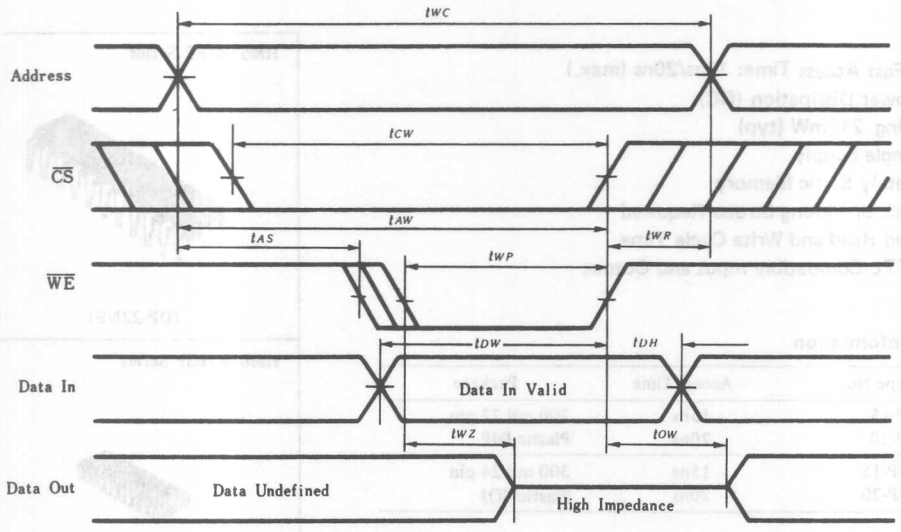


• TIMING WAVEFORM OF READ CYCLE NO. 2[1), 3)]



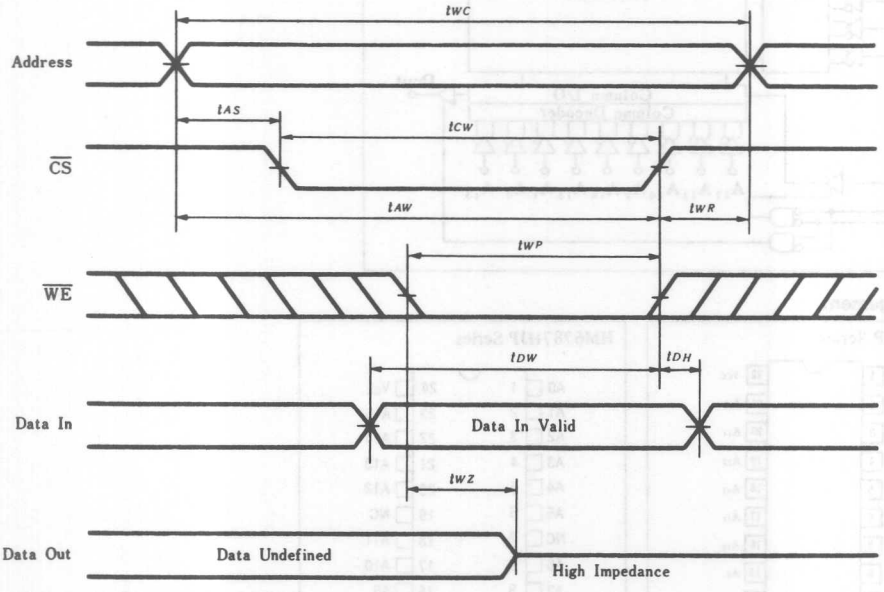
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

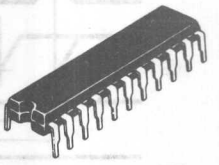
HM6787H Series

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time: 15ns/20ns (max.)
- Low Power Dissipation (DC):
  Operating 210mW (typ)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6787HP Series



(DP-22NB)

HM6787HJP Series

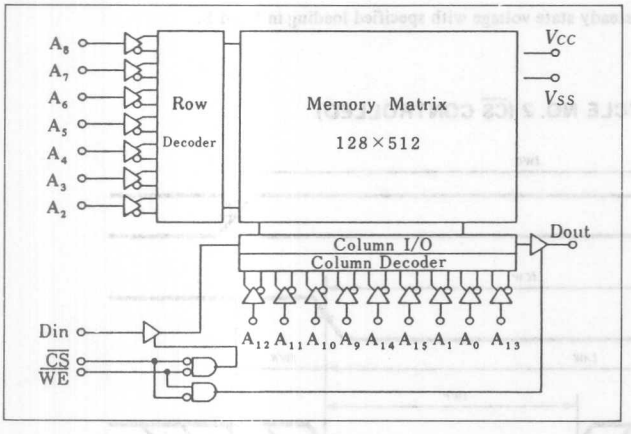


(CP-24D)

Ordering Information

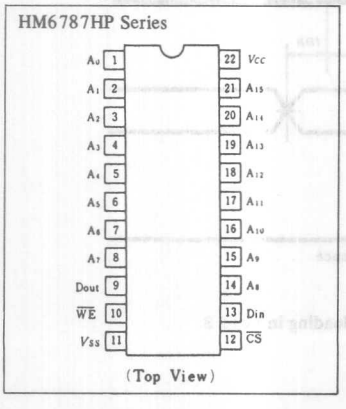
Type No.	Access Time	Package
HM6787HP-15	15ns	300 mil 22 pin
HM6787HP-20	20ns	Plastic DIP
HM6787HJP-15	15ns	300 mil 24 pin
HM6787HJP-20	20ns	Plastic SOJ

Block Diagram



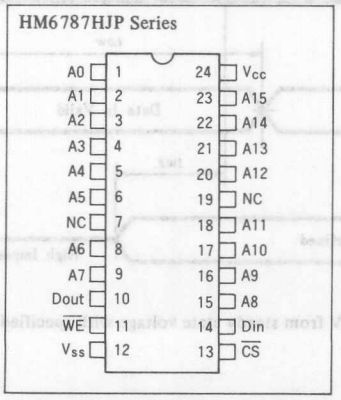
Pin Arrangement

HM6787HP Series



(Top View)

HM6787HJP Series



Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Dout
L	L	Write	I_{CC}, I_{CC1}	High Z

Recommended DC Operating Conditions ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

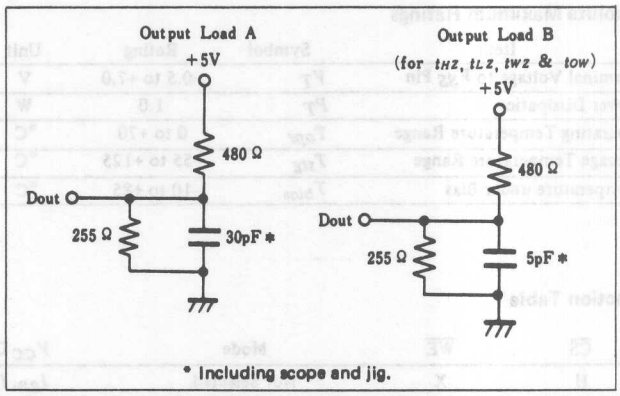
Note) *1. −3.0V for pulse width ≦ 10ns.

DC and Operating Characteristics (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, I_{OUT}=0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100% I_{OUT} = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2

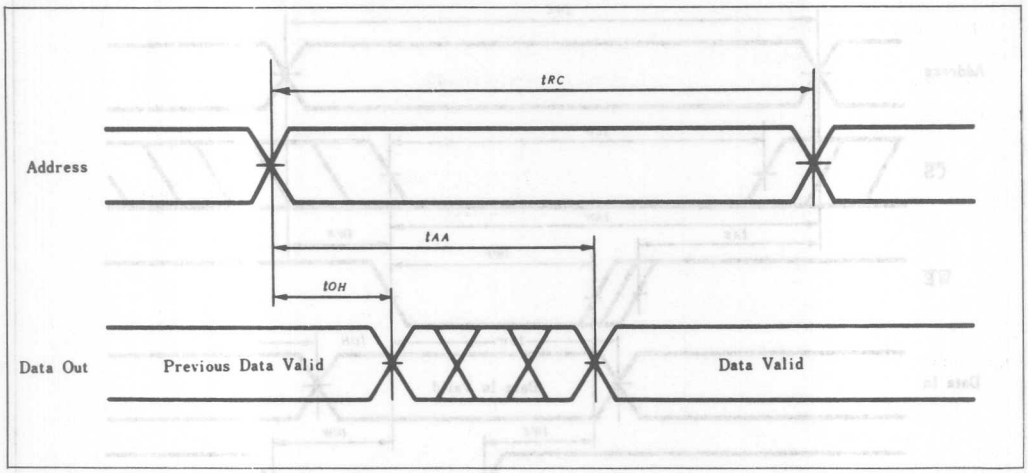
Note: 1. This parameter is sampled and 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Write Cycle

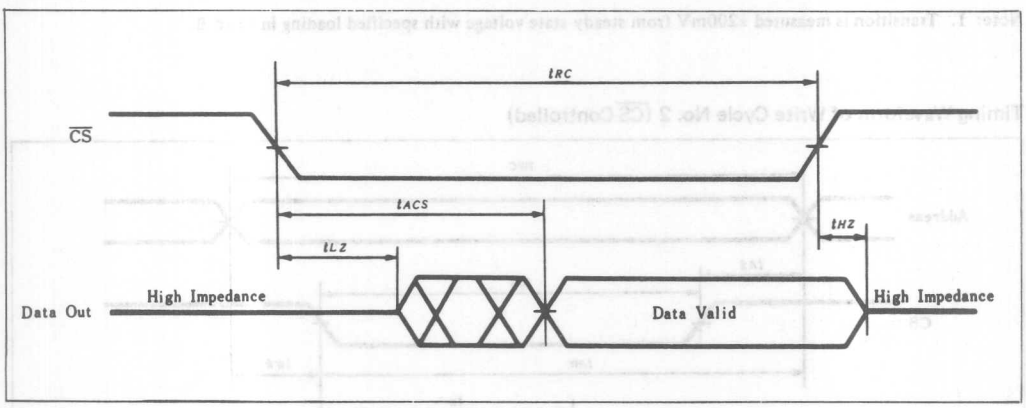
Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Timing Waveform of Read Cycle No. 1[1), 2)]

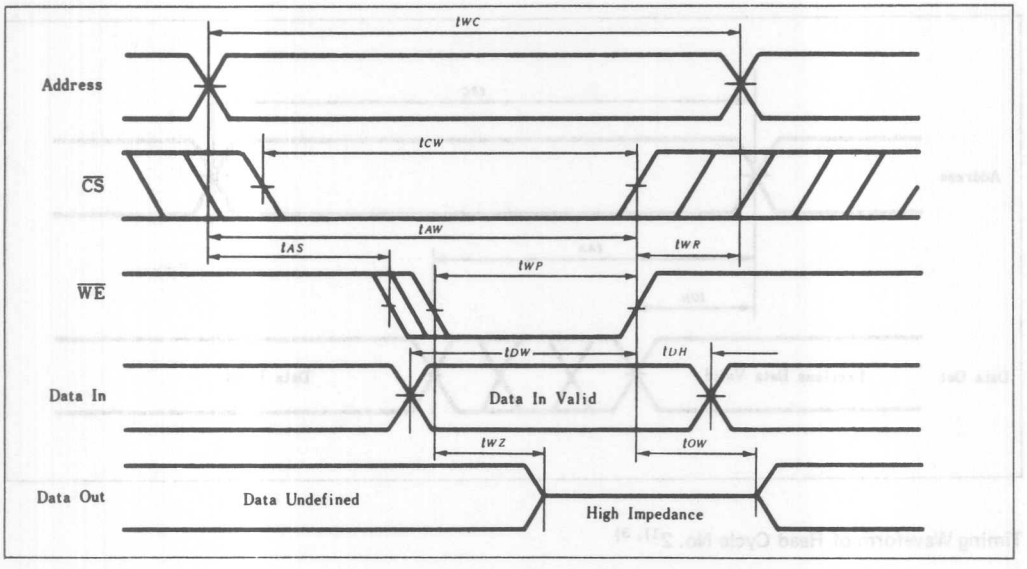


Timing Waveform of Read Cycle No. 2[1), 3)]



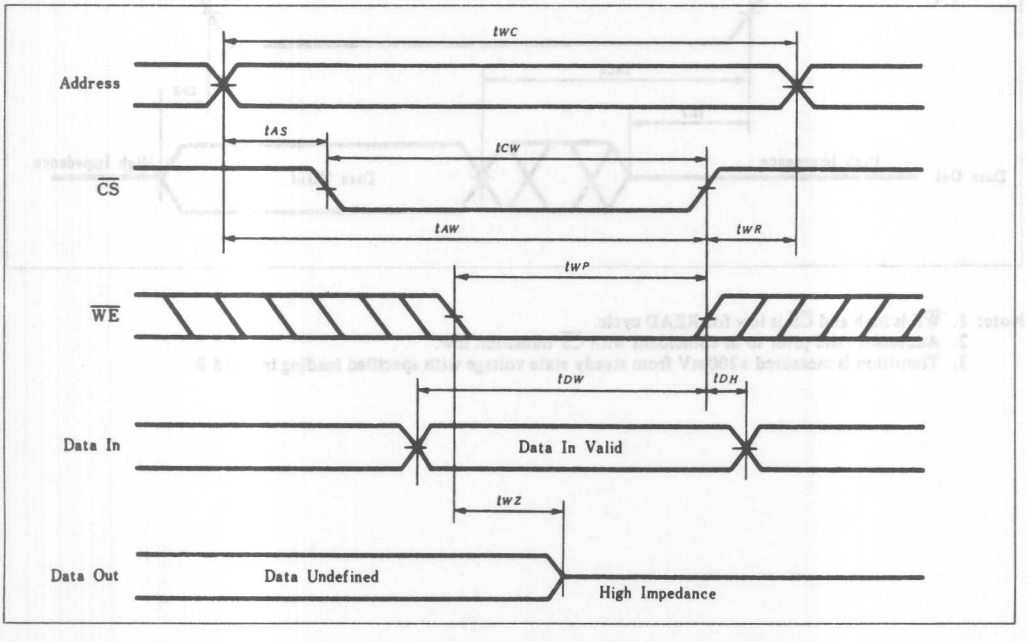
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

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HM6787HA Series — Preliminary

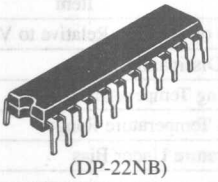
65536-Word × 1-Bit High Speed Static RAM

■ FEATURES

- Super Fast
  Access Time. . . . . .12/15/20ns (max.)
- Low Power Dissipation
  (DC) Operating . . . . . .300mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6787HAP-12 HM6787HAP-15 HM6787HAP-20	12ns 15ns 20ns	300 mil 22 pin Plastic DIP (DP-22NB)
HM6787HAJP-12 HM6787HAJP-15 HM6787HAJP-20	12ns 15ns 20ns	300 mil 24 pin Plastic SOJ (CP-24D)

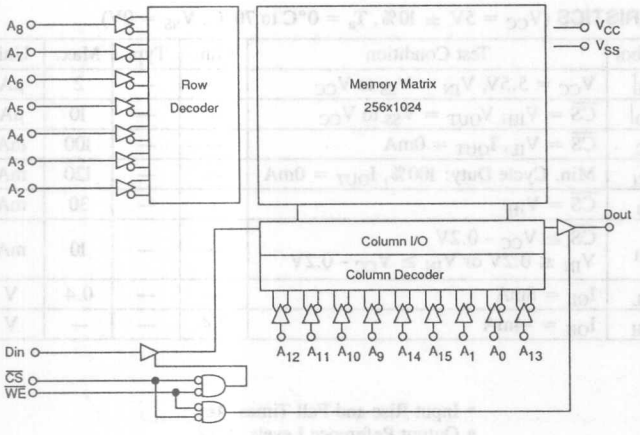


(DP-22NB)



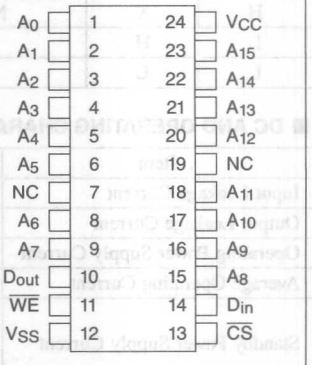
(CP-24D)

■ BLOCK DIAGRAM



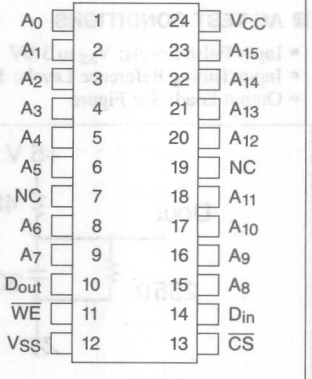
■ PIN ARRANGEMENT

HM6787HAP Series



(Top View)

HM6787HAJP Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width ≤ 10ns, DC: −0.5V

■ TRUTH TABLE

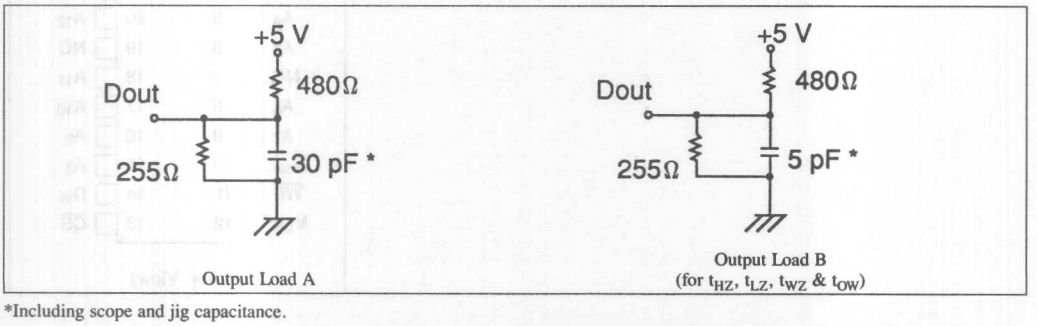
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Data Out
L	L	Write	I_{CC}, I_{CC1}	High Z

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$, $V_{SS} = 0V$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$, $V_{OUT} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{OUT} = 0mA$	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle Duty: 100%, $I_{OUT} = 0mA$	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Load: See Figure
- Input Rise and Fall Times: 4ns
- Output Reference Levels: 1.5V



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a to 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6787HA-12		HM6787HA-15		HM6787HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6787HA-12		HM6787HA-15		HM6787HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	7	—	8	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	3, 4

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

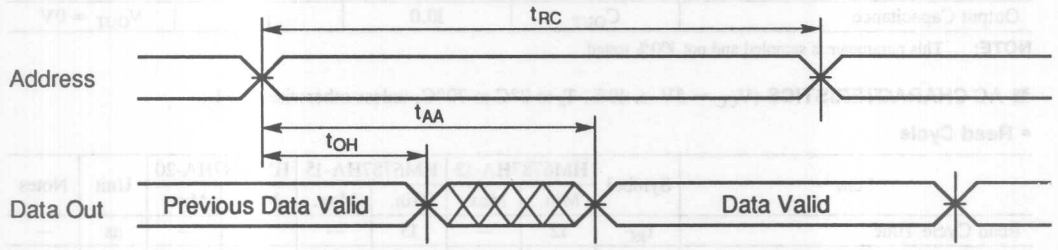
2. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

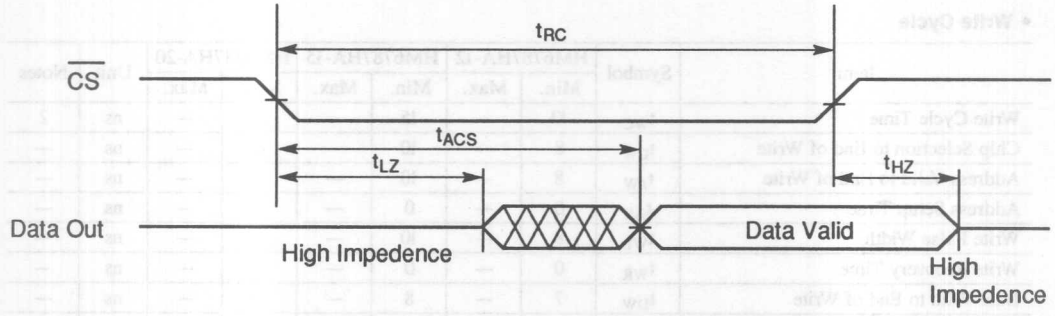
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1) (2)

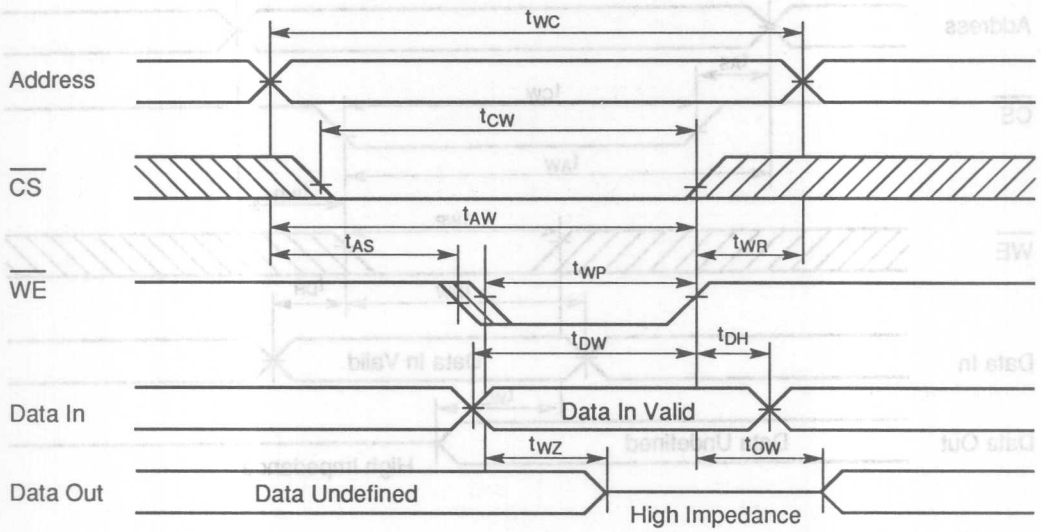


• **Read Cycle (2)** (1) (3)



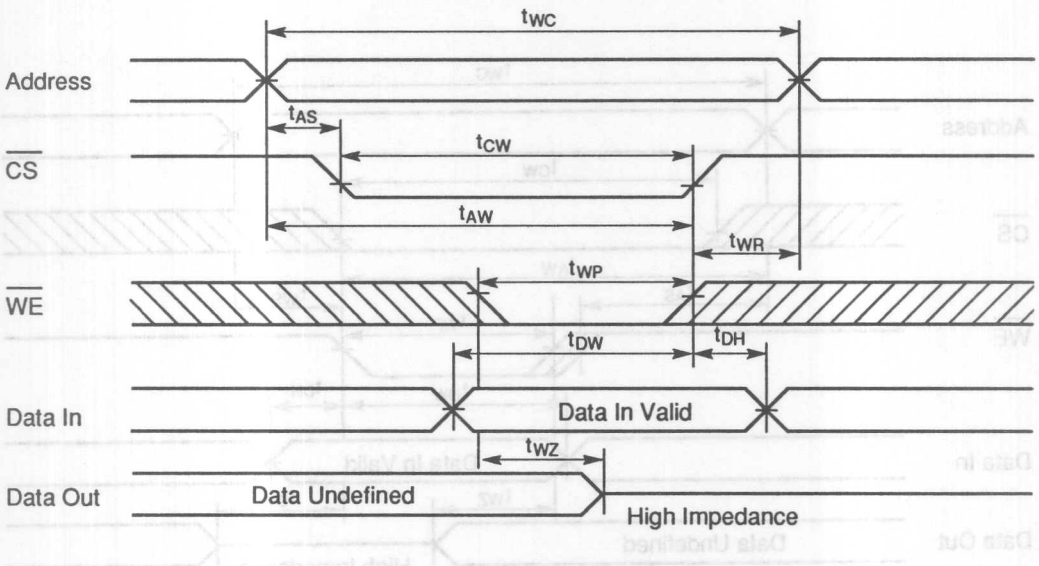
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



NOTE: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTE: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

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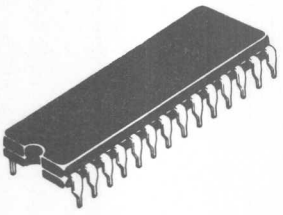
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

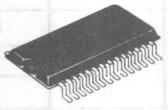
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

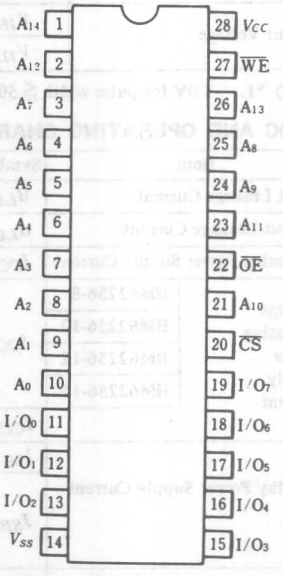


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



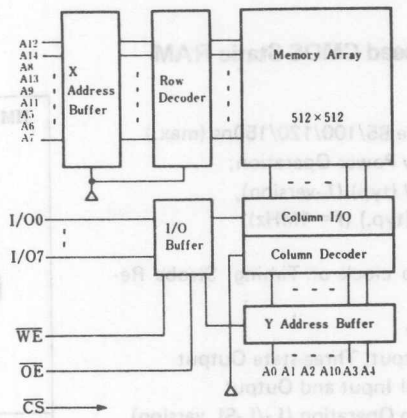
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty=100%, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0V, $I_{I/O}$ = 0mA, f = 1MHZ	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}$ = V_{IH}	–	0.5	3	mA
		I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V, 0V ≦ V_{IN}	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
		V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

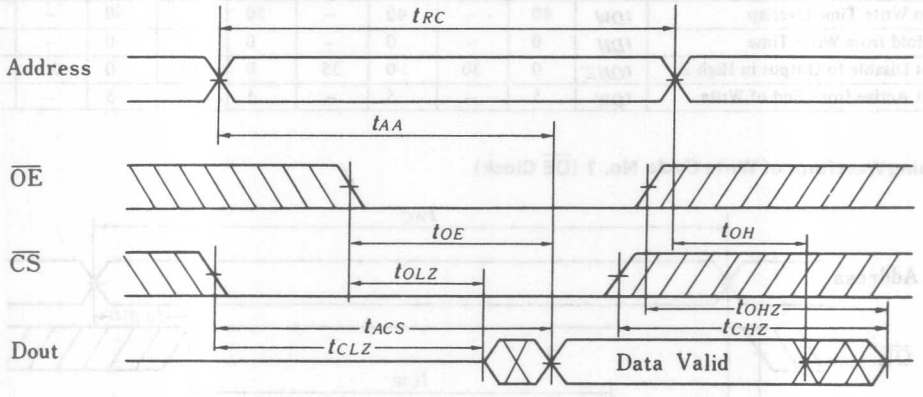
■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

- **AC Test Conditions**
  - ○ Input pulse levels: 0.8V to 2.4V
  - ○ Input rise and fall times: 5ns
  - ○ Input and Output timing reference levels: 1.5V
  - ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

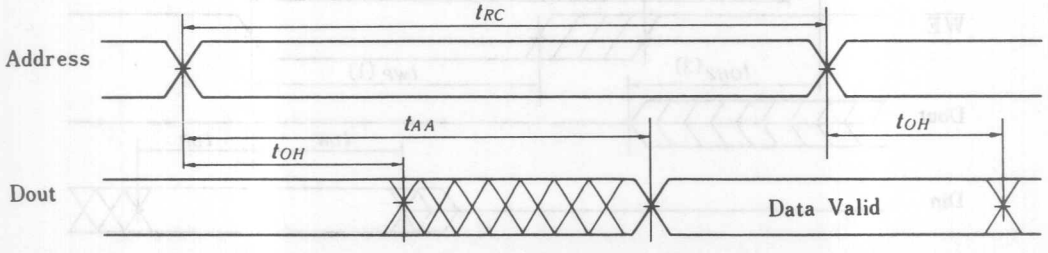
- **Read Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

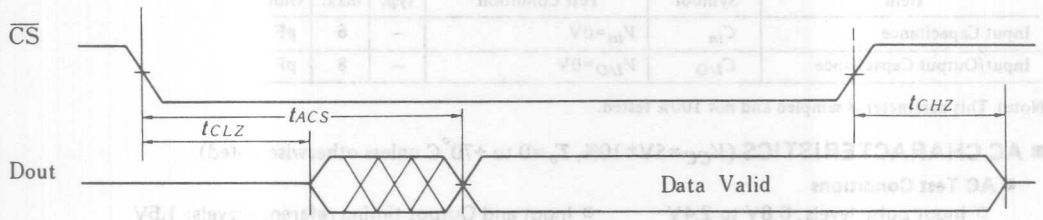
- **Timing Waveform of Read Cycle No. 1[1]**



- **Timing Waveform of Read Cycle No. 2[1][2][4]**



- **Timing Waveform of Read Cycle No. 3[1][3][4]**

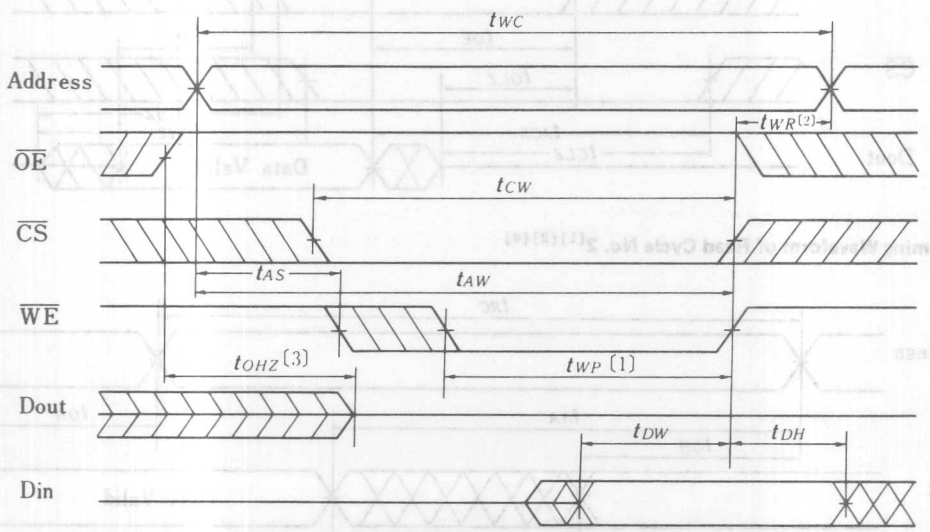


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

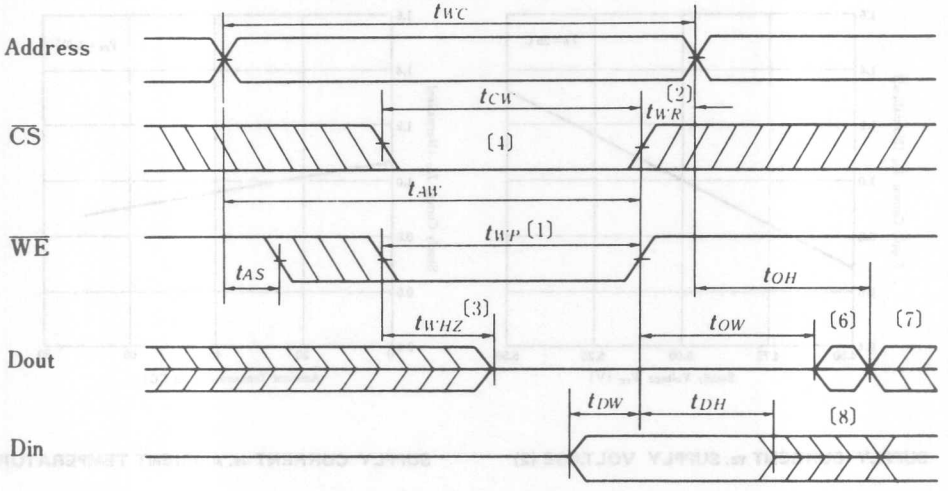
- **Write Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

- **Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)**



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

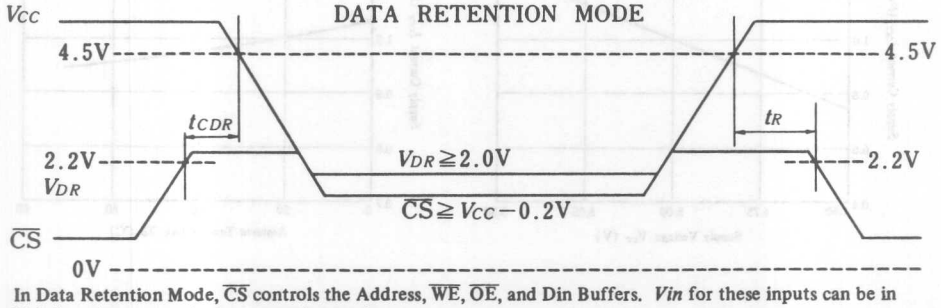
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ –0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq$ 2.8V 0V ≦ V_{in}	–	–	50*2	µA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

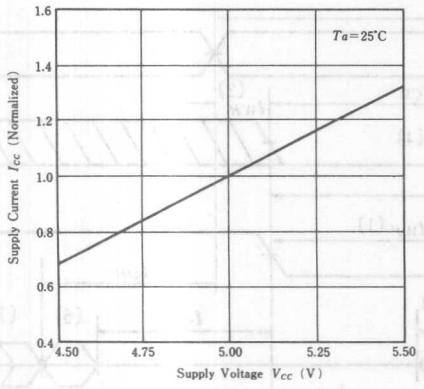
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20µA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3µA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

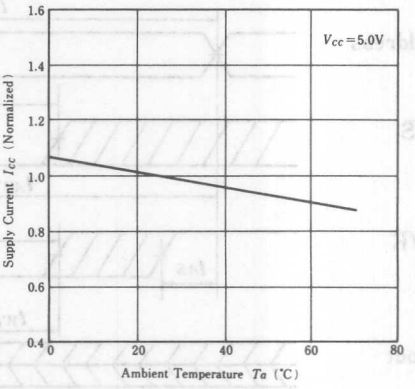


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

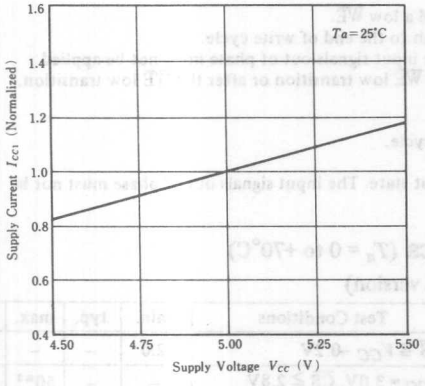
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



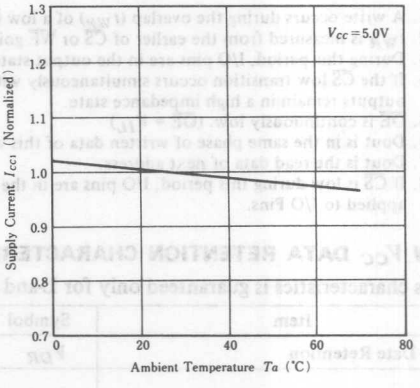
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



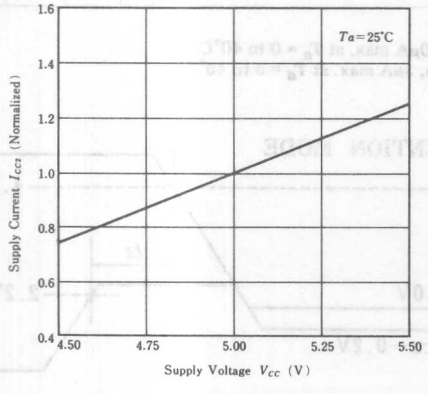
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



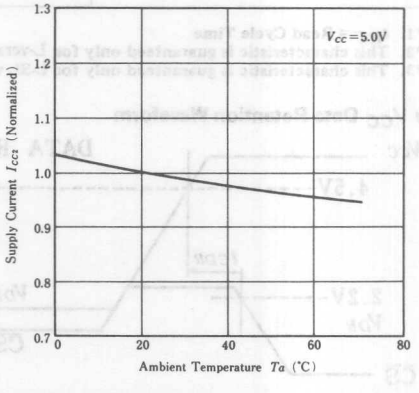
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)

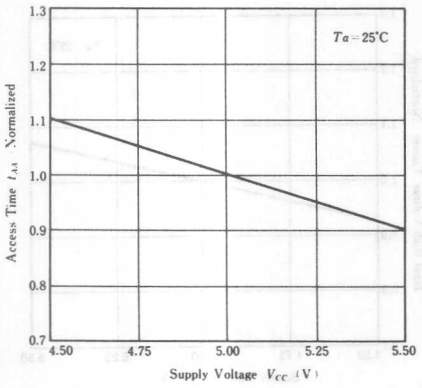


SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)

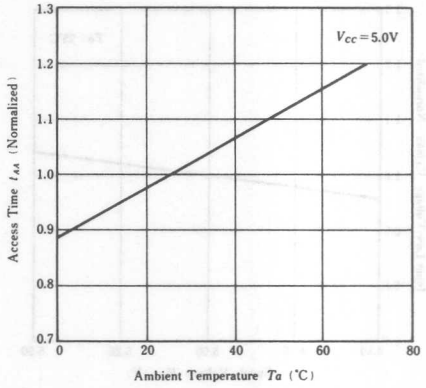


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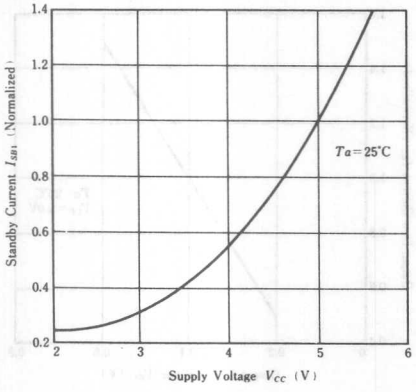
ACCESS TIME vs. SUPPLY VOLTAGE



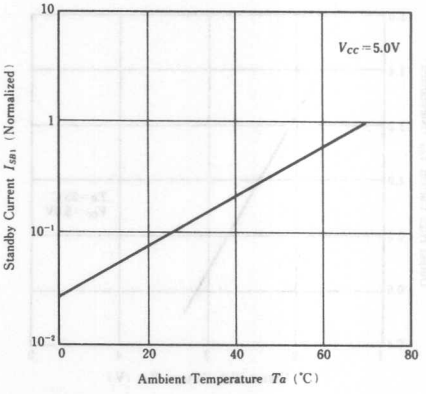
ACCESS TIME vs. AMBIENT TEMPERATURE



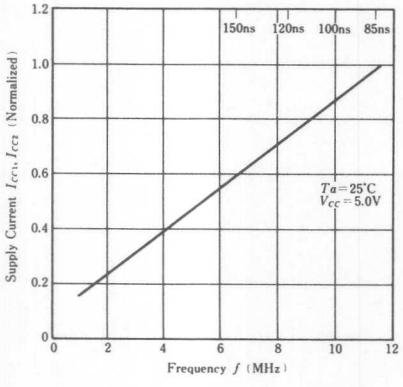
STANDBY CURRENT vs. SUPPLY VOLTAGE



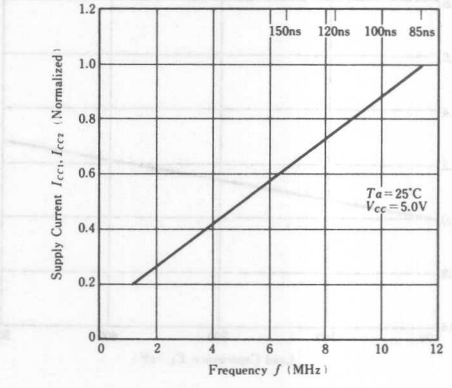
STANDBY CURRENT vs. AMBIENT TEMPERATURE



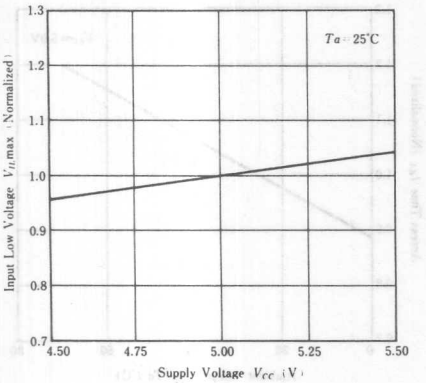
SUPPLY CURRENT vs. FREQUENCY (READ)



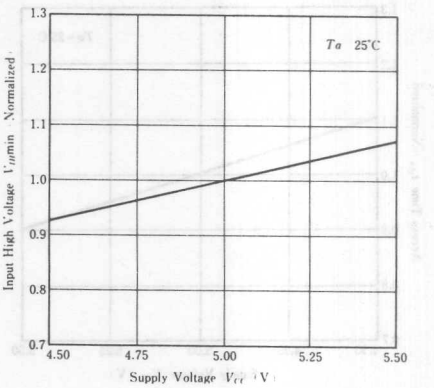
SUPPLY CURRENT vs. FREQUENCY (WRITE)



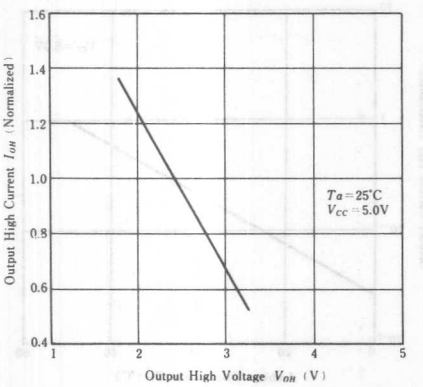
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



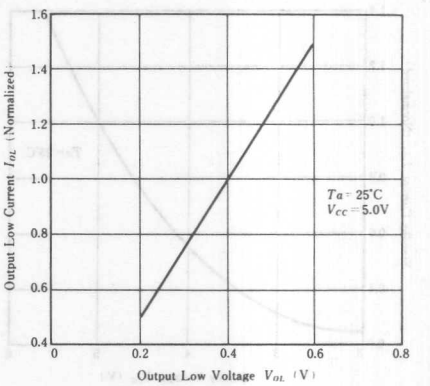
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



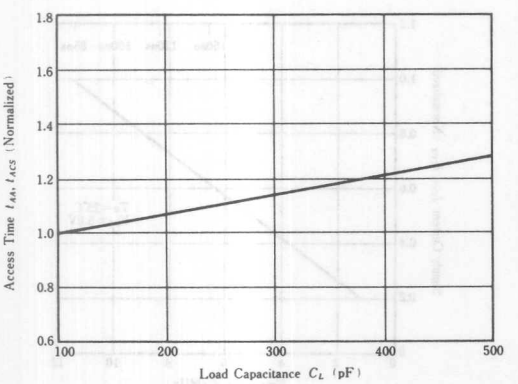
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

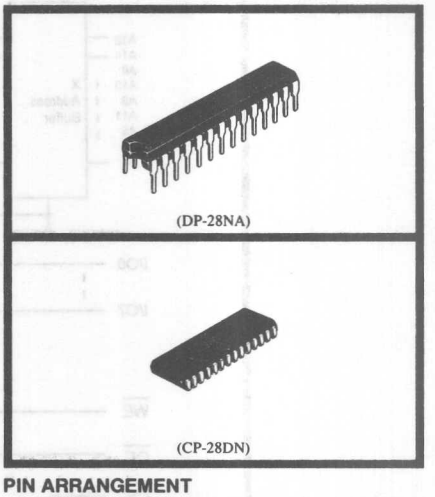


ACCESS TIME vs. LOAD CAPACITANCE



HM62832/HM62832H
8-Bit CMOS Static RAM

32768-WORD × 8-BIT HIGH SPEED CMOS STATIC RAM



■ FEATURES

- High speed: Fast Access time 25/35/45 ns (max.)

HM62832—Low power
Standby: 10 μW (typical) (L-version)
Active: 300 mW (typical)

HM62832H—Low power
Standby: 300 mW (typical)
Active: 30 μW (typical) (L-version)

- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three stage output
- Directly TTL compatible—All inputs and outputs

■ ORDERING INFORMATION

Part No.	Access	Package
HM62832P-35	35 ns	300 mil 28-pin Plastic DIP
HM62832P-45	45 ns	
HM62832LP-35	35 ns	
HM62832LP-45	45 ns	
HM62832JP-35	35 ns	300 mil 28-pin Plastic SOJ
HM62832JP-45	45 ns	
HM62832LJP-35	35 ns	
HM62832LJP-45	45 ns	
HM62832HP-25	25 ns	300 mil 28-pin Plastic DIP (DP-28NA)
HM62832HP-35	35 ns	
HM62832HP-45	45 ns	
HM62832HJP-25	25 ns	300 mil 28-pin Plastic SOJ (CP-28DN)
HM62832HJP-35	35 ns	
HM62832HJP-45	45 ns	

PIN ARRANGEMENT

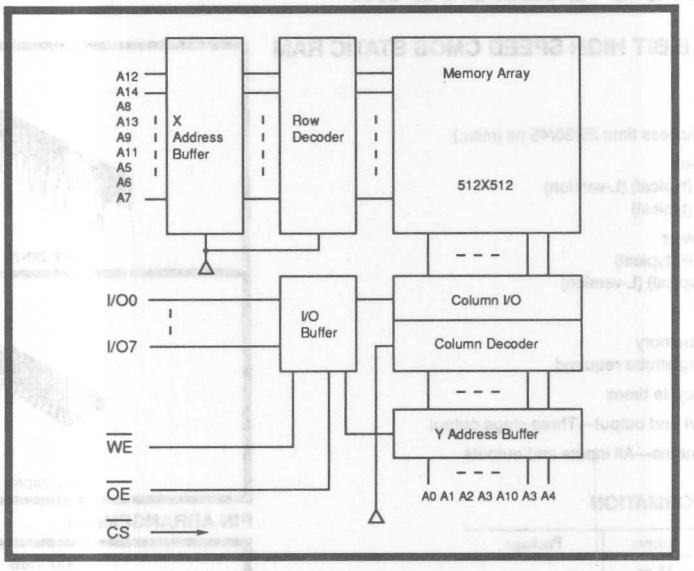
Top View



■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{14}	Address
I/O_0–I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−0.5*1 to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: 1. −2.5 V for pulse width ≤ 10 ns

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	• Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1) to (3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L		I_{CC}	D_{in}	Write Cycle(2)

NOTE: 1. X : H or L

■ DC CHARACTERISTICS for HM62832 (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	10	μA	$V_{in} = V_{SS}$ to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	10	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}	
Average Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0 mA	
Standby V_{CC} Current	I_{SB}	—	15	30	mA	$\overline{CS} = V_{IH}$	
	I_{SB1}	—	2	100	μA	$\overline{CS} \geq V_{CC} - 0.2V$, $0\ V \leq V_{in} \leq 0.2\ V$, or $V_{in} \geq V_{cc} - 0.2\ V$	L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ DC CHARACTERISTICS for HM62832H (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}	
Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0 mA	
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS} = V_{IH}$	
Standby Power Supply Current	I_{SB1}	—	0.02	2	mA	$\overline{CS} \geq V_{CC} - 0.2V$, $0\ V \leq V_{in} \leq 0.2\ V$, or $V_{in} \geq V_{cc} - 0.2\ V$	
		—	0.006	0.1	mA		L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

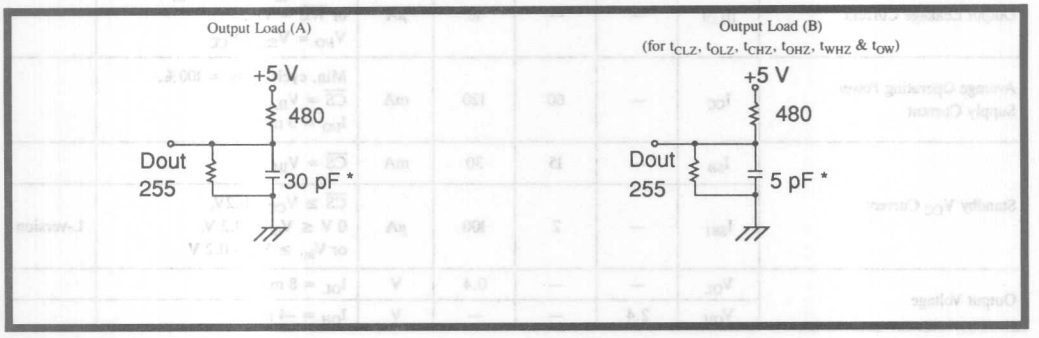
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures

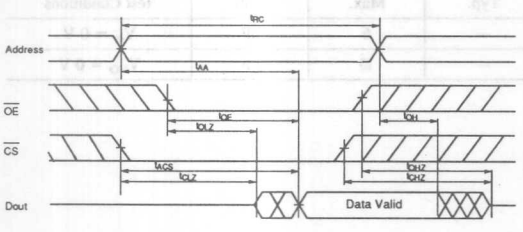


NOTE: *Including scope & jig.

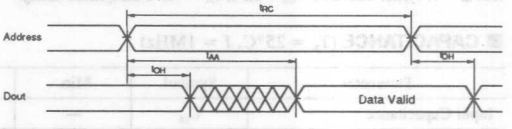
■ Read Cycle

Parameter	Symbol	HM62832H-25		HM62832-35 HM62832H-35		HM62832-45 HM62832H-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	—	20	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{CLZ}	5	—	5	—	5	—	ns
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}	0	12	0	15	0	15	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	0	15	ns

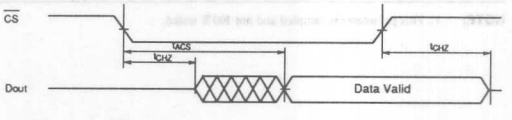
Read Cycle Timing (1) *1



Read Cycle Timing (2) *1, *2, *4



Read Cycle Timing (3) *1, *3, *4



NOTES: *1. $\overline{WE}$ is high for read cycle.

*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

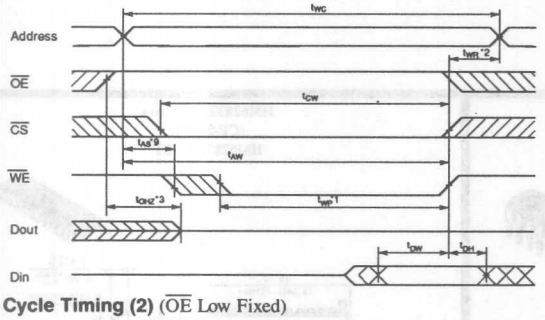
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.

*4. $\overline{OE}$ = V_{IL}.

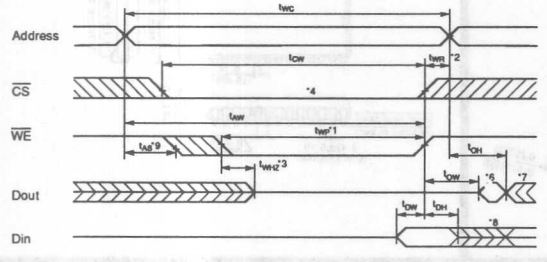
■ Write Cycle

Item	Symbol	HM62832H-25		HM62832-35 HM62832H-35		HM62832-45 HM62832H-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	15	—	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Write to Output in High-Z	t_{WHZ}	0	15	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	0	20	ns
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ Low Fixed)



NOTES:

*1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

*5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$).

*6. D_{out} is in the same phase of written data of this write cycle.

*7. D_{out} is the read data of next address.

*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.

*9. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

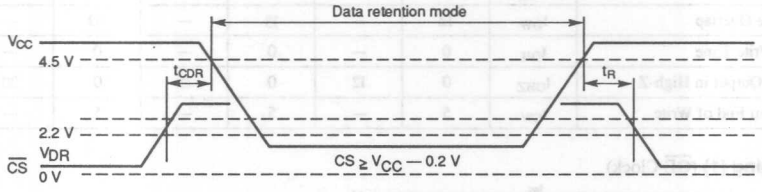
■ Low V_{CC} Data Retention Characteristics (T_A = 0 to +70°C)

This characteristics is guaranteed only for L-version

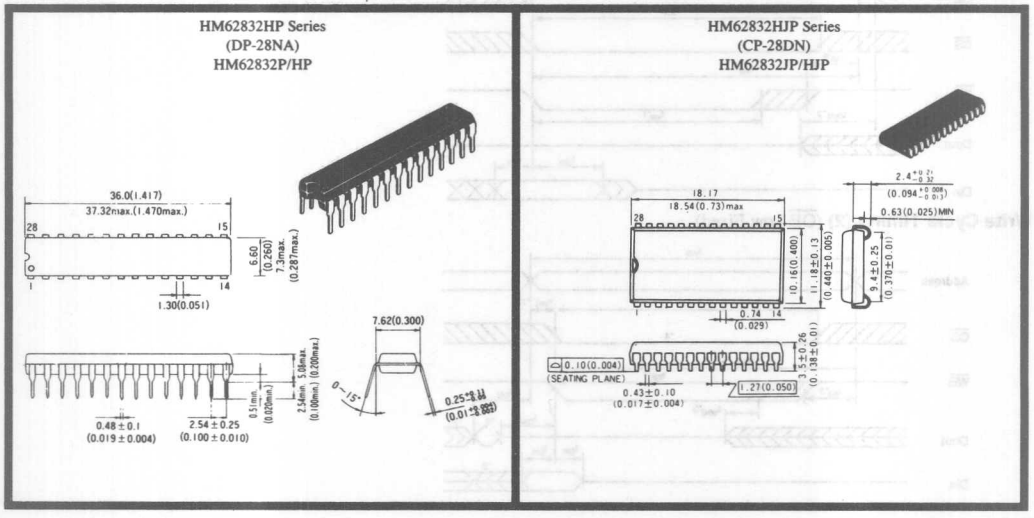
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or $0 V \leq V_{in} \leq 0.2$ V
Data Retention Current	I_{CCDR}	—	1	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_{RC}	t_{RC}*1	—	—	ns	

NOTES: *1. t_{RC} = read cycle time.
*2. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



■ PACKAGE DIMENSIONS Unit: mm (inch)

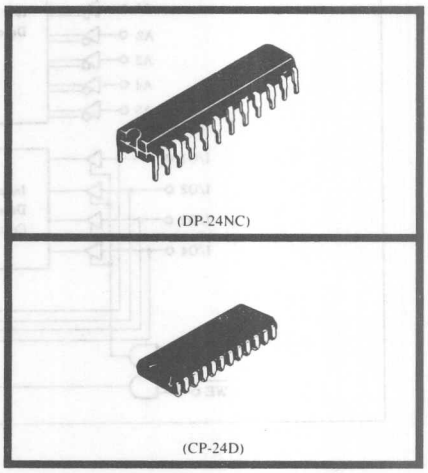


HM6208/HM6208H Series
4-Bit CMOS Static RAM

65536-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM6208 and HM6208H are high speed 256k static RAMS organized as 64k-word × 4 bit. They realize high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous wherever high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6208 and HM6208H are packaged in the industry standard 300-mil, 24 pin, plastic DIP. The HM6208H is also available in a 300-mil, 24 pin, plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



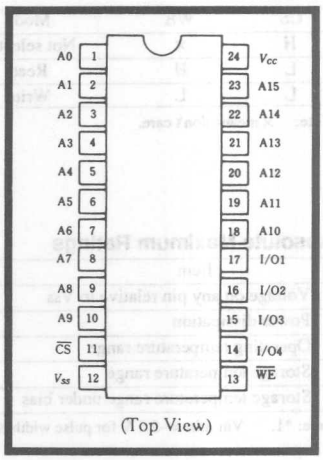
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max.)
- Low power
  - Active: 300 mW (typ.)
  - Standby: 100 μW (typ.)
  - 30 μW (typ.) (L-version)
- Completely static operation requires
  - No clock or timing strobe
- Access and cycle times are equivalent
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208P-35	35 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6208P-45	45 ns	
HM6208LP-35	35 ns	
HM6208LP-45	45 ns	
HM6208HP-25	25 ns	
HM6208HP-35	35 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HLJP-25	25 ns	
HM6208HLJP-35	35 ns	

Pin Arrangement

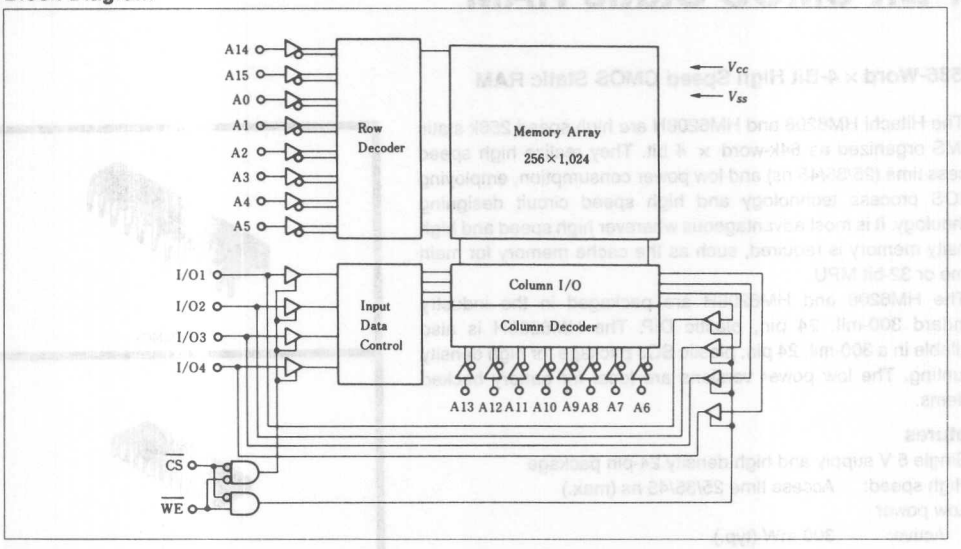


(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	Pr	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	—	2.0	μA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	—	—	10.0	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current "H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current	I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} – 0.2V
Standby Power Supply Current L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

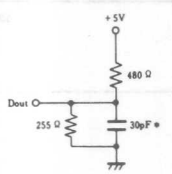
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

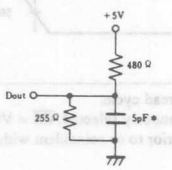
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWZ & tOW)



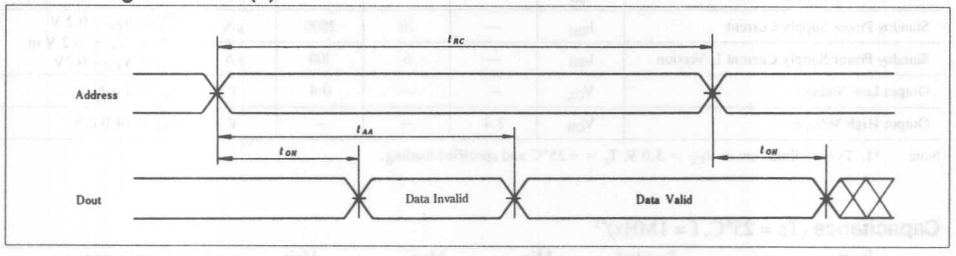
Note: * Including scope & jig.

Read Cycle

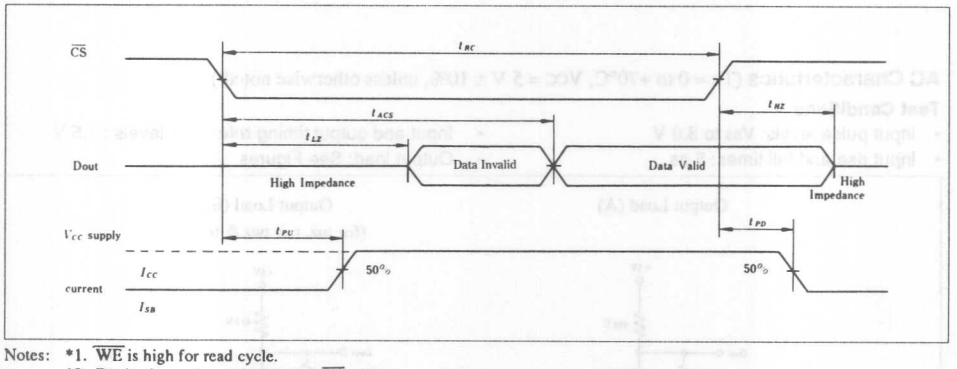
Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



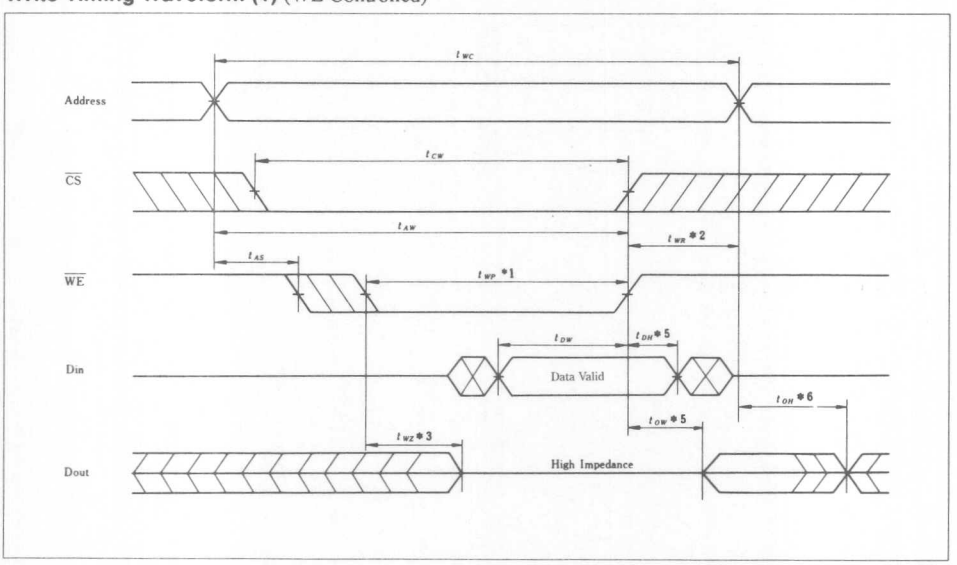
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

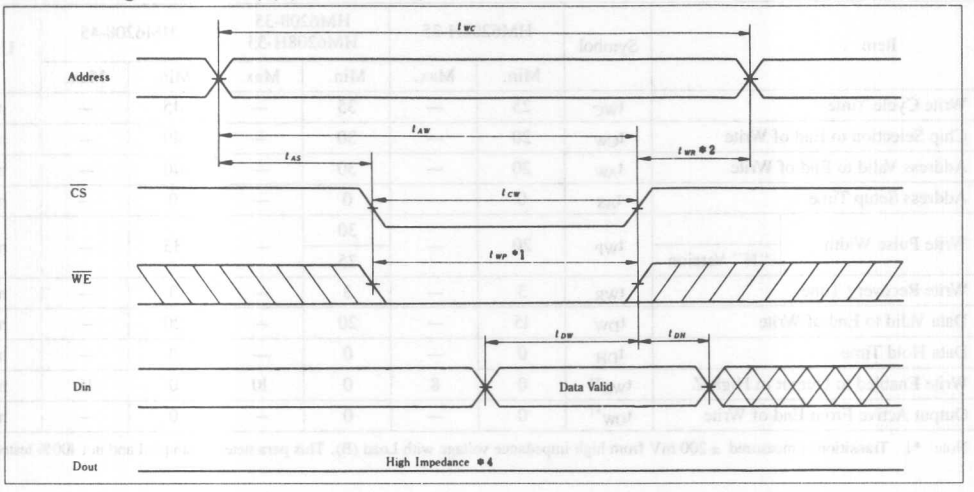
Item		Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	40	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	35	—	ns
	"H" Version				25				
Write Recovery Time		t_{WR}	3	—	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	0	15	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



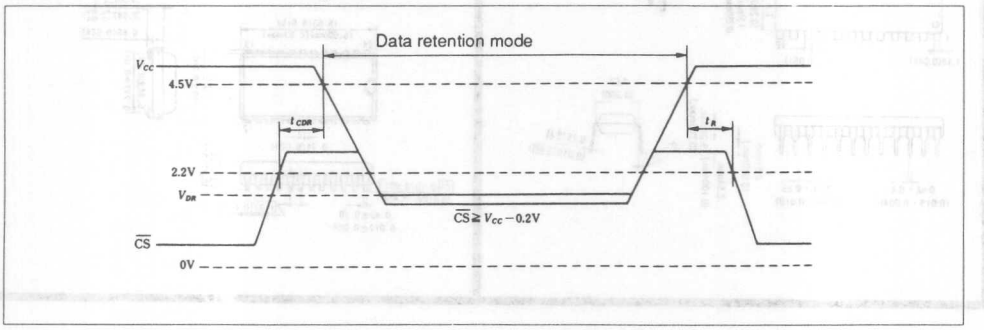
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50 *2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC} *1	—	—	ns	

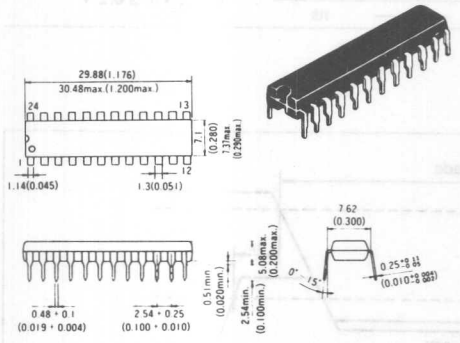
Notes: *1. t_{RC} = read cycle time.
*2. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform

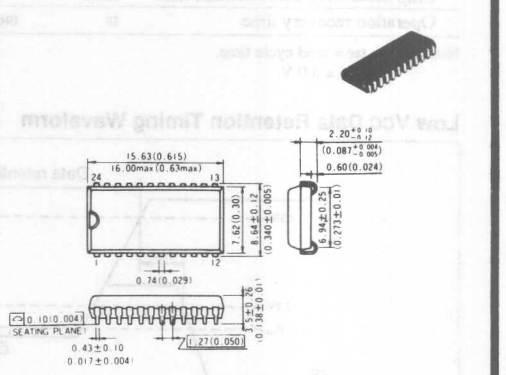


■ PACKAGE DIMENSIONS Unit: mm (inch)

HM6208/HM6208HP Series
(DP-24NC)



HM6208HJP Series
(CP-24D)



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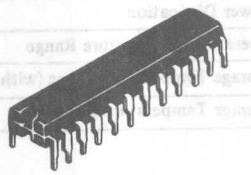
HM6708 Series

65536-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6708P



(DP-24NC)

HM6708JP

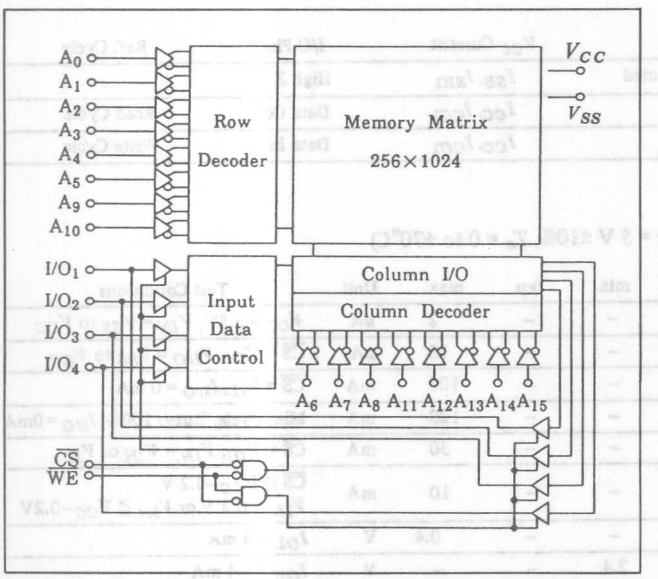


(CP-24D)

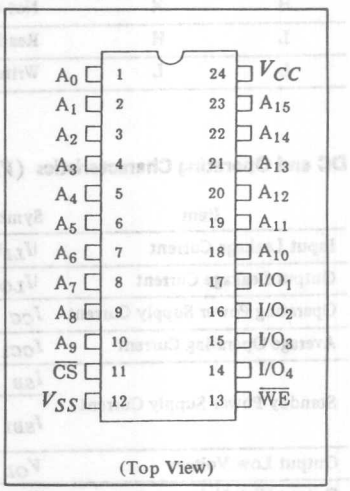
Ordering Information

Type No.	Access Time	Package
HM6708P-20	20ns	300mil 24 pin
HM6708P-25	25ns	Plastic DIP
HM6708JP-20	20ns	300 mil
HM6708JP-25	25ns	24 pin SOJ

Block Diagram



Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	µA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC}$−0.2 V $V_{IN} \leqq$ 0.2 V or $V_{IN} \geqq V_{CC}$−0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

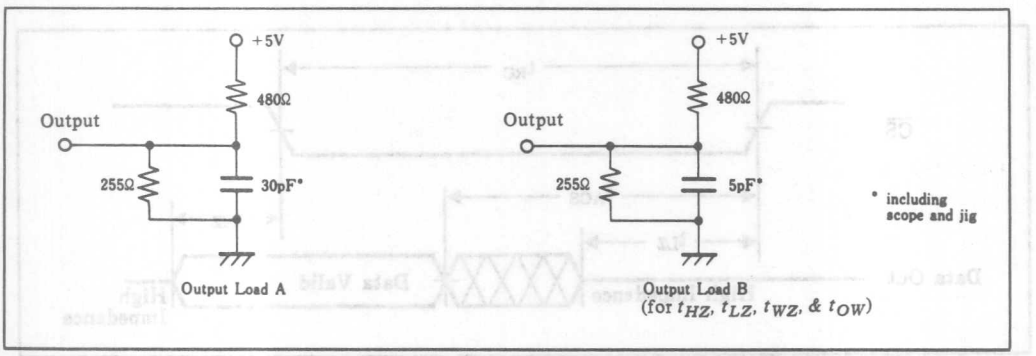
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0 V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

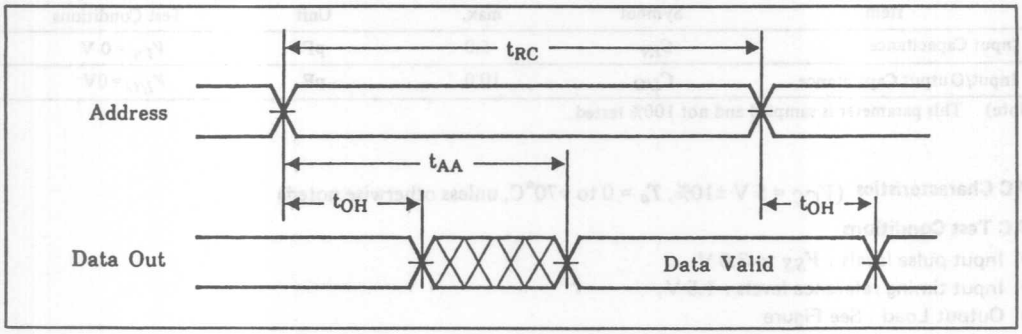


Read Cycle

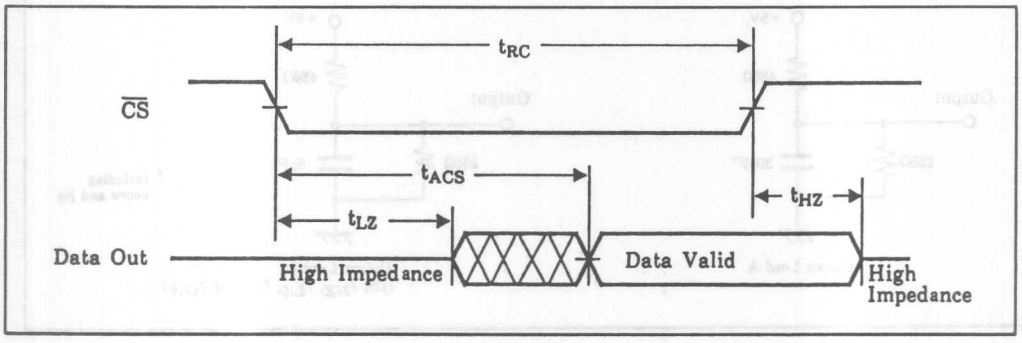
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	0	–	0	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Read Cycle-1*1,*2



Read Cycle-2*1,*3



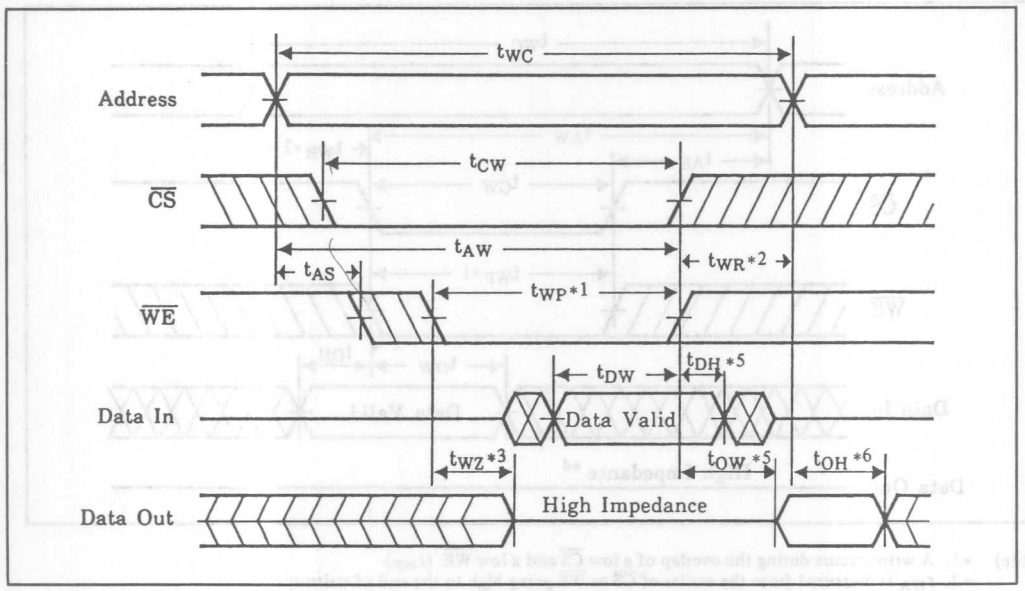
Notes) *1. $\overline{WE}$ is High for Read cycle.
*2. Device is continuously selected, $\overline{CS} = V_{IL}$.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

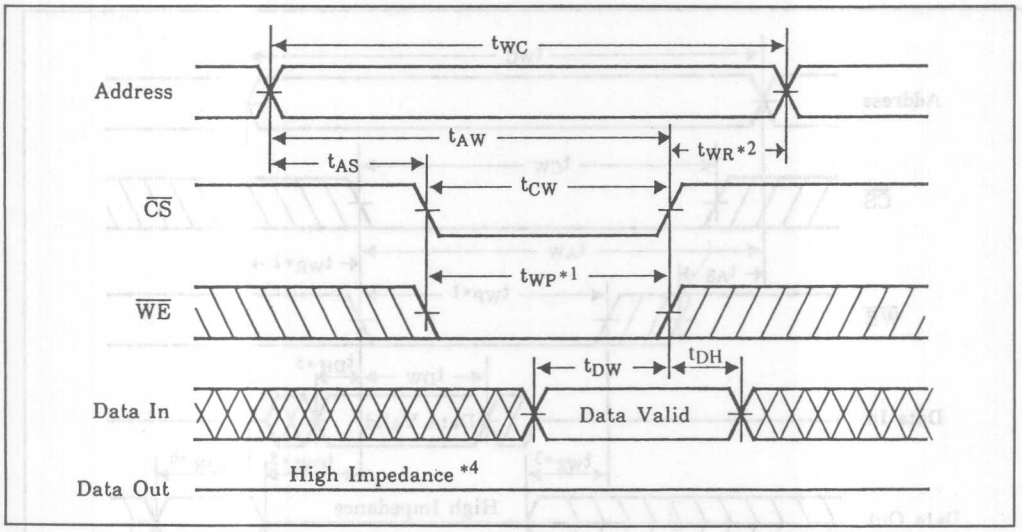
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	3	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	8	0	10	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Write Cycle-2 ($\overline{CS}$ Controlled)



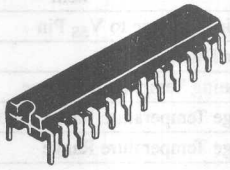
Note) *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Output is the same phase of write data of this write cycle.

6708A Series — Product Preview

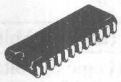
1K-Word × 4-Bit High Speed Static RAM

FEATURES

- Super Fast
  - Access Time . . . . . 15/20/25ns (max.)
- Low Power Dissipation . . . . . 400mW (typ.)
- +5V Single Supply
- Completely Static Memory
  - No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



(DP-24NC)

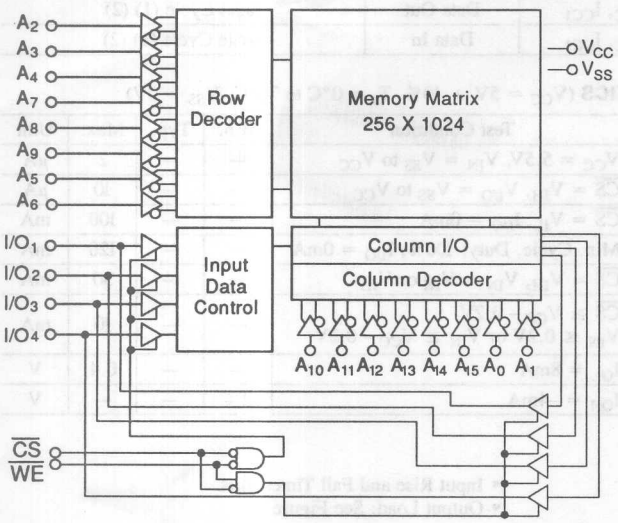


(CP-24D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6708AP-15	15ns	300 mil 24 pin
HM6708AP-20	20ns	Plastic DIP
HM6708AP-25	25ns	(DP-24NC)
HM6708AJP-15	15ns	300 mil 24 pin
HM6708AJP-20	20ns	Plastic SOJ
HM6708AJP-25	25ns	(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low (Logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width ≤ 15ns, DC: −0.5V

■ TRUTH TABLE

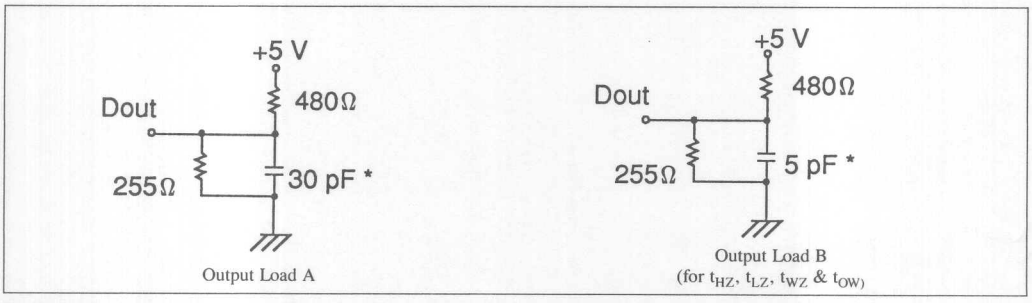
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Reference Levels: 1.5V
- Input Rise and Fall Times: 4ns
- Output Load: See Figure



*Including scope and jig capacitance.

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■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6.0	pF
Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10.0	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6708A-15		HM6708A-20		HM6708A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns	—
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	0	10	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

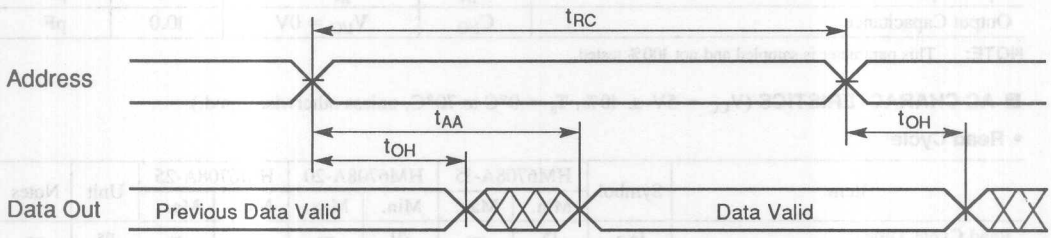
• Write Cycle

Item	Symbol	HM6708A-15		HM6708A-20		HM6708A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	9	—	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	2, 3

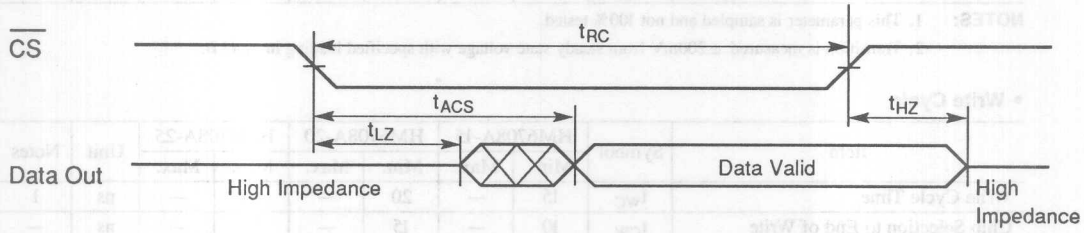
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
3. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1) (2)

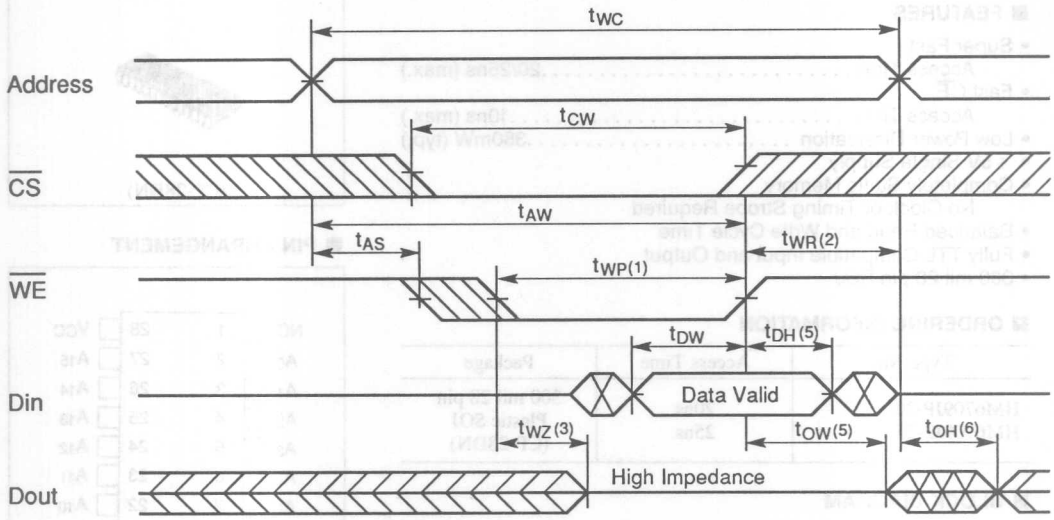


• **Read Cycle (2)** (1) (3)

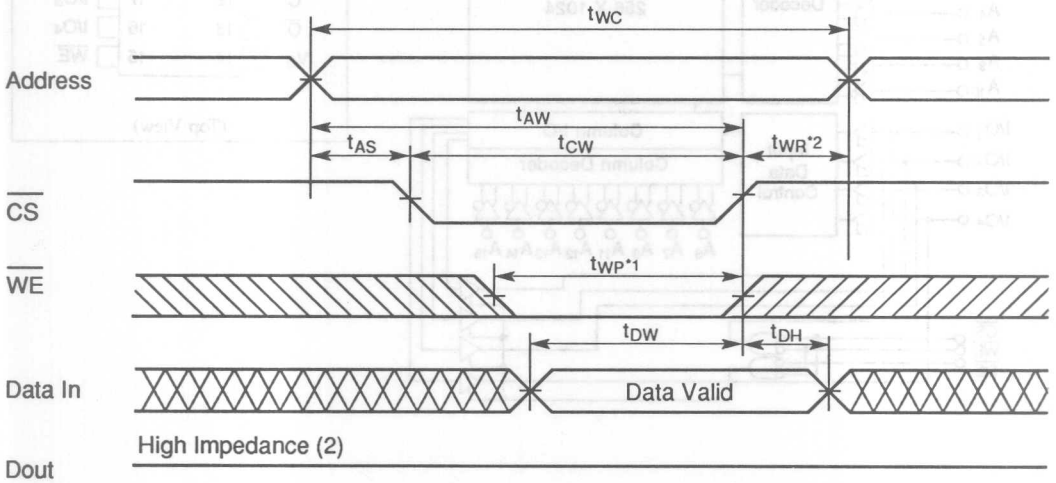


NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:

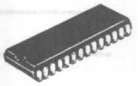
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Output data is the same phase of write data of this write cycle.

HM6709 Series — Preliminary

65536-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

- Super Fast
  - Access Time . . . . . .20/25ns (max.)
- Fast $\overline{OE}$
  - Access Time . . . . . .10ns (max.)
- Low Power Dissipation . . . . . .350mW (typ.)
- +5V Single Supply
- Completely Static Memory
  - No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- 300 mil 28 pin SOJ

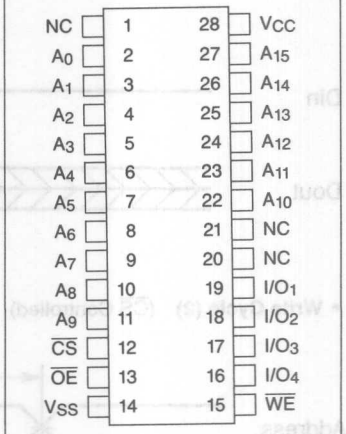


(CP-28DN)

■ ORDERING INFORMATION

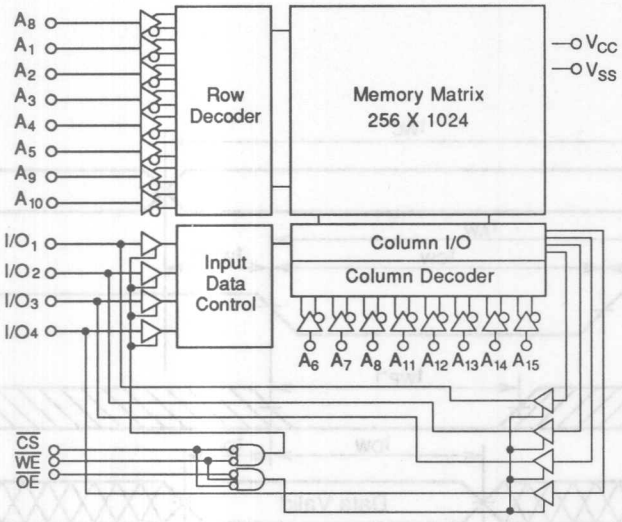
Type No.	Access Time	Package
HM6709JP-20 HM6709JP-25	20ns 25ns	300 mil 28 pin Plastic SOJ (CP-28DN)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	−3.0	—	0.8	V

*Pulse width: 20ns, DC: −0.5V

■ TRUTH TABLE

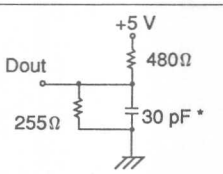
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$)

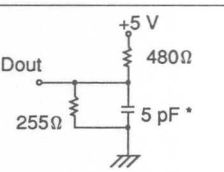
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O} = 0mA$	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O} = 0mA$	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS} \ge V_{CC} - 0.2V$ $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6709JP-20		HM6709JP-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	20	—	25	ns	—
Chip Selection to Output in Low Z	t_{LZ}	0	—	0	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	10	0	10	ns	—
Output Enable to Output in Low Z	t_{OLZ}	0	—	0	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	—

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading is Load B.

• Write Cycle

Item	Symbol	HM6709JP-20		HM6709JP-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	15	—	20	—	ns	—
Write Pulse Width	t_{WP}	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Write to Output in High Z	t_{WZ}	0	8	0	10	ns	2, 3
Data Valid to End of Write	t_{DW}	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	ns	2, 3

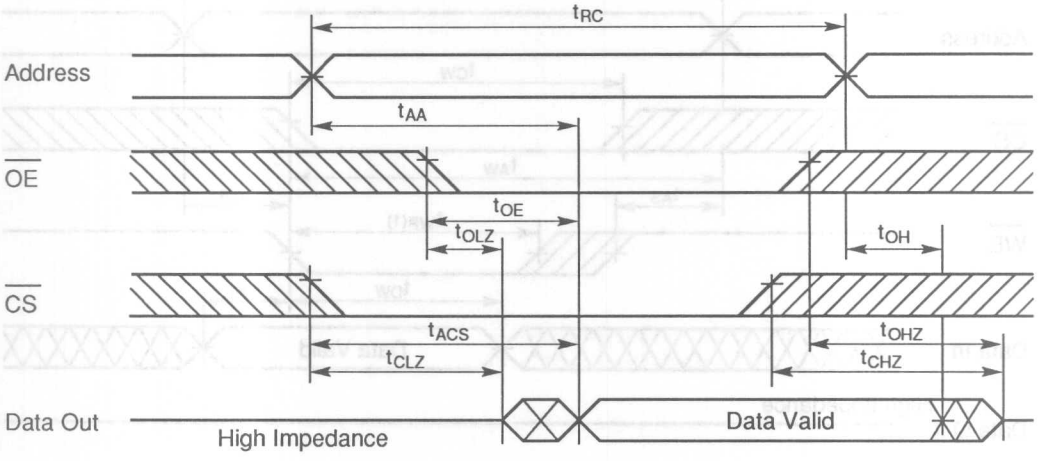
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

2. This parameter is sampled and not 100% tested.

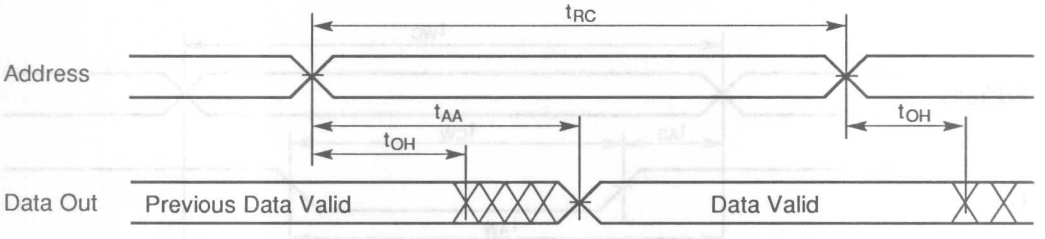
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

■ TIMING WAVEFORM

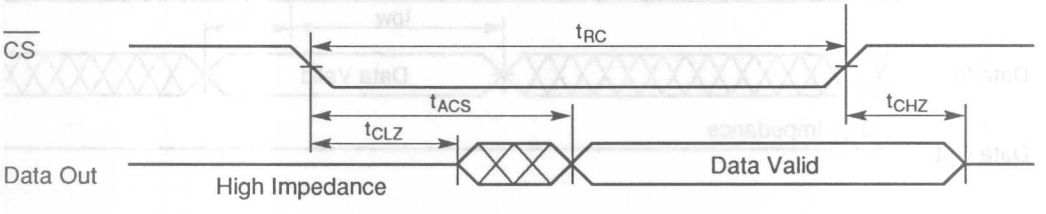
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)

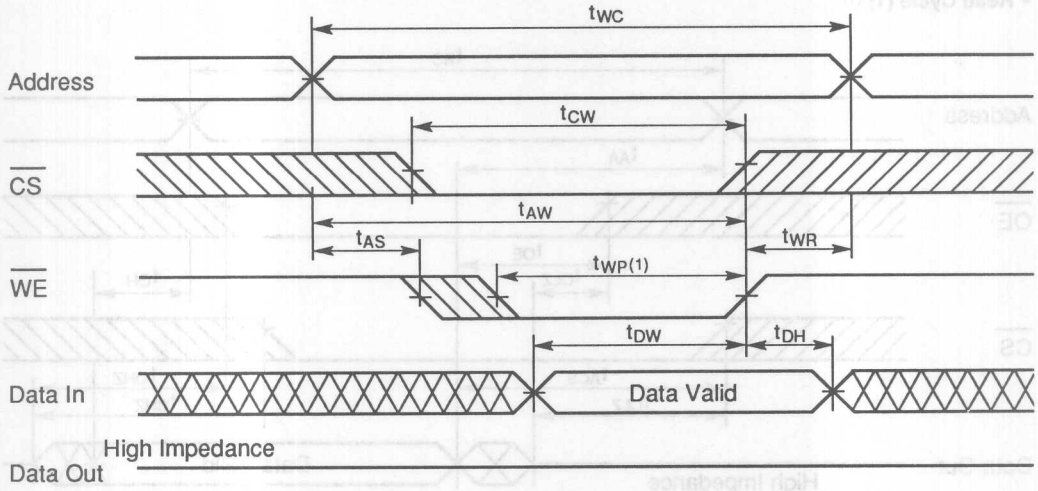


• **Read Cycle (3)** (1) (3) (4)

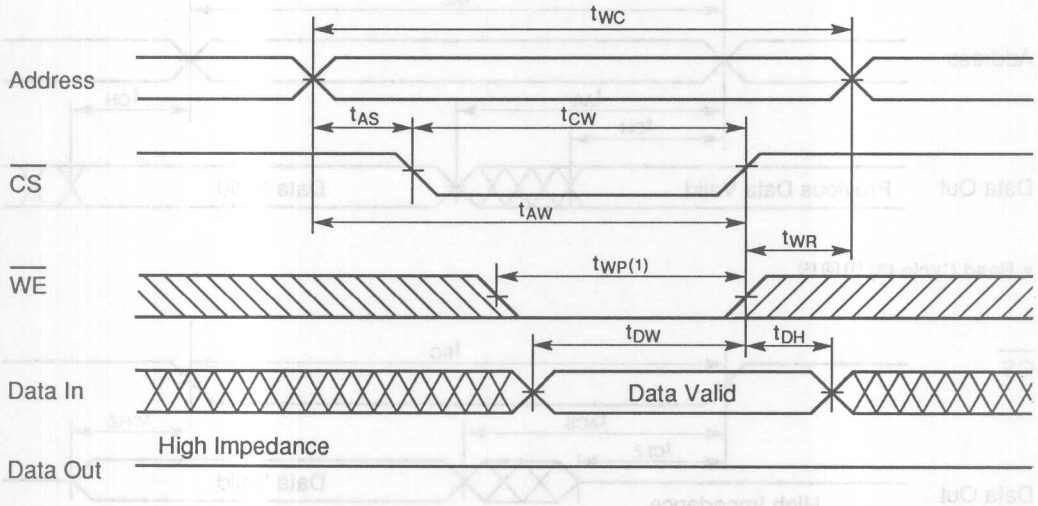


NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

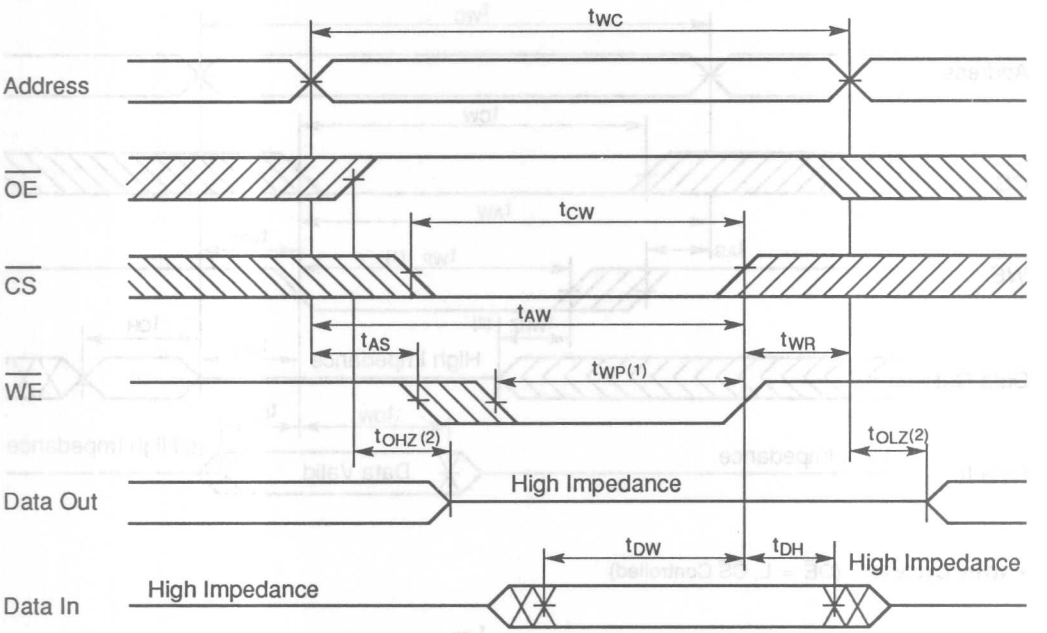
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



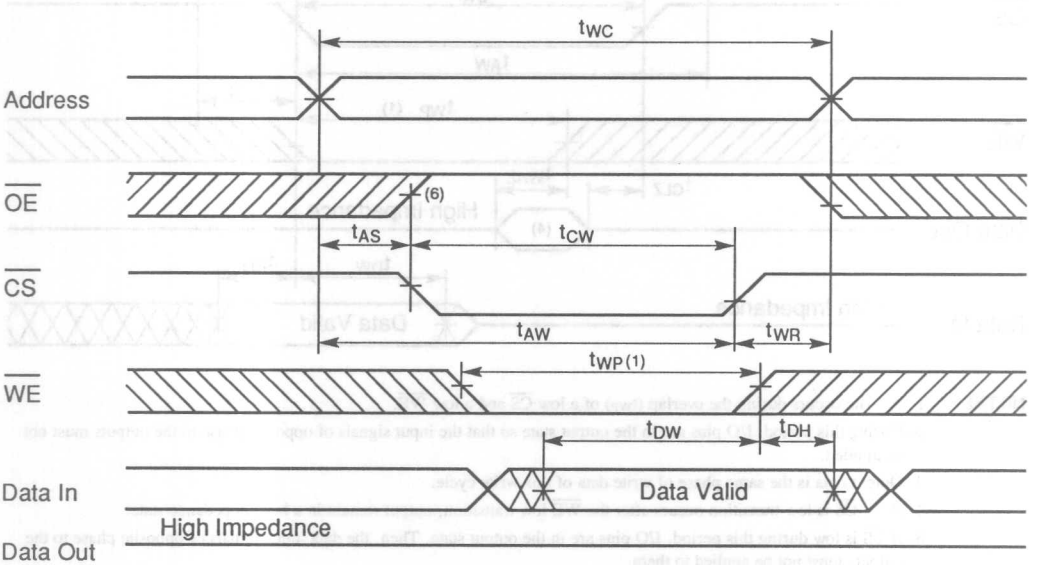
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



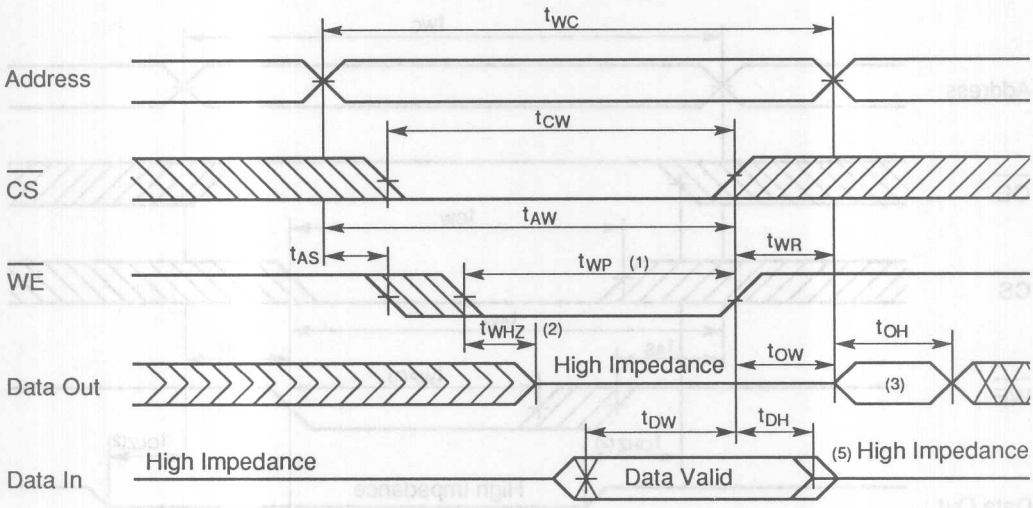
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



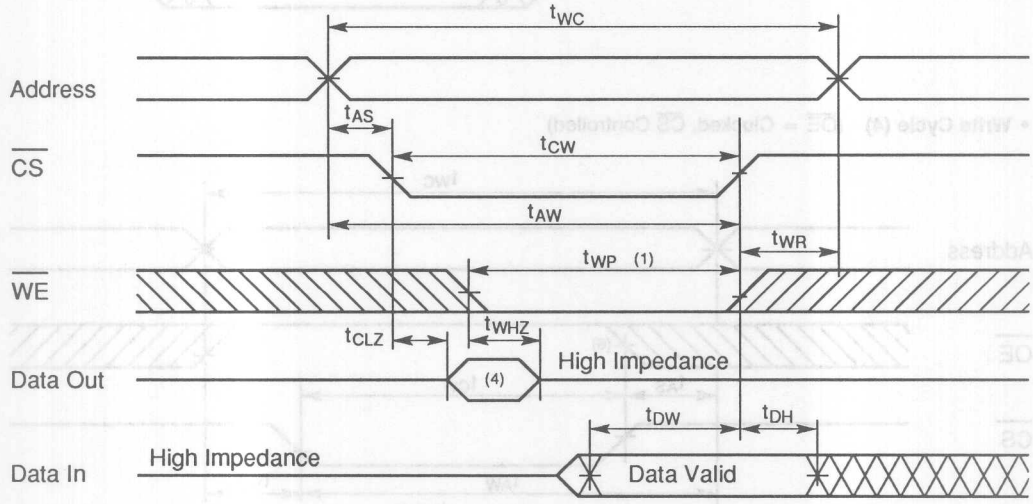
• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

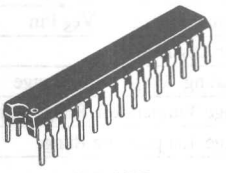
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6709A Series — Product Preview

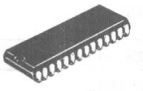
65536-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

- Super Fast
  Access Time . . . . . .15/20/25ns (max.)
- Fast $\overline{OE}$
  Access Time. . . . . .8/10/10ns (max.)
- Low Power Dissipation . . . . . .400mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



(DP-28N)

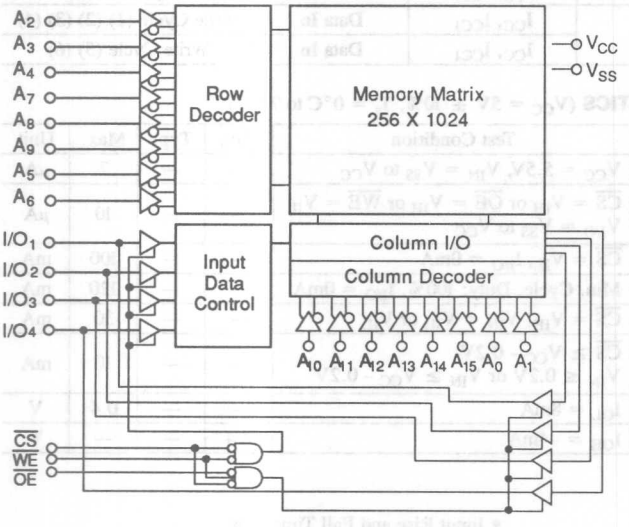


(CP-28DN)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6709AP-15	15ns	300 mil 28 pin
HM6709AP-20	20ns	Plastic DIP
HM6709AP-25	25ns	(DP-28N)
HM6709AJP-15	15ns	300 mil 28 pin
HM6709AJP-20	20ns	Plastic SOJ
HM6709AJP-25	25ns	(CP-28DN)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	−3.0	—	0.8	V

*Pulse width: 15ns, DC: −0.5V

■ TRUTH TABLE

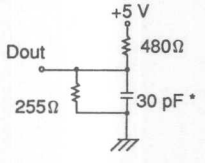
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$)

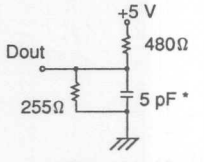
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O} = 0mA$	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O} = 0mA$	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS} \ge V_{CC} - 0.2V$ $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	3	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	8	0	10	0	10	ns	—
Output Enable to Output in Low Z	t_{OLZ}	3	—	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	0	10	ns	1, 2
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns	—

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

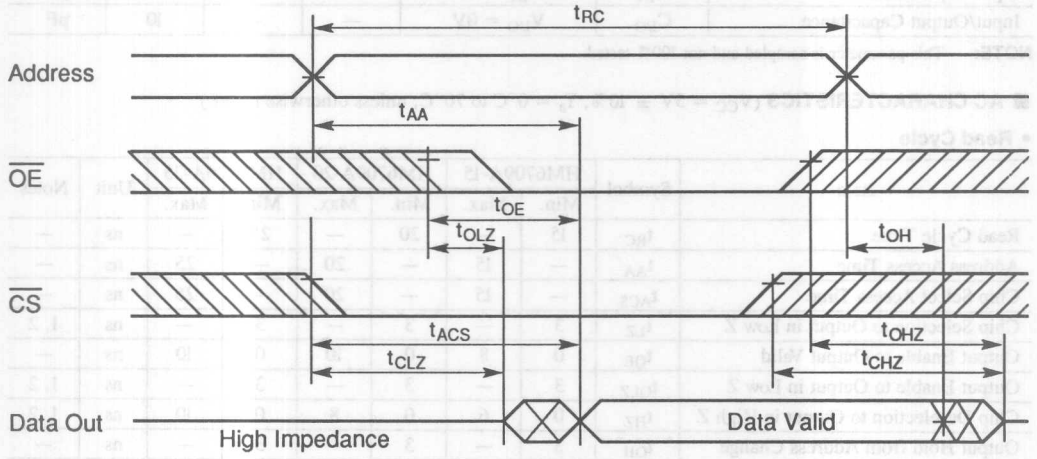
• Write Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Write to Output in High Z	t_{WZ}	0	6	0	8	0	10	ns	2, 3
Data Valid to End of Write	t_{DW}	9	—	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	0	6	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	2, 3

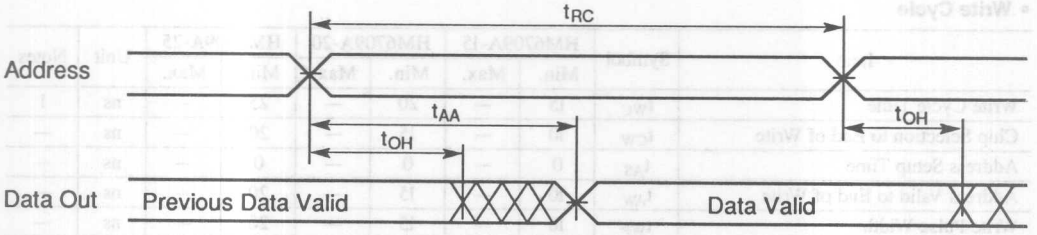
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

■ TIMING WAVEFORM

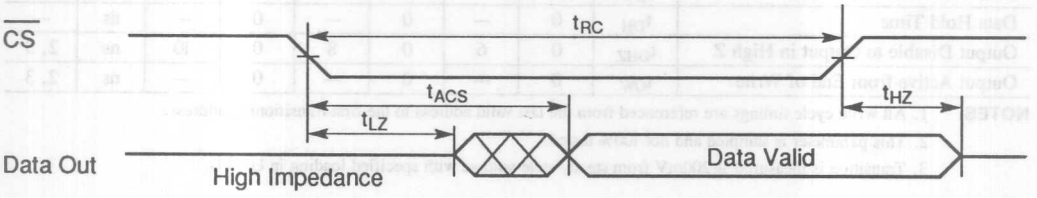
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)

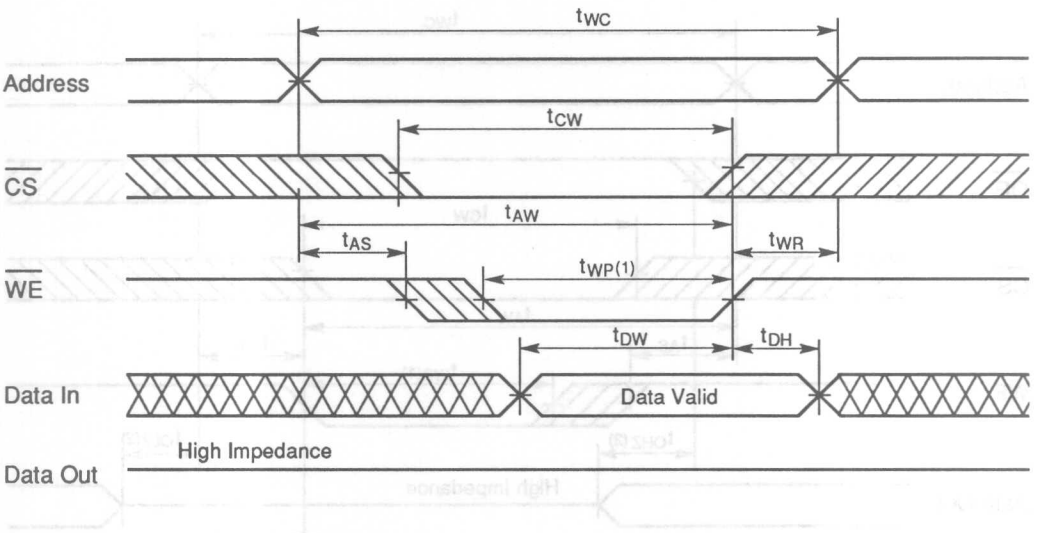


• **Read Cycle (3)** (1) (3) (4)

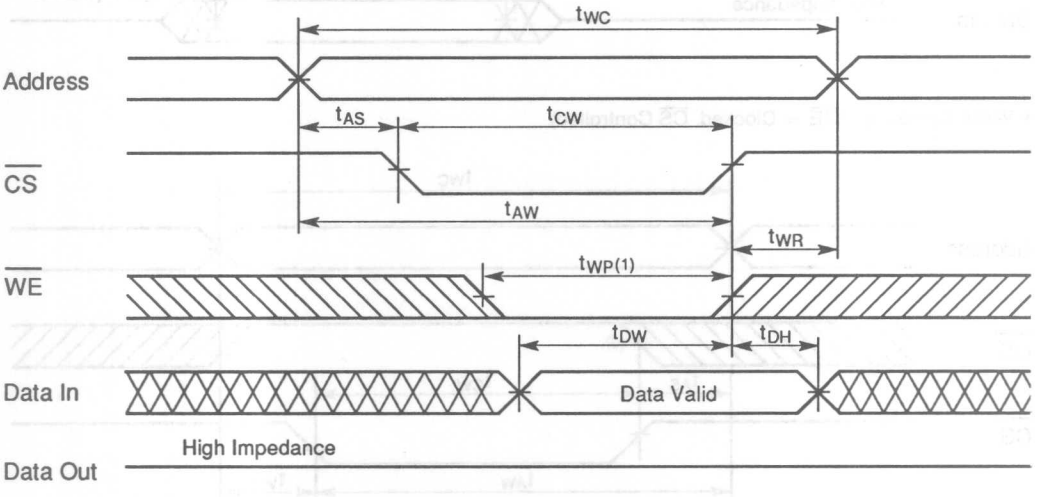


NOTES: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$.
3. $\overline{OE} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

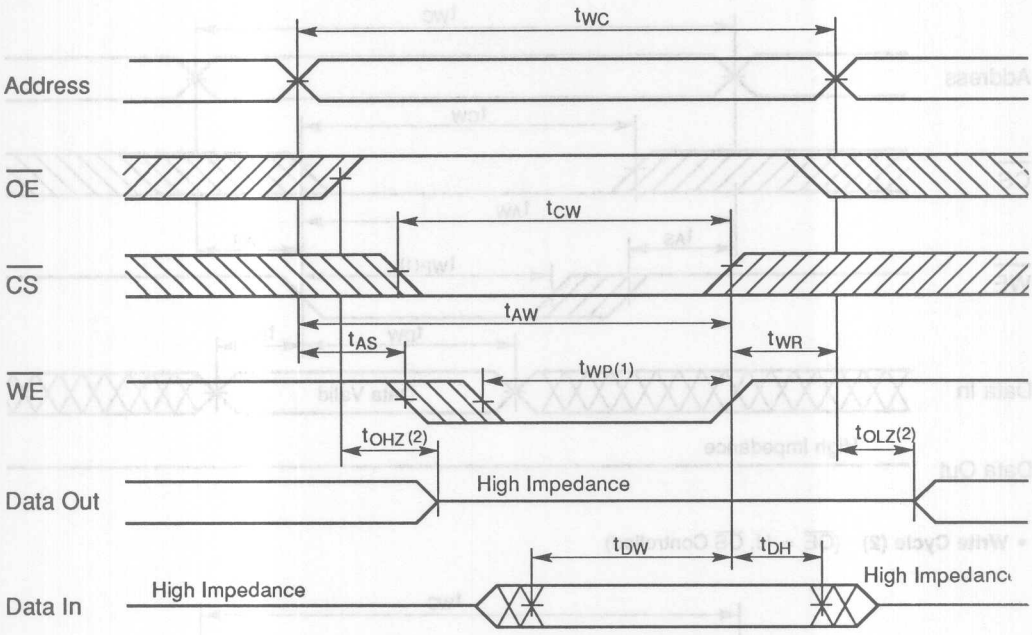
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



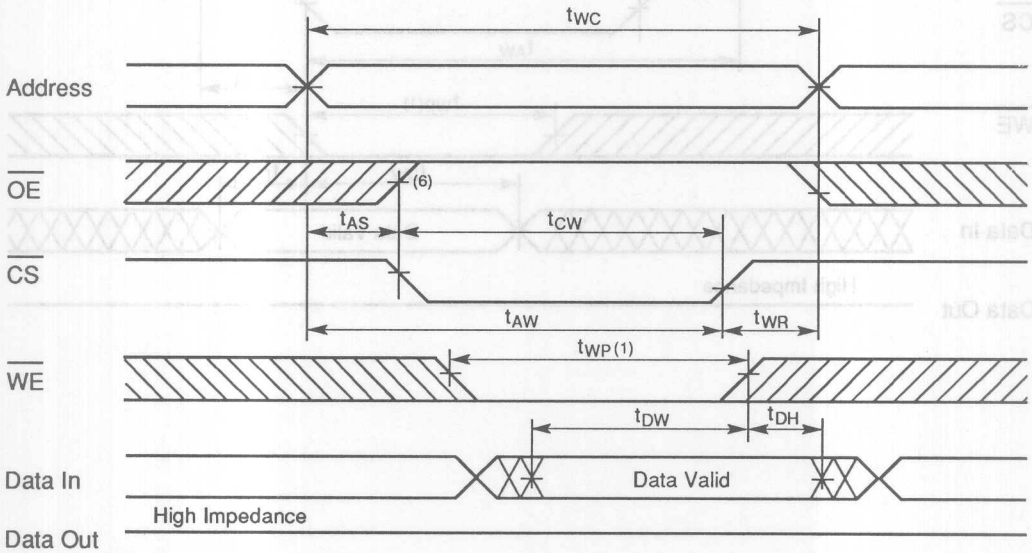
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)

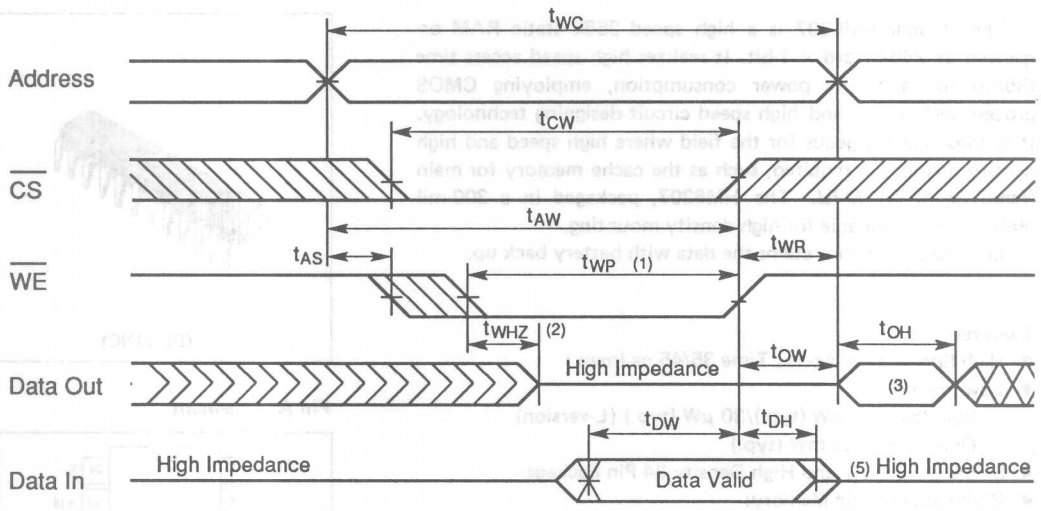


• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)

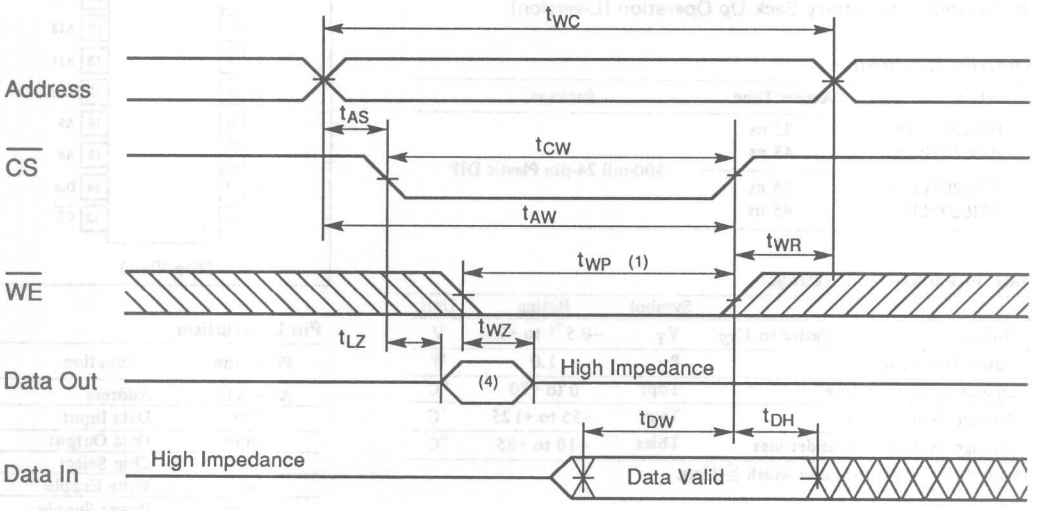


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• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

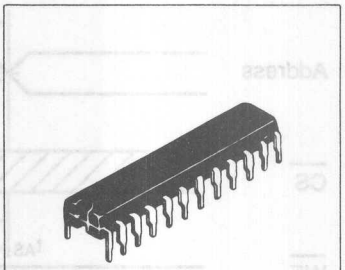
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6207 Series

262144-word x 1-bit High Speed CMOS Static RAM

The Hitachi HM6207 is a high speed 256k static RAM organized as 256-kword x 1-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6207, packaged in a 300 mil plastic DIP, is available for high density mounting.

Low power version retains the data with battery back up.

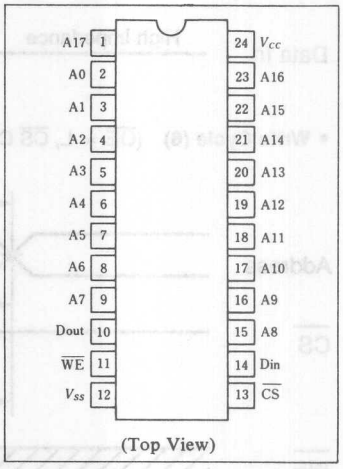


(DP-24NC)

Features

- High Speed: Fast Access Time 35/45 ns (max.)
- Low Power
  - Standby: 100 μW (typ.)/30 μW (typ.) (L-version)
  - Operation: 300 mW (typ.)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static Memory:
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

Pin Arrangement



(Top View)

Ordering Information

Type No.	Access Time	Package
HM6207P-35	35 ns	300-mil 24-pin Plastic DIP
HM6207P-45	45 ns	
HM6207LP-35	35 ns	
HM6207LP-45	45 ns	

Absolute Maximum Ratings

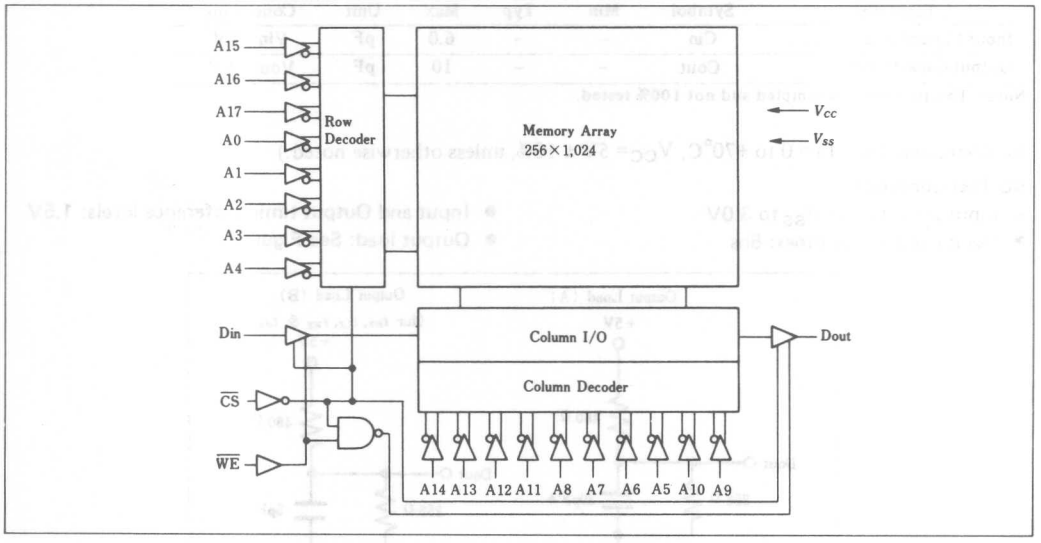
Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

Note) *1. −2.5V for pulse width ≦ 10ns.

Pin Description

Pin Name	Function
A0 - A17	Address
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	NOT SELECTED	I_{SB}, I_{SB1}	HIGH-Z	---
L	H	READ	I_{CC}	Dout	READ CYCLE
L	L	WRITE	I_{CC}	HIGH-Z	WRITE CYCLE

Note) × means don't care.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5 *1	–	0.8	V

Note) *1. −2.0V for pulse width ≦ 10 ns

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	min	typ *1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	2.0	μA	V_{CC} = MAX. V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10.0	μA	$\overline{CS}$ = V_{IH} Vout = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	60	100	mA	$\overline{CS}$ = V_{IL} Iout = 0mA, min. cycle
Standby Power Supply Current	I_{SB}	–	15	30	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	–	0.02	2.0	mA	$\overline{CS}$ ≧ V_{CC}−0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V
		–	0.006 *2	0.1 *2		
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4.0mA

Note) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0MHz)

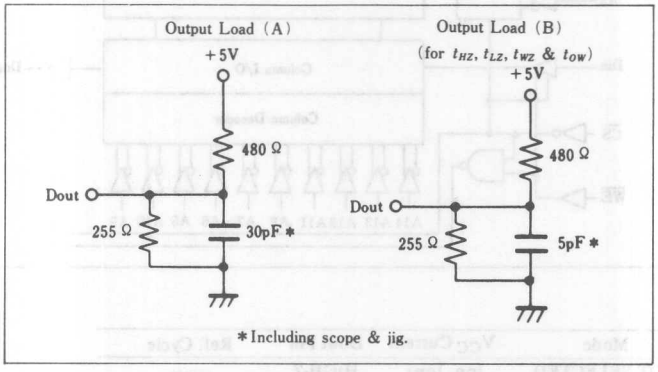
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance	Cin	–	–	6.0	pF	Vin = 0V
Output Capacitance	Cout	–	–	10	pF	Vout = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

AC Test Conditions

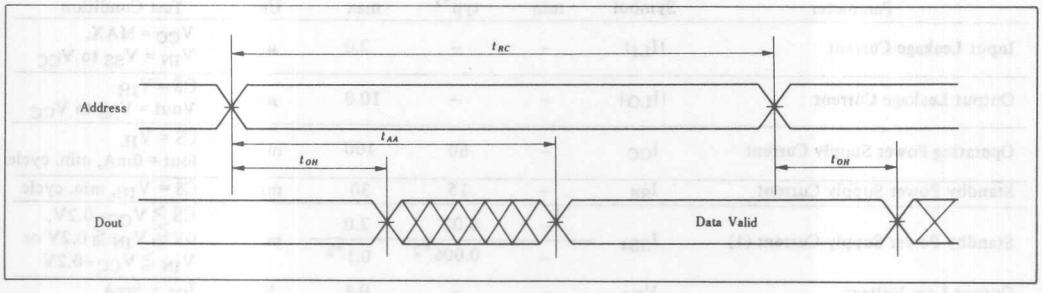
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figures.



Read Cycle

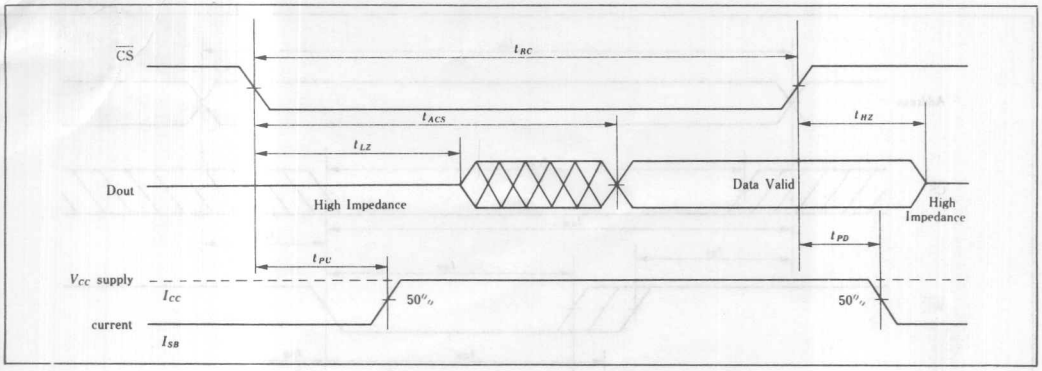
Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	–	45	–	ns	*1
Address Access Time	t_{AA}	–	35	–	45	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	*2, *3, *7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	*2, *3, *7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	*7
Chip Deselection to Power Down Time	t_{PD}	–	30	–	40	ns	*7

Timing Waveform of Read Cycle No. 1 *4, *5



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Timing Waveform of Read Cycle No. 2*4, *6

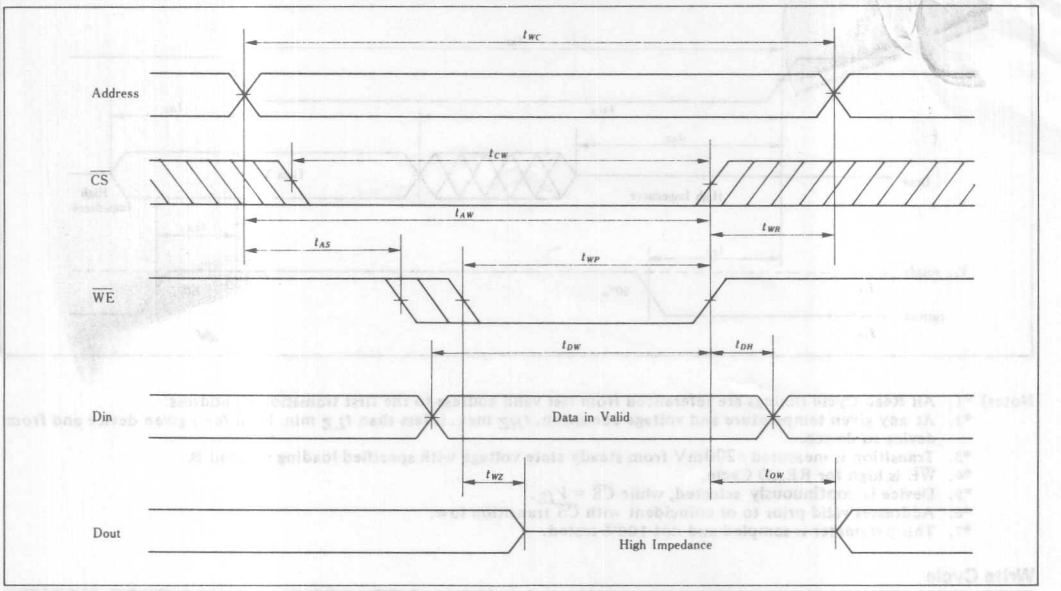


Notes) *1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
*2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. $\overline{WE}$ is high for READ Cycle.
*5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
*6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*7. This parameter is sampled and not 100% tested.

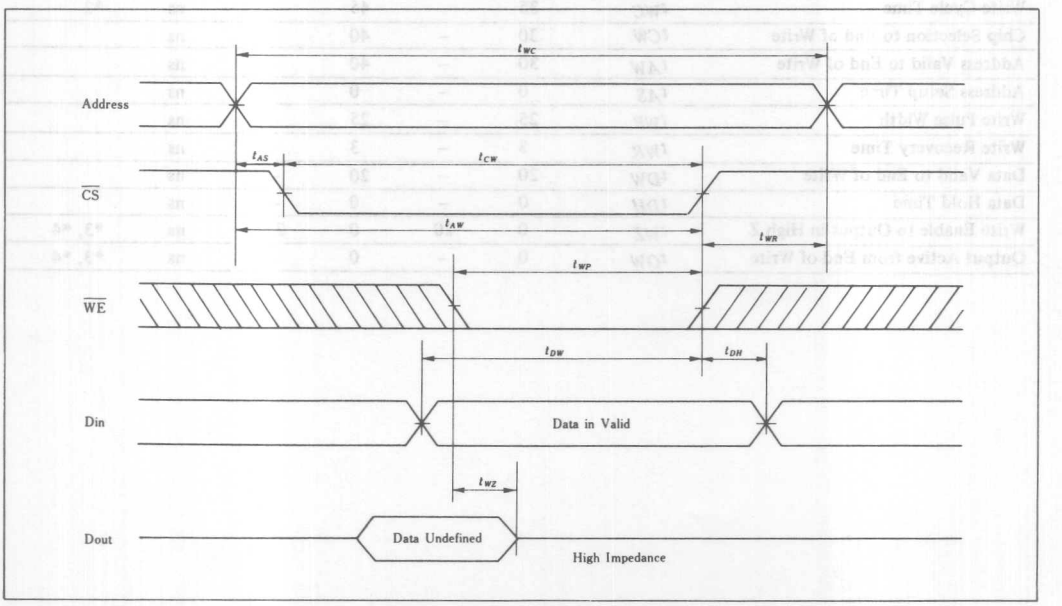
Write Cycle

Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	ns	*2
Chip Selection to End of Write	t_{CW}	30	–	40	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	25	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	20	–	20	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	ns	*3, *4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*3, *4

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



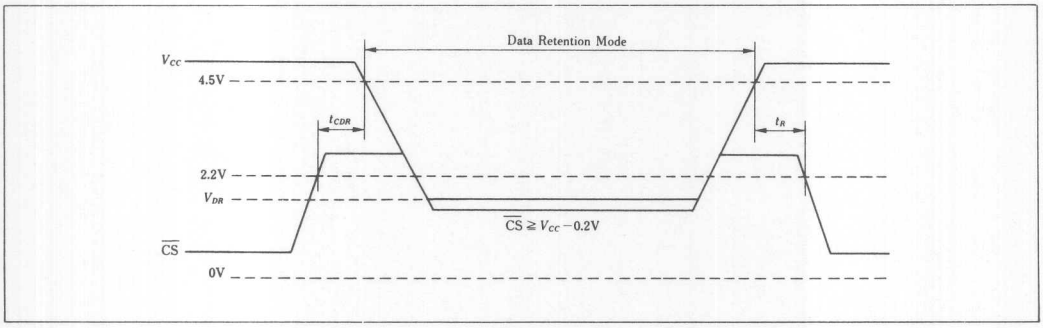
Notes) *1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
*2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. This parameter is sampled and not 100% tested.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)
(This characteristics is guaranteed only for L-version)

Parameter	Symbol	min	typ.	max.	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data Retention Current	I_{CCDR}	–	2	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See retention waveform
Operation Recovery Time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time *2. V_{CC} = 3.0V

Low V_{CC} Data Retention Waveform

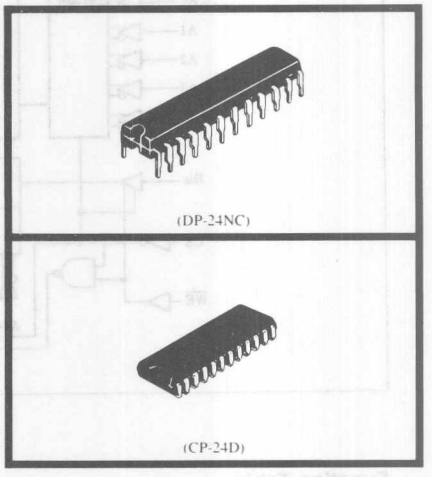


HM6207/HM6207H Series
1-Bit CMOS Static RAM

262144-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6207 and HM6207H are high speed 256k static RAMs organized as 256-kword × 1-bit. They realize high speed access time (25/35/45ns) and low power consumption, employing CMOS process technology and high speed circuit design technology. It is most advantageous wherever high speed and high density memory is required.

The HM6207 and HM6207H are packaged in the industry standard 300-mil, 24-pin plastic DIP. The HM6207H is also available in a 300-mil, 25-pin plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



Features

- Single 5 V supply and high density 24-pin package
- High speed
  Access time: 25/35/45 ns (max.)
- Low power
  Active: 300 mW (typ.)
  Standby: 100 μW (typ.)
  30 μW (typ.) (L-version)
- Completely static memory requires
  No clock or timing strobe requires
- Equal access and cycle time
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

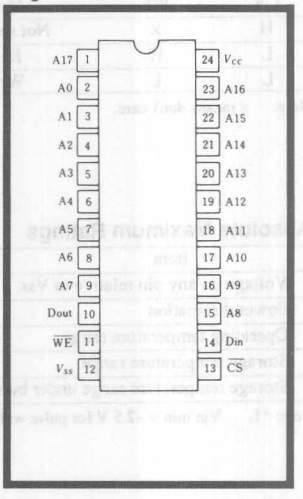
Ordering Information

Type No.	Access Time	Package
HM6207P-35	35 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6207P-45	45 ns	
HM6207HP-25	25 ns	
HM6207HP-35	35 ns	
HM6207HLP-25	25 ns	
HM6207HLP-35	35 ns	
HM6207HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6207HJP-35	35 ns	
HM6207HLJP-25	25 ns	
HM6207HLJP-35	35 ns	

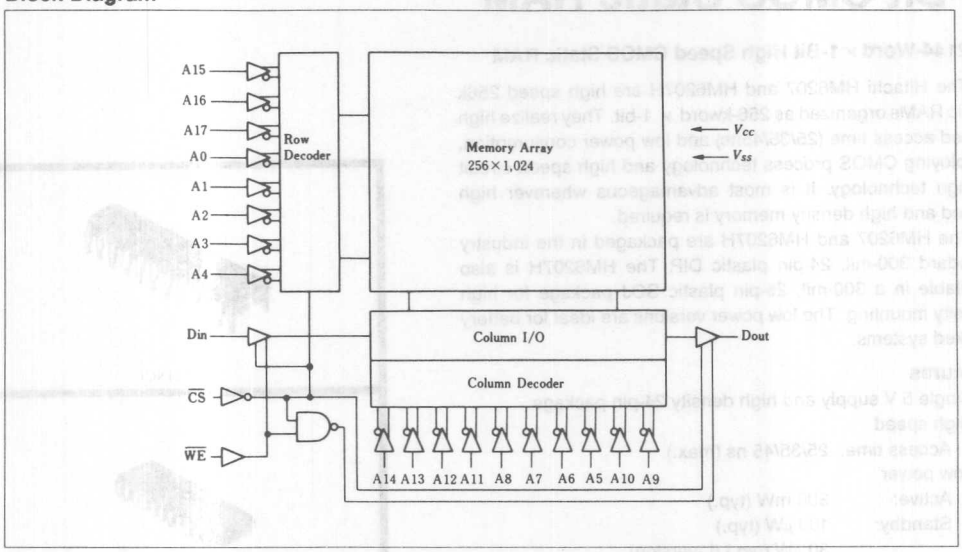
Pin Description

Pin Name	Function
A0 – A17	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Pin Arrangement



Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	High-Z	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current		$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current		$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current		I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current		I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current	"H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current (1)		I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} – 0.2V
Standby Power Supply Current (1)	L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage		V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage		V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	V_{out} = 0 V

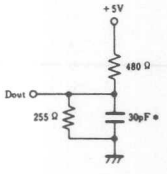
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

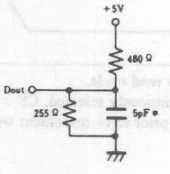
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, twz & tow)



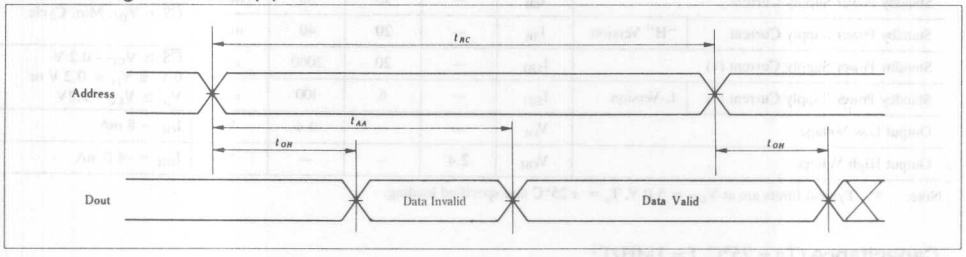
Note: * Including scope & jig.

Read Cycle

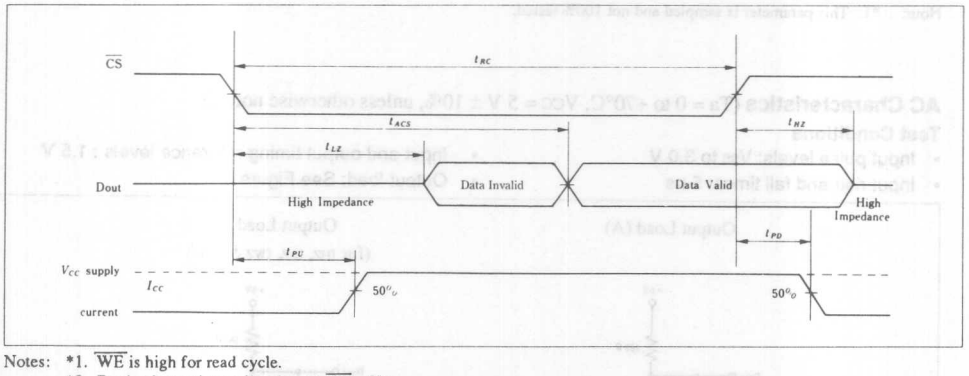
Item	Symbol	HM6207H-25		HM6207-35 HM6207H-35		HM6207-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	0	30	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	—	40	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

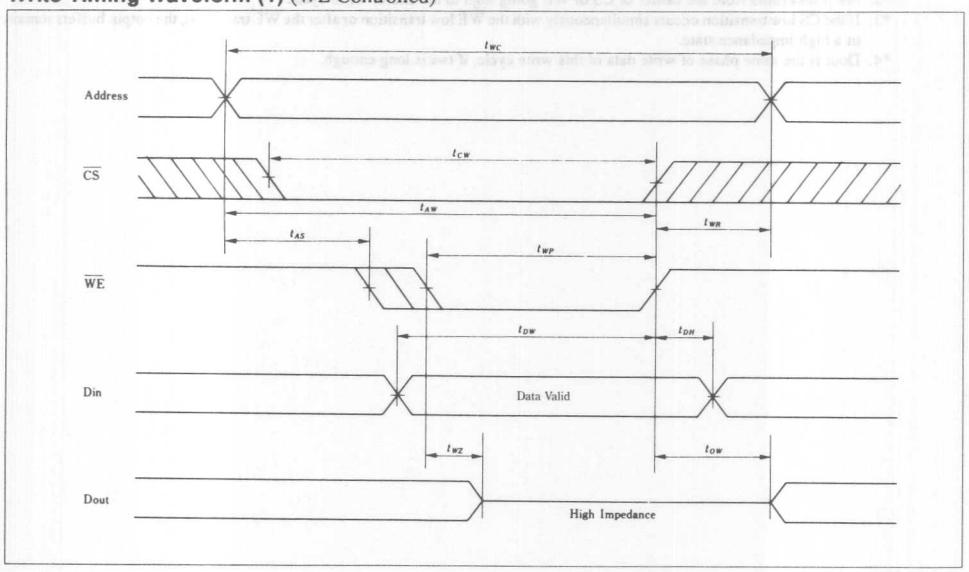
HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ Write Cycle

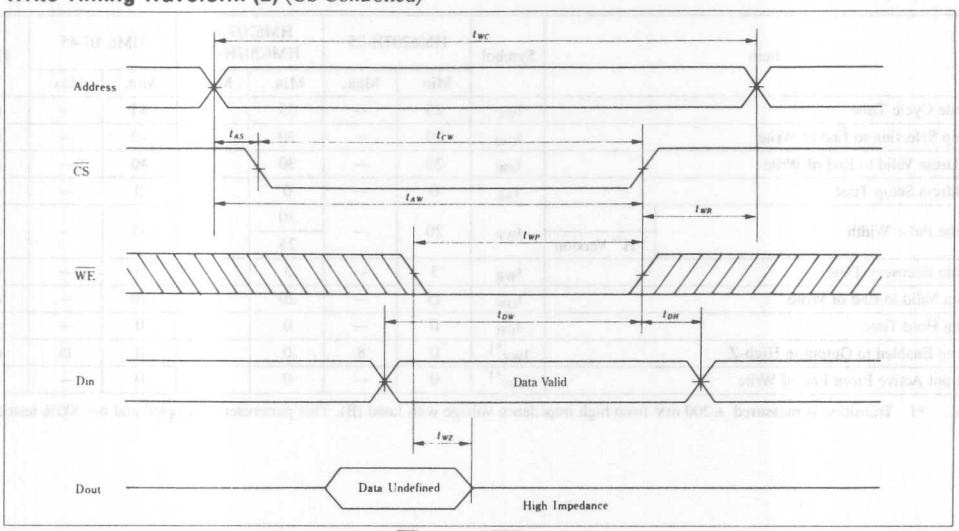
Item		Symbol	HM6207H-25		HM6207-35 HM6207H-35		HM6207-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	40	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	35	—	ns
	"H" Version				25				
Write Recovery Time		t_{WR}	3	—	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	0	15	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

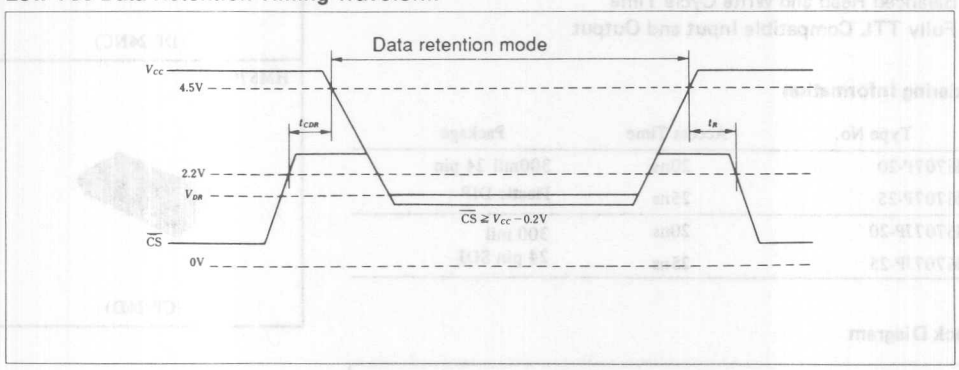
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

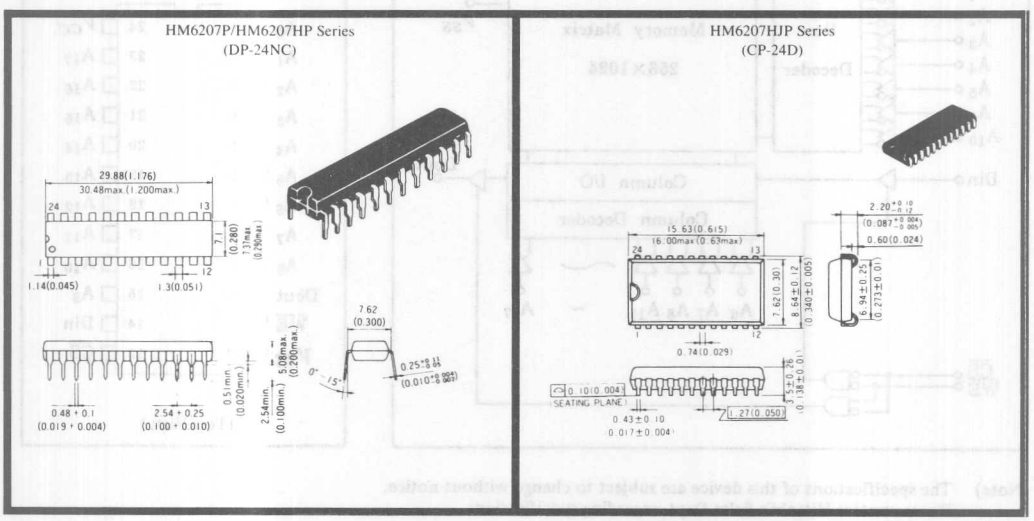
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC} *1	—	—	ns	

Notes: *1. t_{RC} = read cycle time.
*2. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform



■ PACKAGE DIMENSIONS Unit: mm (inch)



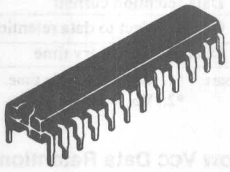
HM6707 Series

262144-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6707P



(DP-24NC)

HM6707JP

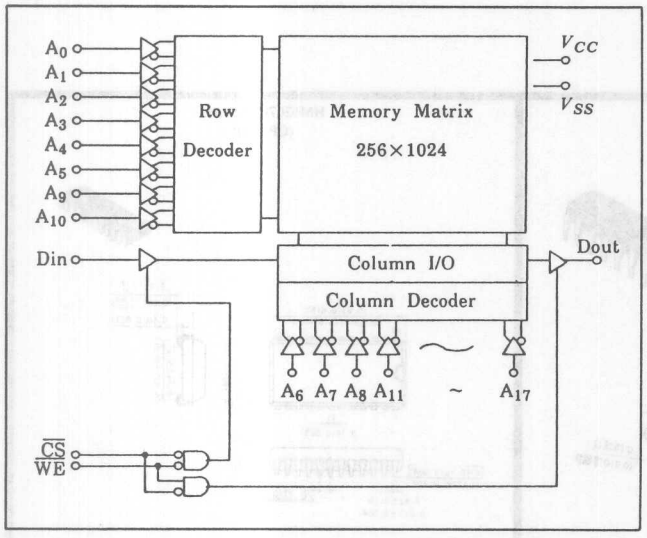


(CP-24D)

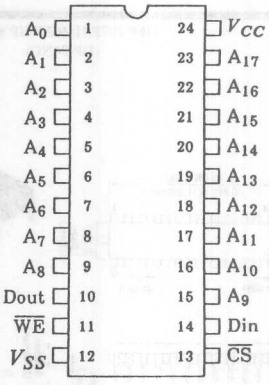
Ordering Information

Type No.	Access Time	Package
HM6707P-20	20ns	300mil 24 pin Plastic DIP
HM6707P-25	25ns	
HM6707JP-20	20ns	300 mil 24 pin SOJ
HM6707JP-25	25ns	

Block Diagram



Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1 : −3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	D_{out}
L	L	Write	I_{CC}, I_{CC1}	High Z

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC}=5.5 V, V_{IN}=V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, V_{OUT}=V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty : 100%, I_{OUT} = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC}-0.2$ V $V_{IN} \leqq 0.2$ V or $V_{IN} \geqq V_{CC}-0.2$V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

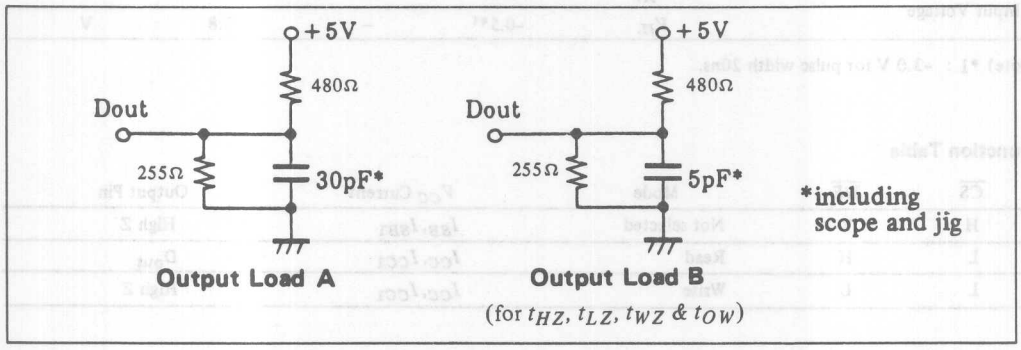
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

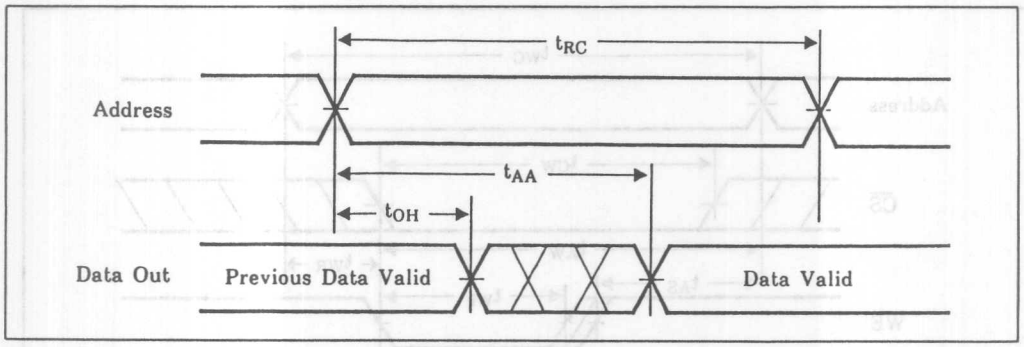


Read Cycle

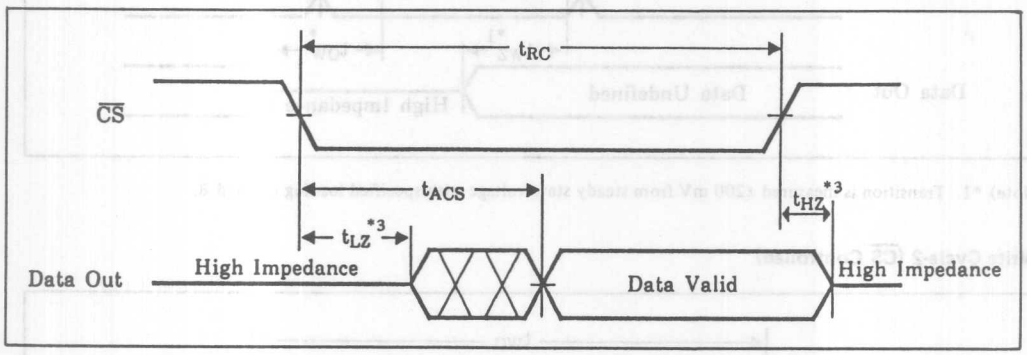
Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Read Cycle-1*1



Read Cycle-2*2



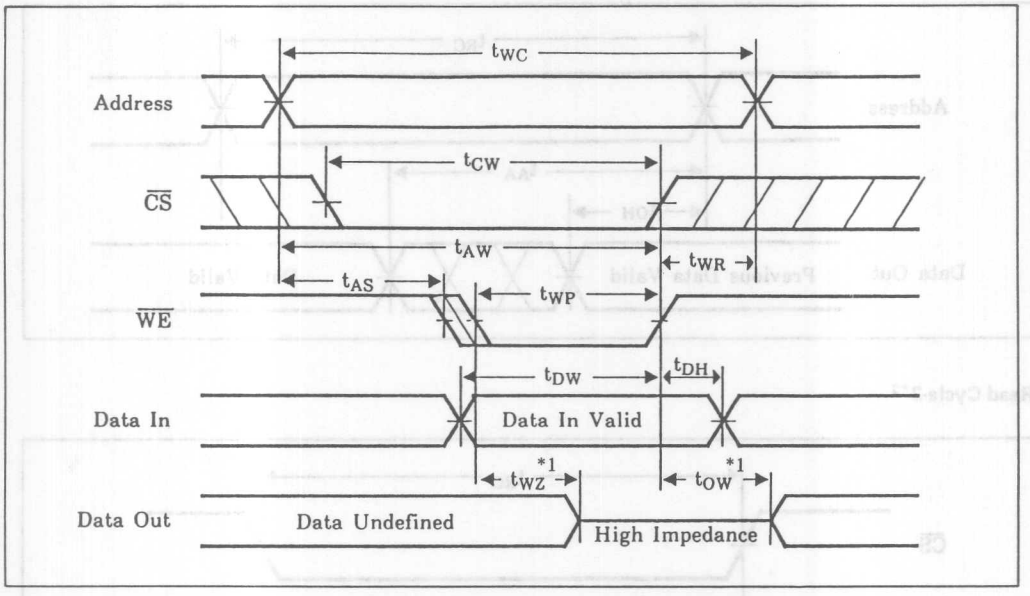
Notes) *1. $\overline{WE}$ is high and $\overline{CS}$ is low for Read cycle.
*2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Write Cycle

Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	3	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	15	–	20	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

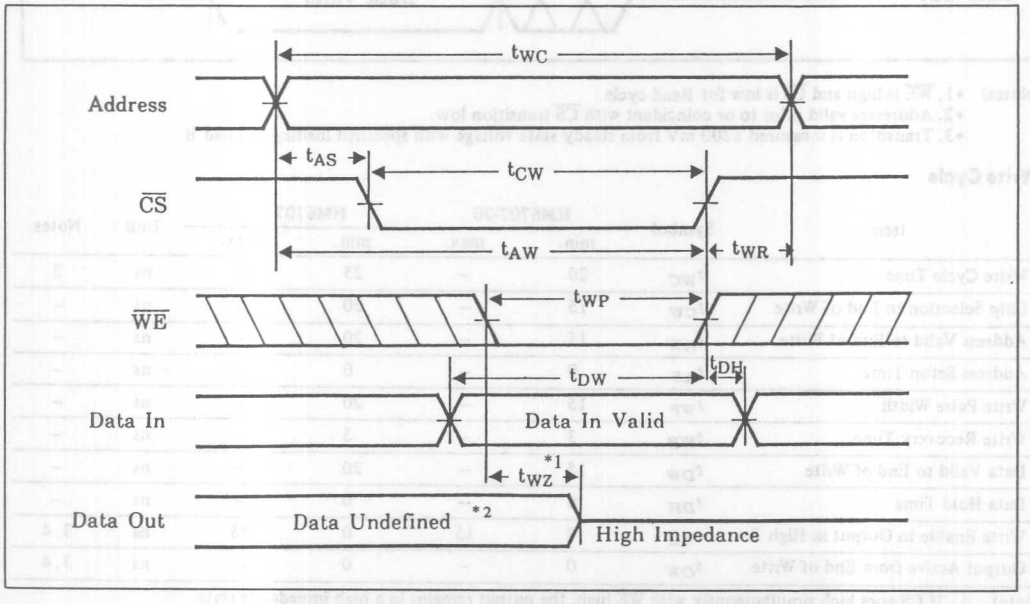
Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Note) *1. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Write Cycle-2 ($\overline{CS}$ Controlled)



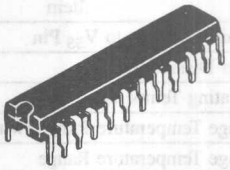
Note) *1. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
*2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer remains in a high impedance state.

HM6707A Series — Product Preview

262144-Word × 1-Bit High Speed Static RAM

■ FEATURES

- Super Fast
  Access Time . . . . . 15/20/25ns (max.)
- Low Power Dissipation . . . . . 400mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



(DP-24NC)

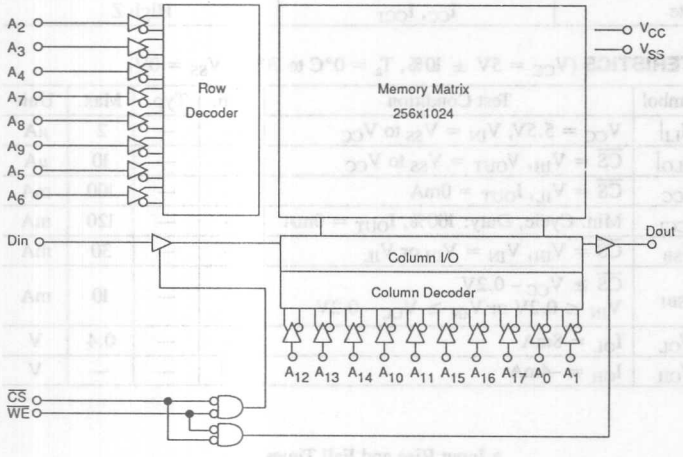


(CP-24D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6707AP-15 HM6707AP-20 HM6707AP-25	15ns 20ns 25ns	300 mil 24 pin Plastic DIP (DP-24NC)
HM6707AJP-15 HM6707AJP-20 HM6707AJP-25	15ns 20ns 25ns	300 mil 24 pin Plastic SOJ (CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width: 15ns, DC: −0.5V

■ TRUTH TABLE

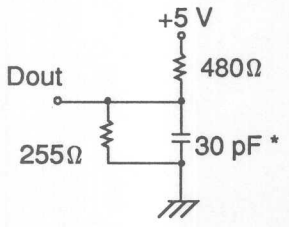
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Data Out
L	L	Write	I_{CC}, I_{CC1}	High Z

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

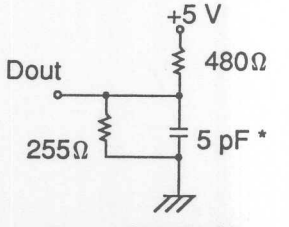
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, I_{OUT} = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Reference Levels: 1.5V
- Input Rise and Fall Times: 4ns
- Output Load: See Figure



Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6.0	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	10.0	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6707A-15		HM6707A-20		HM6707A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns	—
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	0	10	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

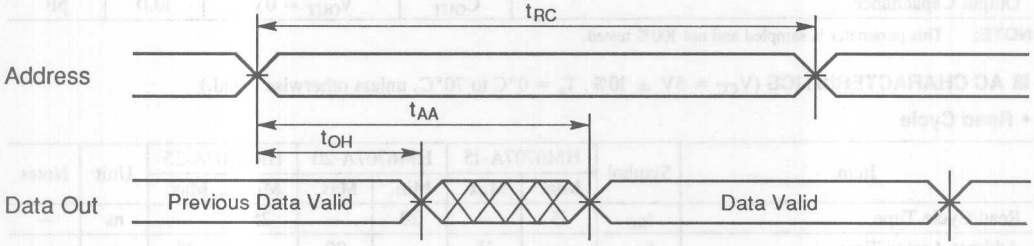
• Write Cycle

Item	Symbol	HM6707A-15		HM6707A-20		HM6707A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	9	—	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	2, 3

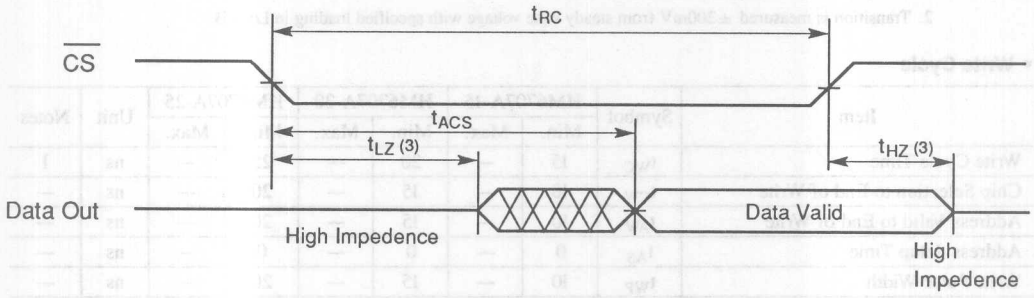
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
3. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1)

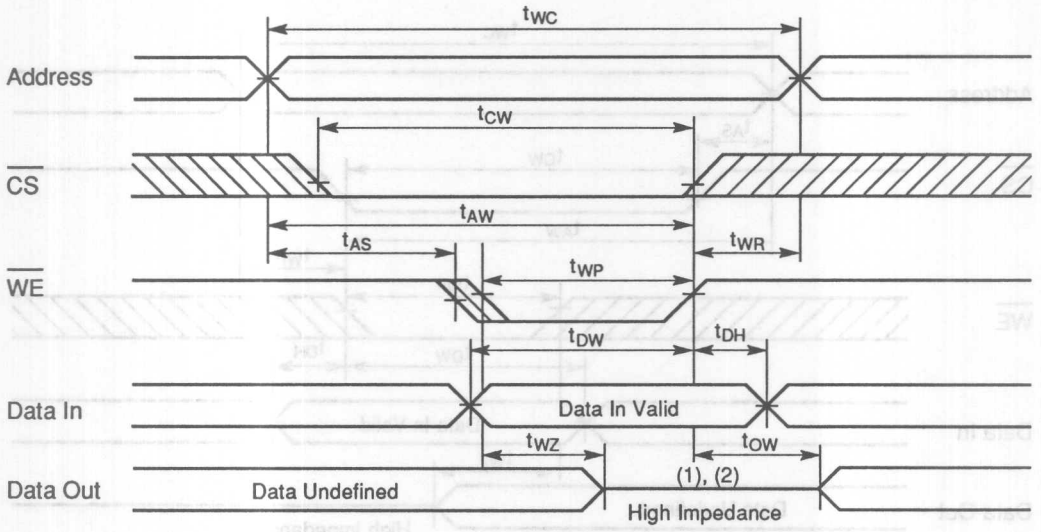


• **Read Cycle (2)** (2)



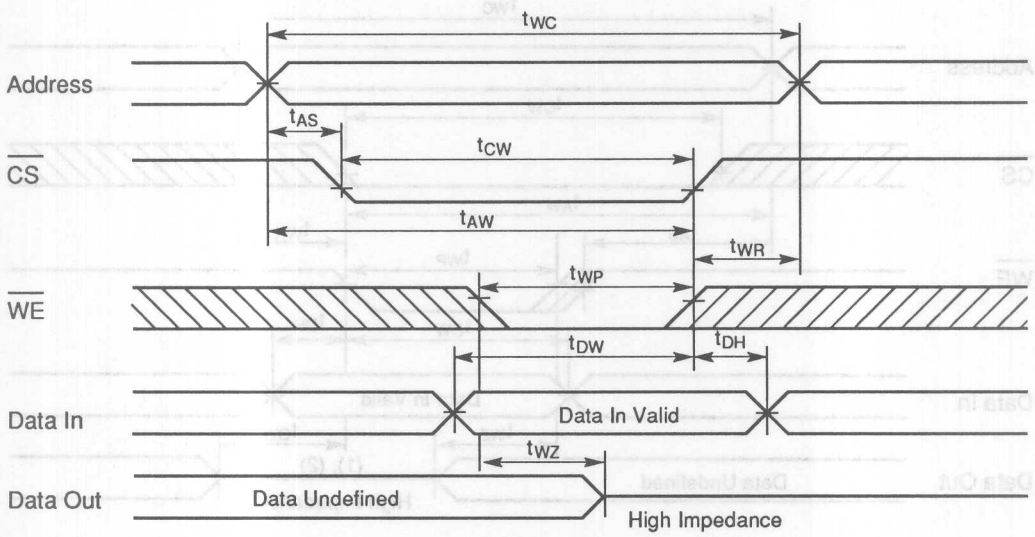
NOTES:
1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



NOTES: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

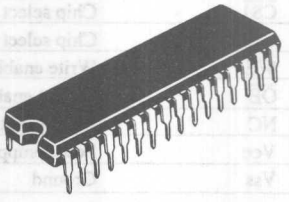
HM628128 Series

131072-Word × 8-Bit High Speed CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128-kword x 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.

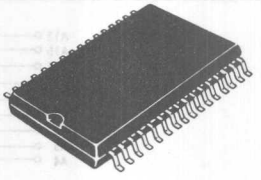
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, is available for high density mounting.

HM628128P Series



(DP-32)

HM628128FP Series



(FP-32D)

Features

- High speed: Fast access time 70/85/100/120 ns (max.)
- Low power
  - Standby: 10 µW (typ) (L-version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)
  - 2 chip selection for battery back up

Ordering Information

Type No.	Access Time	Package
HM628128P-7	70 ns	600 mil 32-pin plastic DIP (DP-32)
HM628128P-8	85 ns	
HM628128P-10	100 ns	
HM628128P-12	120 ns	
HM628128LP-7	70 ns	
HM628128LP-8	85 ns	
HM628128LP-10	100 ns	
HM628128LP-12	120 ns	
HM628128FP-7	70 ns	525 mil 32-pin plastic SOP (FP-32D)
HM628128FP-8	85 ns	
HM628128FP-10	100 ns	
HM628128FP-12	120 ns	
HM628128LFP-7	70 ns	
HM628128LFP-8	85 ns	
HM628128LFP-10	100 ns	
HM628128LFP-12	120 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Arrangement

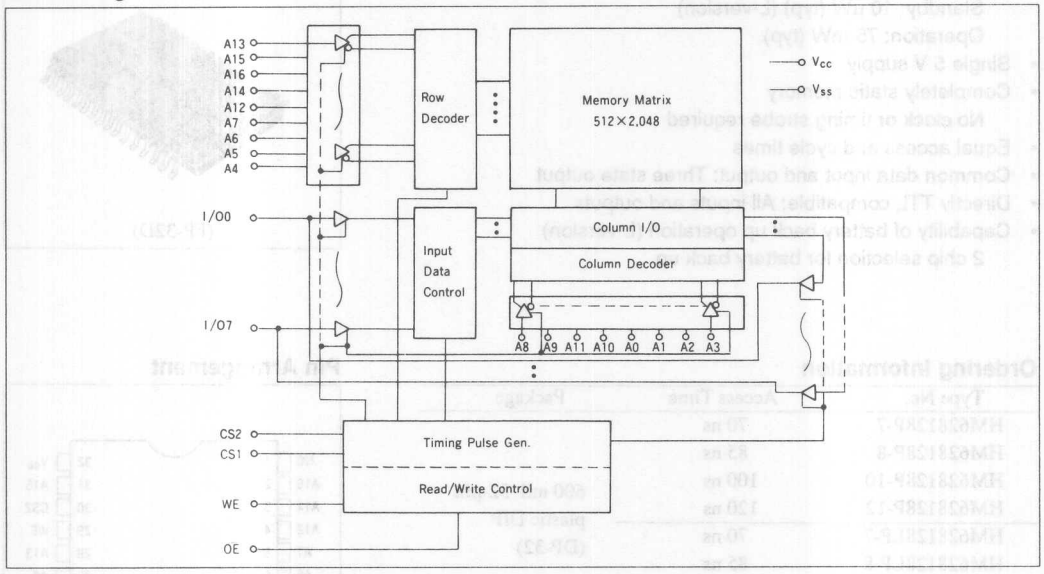


(Top View)

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: *1. –3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	–0.3*1	—	0.8	V	

Note: *1. –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$= Vss to Vcc
Operating power supply current: DC	I_{CC}	—	15	30	mA	$\overline{CS1}$= V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$= 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥Vcc – 0.2 V V_{IH} ≥ Vcc – 0.2V, V_{IL} ≤ 0.2V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V
		—	2*2	100*2	µA	$\overline{CS1}$ ≥ Vcc – 0.2 V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: *1. Typical values are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{in}	—	—	8	pF	V_{in} = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted)

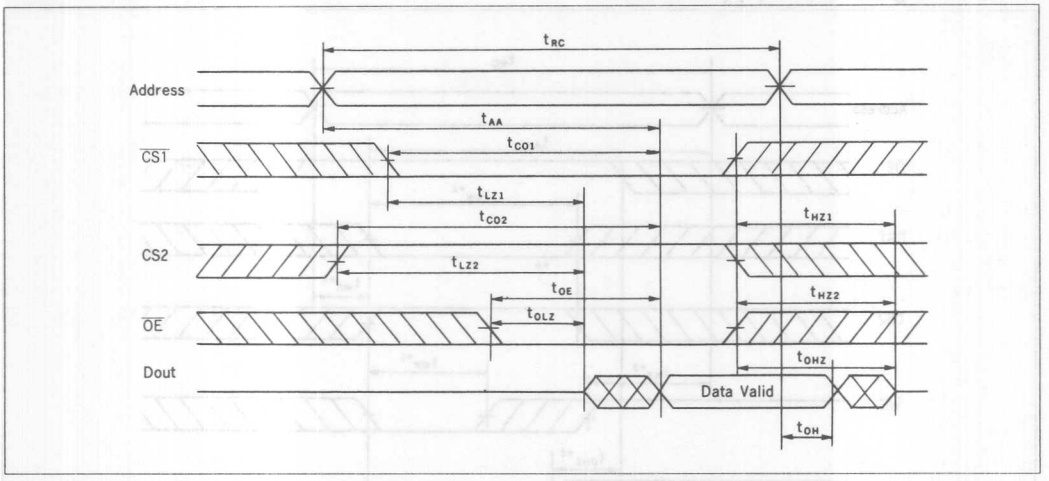
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF) (Including scope & jig)

Read Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	t_{CO1}	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	t_{CO2}	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	t_{LZ1}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Chip selection (CS2) to output in low-Z	t_{LZ2}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Output enable ($\overline{OE}$) to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	*1, *2, *3
Chip deselection ($\overline{CS1}$) to output in high-Z	t_{HZ1}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Chip deselection (CS2) to output in high-Z	t_{HZ2}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output disable ($\overline{OE}$) to output in high-Z	t_{OHZ}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

Read Timing Waveform*4

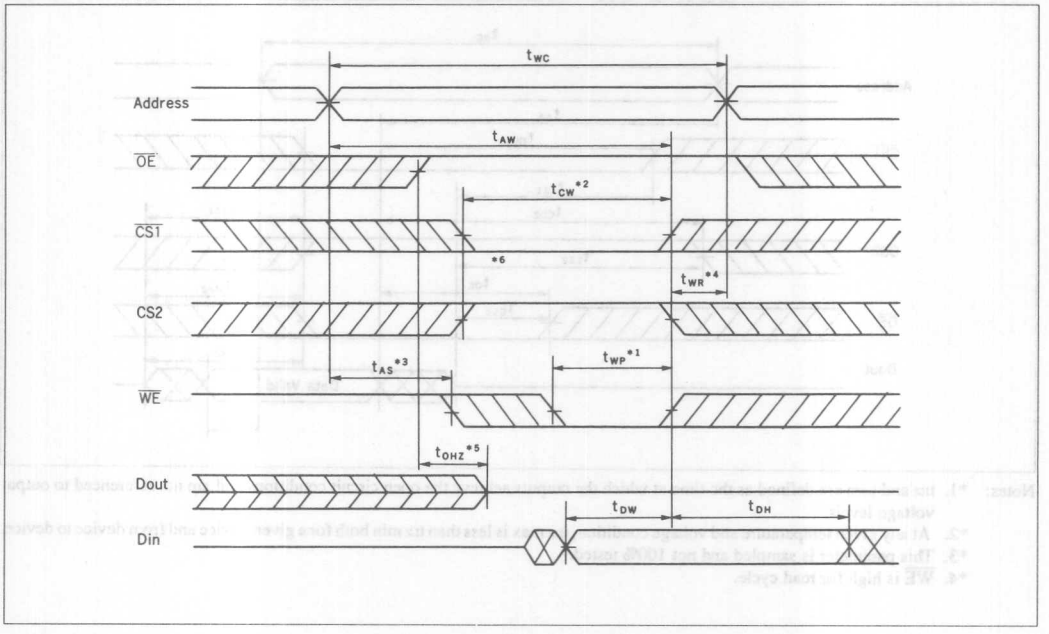


Notes: *1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
*3. This parameter is sampled and not 100% tested.
*4. $\overline{WE}$ is high for read cycle.

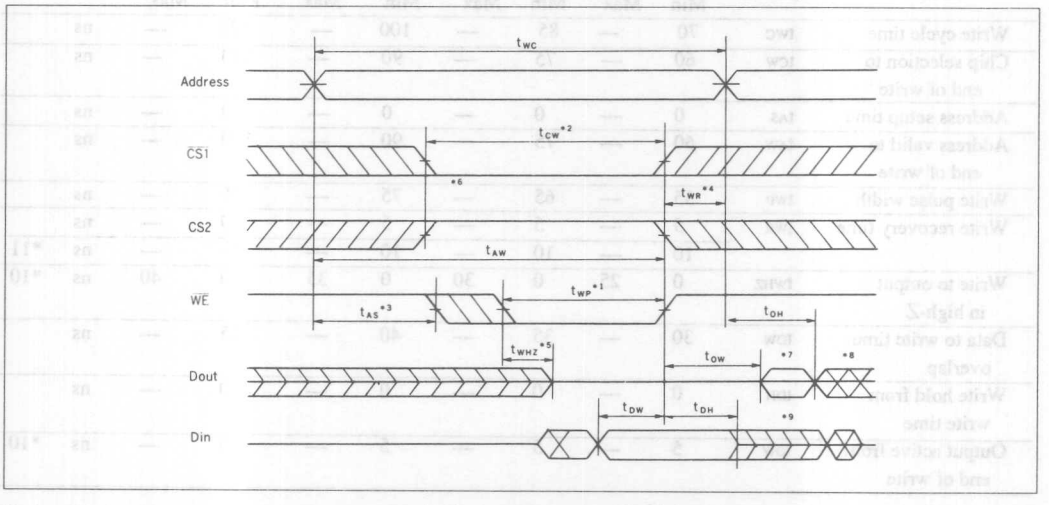
Write Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	90	—	100	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	60	—	75	—	90	—	100	—	ns	
Write pulse width	t_{WP}	55	—	65	—	75	—	85	—	ns	
Write recovery time	t_{WR}	5	—	5	—	5	—	10	—	ns	
		10	—	10	—	10	—	15	—	ns	*11
Write to output in high-Z	t_{WHZ}	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	t_{DW}	30	—	35	—	40	—	45	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

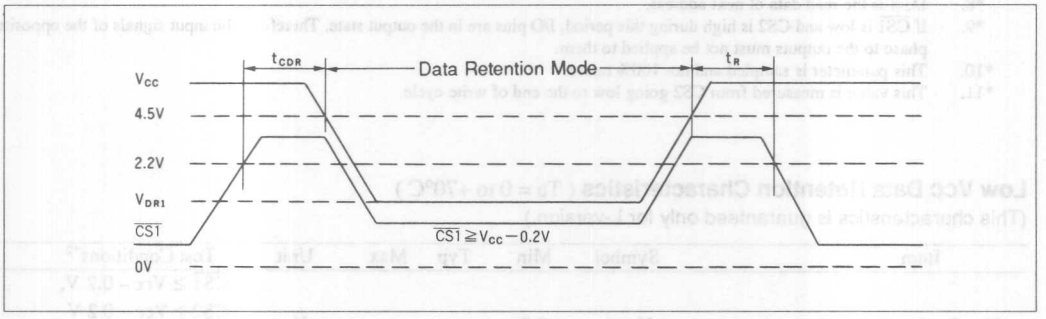
*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
*7. Dout is the same phase of the latest written data in this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
*10. This parameter is sampled and not 100% tested.
*11. This value is measured from CS2 going low to the end of write cycle.

Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

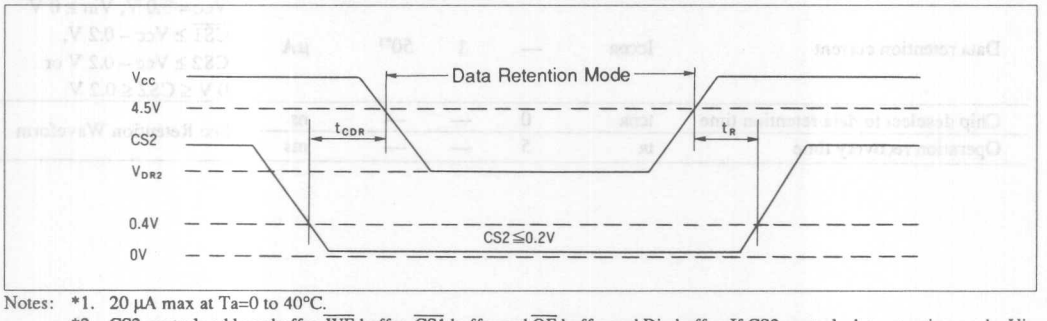
(This characteristics is guaranteed only for L-version.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions*2
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current	I_{CCDR}	—	1	50*1	µA	Vcc = 3.0 V, Vin ≥ 0 V $\overline{CS1} \geq$ Vcc – 0.2 V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation recovery time	t_R	5	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: *1. 20 μA max at Ta=0 to 40°C.

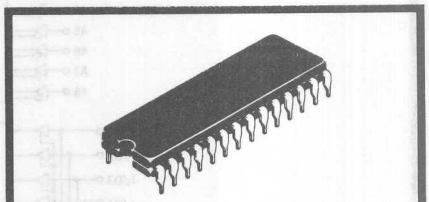
*2. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM624256 Series
4-Bit CMOS Static RAM

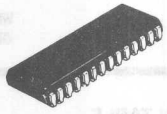
HM624256 SERIES
262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624256 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256, packaged in a 400-mil plastic SOJ is available for high density mounting.



(DP-28C)



(CP-28D)

■ FEATURES

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed: Fast access time 35/45 ns (max.)
- Low power
  Operation: 350 mW (typ.)
  Standby: 100 μW (typ.)
- Completely static memory:
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624256P-35	35 ns	400 mil
HM624256P-45	45 ns	28-pin
HM624256LP-35	35 ns	Plastic DIP
HM624256LP-45	45 ns	(DP28C)
HM624256JP-35	35 ns	400 mil
HM624256JP-45	45 ns	28-pin
HM624256LJP-35	35 ns	Plastic SOJ
HM624256LJP-45	45 ns	(CP-28D)

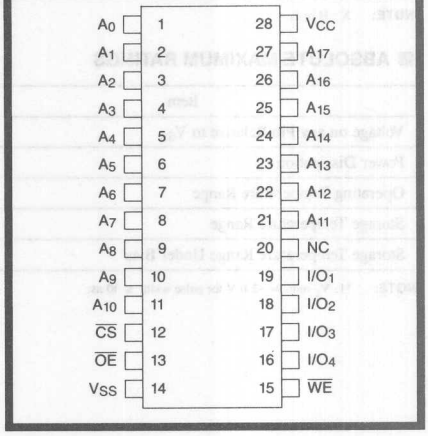
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{17}	Address
I/O_1–I/O_4	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

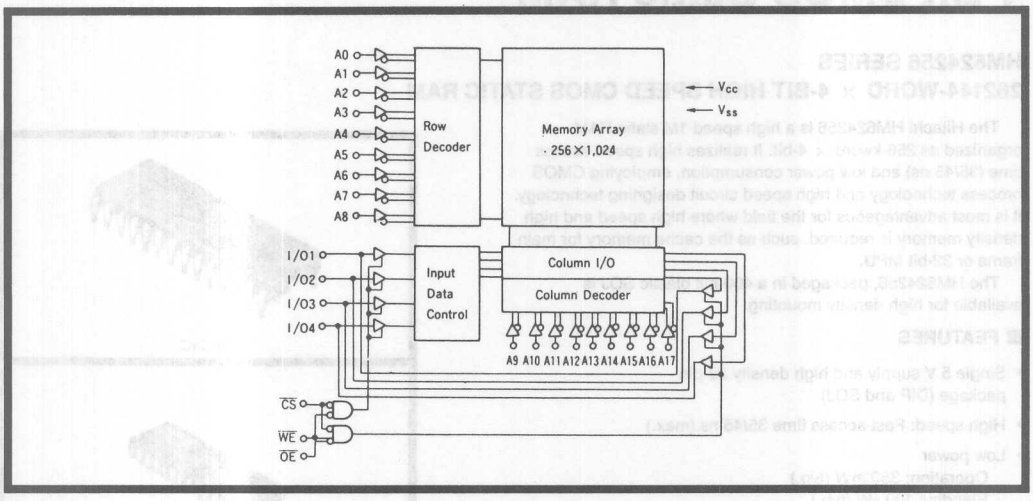
Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

PIN ARRANGEMENT

(DIP and SOJ)
Top View



■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1)-(3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle(2)

NOTE: X : H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: *1. V_T min. = −2.0 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = -2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	μA	$\overline{CS}$ = V_{IH} V_{out} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, I_{out} = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}*2 I_{SB1}*3	— —	0.02 —	2.0 0.2	mA mA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

NOTES: *1. Typical limits are at V_{CC} = 5.0 V, T_a = 25°C and specified loading.
*2. JP-version
*3. LJP-version

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

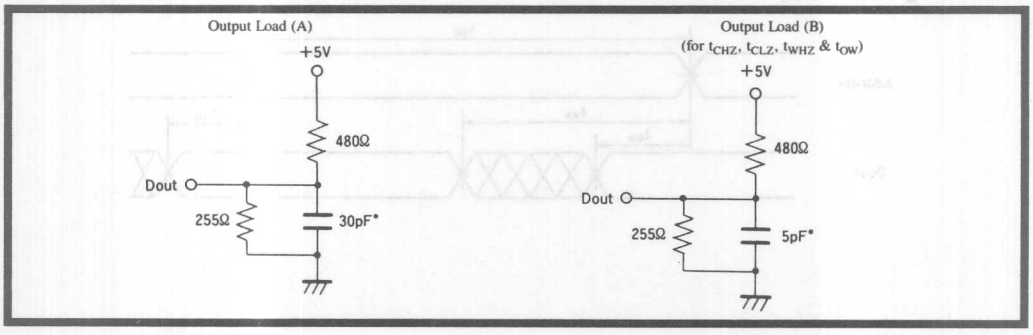
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures

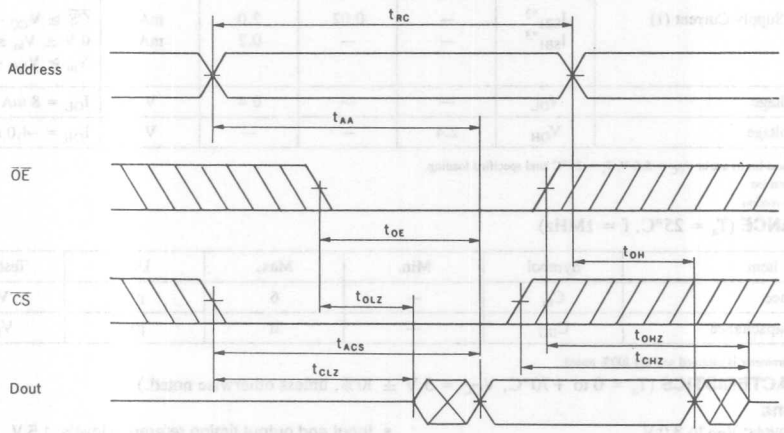


NOTE: *Including scope & jig.

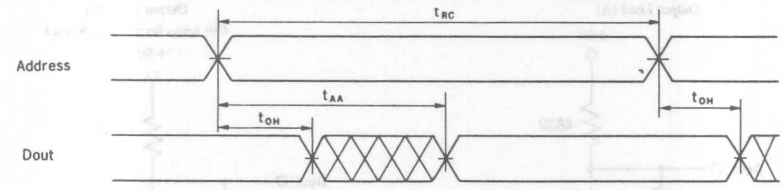
■ Read Cycle

Item	Symbol	HM624256-35		HM624256-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ} *1	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	18	—	23	ns
Output Enable to Output in Low-Z	t_{OLZ} *1	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ} *1	0	20	0	20	ns
Chip Disable to Output in High-Z	t_{OHZ} *1	0	10	0	15	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

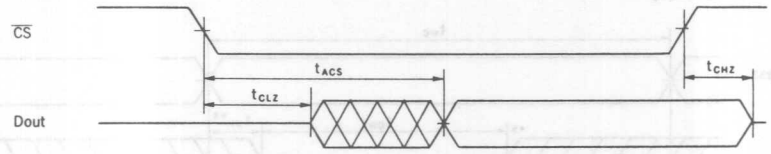
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5



NOTES: *1. Transition is measured ±200 mv from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

*2. $\overline{WE}$ is high for read cycle.

*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.

*4. Address valid prior to or coincident with $\overline{CS}$ transition low.

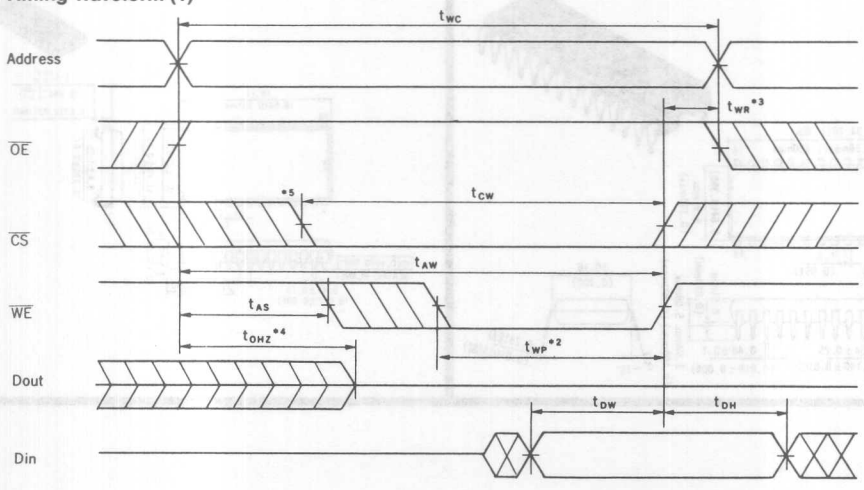
*5. $\overline{OE}$ = V_{IL}.

■ Write Cycle

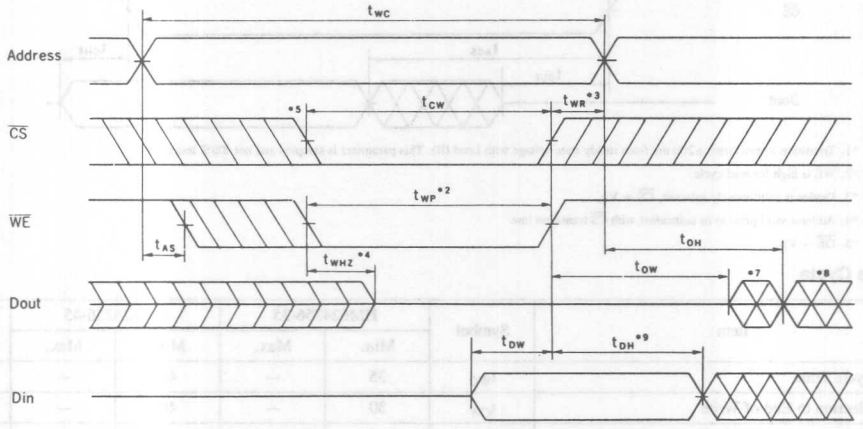
Item	Symbol	HM624256-35		HM624256-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Output Disable to Output in High-Z*1	t_{OHZ}	0	10	0	15	ns
Write to Output in High-Z*1	t_{WHZ}	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	20	—	25	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	ns
Output Active From End of Write*1	t_{OW}	0	—	0	—	ns

NOTE: 1. Transition is measured ± 200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1)



Write Timing Waveform (2) *6



NOTES:

*1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

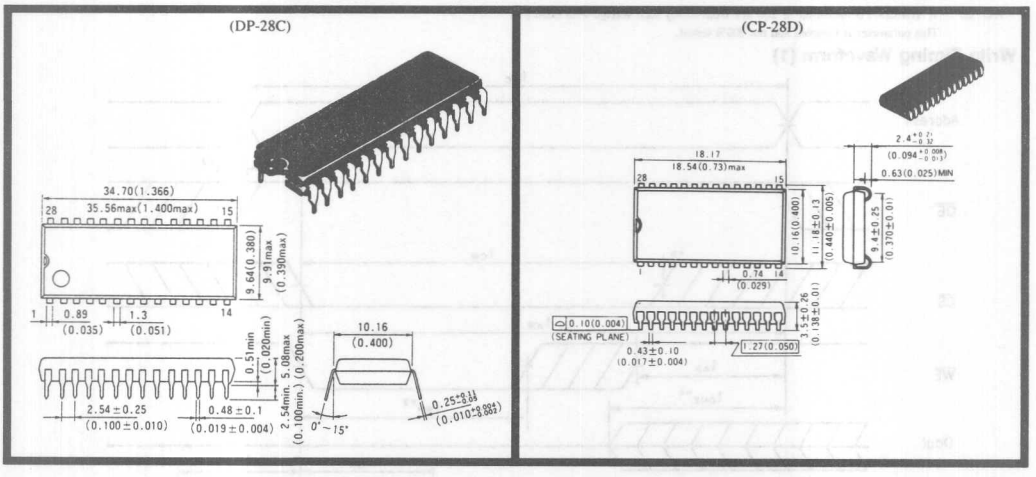
*5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.

*6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})

*7. D_{OUT} is the same phase of write data of this write cycle.

*8. D_{OUT} is the read data of next address.

*9. If $\overline{CS}$ is low during this period, I/O pins are the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.



HITACHI

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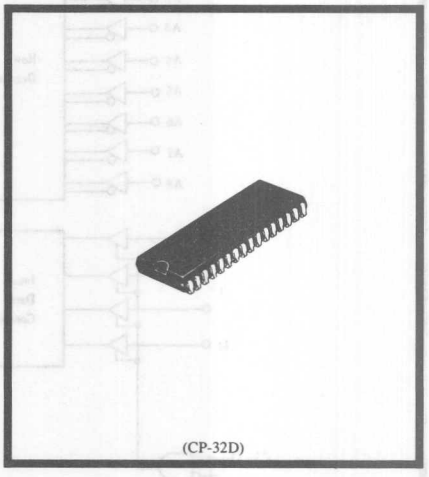
HM624257 Series
4-Bit CMOS Static RAM

Under Development

HM624257 SERIES
262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624257 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257, packaged in a 400-mil plastic SOJ is available for high density mounting.



(CP-32D)

■ FEATURES

- Single 5 V supply and high density 32-pin package (SOJ)
- High speed: Access time 35/45 ns (max.)
- Low power dissipation
  - Active mode: 350 mW (typ.)
  - Standby: 100 μW (typ.)
- Completely static memory:
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

■ ORDERING INFORMATION

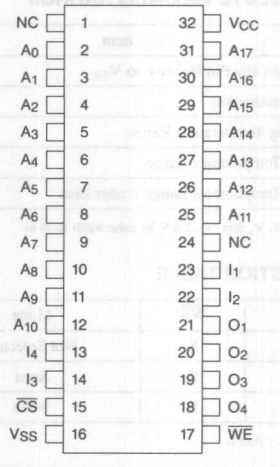
Type No.	Access Time	Package
HM624257JP-35	35 ns	400 mil 32-pin Plastic SOJ (CP-32D)
HM624257JP-45	45 ns	
HM624257LJP-35	35 ns	
HM624257LJP-45	45 ns	

■ PIN DESCRIPTION

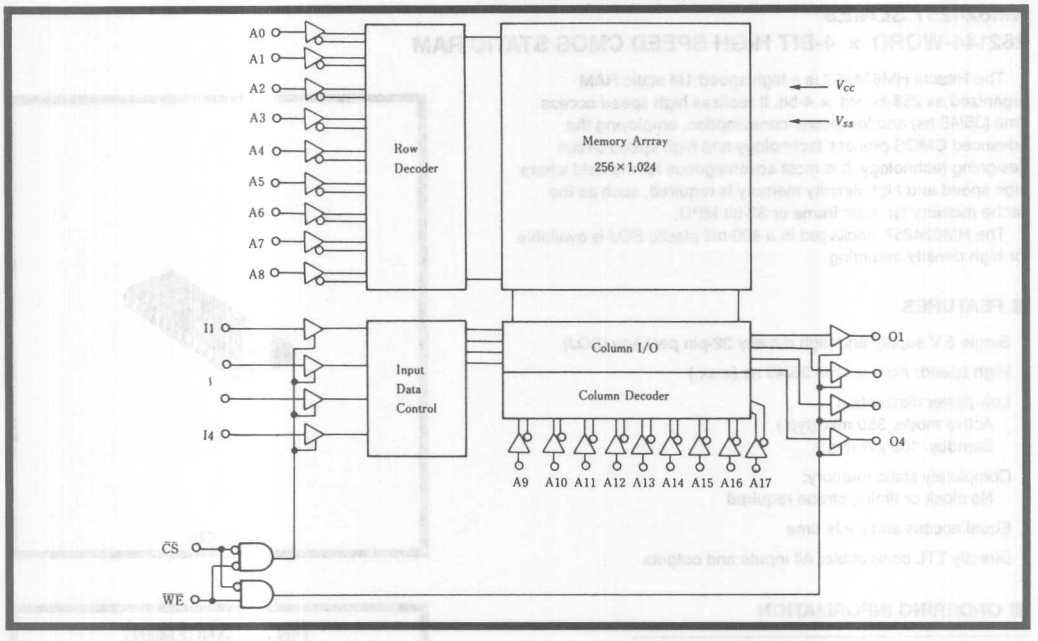
Pin Name	Function
A_0–A_{17}	Address
I_1–I_4	Data Input
I_1–O_4	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

PIN ARRANGEMENT

Top View



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{in}	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: *1. V_{in} min. = −2.0 V for pulse width ≤ 10 ns.

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle(1)–(2)
L	L	Write	I_{CC}	High-Z	Write Cycle(1)–(2)

NOTE: X : H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = −2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} − 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4.0 mA

NOTE: 1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

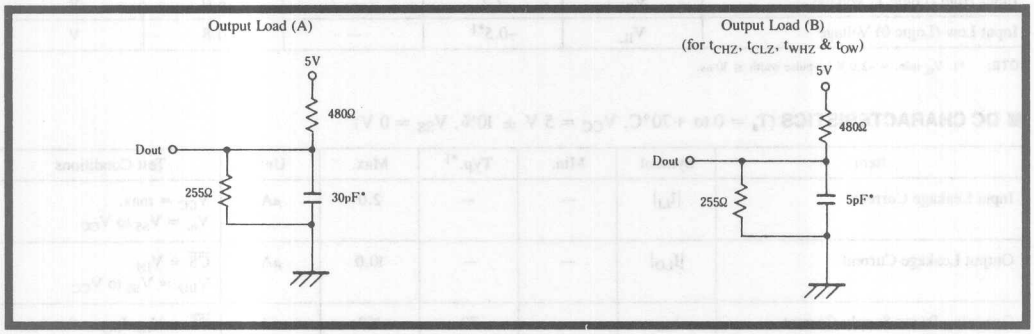
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Output Capacitance	C_{out}	—	11	pF	V_{out} = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures



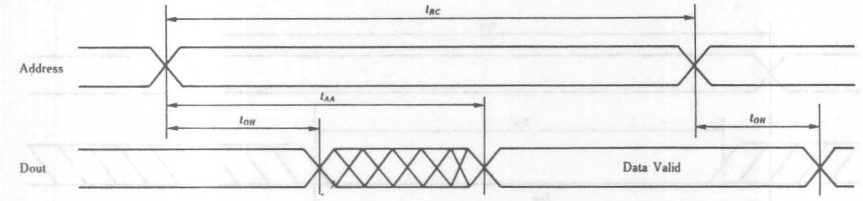
NOTE: *Including scope & jig.

■ Read Cycle

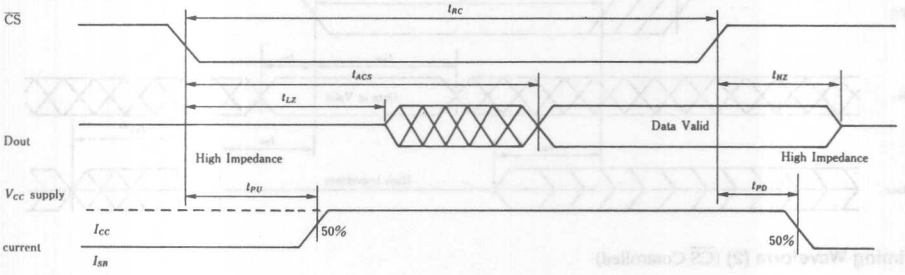
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—		—	30	ns

NOTE: 1. Transition is measured ±200 mV from steady voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



NOTES: *1. $\overline{WE}$ is high for read cycle.

*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

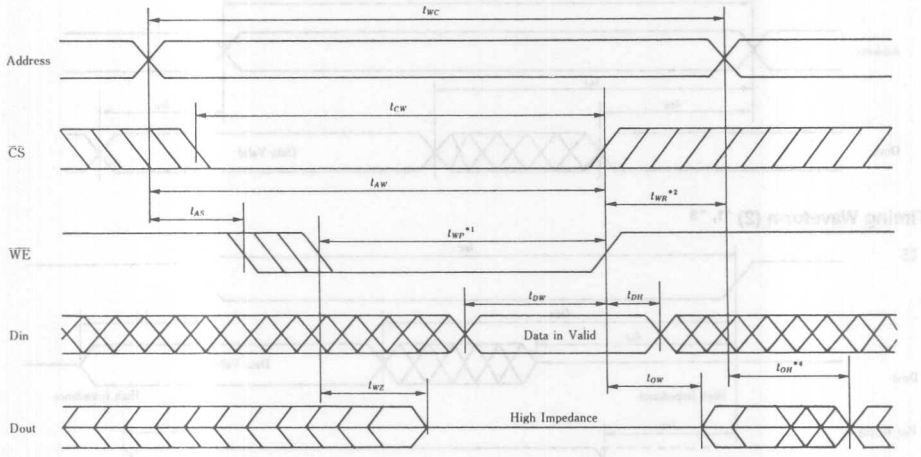
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ Write Cycle

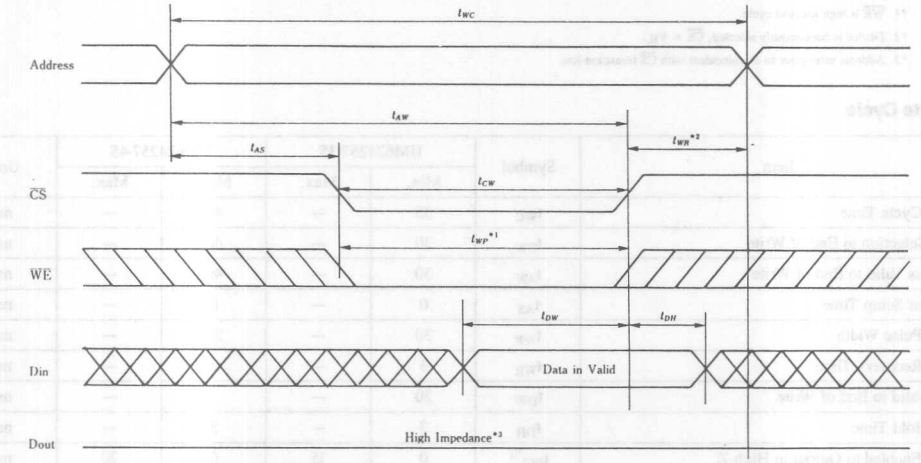
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	20	—		—	ns
Data Hold Time	t_{DH}	3	—	3	—	ns
Write Enabled to Output in High-Z	t_{WZ}*1	0	15	0	20	ns
Output Active From End of Write	t_{OW}*1	5	—	5	—	ns

NOTE: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



NOTES: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output buffers remain in a high impedance state.

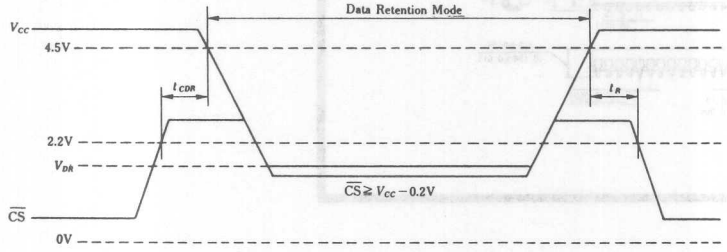
*4. D_{OUT} is the same phase of write data of this write cycle.

■ Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

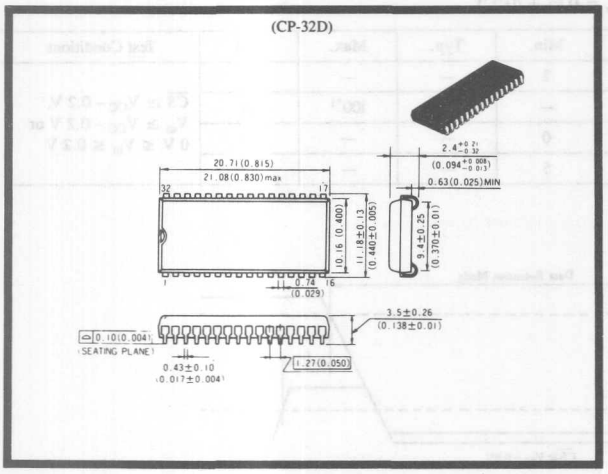
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or 0 V ≤ V_{in} ≤ 0.2 V
Data Retention Current	I_{CCDR}	—	2	100*1	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

NOTE: *1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



(CP-32D)


20.71(0.815)
21.08(0.830)max
32
17
1
16
10.16 (0.400)
11.18±0.13
(0.440±0.005)
2.4 +0.21 −0.32
(0.094 +0.008 −0.013)
0.63(0.025)MIN
9.4±0.25
(0.370±0.01)
0.74
(0.029)
3.5±0.26
(0.138±0.01)
0.10(0.004)
SEATING PLANE
0.43±0.10
(0.017±0.004)
1.27(0.050)

HM66204 Series — Maintenance Only

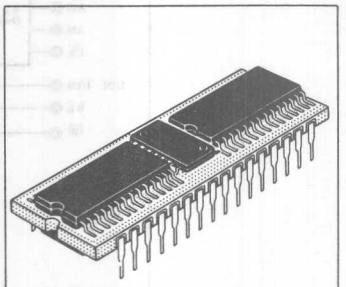
131072-word x 8-bit High Density CMOS Static RAM Module

The HM66204 is a high density 1 M-bit static RAM module consisted of 4 pieces of HM62256FP/LFP products (SOP type 256k static RAM) and a HD74HC138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66204 is the standard 600 mil width 32 pin dual-in-line package. Its pin arrangement is completely compatible with 1 M-bit monolithic static RAM.

The HM66204 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66204 makes high density mounting possible with no surface mount technology.

These features make the HM66204 ideally suited for high density compacted memory systems.



(DM-32A)

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 256k static RAM (SOP; HM62256FP/LFP) and CMOS decoder logic (SOP; HD74HC138FP equivalent)
- Pin compatible with 1M monolithic static RAM
- High speed
  - Fast access time 120 ns/150 ns (maximum)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby 40 μW (typical) (L-version)
  - Operation 50 mW(typical) (f = 1 MHz)
- Common data input and output, three state outputs
- Capable of battery backup operation (L-version)

Pin Arrangement



(Top View)

Ordering Information

Part No.	Access Time	Package
HM66204-12	120 ns	600-mil 32-pin DIP
HM66204-15	150 ns	
HM66204L-12	120 ns	
HM66204L-15	150 ns	

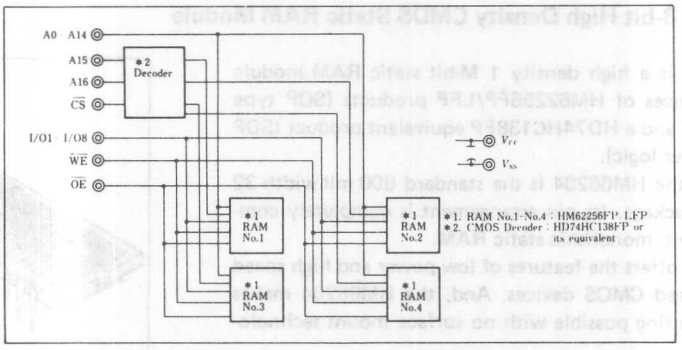
Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C
Power dissipation	P_T	1.0	W

Pin Description

Pin Name	Function
A0 - A16	Address
I/O1 - I/O8	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Mode Selection

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not selected (Power down)	H	×	×	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note) × = Don't care (H or L)

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) Voltage	V_{IH}	3.85*1	–	6.0	V	A15, A16, $\overline{CS}$
		2.2	–	6.0	V	Others except A15, A16, $\overline{CS}$
Input low (logic 0) Voltage	V_{IL}	–0.5	–	0.8	V	

Note) *1. V_{IH} min is determined by V_{CC} × 0.7.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	–	–	8	μA	$V_{in} = V_{SS}$ to V_{CC}	
		–	–	2	μA	$V_{in} = V_{SS}$ to 3.5V	
Output leakage current	$\|I_{LO}\|$	–	–	8	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	
		–	–	2	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to 3.5V	
Operating power supply current: DC	I_{CC}	–	10	25	mA	$\overline{CS} = V_{IL}$ $I_{I/O}$ = 0mA	
Average operating power supply current (1)	I_{CC1}	–	37	80	mA	MIN. cycle duty = 100%	–12
		–	35	80		$I_{I/O}$ = 0mA	–15
Average operating power supply current (2)	I_{CC2}	–	10	15	mA	$\overline{CS} = V_{IL}$, $V_{IH} = V_{CC}$ V_{IL} = 0V, $I_{I/O}$ = 0mA f = 1MHz	
Standby power supply current: DC	I_{SB}	–	2	12	mA	$\overline{CS} = V_{IH}$	
Standby power supply current (1): DC	I_{SB1}	–	8	400	μA	$\overline{CS} \geq V_{CC}-0.2V$ A15·A16 $\geq V_{CC} - 0.2V$ or 0V ≦ A15·A16 ≦ 0.2V	HM66204L Series
		–	0.16	8	mA		
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA	
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = –1.0 mA	

Note) *1. Typical values are at V_{CC} = 5.0V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	–	45	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	–	–	50	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

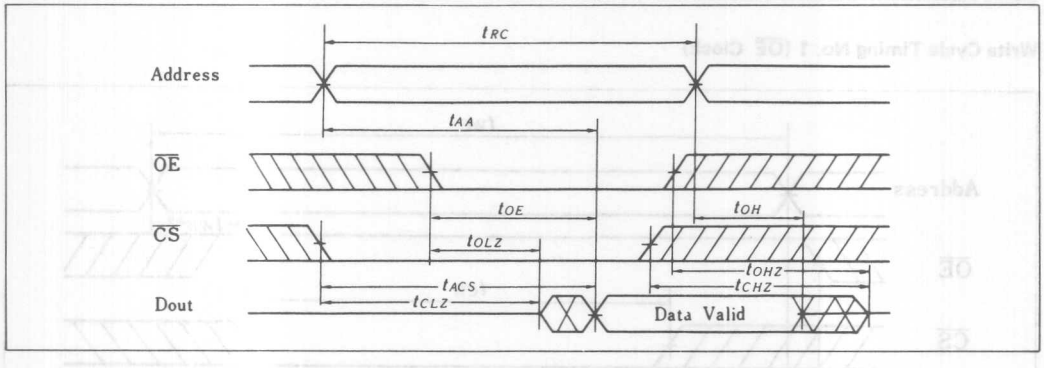
AC Test Conditions

- Input pulse levels:
  - 0.8V to 4.0V . . . $\overline{CS}$, A15, A16
  - 0.8V to 2.4V . . . Other pin except $\overline{CS}$, A15, A16
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5V
- Output load: 1 TTL Gate and C_L (100pF) (Including scope & jig)

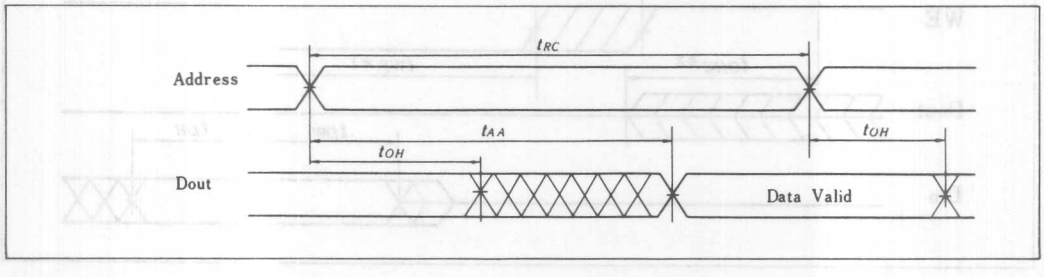
Read Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip select access time	t_{ACS}	–	120	–	150	ns
Output enable to output valid	t_{OE}	–	60	–	70	ns
Output hold from address change	t_{OH}	10	–	10	–	ns
Chip selection to output in low Z	t_{CLZ}	10	–	10	–	ns
Output enable to output in low Z	t_{OLZ}	5	–	5	–	ns
Chip deselection to output in high Z	t_{CHZ}	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns

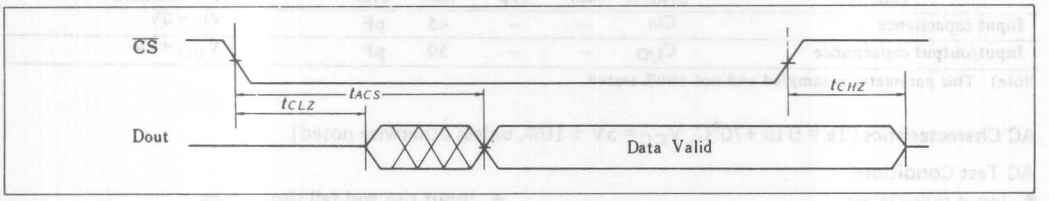
Read Cycle Timing No. 1 *1



Read Cycle Timing No. 2 *1,*2,*4



Read Cycle Timing No. 3 *1, *3, *4

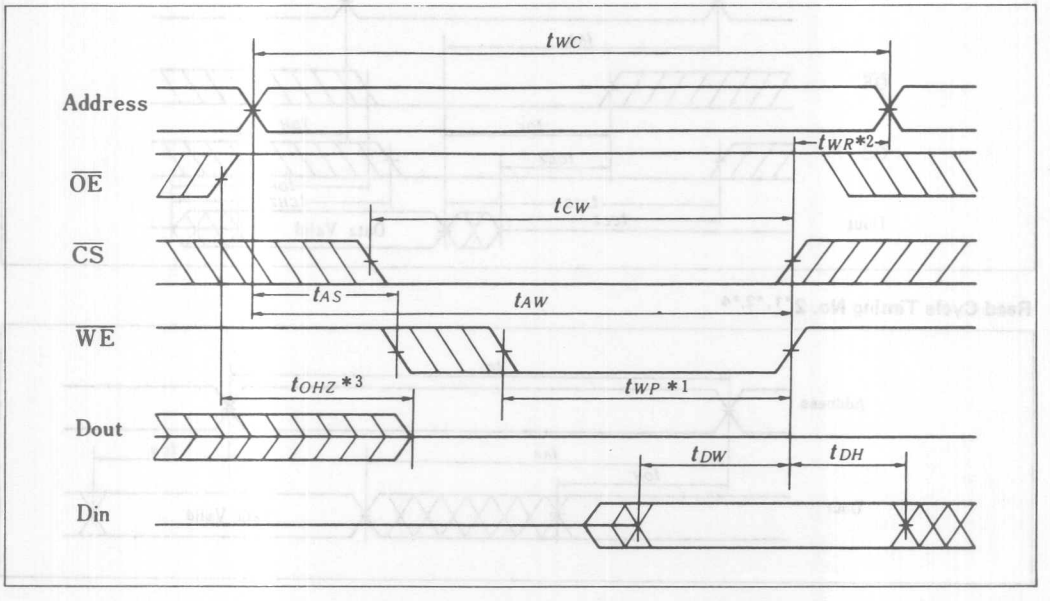


Notes) *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

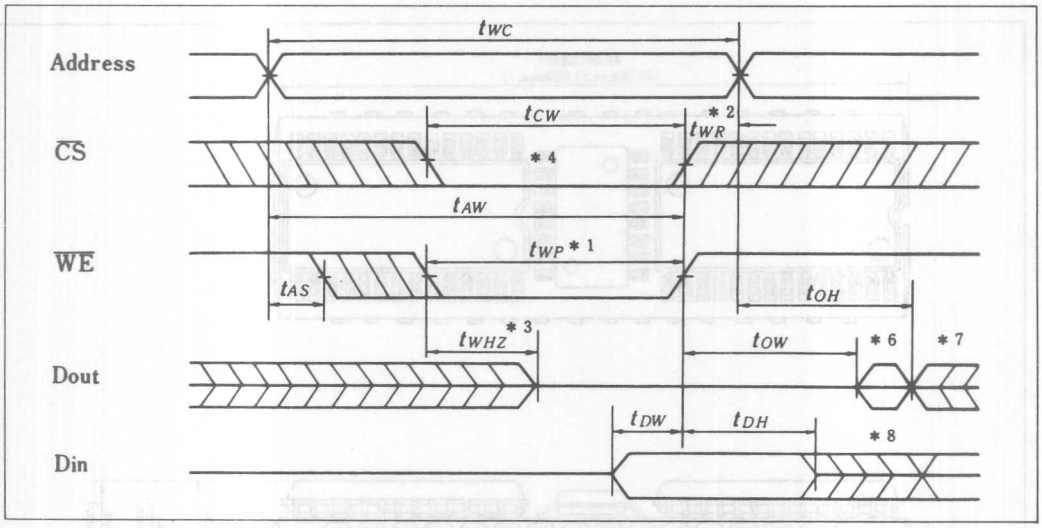
Write Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Chip selection to end of write	t_{CW}	100	–	120	–	ns
Address valid to end of write	t_{AW}	100	–	120	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	90	–	110	–	ns
Write recovery time	t_{WR}	5	–	5	–	ns
Write to output in high Z	t_{WHZ}	0	40	0	50	ns
Data to write time overlap	t_{DW}	50	–	60	–	ns
Data hold from write time	t_{DH}	0	–	0	–	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns
Output active from end of write	t_{OW}	5	–	5	–	ns

Write Cycle Timing No. 1 ($\overline{OE}$ Clock)



Write Cycle Timing No. 2*5 ($\overline{OE}$ Low Fixed)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*6. D_{out} should be held in phase of the written data during this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

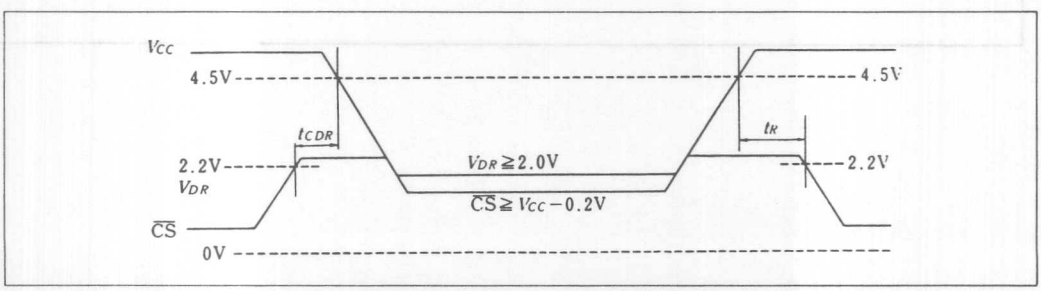
Low V_{CC} Data Retention Characteristics (Ta = 0°C to +70°C)

Data retention characteristics is guaranteed only for L version.

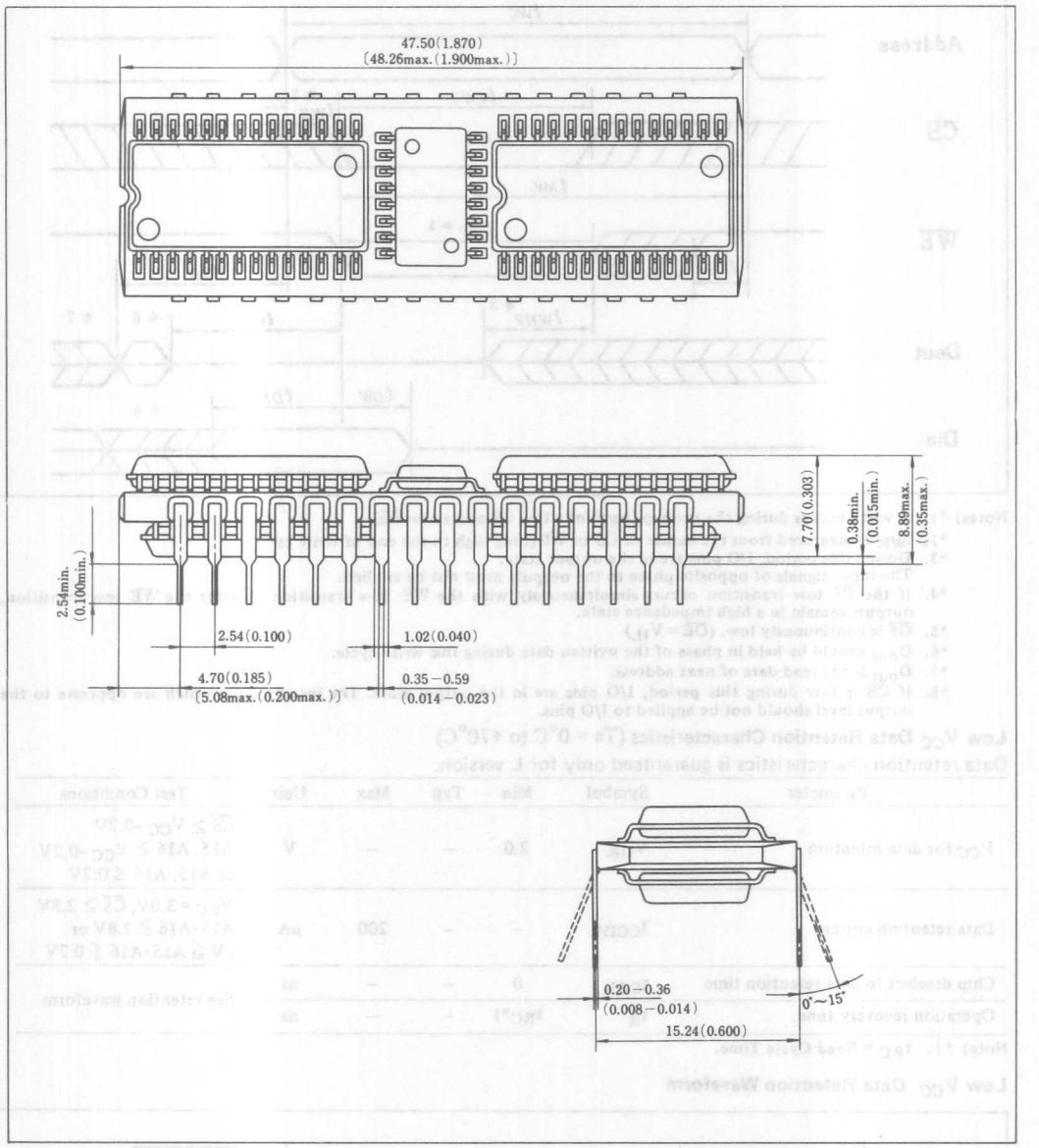
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}-0.2V$ A15, A16 $\geq V_{CC}-0.2V$ or A15, A16 $\leq 0.2V$
Data retention current	I_{CCDR}	–	–	200	µA	V_{CC} = 3.0V, $\overline{CS} \geq 2.8V$ A15·A16 $\geq 2.8V$ or $0V \leqq$ A15·A16 $\leqq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Package Dimensions; Unit: mm (inch)



HM63921-20/25/35 — Product Preview

2K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63921 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and half-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

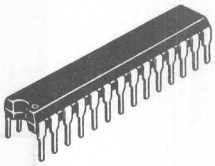
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 30/35/45ns. Organization of HM63921 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 2k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (±10%) Power Supply
- Empty and Full Warning Flags
- Half-Full Flag
- Access Time 20/25/35ns
- Package . . . . . .300-mil 28-pin Plastic DIP Package

■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63921P-20	20ns	300-mil 28-pin
HM63921P-25	25ns	Plastic DIP
HM63921P-35	35ns	(DP-28NA)



(DP-28NA)

■ PIN ARRANGEMENT

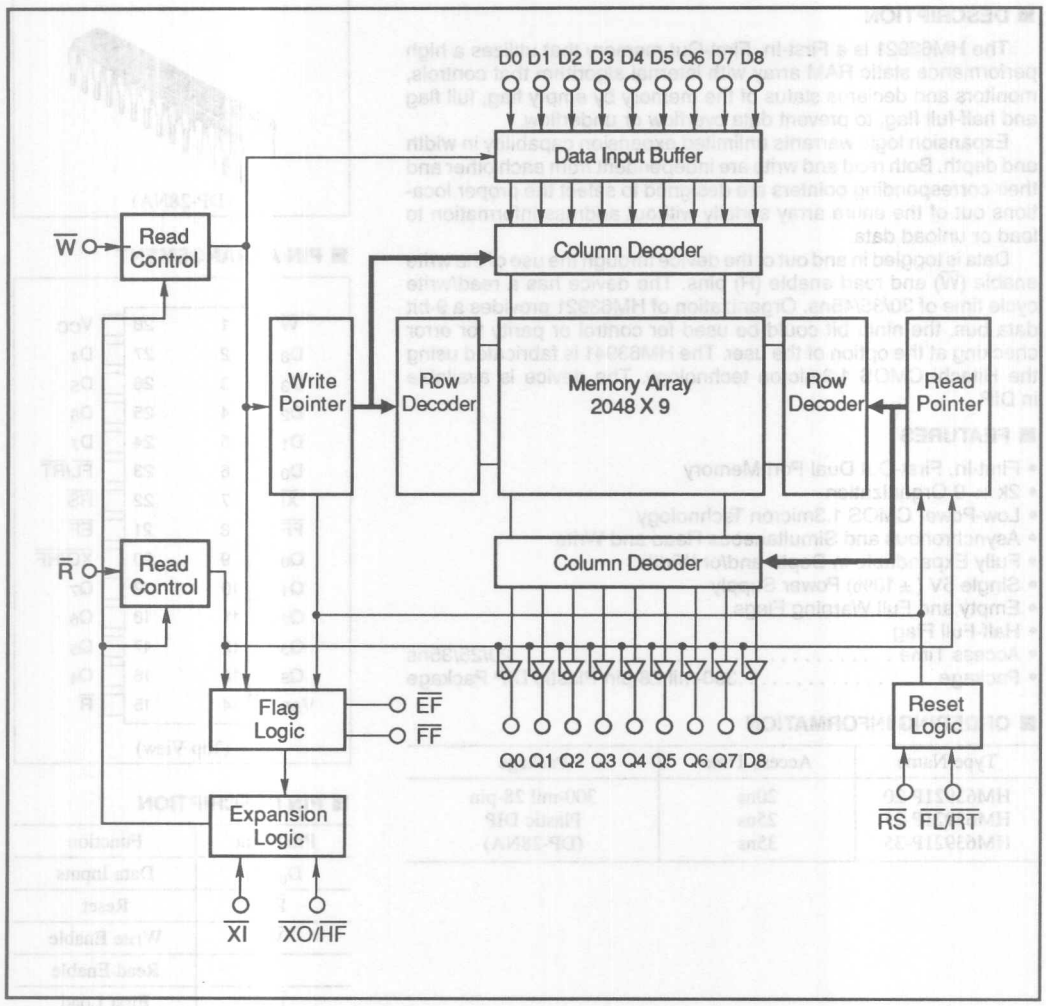


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0–D_8	Data Inputs
$\overline{RS}$	Reset
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{FL}$	First Load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-In
$\overline{XO}$	Expansion-Out
$\overline{HF}$	Half-Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
Q_0–Q_8	Data Outputs

■ BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	−0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. −3.5V for pulse width ≤ 10ns.

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5(1)	—	0.8	V

NOTE: 1. −3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V − V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V − V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	−20	—	120	mA
			−25	—	110	mA
			−35	—	100	mA
Standby Power Supply Current	I_{SB1}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	—	—	10	mA
	I_{SB2}	All inputs ≥ V_{CC} − 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

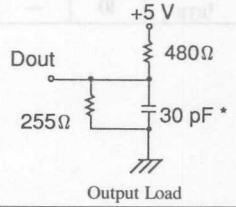
Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	10	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



Output Load

*Including scope and jig.

• Read Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	30	—	35	—	45	—	ns
Access Time	t_A	—	20	—	25	—	35	ns
Read Recovery Time	t_{RR}	10	—	10	—	10	—	ns
Read Pulse Width	t_{RPW}	20	—	25	—	35	—	ns
Read Low to DB Low Z	t_{RLZ}(1)	5	—	5	—	5	—	ns
Read High to DB High Z	t_{RHZ}(1)	—	15	—	15	—	20	ns
Data Valid from Read High	t_{OH}	3	—	3	—	3	—	ns
Read Pulse Width After Empty Flag High	t_{RPE}	20	—	25	—	35	—	ns
Write High to DB Low Z (Read Data Flow Through Mode)	t_{WLZ}(1)	3	—	3	—	3	—	ns

NOTE: 1. t_{RLZ}, t_{RHZ} and t_{WLZ} are sampled and not 100% tested.

• Write Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	30	—	35	—	45	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	10	—	ns
Write Pulse Width	t_{WPW}	20	—	25	—	35	—	ns
Data Setup Time	t_{DS}	10	—	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns
Effective Write Pulse Width After Full Flag High	t_{WPF}	20	—	25	—	35	—	ns

• Reset Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	30	—	35	—	45	—	ns
Reset Pulse Width	t_{RS}	20	—	25	—	35	—	ns
Reset Setup Time	t_{RSS}	0	—	0	—	0	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	10	—	ns

• Retransmit Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	30	—	35	—	45	—	ns
Retransmit Pulse Width	t_{RT}	20	—	20	—	35	—	ns
Retransmit Setup Time	t_{RTS}	0	—	0	—	0	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	10	—	ns

• Flag Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	20	—	25	—	35	ns
Reset to Full Flag High	t_{FFH}	—	20	—	25	—	35	ns
Reset to Half-Full Flag High	t_{HFH}	—	30	—	35	—	45	ns
Read Low to Empty Flag Low	t_{REF}	—	20	—	25	—	35	ns
Read High to Full Flag High	t_{RFF}	—	20	—	25	—	35	ns
Write High to Empty Flag High	t_{WEF}	—	20	—	25	—	35	ns
Write Low to Full Flag Low	t_{WFF}	—	20	—	25	—	35	ns
Write Low to Half-Full Flag Low	t_{WHF}	—	30	—	35	—	45	ns
Read High to Half-Full Flag High	t_{RHF}	—	30	—	35	—	45	ns

• Expansion Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Expansion in Setup to Write or Read	t_{EFL}	—	15	—	20	—	30	ns
Expansion in Recovery Time	t_{RFF}	—	15	—	20	—	30	ns
Expansion in Pulse Width	t_{WHF}	10	—	10	—	10	—	ns
Expansion Out High Delay From Clock	t_{REF}	10	—	10	—	10	—	ns
Expansion Out Low Delay From Clock	t_{RFF}	10	—	10	—	15	—	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and half-full ($\overline{HF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Half-full flag ($\overline{HF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

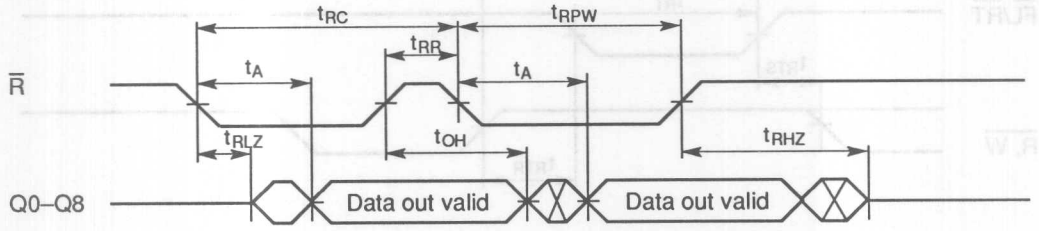
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 2k × 9 as (N) × (2k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

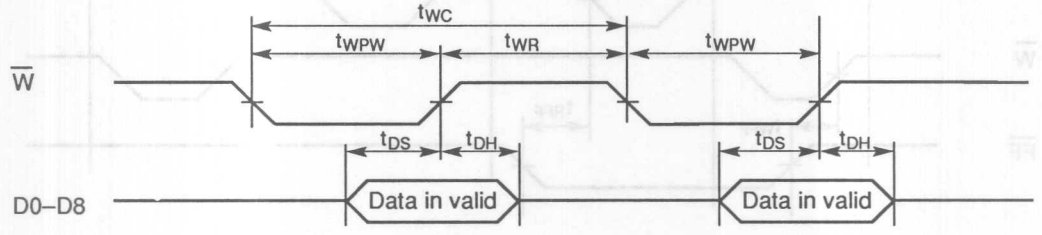
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

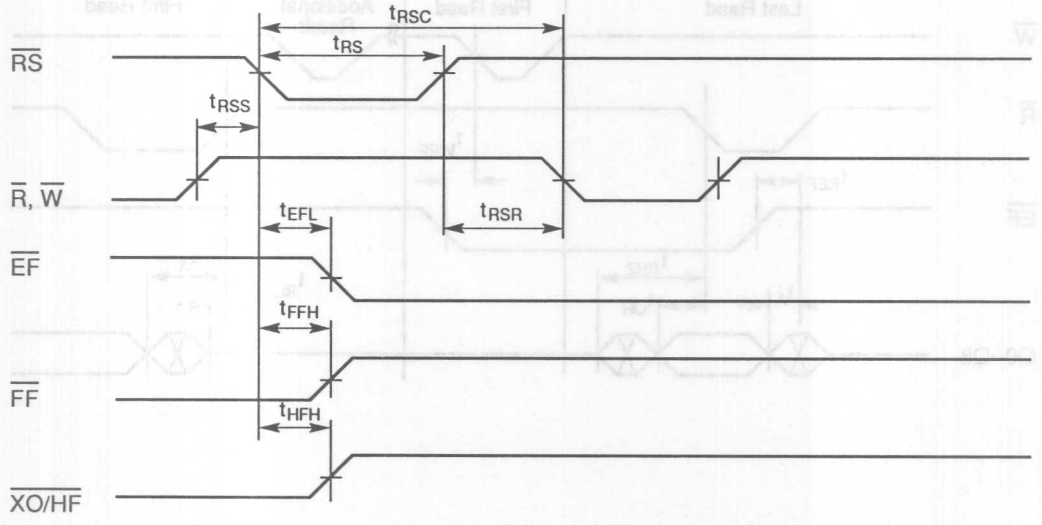
• Read Cycle



• Write Cycle



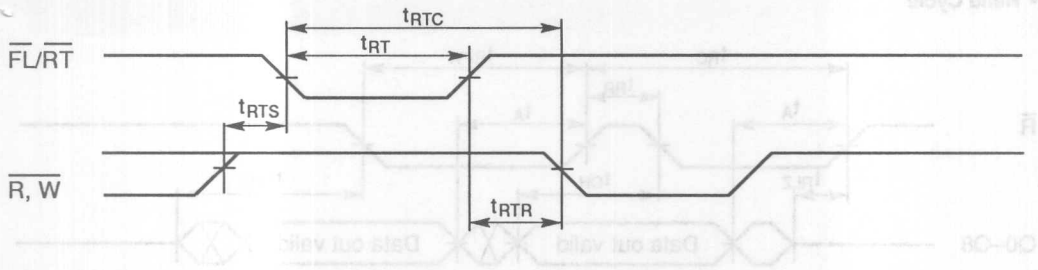
• Reset Cycle



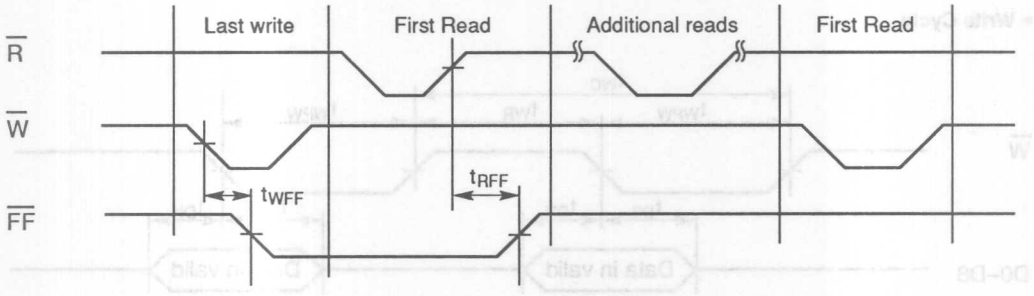
NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.

2. $t_{RSC} = t_{RST}, t_{RSR}$.

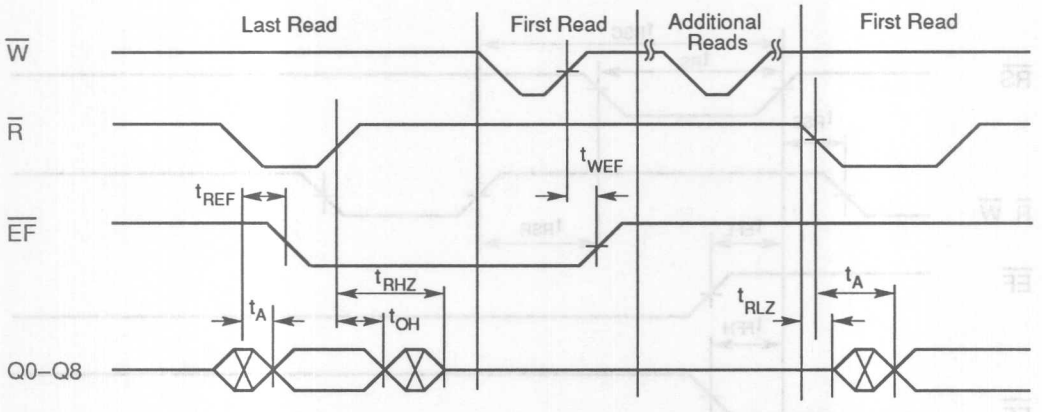
• **Retransmit Cycle**



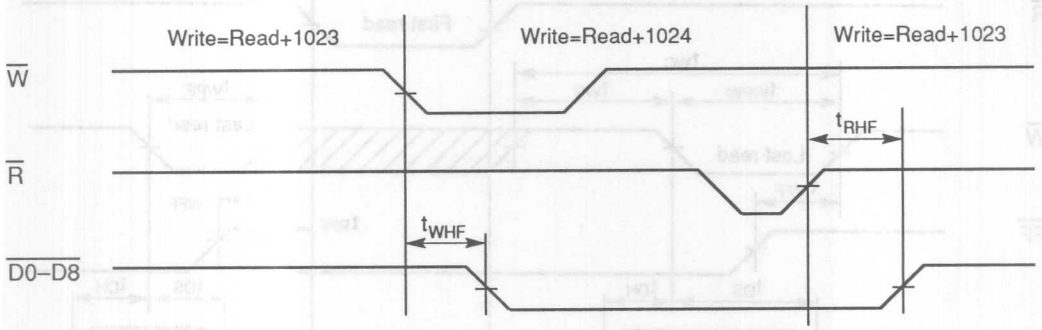
• **Full-Flag Cycle** (From Last Write to First Read)



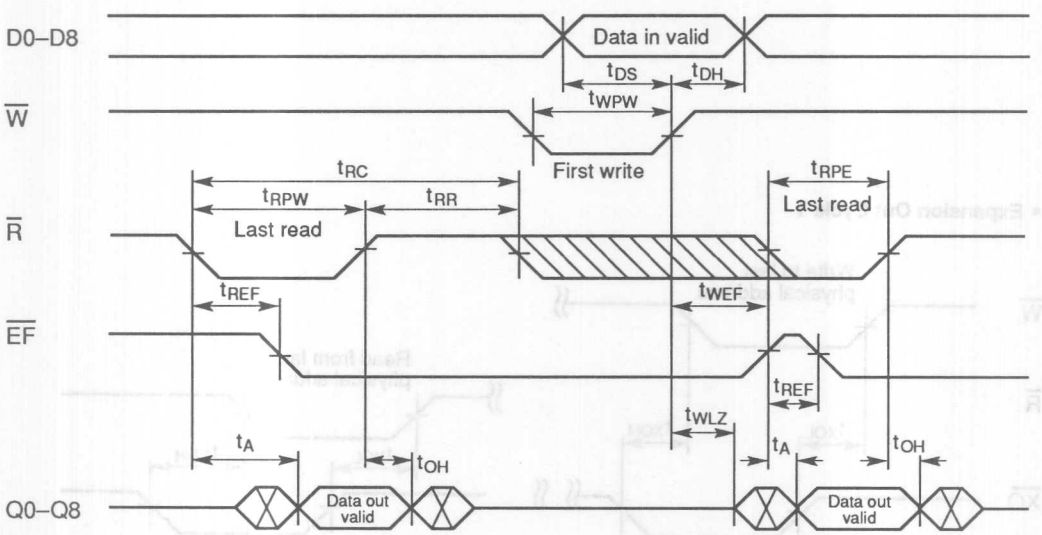
• **Empty-Flag Cycle** (From Last Read to First Write)



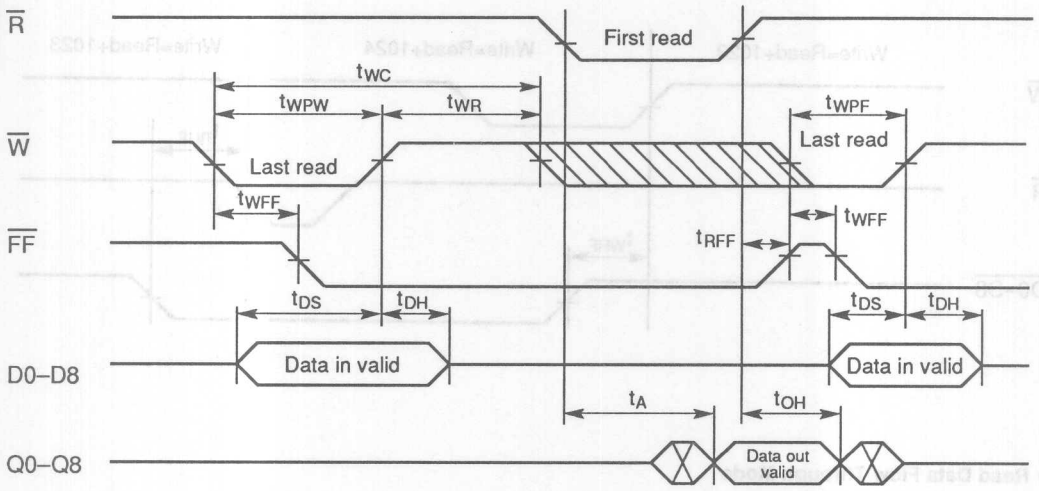
• **Half-Full Flag Cycle**



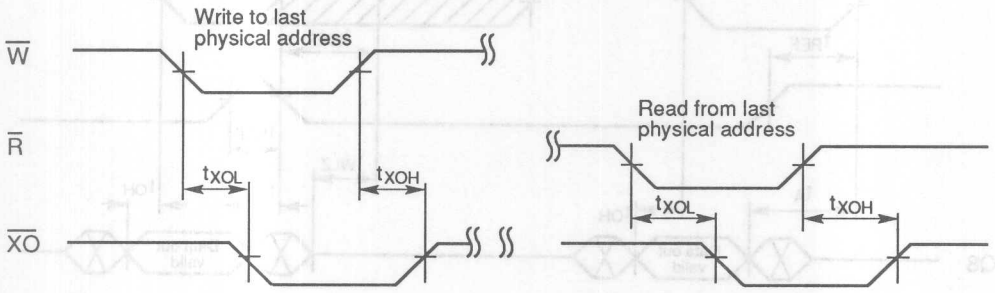
• **Read Data Flow Through Mode**



• **Write Data Flow Through Mode**

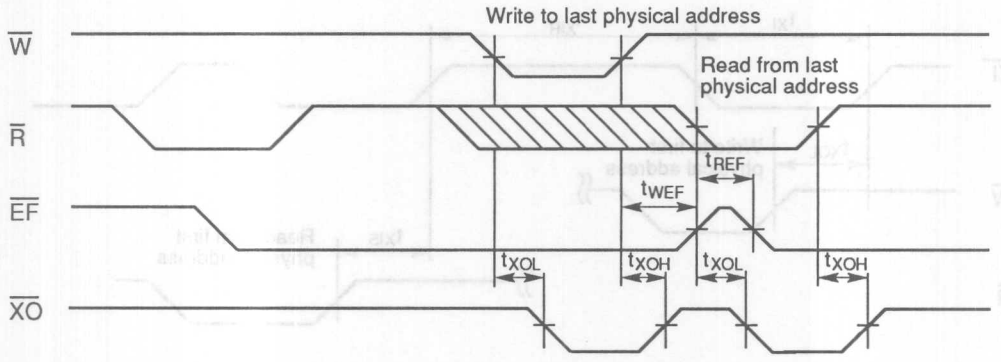


• **Expansion Out Cycle 1**

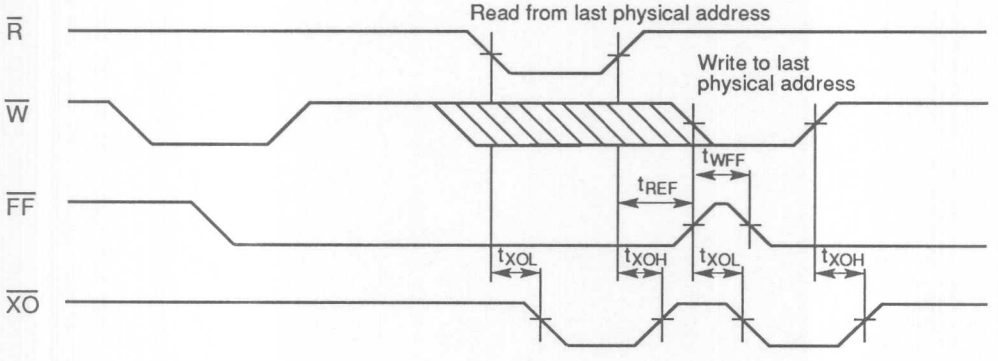


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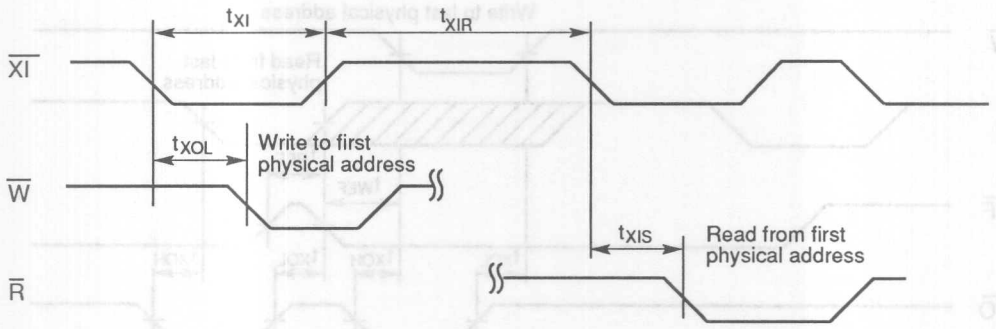
• **Expansion Out Cycle 2** (Read Data Flow Through Mode)



• **Expansion Out Cycle 3** (Write Data Flow Through Mode)



- **Expansion In Cycle**



HM63941-25/35/45 — Preliminary

4K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63941 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and almost-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

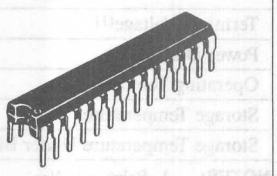
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 35/45/60ns. Organization of HM63941 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 4k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (±10%) Power Supply
- Empty and Full Warning Flags
- Almost-Full Flag
- Access Time 25/35/45ns
- Package. . . . . .28-pin DIP Package

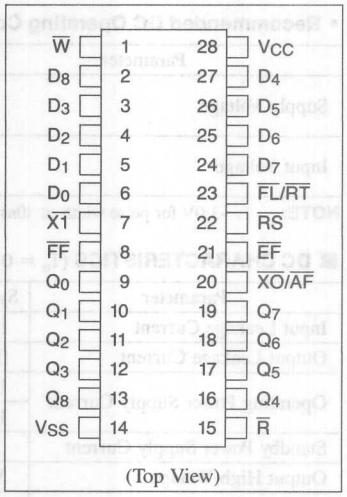
■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63941P-25	25ns	28-pin Plastic DIP
HM63941P-35	35ns	
HM63941P-45	45ns	



(DP-28NA)

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0–D_8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{AF}$	Almost-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q_0–Q_8	Data outputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	−0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. −3.5V for pulse width ≤ 10ns.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	—	6.0	V
	V_{IL}	−0.5(1)	—	0.8	V

NOTE: 1. −3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V − V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V − V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	—	—	80	mA
	I_{CC2}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	—	—	10	mA
Standby Power Supply Current	I_{SB}	All Inputs ≥ V_{CC} − 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

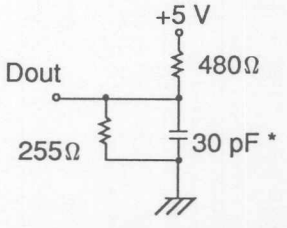
■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	TBD	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	TBD	pF

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



Output Load

*Including scope and jig.

• Read Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	60	—	ns
Access Time	t_A	—	25	—	35	—	45	ns
Read Recovery Time	t_{RR}	10	—	10	—	15	—	ns
Read Pulse Width	t_{RPW}	25	—	35	—	45	—	ns
Read Low to DB Low Z	t_{RLZ}	5	—	5	—	10	—	ns
Read High to DB High Z	t_{RHZ}	—	15	—	20	—	25	ns
Data Valid from Read High	t_{OH}	5	—	5	—	5	—	ns

• Write Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	60	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	15	—	ns
Write Pulse Width	t_{WPW}	20	—	35	—	45	—	ns
Data Setup Time	t_{DS}	15	—	20	—	25	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns

• Reset Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	35	—	45	—	60	—	ns
Reset Pulse Width	t_{RS}	25	—	35	—	45	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	15	—	ns

• Retransmit Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	35	—	45	—	60	—	ns
Retransmit Pulse Width	t_{RT}	20	—	35	—	45	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	15	—	ns

• Flag Timing

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	30	—	45	—	60	ns
Read Low to Empty Flag Low	t_{REF}	—	25	—	35	—	45	ns
Read High to Full Flag High	t_{RFF}	—	25	—	35	—	45	ns
Write High to Empty Flag High	t_{WEF}	—	25	—	35	—	45	ns
Write Low to Full Flag Low	t_{WFF}	—	25	—	35	—	45	ns
Write Low to Almost-Full Low	t_{WAF}	—	30	—	40	—	55	ns
Read High to Almost-Full High	t_{RAF}	—	30	—	40	—	55	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and almost-full ($\overline{AF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Almost-full flag ($\overline{AF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

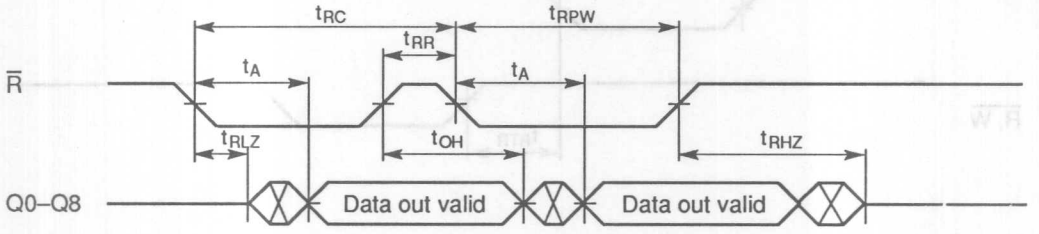
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 4k × 9 as (N) × (4k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

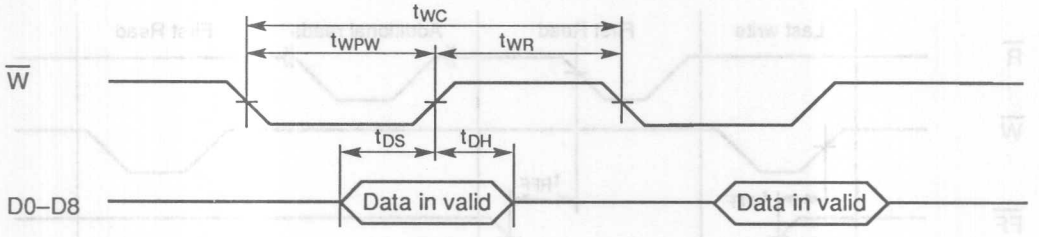
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

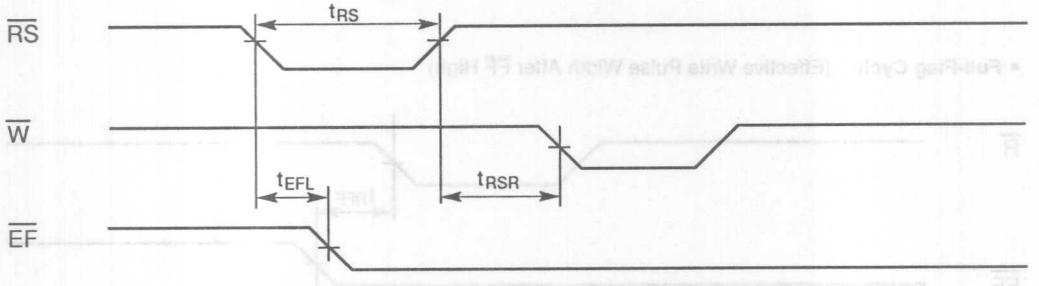
• **Read Cycle**



• **Write Cycle**



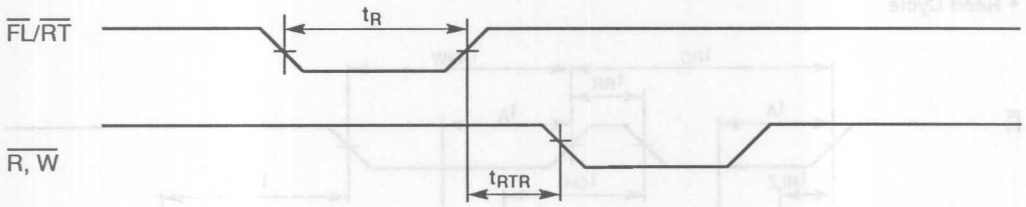
• **Reset Cycle**



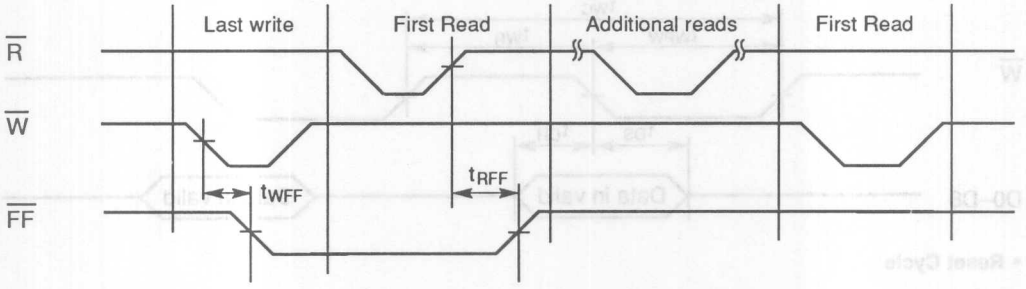
NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.

2. $t_{RSC} = t_{RST}, t_{RSR}$.

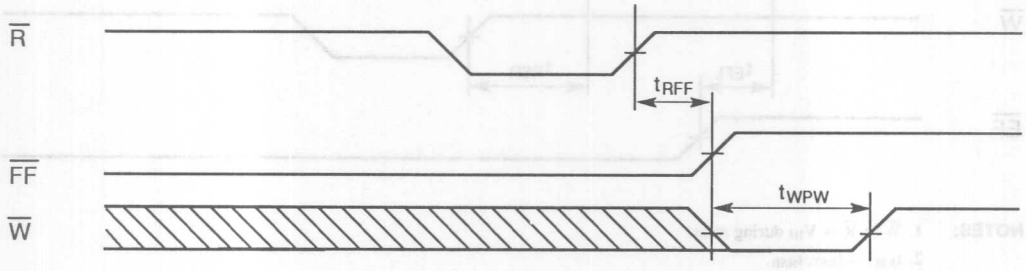
• **Retransmit Cycle**



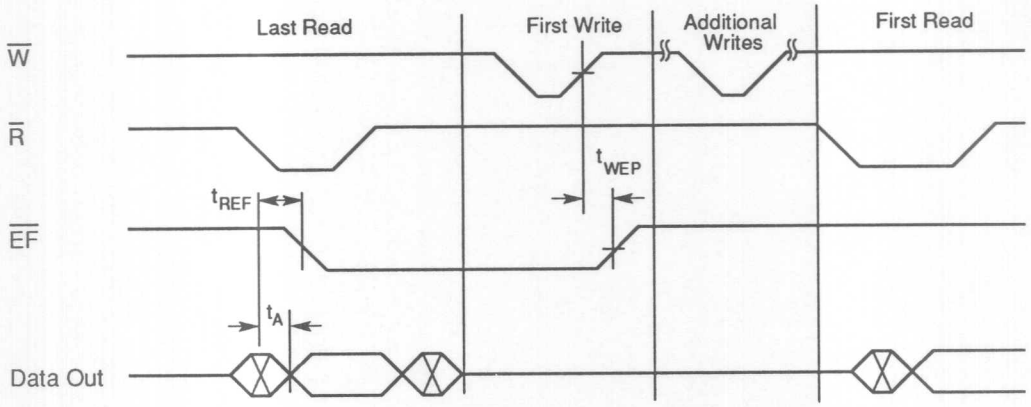
• **Full-Flag Cycle** (From Last Write to First Read)



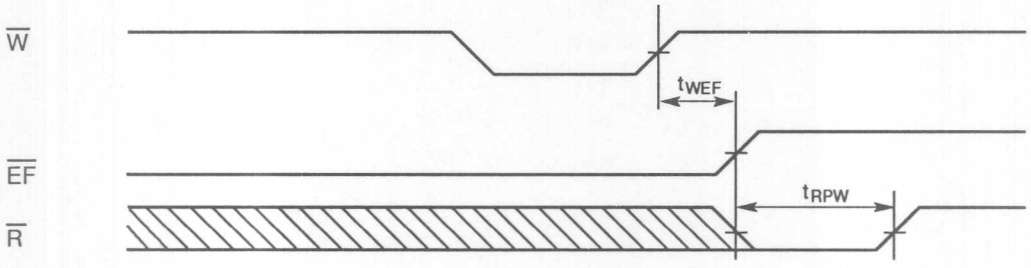
• **Full-Flag Cycle** (Effective Write Pulse Width After $\overline{FF}$ High)



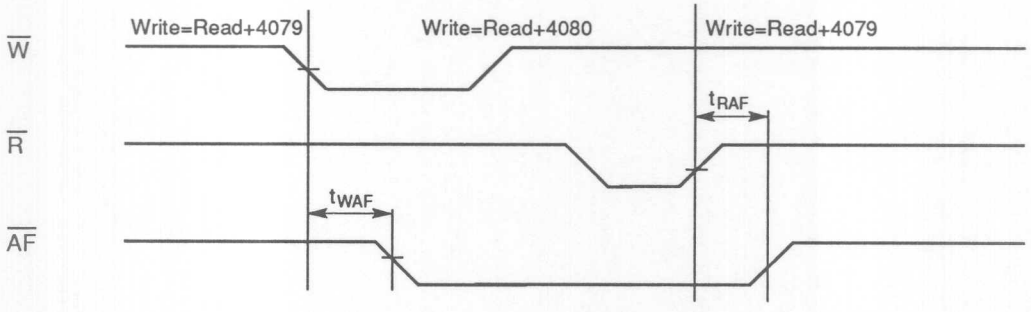
• **Empty-Flag Cycle** (From Last Write to First Read)



• **Empty-Flag Cycle** (Effective Read Pulse Width After $\overline{EF}$ High)



• **Almost-Full Flag Cycle**



2

Section 2
Cache Static RAM
and
Fast SRAM Modules

HITACHI®

HM62A168/HM62A188 Series — Preliminary

Direct Mapped 8,192-Word × 16/18-Bit
2-Way 4,096-Word × 16/18-Bit Static Cache RAM

■ DESCRIPTION

The Hitachi HM62A168/HM62A188 is a high speed 128/144-kbit static cache RAM organized as 2-way set associative 4k × 16/18 or direct mapped 8k × 16/18. By using two HM62A168/HM62A188 with Intel's 82385 cache controller a high performance 80386 system can be achieved.

The HM62A168/HM62A188, packaged in a 52-pin PLCC is available for high density mounting.

■ FEATURES

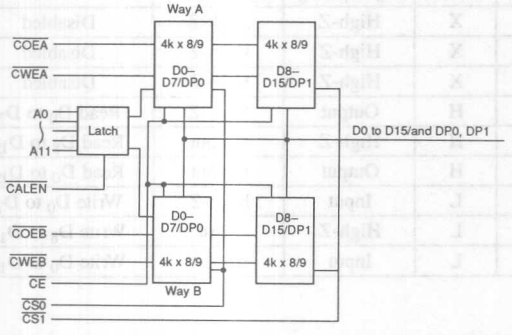
- Meets INTEL 82385 cache memory controller
- High Speed
  Access Time . . . . . .25/35/45ns (max.)
- Address Latch
- Pin Programmable for 8k × 16/18 or 2-Way 4k × 16/18

■ ORDERING INFORMATION

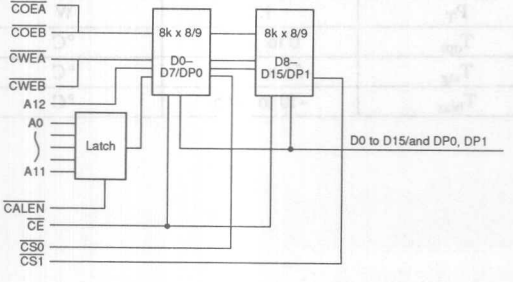
Type No.	Access	Package
HM62168CP-25	25ns	52-pin PLCC
HM62168CP-35	35ns	
HM62168CP-45	45ns	
HM62188CP-25	25ns	52-pin PLCC
HM62188CP-35	35ns	
HM62188CP-45	45ns	

■ BLOCK DIAGRAM

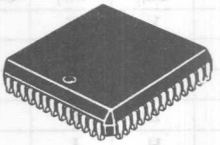
Topology Two-Way Set Associative (MODE = Logic Low)



Topology Direct Map (MODE = Logic Low)



■ PIN-OUT

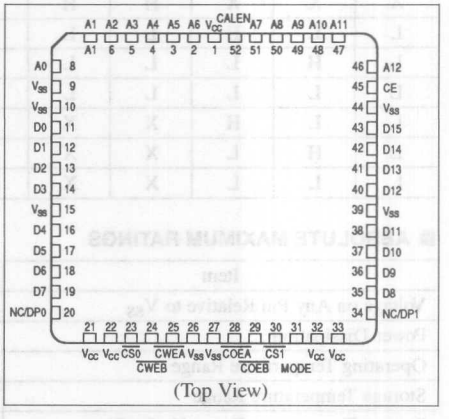


(CP-52)

■ PIN DESCRIPTION

Pin Name	Function
CALEN	Cache Address Latch Enable
MODE	Mode Select
A_0 to A_{12}	Address
$\overline{CS_0}$, $\overline{CS_1}$	Cache Chip Select
$\overline{COEA}$, $\overline{COEB}$	Cache Output Enable
$\overline{CWEA}$, $\overline{CWEB}$	Cache Write Enable
D_0 to D_{15}	Data Input/Output
$\overline{CE}$	Cache Chip Enable
NC/DP_0, DP_1	No connection Parity Input/Output

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

• Two-Way Mode (Mode = High) 2-4K × 16/18

Input Signal							I/O Pin		Function
$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D_0–D_7/DP_0	D_8–D_{15}/DP_1	
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
L	L	H	L	H	H	H	Output	High-Z	Read Way A
L	L	H	H	L	H	H	Output	High-Z	Read Way B
L	H	L	L	H	H	H	High-Z	Output	Read Way A
L	H	L	H	L	H	H	High-Z	Output	Read Way B
L	L	L	L	H	H	H	Output	Output	Read Way A
L	L	L	H	L	H	H	Output	Output	Read Way B
L	L	H	X	X	L	H	Input	High-Z	Write Way A
L	L	H	X	X	H	L	Input	High-Z	Write Way B
L	H	L	X	X	L	H	High-Z	Input	Write Way A
L	H	L	X	X	H	L	High-Z	Input	Write Way B
L	L	L	X	X	L	H	Input	Input	Write Way A
L	L	L	X	X	H	L	Input	Input	Write Way B
L	L	H	X	X	L	L	Input	High-Z	Write Way A & B
L	H	L	X	X	L	L	High-Z	Input	Write Way A & B
L	L	L	X	X	L	L	Input	Input	Write Way A & B

• Direct Mode (Mode = Low) 8K × 16/18

Input Signal							I/O Pin		Function
$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D_0–D_7/DP_0	D_8–D_{15}/DP_1	
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Disabled
L	L	H	L	L	H	H	Output	High-Z	Read D_0 to D_7
L	H	L	L	L	H	H	High-Z	Output	Read D_8 to D_{15}
L	L	L	L	L	H	H	Output	Output	Read D_0 to D_{15}
L	L	H	X	X	L	L	Input	High-Z	Write D_0 to D_7
L	H	L	X	X	L	L	High-Z	Input	Write D_8 to D_{15}
L	L	L	X	X	L	L	Input	Input	Write D_0 to D_{15}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	−0.5[1] to +7.0	V
Power Dissipation	P_T	1.2	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: 1. V_{in} min. = −2.5V for pulse width ≤ 10ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low (Logic 0) Voltage	V_{IL}	–0.3[1]	—	0.8	V

NOTE: 1. V_{IL} min. = –2.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.[1]	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	—	—	2.0	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10.0	μA
Operating Power Supply Current	I_{CC}	V_{in} = 0V/V_{CC}, $I_{I/O}$ = 0mA Min. Cycle, Duty = 100%	—	—	220	mA
Output Low Voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –1.0mA	2.4	—	—	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

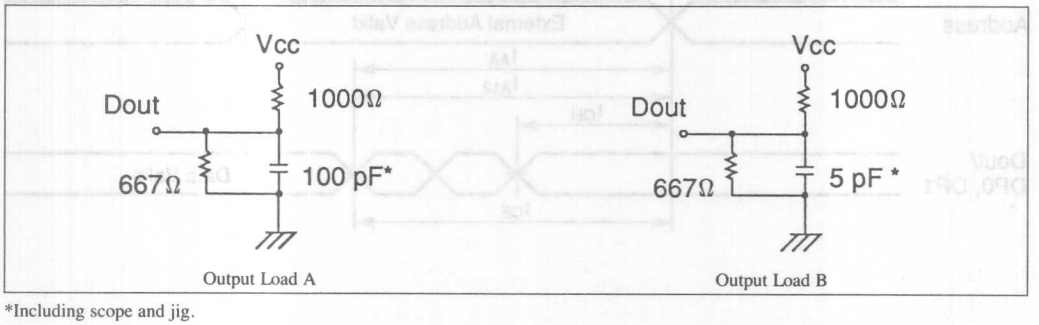
■ CAPACITANCE (T_a = 25°C, f = 1MHz)[1]

Parameter	Symbol	Max.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

- **Test Conditions**
  - Input Pulse Levels: V_{SS} to 3.0V
  - Input and Output Timing Reference Levels: 1.5V
  - Input Rise and Fall Times: 3ns
  - Output Load: See Figures



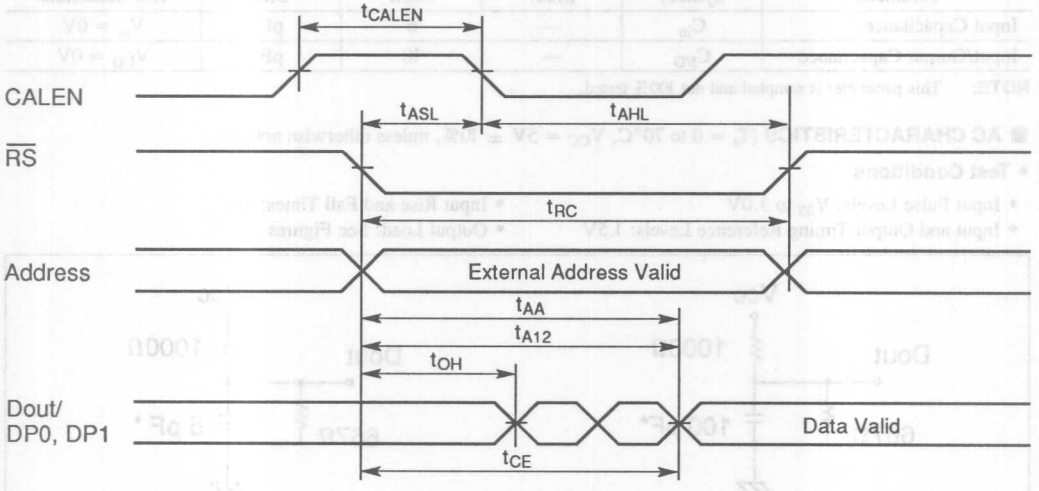
Output Load A　　Output Load B

*Including scope and jig.

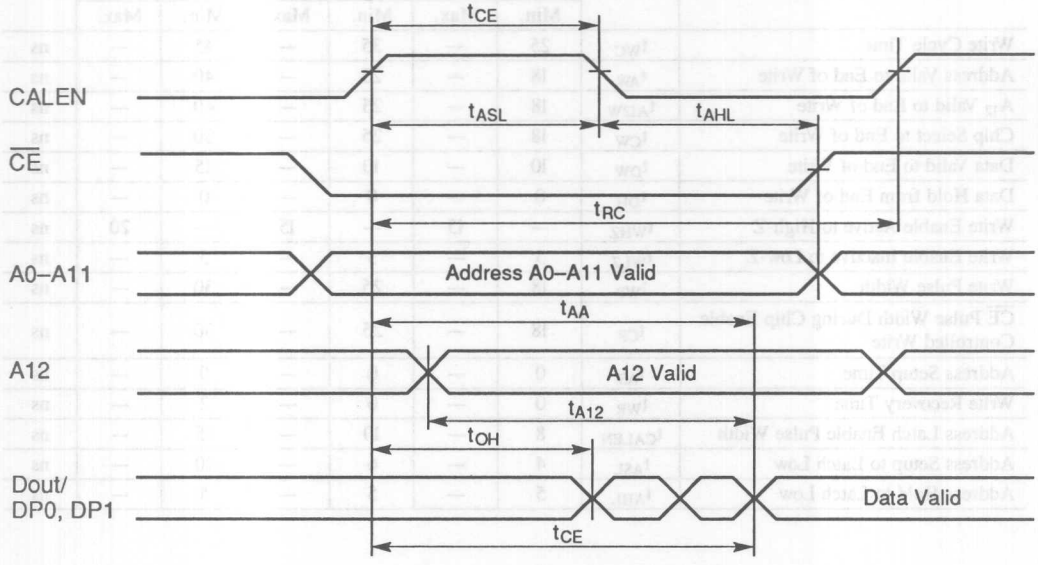
• Read Cycle

Parameter	Symbol	HM62168-25 HM62188-25		HM62168-35 HM62188-35		HM62168-45 HM62188-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
A_{12} Address Access Time	t_{A12}	—	17	—	25	—	30	ns
Chip Select Access Time	t_{CS}, t_{CE}	—	20	—	25	—	30	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	16	ns
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	t_{LZ}	3	—	3	—	3	—	ns
Output Enable to Output Low-Z	t_{OLZ}	2	—	2	—	2	—	ns
Chip Deselect to Output in High-Z	t_{HZ}	—	15	—	25	—	30	ns
Output Disable to Output High-Z	t_{OHZ}	—	10	—	14	—	14	ns
Address Latch Enable Pulse Width	t_{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t_{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	ns

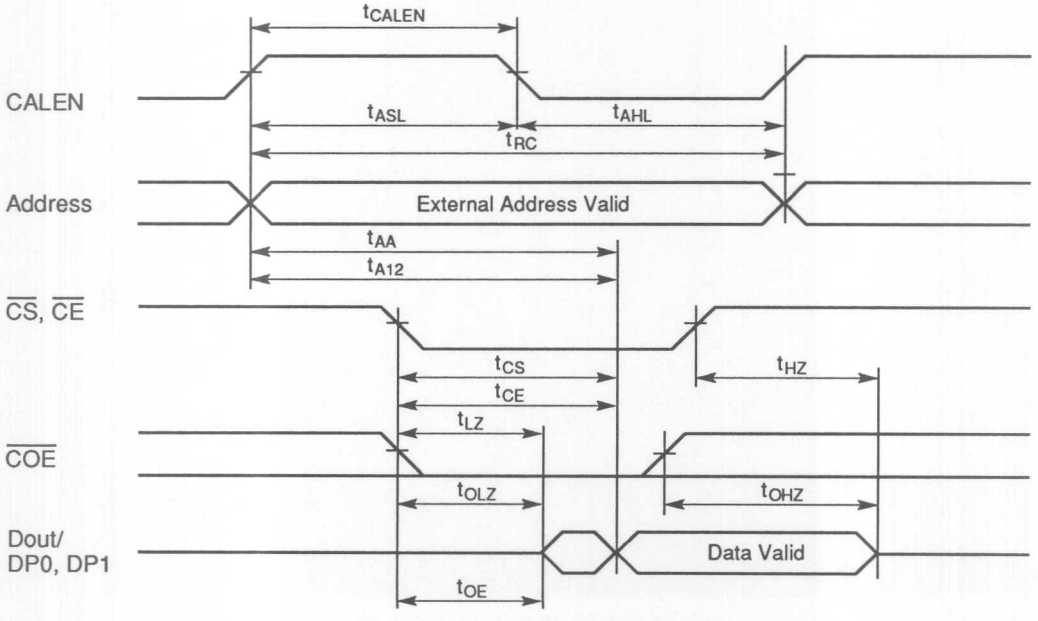
• Read Timing Waveform (1) ($\overline{CWE}$ = High, $\overline{COE}$ = Low, $\overline{CS}$ = Low)



• **Read Timing Waveform (2)** ($\overline{CWE}$ = High, $\overline{COE}$ = Low, $\overline{CS}$ = Low)



• **Read Timing Waveform (3)** ($\overline{CWE}$ = High)

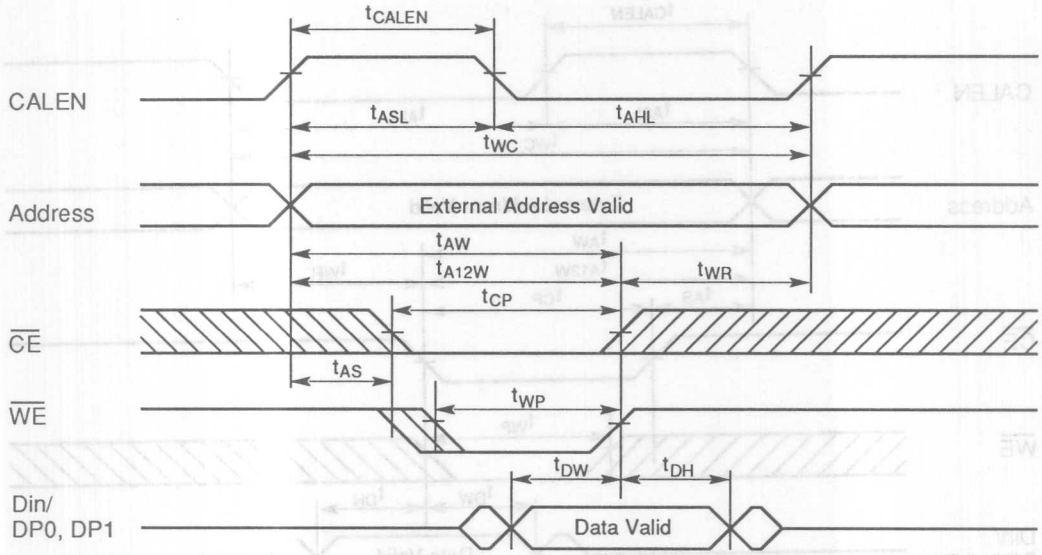


• Write Cycle

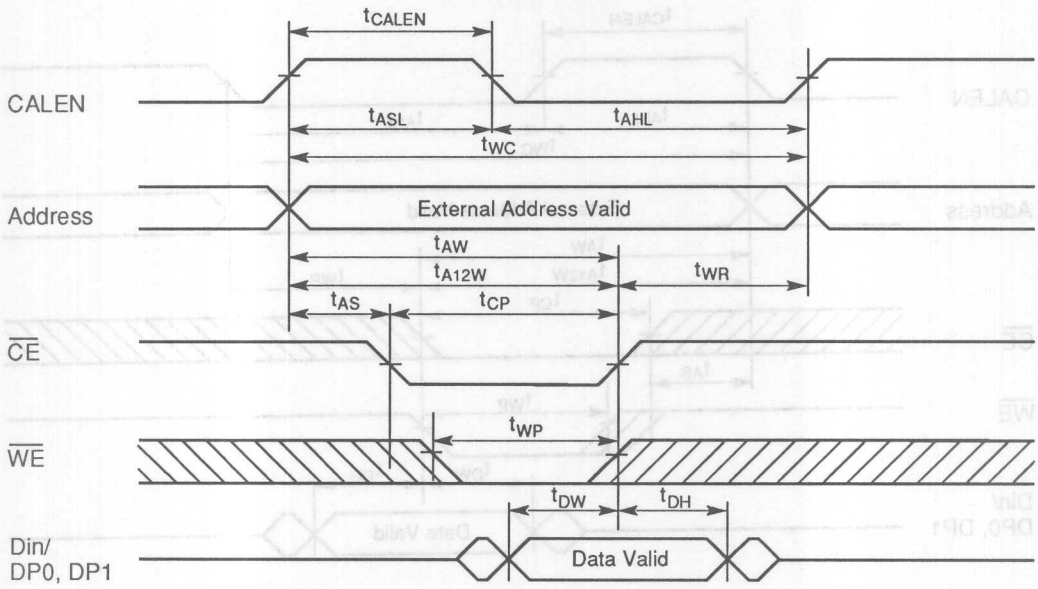
Parameter	Symbol	HM62168-25 HM62188-25		HM62168-35 HM62188-35		HM62168-45 HM62188-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Address Valid to End of Write	t_{AW}	18	—	25	—	40	—	ns
A_{12} Valid to End of Write	t_{A12W}	18	—	25	—	40	—	ns
Chip Select to End of Write	t_{CW}	18	—	25	—	30	—	ns
Data Valid to End of Write	t_{DW}	10	—	10	—	15	—	ns
Data Hold from End of Write	t_{DH}	0	—	0	—	0	—	ns
Write Enable Active to High-Z	t_{WHZ}	—	15	—	15	—	20	ns
Write Enable Inactive to Low-Z	t_{WLZ}	3	—	3	—	3	—	ns
Write Pulse Width	t_{WP}	18	—	25	—	30	—	ns
$\overline{CE}$ Pulse Width During Chip Enable Controlled Write	t_{CP}	18	—	25	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	2	—	ns
Address Latch Enable Pulse Width	t_{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t_{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	ns

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• **Write Timing Waveform (1)** ($\overline{COE}$ = High, $\overline{WE}$ Controlled)



• **Write Timing Waveform (2)** ($\overline{COE}$ = High, $\overline{CE}$ Controlled)



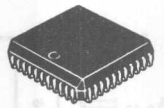
HM67C932 Series — Preliminary

8,192-Word × 9-Bit × 4-Row Static Cache RAM

■ DESCRIPTION

The Hitachi HM67C932 is a high speed 288-kbit static cache RAM organized as 4-way set associative 8k × 9 or direct mapped 32k × 9 with 4-row selector for burst mode. By using HM67C932 with high speed standard microprocessors a high performance computer system can be achieved.

The HM67C932, packaged in a 44-pin PLCC is available for high density mounting.



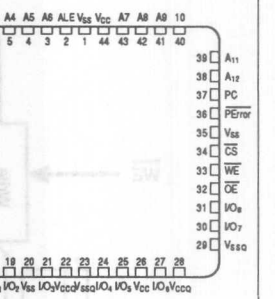
(CP-44)

■ FEATURES

- For High Speed Standard Microprocessors
- High Speed Access Capability with Lower 2-address by Selector
- Pipeline Access Capability with On Chip Address and Row Latches (Edge Trigger Type Row Latch)*
- On Chip Parity Generator and Checker
- Organization.....288-kbit (8-kw × 9 bit × 4 row)
- Drivability for Heavy Load (C_L = 100 pF) ⚠
- PLCC 44-pin
- TTL I/O

*For cache RAM with transparent row latch, request data sheet HM67B932.

■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM67C932CP-20	20ns	44-pin PLCC
HM67C932CP-25	25ns	

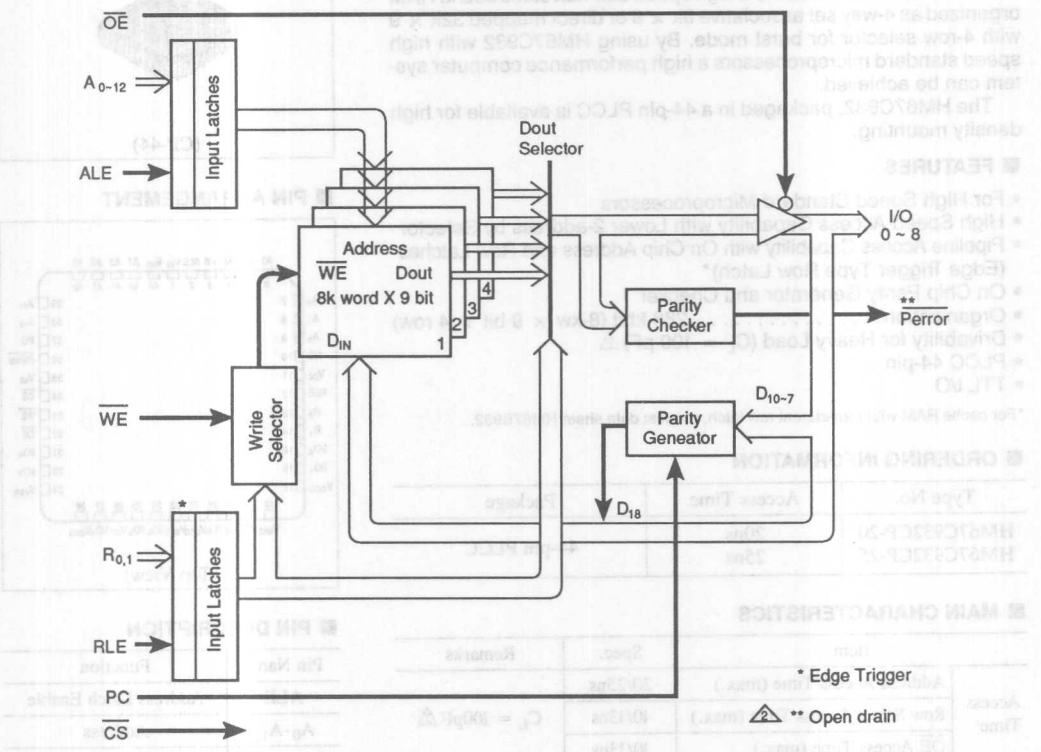
■ MAIN CHARACTERISTICS

Item		Spec.	Remarks
Access Time	Address Access Time (max.)	20/25ns	C_L = 100pF ⚠
	Row Select Access Time (max.)	10/13ns	
	$\overline{OE}$ Access Time (max.)	10/13ns	
Cycle Time (min.)		25/30ns	Clock Frequency 33 ~ 40 MHz
Power Dissipation (typ.)		0.8W	V_{CC} = 5.0V t_{CYC} = 60ns

■ PIN DESCRIPTION

Pin Name	Function
ALE	Address Latch Enable
A_0–A_{12}	Address
RLE	Row Latch Enable (Edge Trigger)
R_0–R_1	Row
I/O_0–I/O_7	Data Input/Output
I/O_8	Data Input/Output (Even Parity)
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PC	Parity Control
$\overline{PError}$	Parity Error Output (Open Drain)
V_{CC}	Power
V_{SS}	Ground
V_{CCQ}	Power (For Output Transistors)
V_{SSQ}	Ground (For Output Transistors)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

• Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	PC	Mode	V_{CC} Current	I/O Pin	$\overline{PError}$ Pin	Ref. Cycle
H	X	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	High Z	
L	H	H	X	Output Disabled	I_{CC}, I_{CC1}	High Z	High Z	
L	L	H	X	Read	I_{CC}, I_{CC1}	D_{out}	High Z or L (Error)	Read Cycle No. 1, 2
L	H	L	L	Write	I_{CC}, I_{CC1}	D_{in}	High Z	Write Cycle No. 1–5
L	L	L	L	Write	I_{CC}, I_{CC1}	D_{in}	High Z	Write Cycle No. 6, 7
L	H	L	H	Write (Parity Generate)	I_{CC}, I_{CC1}	D_{in}(1)	High Z	Write Cycle No. 1
L	L	L	H	Write (Parity Generate)	I_{CC}, I_{CC1}	D_{in}(1)	High Z	

NOTE: 1. D_{I8} input is ignored and generated as parity bit from D_{I0} to D_{I7}.

• Input Latch Table

• Address Latch

ALE	Mode	Latch Output
H	Load	Address Input
L	Hold	Previous Address

• Row Latch

RLE	Mode	Latch Output
↑	Load	Row Input
H or L	Hold	Previous Row

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (With Bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	−0.5(1)	—	0.8	V

NOTE: 1. −3.0V for pulse width ≤ 20ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to +70°C, V_{SS} = 0V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	—	TBD	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	TBD	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	TBD	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V	—	—	TBD	mA
Output Low Voltage	V_{OL}(1)	I_{OL} = 16mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −8mA	2.4	—	—	V
		I_{OH} = −100μA	2.7	—	—	V

NOTE: 1. Including $\overline{PError}$ Output.

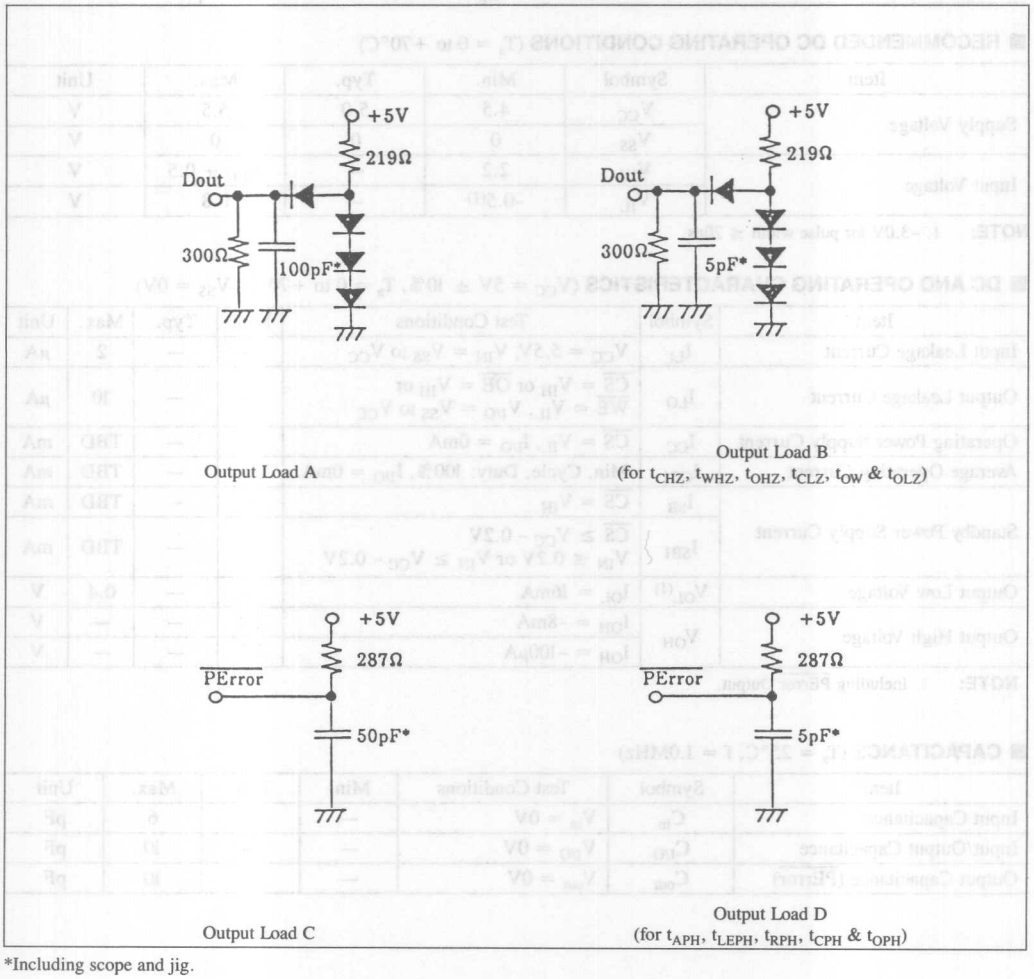
■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF
Output Capacitance ($\overline{PError}$)	C_{out}	V_{out} = 0V	—	—	10	pF

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

• AC Test Conditions

- Input Pulse Levels: 0.4V to 2.4V
- Input Timing Reference Levels: 0.8V, 2.0V
- Output Timing Reference Levels: V_{OL} = 0.8V, V_{OH} = 2.0V
- Input Rise and Fall Times: 4ns
- Output Load: See Figure



Output Load A

Output Load B
(for t_{CHZ}, t_{WHZ}, t_{OHZ}, t_{CLZ}, t_{OW} & t_{OLZ})

Output Load C

Output Load D
(for t_{APH}, t_{LEPH}, t_{RPH}, t_{CPH} & t_{OPH})

*Including scope and jig.

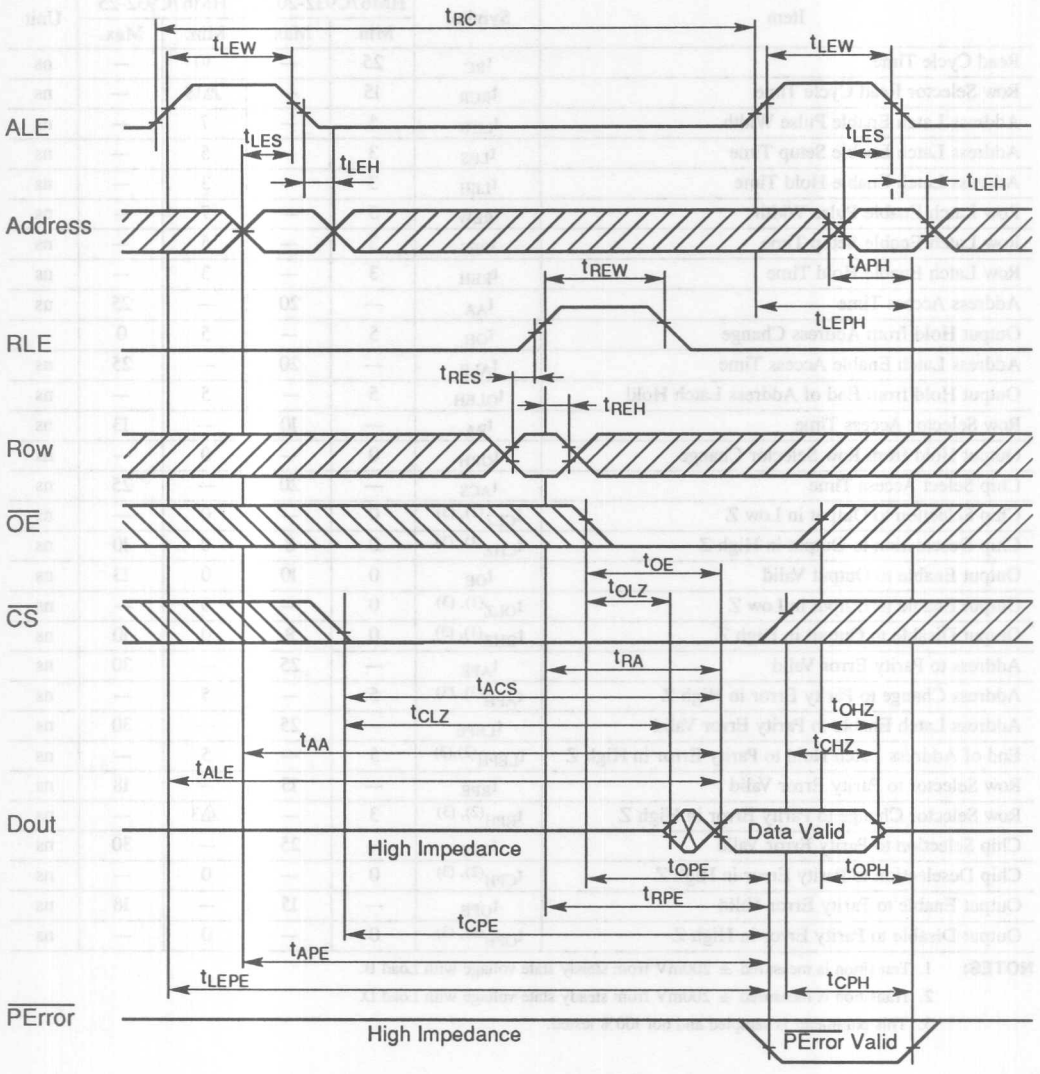
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• Read Cycle

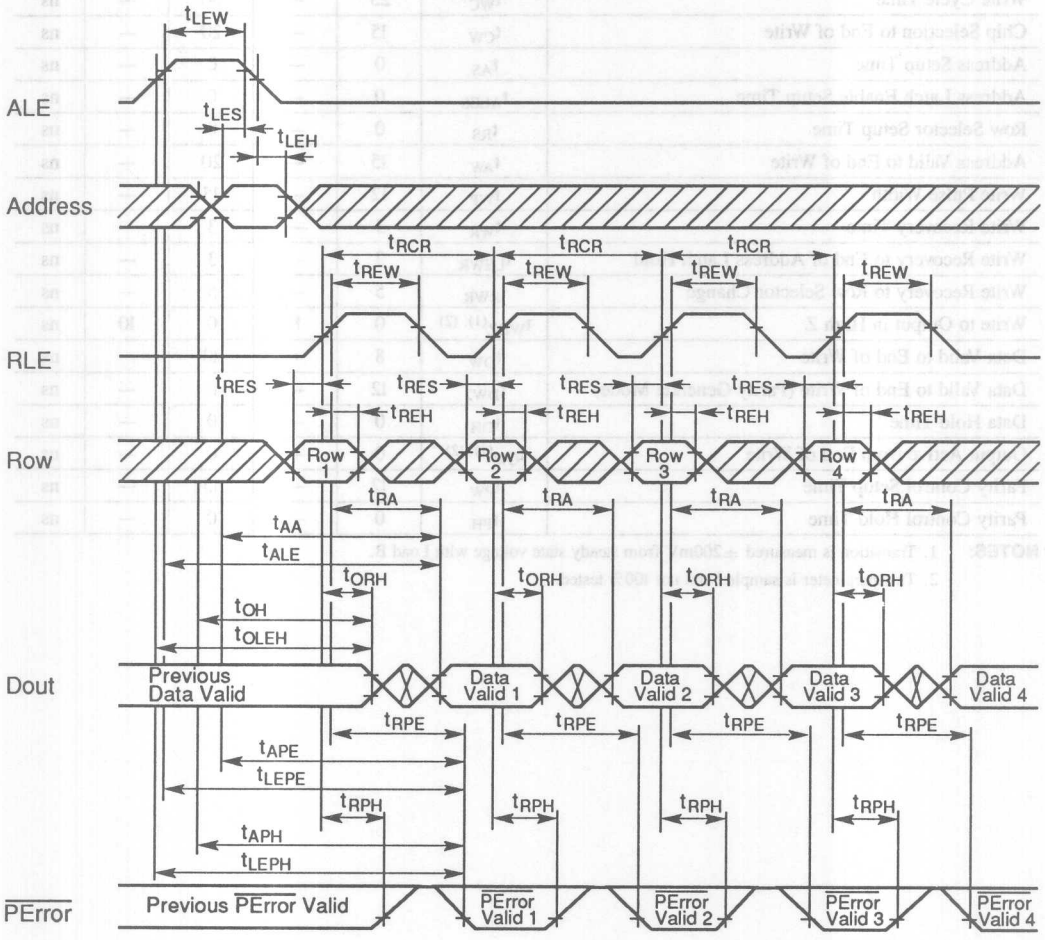
Item	Symbol	HM67C932-20 ⚠		HM67C932-25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Row Selector Read Cycle Time	t_{RCR}	15	—	⚠18	—	ns
Address Latch Enable Pulse Width	t_{LEW}	5	—	7	—	ns
Address Latch Enable Setup Time	t_{LES}	3	—	5	—	ns
Address Latch Enable Hold Time	t_{LEH}	3	—	3	—	ns
Row Latch Enable Pulse Width	t_{REW}	5	—	7	—	ns
Row Latch Enable Setup Time	t_{RES}	3	—	5	—	ns
Row Latch Enable Hold Time	t_{REH}	3	—	3	—	ns
Address Access Time	t_{AA}	—	20	—	25	ns
Output Hold from Address Change	t_{OH}	5	—	5	0	—
Address Latch Enable Access Time	t_{ALE}	—	20	—	25	ns
Output Hold from End of Address Latch Hold	t_{OLEH}	5	—	5	—	ns
Row Selector Access Time	t_{RA}	—	10	—	13	ns
Output Hold from Row Selector Change	t_{ORH}	0	—	0	—	ns
Chip Select Access Time	t_{ACS}	—	20	—	25	ns
Chip Selection to Output in Low Z	$t_{CLZ}^{(1),(3)}$	0	—	0	—	ns
Chip Deselection to Output in High Z	$t_{CHZ}^{(1),(3)}$	0	8	0	10	ns
Output Enable to Output Valid	t_{OE}	0	10	0	13	ns
Output Enable to Output in Low Z	$t_{OLZ}^{(1),(3)}$	0	—	0	—	ns
Output Disable to Output in High Z	$t_{OHZ}^{(1),(3)}$	0	8	0	10	ns
Address to Parity Error Valid	t_{APE}	—	25	—	30	ns
Address Change to Parity Error in High Z	$t_{APH}^{(2),(3)}$	5	—	5	—	ns
Address Latch Enable to Parity Error Valid	t_{LEPE}	—	25	—	30	ns
End of Address Latch Hold to Parity Error in High Z	$t_{LEPH}^{(2),(3)}$	5	—	5	—	ns
Row Selector to Parity Error Valid	t_{RPE}	—	15	—	18	ns
Row Selector Change to Parity Error in High Z	$t_{RPH}^{(2),(3)}$	3	—	⚠3	—	ns
Chip Selection to Parity Error Valid	t_{CPE}	—	25	—	30	ns
Chip Deselection to Parity Error in High Z	$t_{CPH}^{(2),(3)}$	0	—	0	—	ns
Output Enable to Parity Error Valid	t_{OPE}	—	15	—	18	ns
Output Disable to Parity Error in High Z	$t_{OPH}^{(2),(3)}$	0	—	0	—	ns

NOTES: 1. Transition is measured ± 200mV from steady state voltage with Load B.
2. Transition is measured ± 200mV from steady state voltage with Load D.
3. This parameter is sampled and not 100% tested.

• **Timing Waveform of Read Cycle No. 1** (Cache Read Cycle) (1)



• **Timing Waveform of Read Cycle No. 2** (Serial Read Cycle With Row Selector) (1), (2)



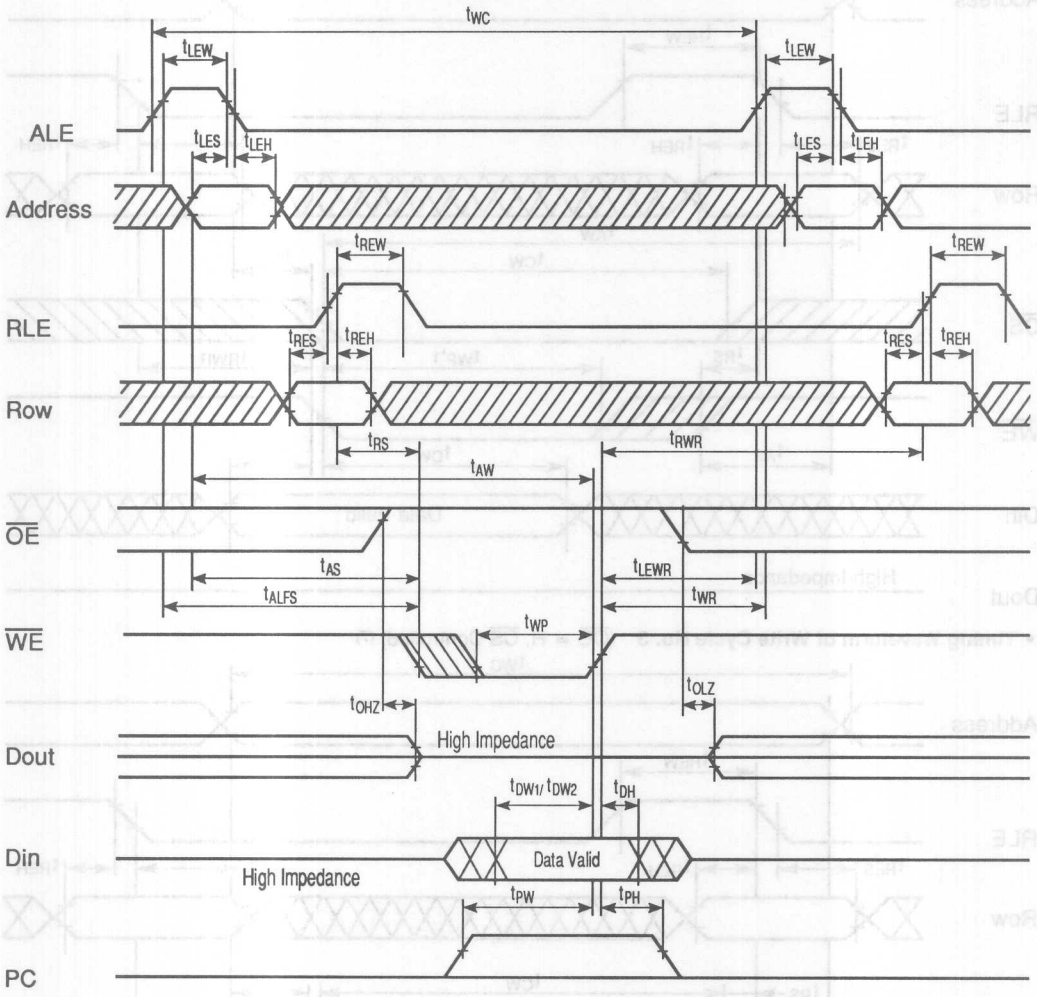
NOTES: 1. $\overline{WE}$ = V_{IH}, PC: Do not care
2. $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL}

• Write Cycle

Item	Symbol	HM67C932-20		HM67C932-25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	15	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Latch Enable Setup Time	t_{ALES}	0	—	0	—	ns
Row Selector Setup Time	t_{RS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	15	—	20	—	ns
Write Pulse Width	t_{WP}	12	—	15	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Write Recovery to End of Address Latch Hold	t_{LEWR}	3	—	3	—	ns
Write Recovery to Row Selector Change	t_{RWR}	5	—	5	—	ns
Write to Output in High Z	t_{WHZ}(1), (2)	0	8	0	10	ns
Data Valid to End of Write	t_{DW}	8	—	10	—	ns
Data Valid to End of Write (Parity Generate Mode)	t_{DW2}	12	—	15	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}(1), (2)	0	—	0	—	ns
Parity Control Setup Time	t_{PW}	12	—	15	—	ns
Parity Control Hold Time	t_{PH}	0	—	0	—	ns

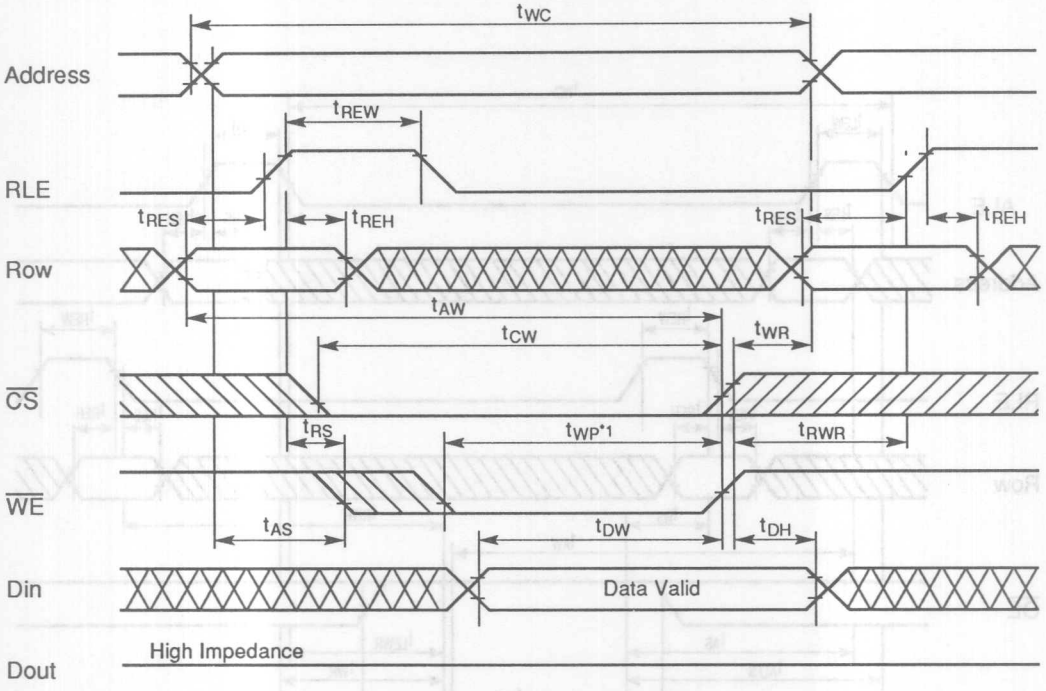
NOTES: 1. Transition is measured ±200mV from steady state voltage with Load B.
2. This parameter is sampled and not 100% tested.

• **Timing Waveform of Write Cycle No. 1** (Cache Write Cycle) (1), (2)

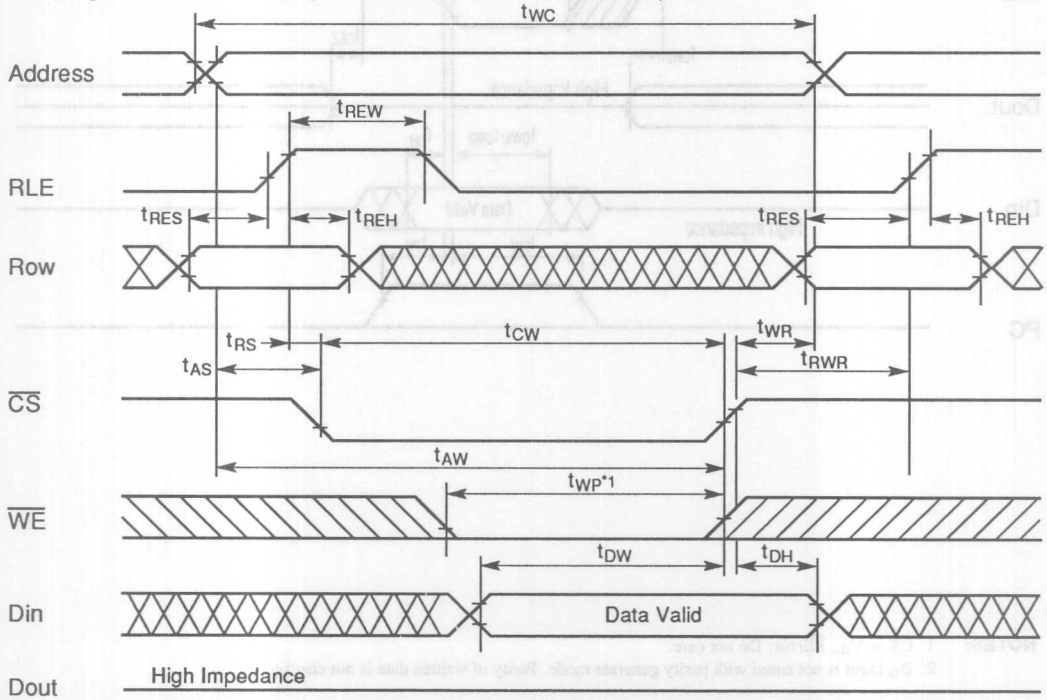


NOTES: 1. $\overline{CS}$ = V_{IL}, $\overline{PError}$: Do not care.
2. D_{I8} input is not cared with parity generate mode. Parity of written data is not checked.

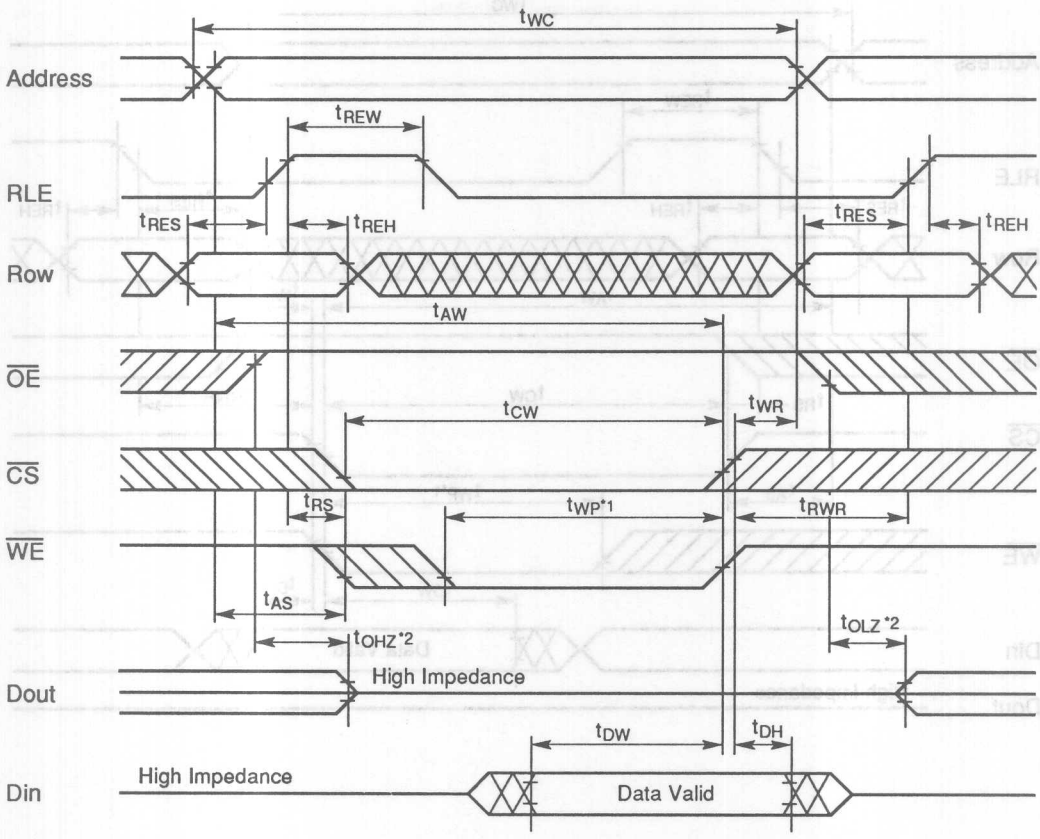
• **Timing Waveform of Write Cycle No. 2** ($\overline{OE}$ = H, $\overline{WE}$ Controlled) (7)



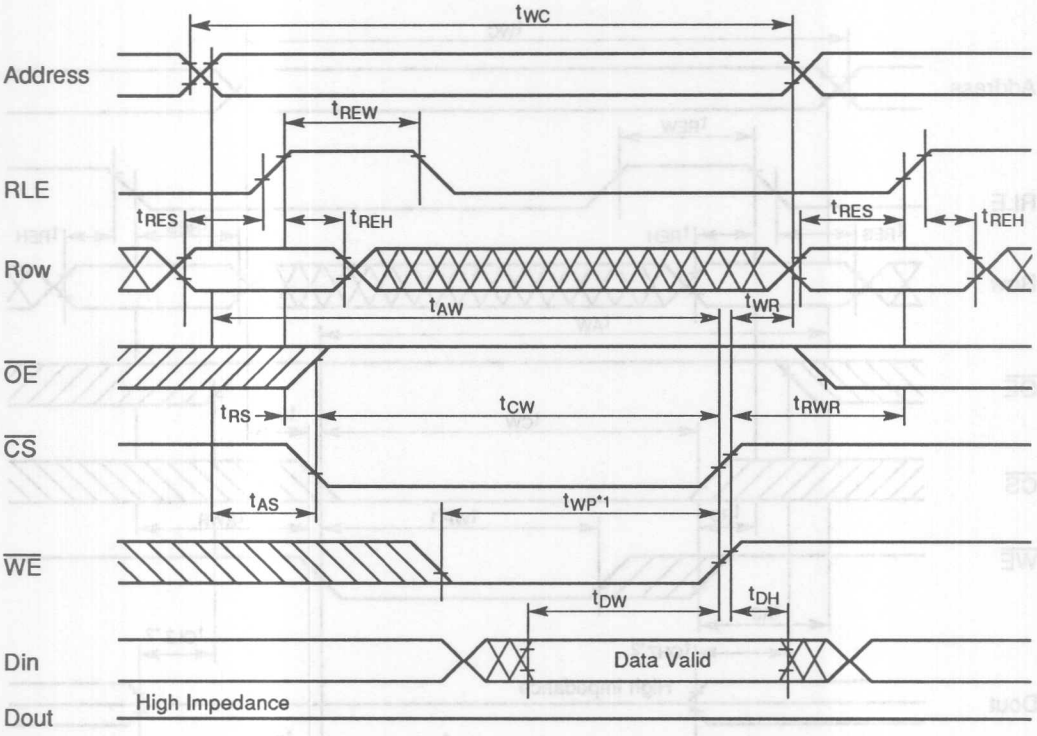
• **Timing Waveform of Write Cycle No. 3** ($\overline{OE}$ = H, $\overline{CS}$ Controlled) (7)



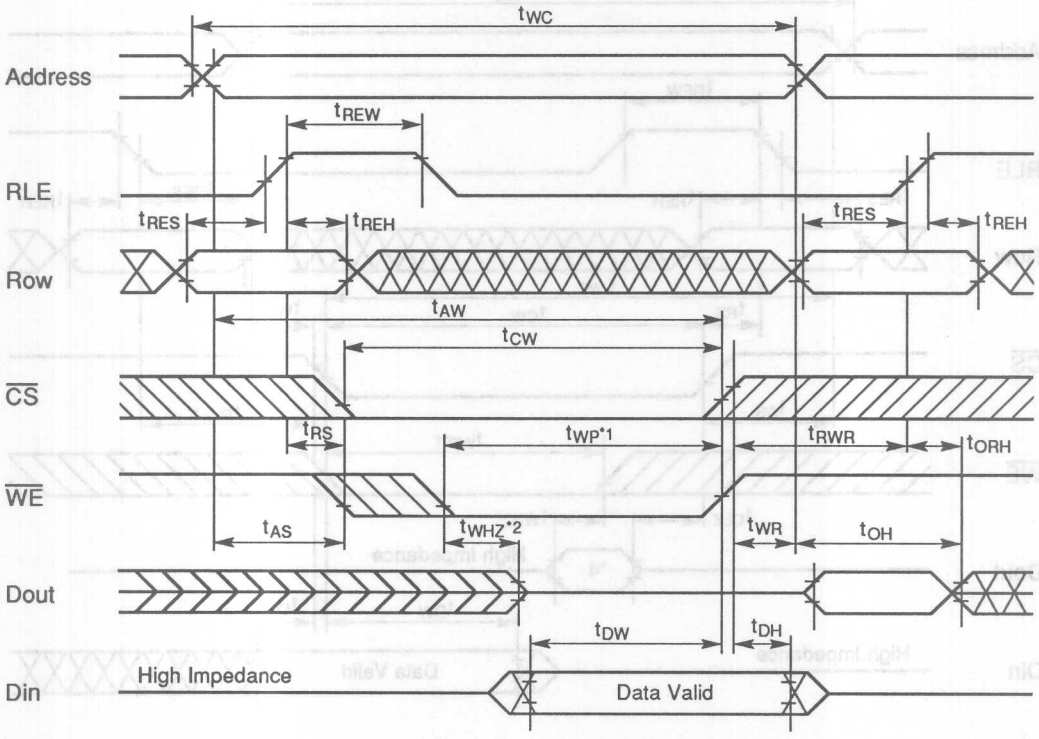
• **Timing Waveform of Write Cycle No. 4** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled) (7)



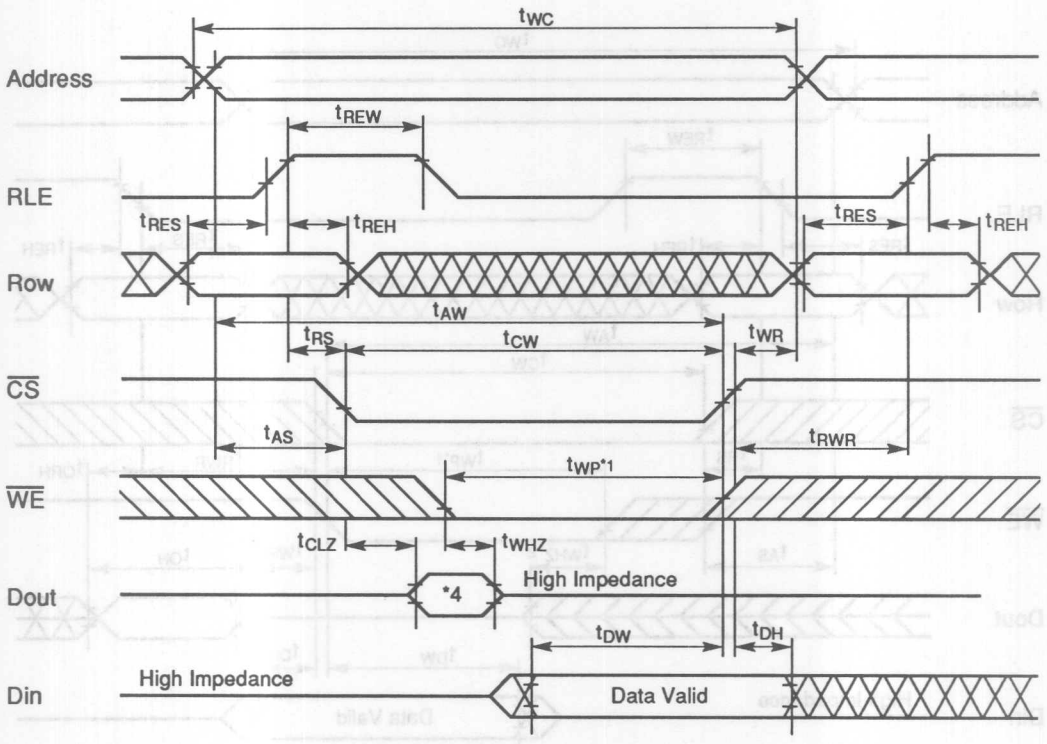
• **Timing Waveform of Write Cycle No. 5** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled) (7)



• **Timing Waveform of Write Cycle No. 6** ($\overline{OE}$ = L, $\overline{WE}$ Controlled) (7)



• Timing Waveform of Write Cycle No. 7 ($\overline{OE}$ = L, $\overline{CS}$ Controlled) (7)



NOTES:

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remains in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remains in high impedance state.
7. ALE = V_{IH}, PC = V_{IL}, $\overline{PError}$: Do not care.

HB66B1616A-25/35

16,384-Word × 16-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66B1616A is a high speed 16K × 16 Static RAM module, mounted 4 pieces of 64K bit SRAM (HM6289JP) sealed in SOJ package. An outline of the HB66B1616A is 36-pin dual in-line package. Therefore, the HB66B1616A makes high density mounting possible without surface mount technology. The HB66B1616A provides common data inputs and outputs. Its module board has decoupling capacitors to reduce noise.

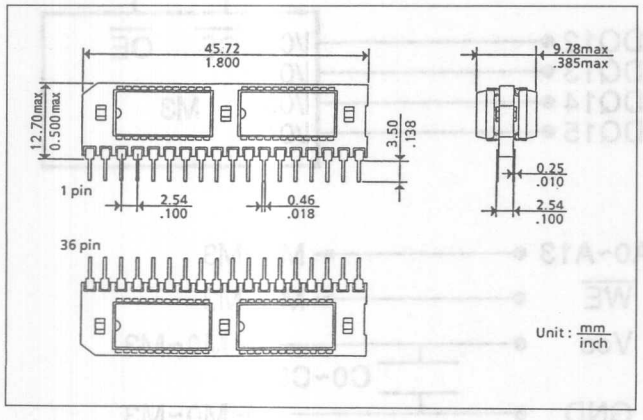
■ FEATURES

- Single 5V (± 5%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .1200mW typ.
  - Standby Mode . . . . . .300mW typ. (TTL level)
  - 0.4mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

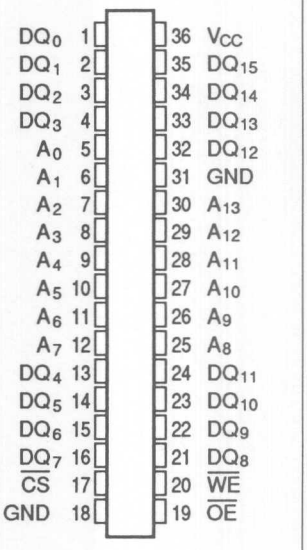
■ ORDERING INFORMATION

Part No.	Access	Package
HB66B1616A-25	25ns	36-pin dual in-line leaded type
HB66B1616A-35	35ns	

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT

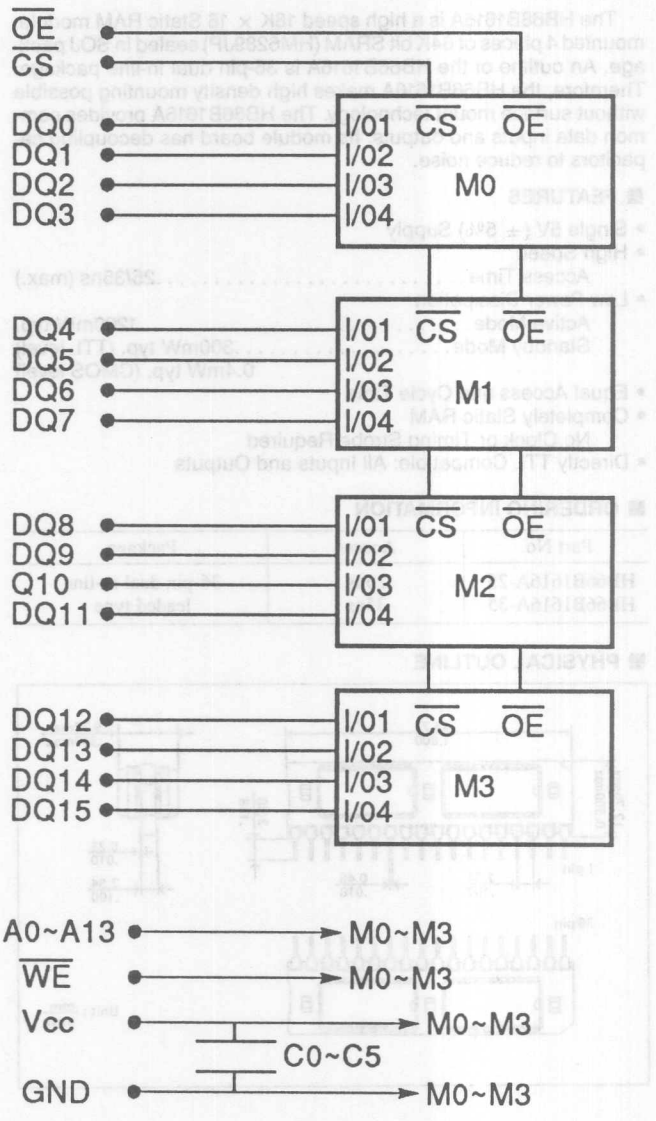


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_{13}	Address Input
DQ_0 ~ DQ_{15}	Data-in, Data-out
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
GND	Ground

■ BLOCK DIAGRAM



* M0~M3 : HM6289JP

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	−0.5(1) to +7.0	V
Power Dissipation	P_T	4.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: 1. V_{in} min. = −2.0V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle (1–3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle (1) (2)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (3–6)

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5(1)	—	0.8	V

NOTE: 1. V_{IL} min. = −2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.(1)	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	−2	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle	—	240	480	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} Min. Cycle	—	60	120	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ = ≥ V_{CC} −0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} −0.2V	—	0.08	8	mA
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)(1)

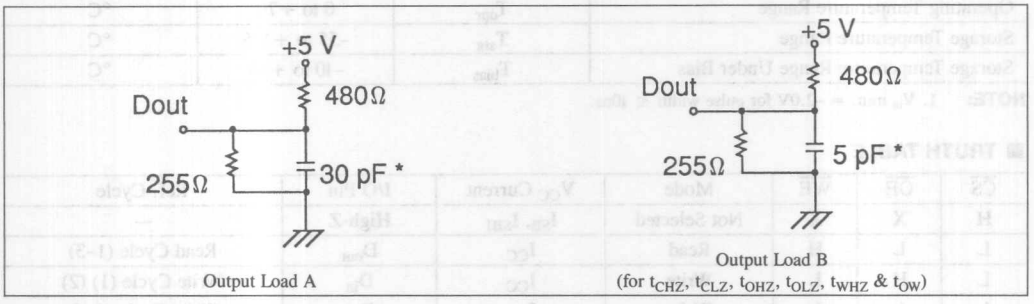
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	C_{in}	V_{in} = 0V	—	35	pF
Input/Output Capacitance (DQ)	$C_{I/O}$	$V_{I/O}$ = 0V	—	15	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input Rise and Fall Times: 5ns
- Input and Output Timing Reference Levels: 1.5V
- Output Load: See Figures



Output Load A

Output Load B
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} & t_{OW})

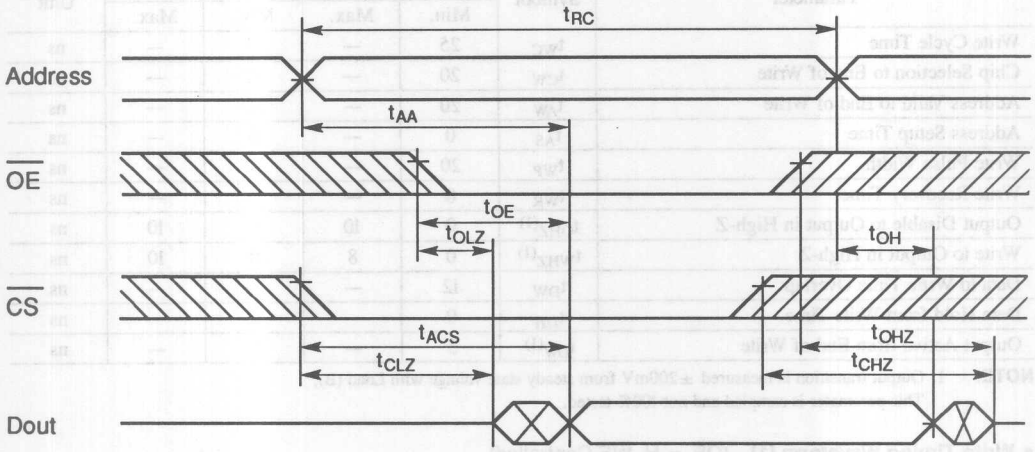
*Including scope and jig capacitance.

• Read Cycle

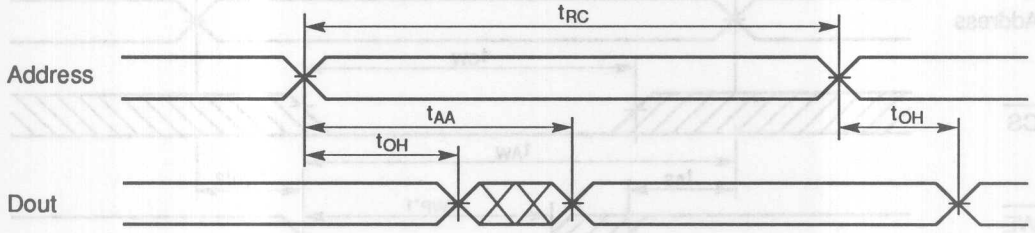
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Chip Selection to Output in Low-Z	t_{CLZ}(1)	5	—	5	—	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	ns
Output Enable to Output in Low-Z	t_{OLZ}(1)	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}(1)	0	12	0	20	ns
Chip Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	30	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

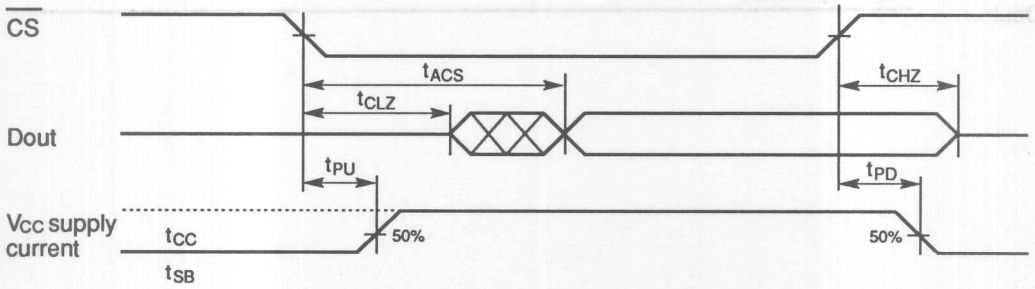
• **Read Timing Waveform (1)** (1)



• **Read Timing Waveform (2)** (1) (2) (4)



• **Read Timing Waveform (3)** (1) (3) (4)



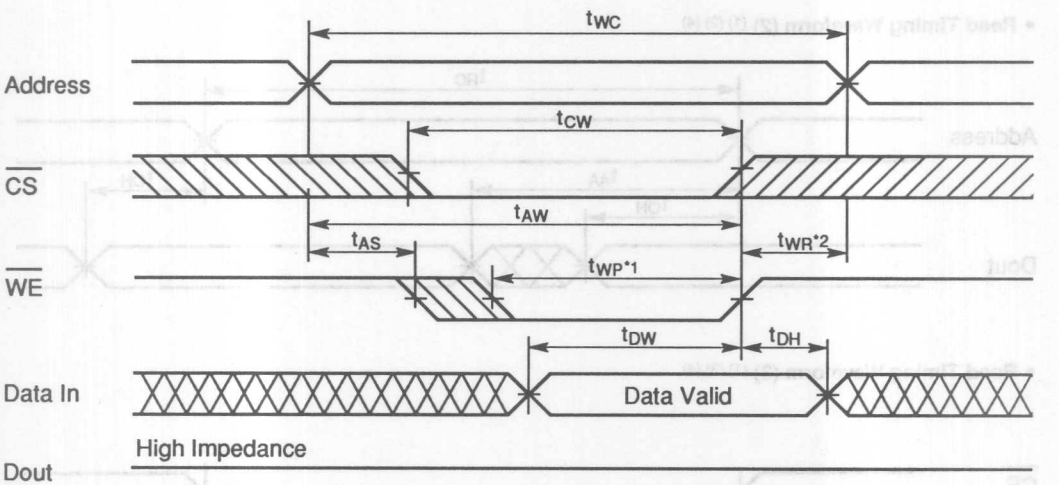
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.

• Write Cycle

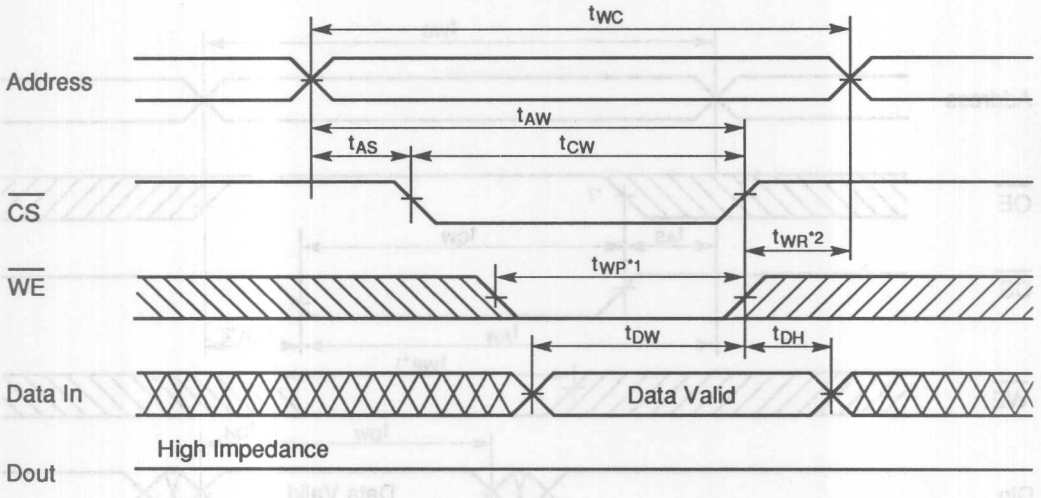
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Write to Output in High-Z	t_{WHZ}(1)	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	12	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}(1)	5	—	5	—	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

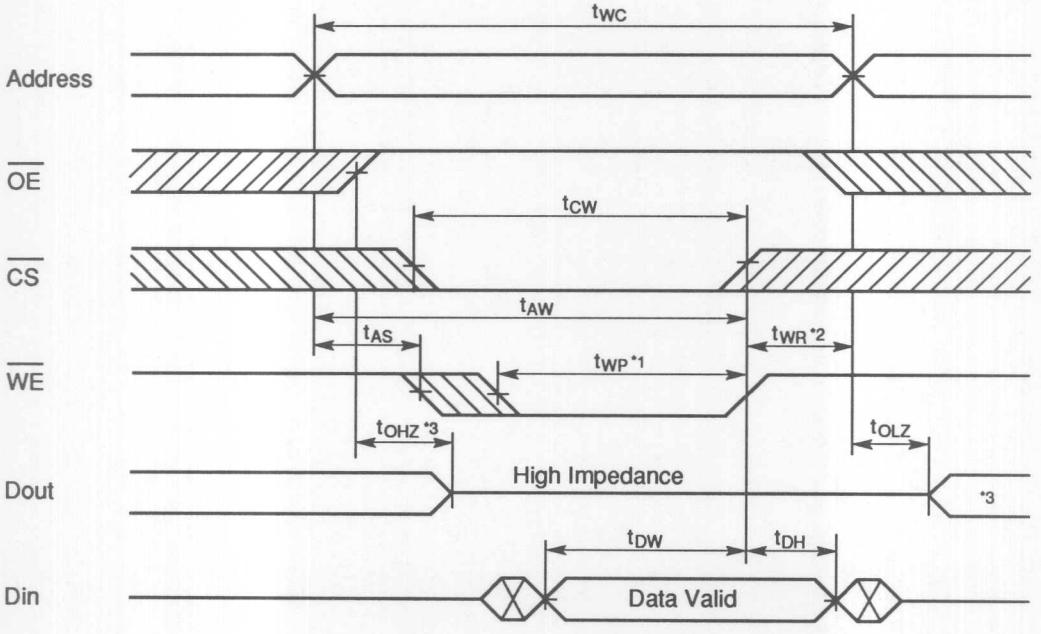
• Write Timing Waveform (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



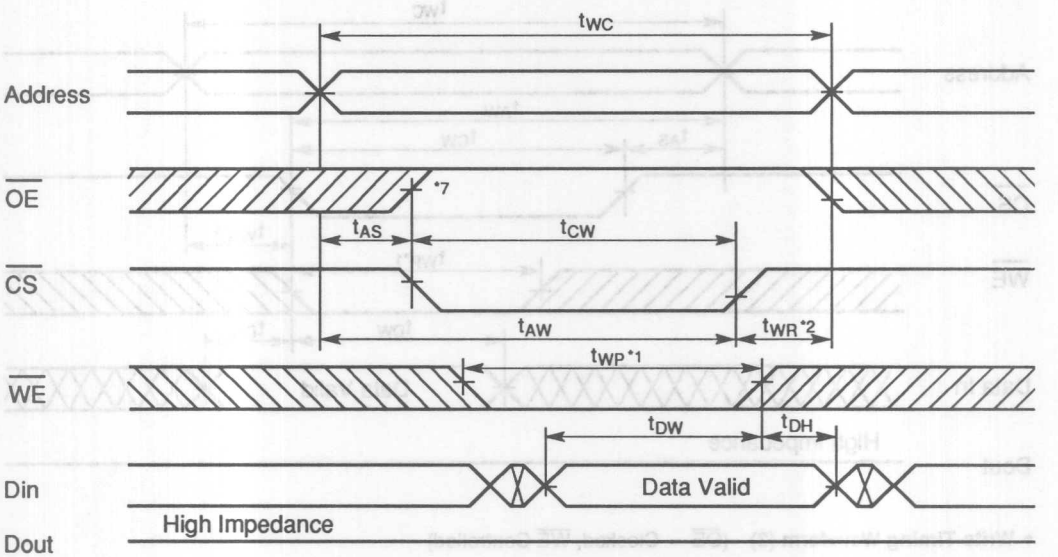
• **Write Timing Waveform (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



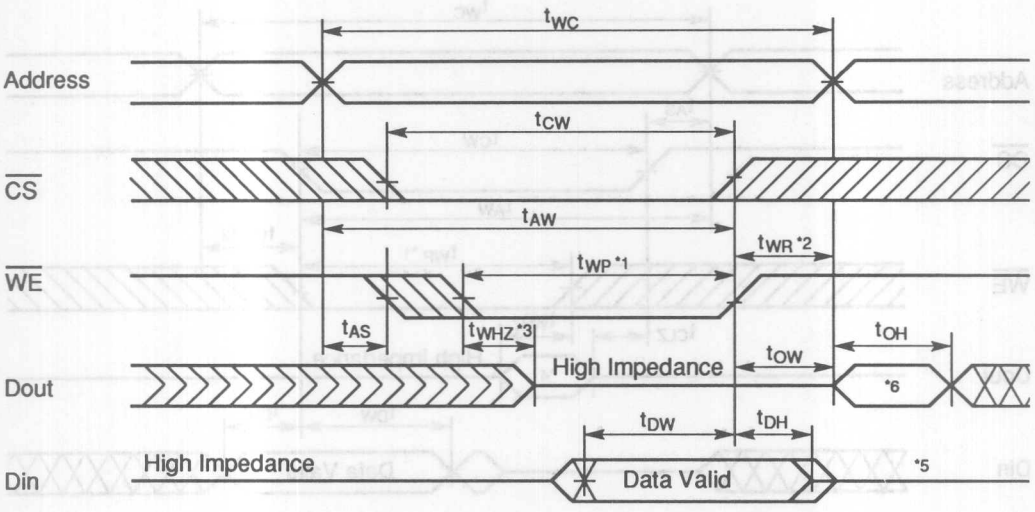
• **Write Timing Waveform (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



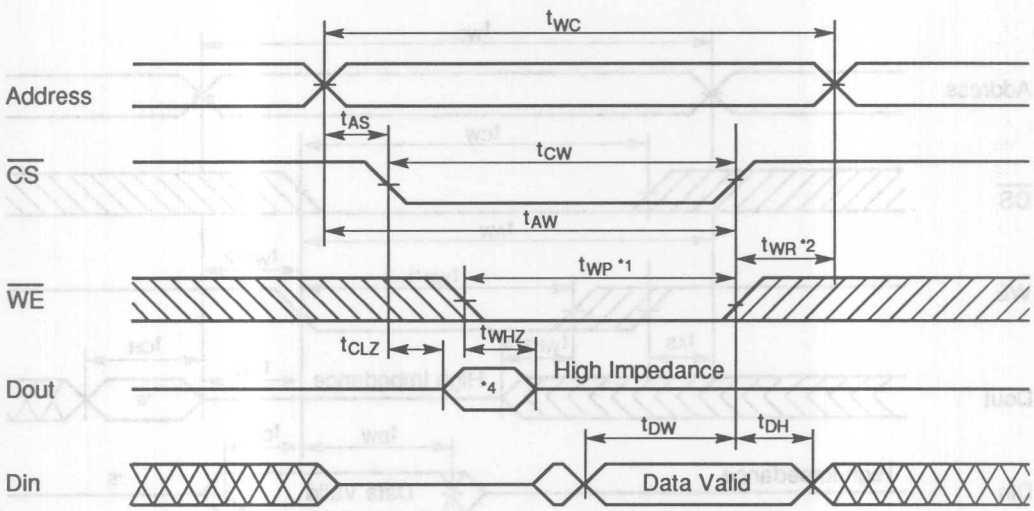
• **Write Timing Waveform (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Timing Waveform (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Timing Waveform (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.
7. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, the output buffers remain in a high impedance state.

HB66A2568A-25/35

262,144-Word × 8-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66A2568A is a high speed 256K × 8 Static RAM module, mounted 8 pieces of 256K bit SRAM (HM6207HJP) sealed in SOJ package. An outline of the HB66A2568A is 60-pin zigzag in-line package. Therefore, the HB66A2568A makes high density mounting possible without surface mount technology. The HB66A2568A provides separate data inputs and output. Its module board has decoupling capacitors to reduce noise.

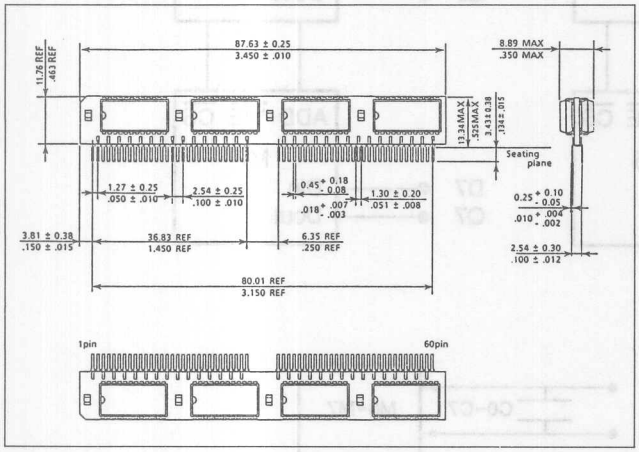
■ FEATURES

- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .2400mW typ.
  - Standby Mode . . . . . .800mW typ. (TTL level)
    0.8mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

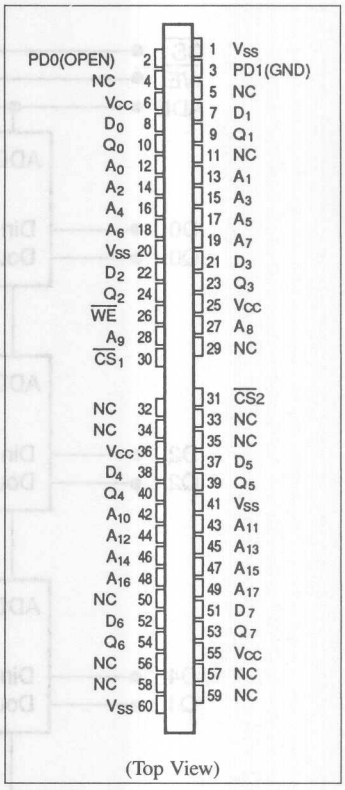
■ ORDERING INFORMATION

Part No.	Access	Package
HB66A2568A-25	25ns	60-pin zigzag in-line leaded type
HB66A2568A-35	35ns	

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT

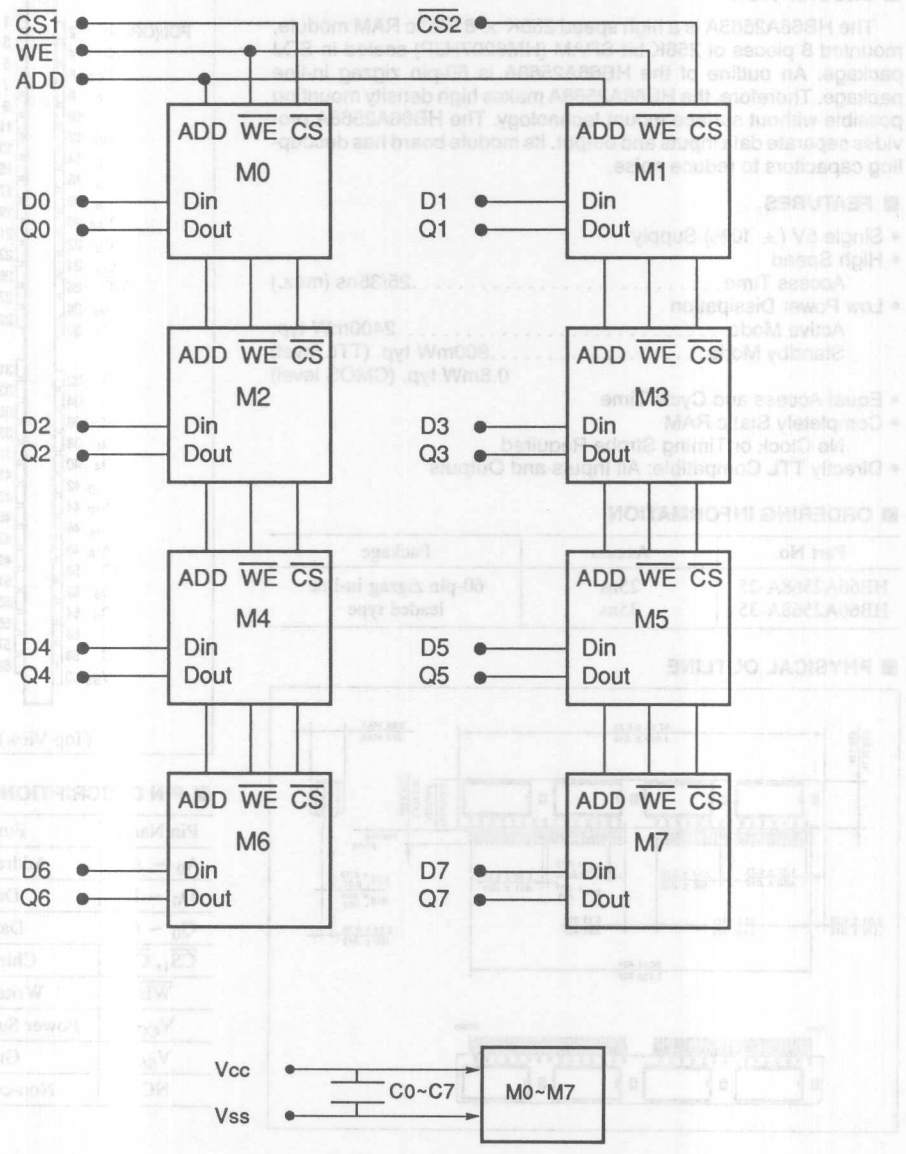


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_{17}	Address Input
D_0 ~ D_7	Data-in
Q_0 ~ Q_7	Data-out
$\overline{CS_1}$, $\overline{CS_2}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

■ BLOCK DIAGRAM



* M0~M7 : HM6207HJP

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	−0.5(1) to +7.0	V
Power Dissipation	P_T	8.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: 1. V_{in} min. = −2.5V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}_1$, $\overline{CS}_2$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5(1)	—	0.8	V

NOTE: 1. V_{IL} min. = −2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.(1)	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	−10	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle, Duty = 100%	—	480	960	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH} Min. Cycle	—	160	320	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}_1$, $\overline{CS}_2$ = ≥ V_{CC} −0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} −0.2V	—	0.16	16	mA
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)(1)

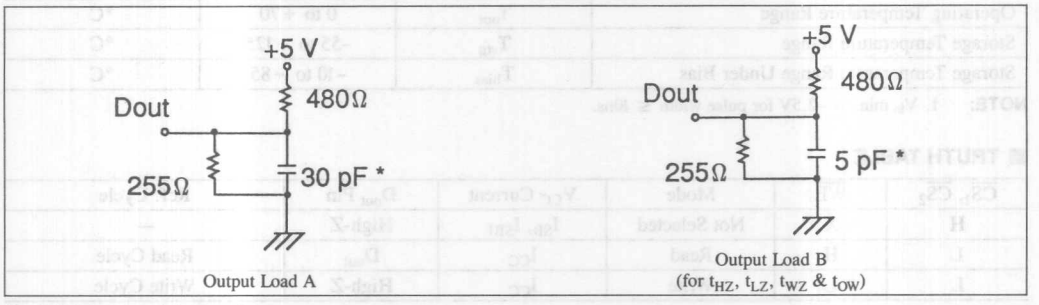
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{WE}$)	C_{I1}	V_{in} = 0V	—	70	pF
Input Capacitance ($\overline{CS}$)	C_{I2}	V_{in} = 0V	—	45	pF
Input Capacitance (Data in)	C_{I3}	V_{in} = 0V	—	12	pF
Output Capacitance (Data out)	C_O	V_{out} = 0V	—	16	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input Rise and Fall Times: 5ns
- Input and Output Timing Reference Levels: 1.5V
- Output Load: See Figures



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

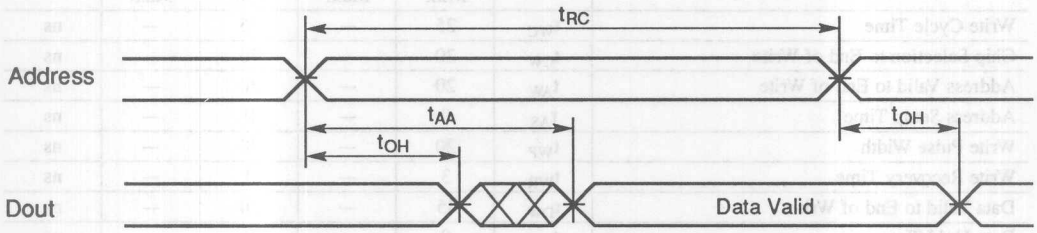
*Including scope and jig capacitance.

• Read Cycle

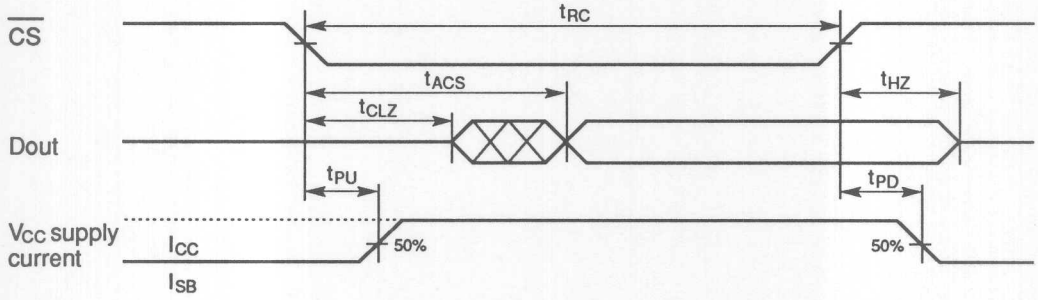
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}(1)	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}(1)	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	ns

NOTE: 1. Transition is measured ±200mV from steady state voltage with Load (B)
This parameter is sampled and not 100% tested.

• **Timing Waveform of Read Cycle (1)** (1) (2)



• **Timing Waveform of Read Cycle (2)** (1) (3)



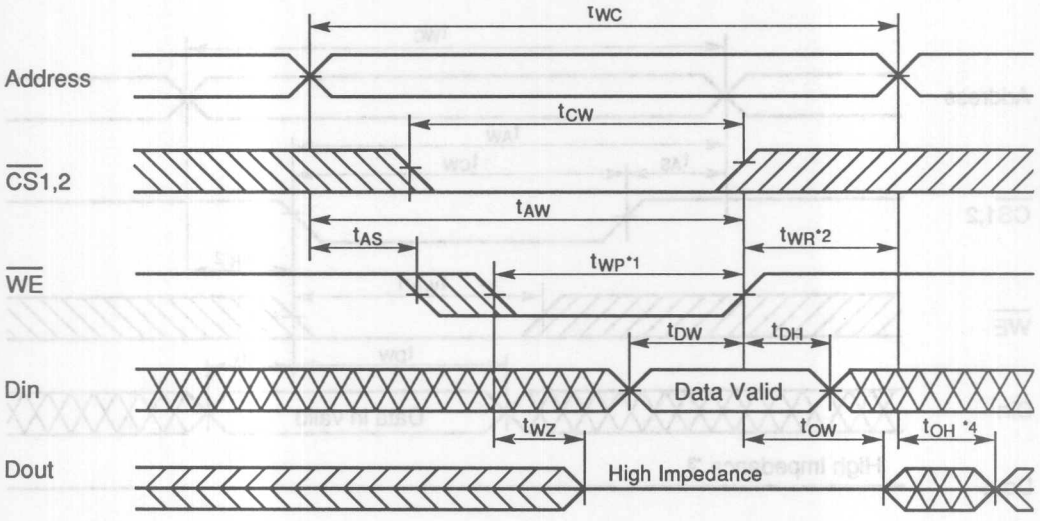
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• Write Cycle

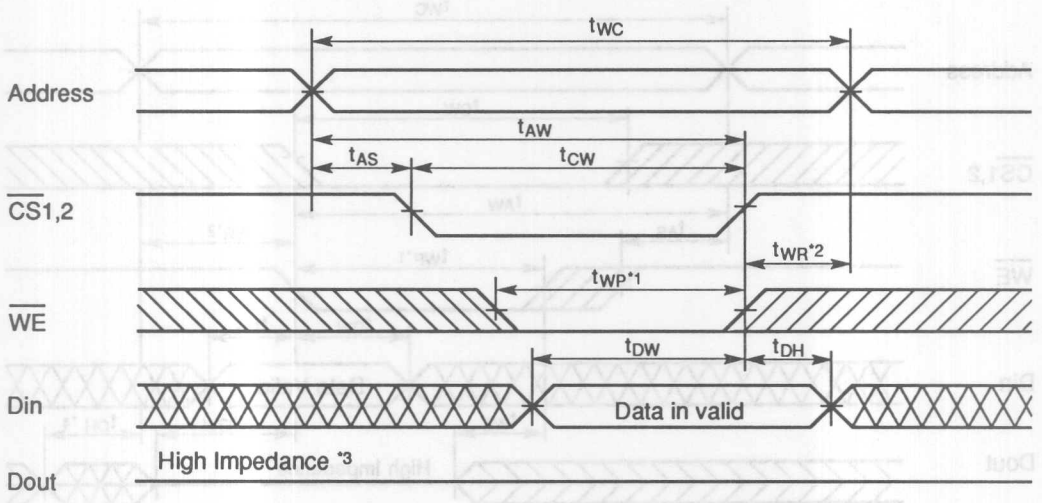
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High-Z	t_{WZ}(1)	0	8	0	10	ns
Output Active from End of Write	t_{OW}(2)	0	—	0	—	ns

NOTE: 1. Transition is measured ±200mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• **Timing Waveform of Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Timing Waveform of Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
4. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.

HM644332

2K Entry TAG Memory for Cache Sub System

The HM644332 TAGM is a 2048-entry tag memory fabricated with CMOS technology. It supports compact cache systems with 2-way or 4-way set associativity and a high level of performance for 32-bit microprocessor systems, when used together with fast static RAMs as data RAMs.

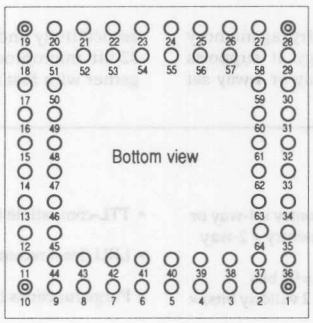
Features

- Programmable organization: 512-entry × 4-way or 1024-entry × 2-way
- Memory organization: 512 words × 98 bits
  98 bits = (20 tag bits + 1 parity bit + 2 validity bits) × 4 ways + 6 LRU bits
- Fast access time: 25/30 ns max from address inputs, 18 ns max from tag data inputs
- Single + 5 V supply
- TTL-compatible inputs and outputs
- LRU (least recently used) replacement algorithm
- Purge functions (all purge and partial purge)
- Internal parity generator/checker
- 64-pin pin-grid-array

Ordering Information

	Access Time		
Part No.	From Address	From Tag Data	Package
HM644332G-25	25 ns	18 ns	64-pin PGA
HM644332G-30	30 ns	18 ns	

Pin Arrangement

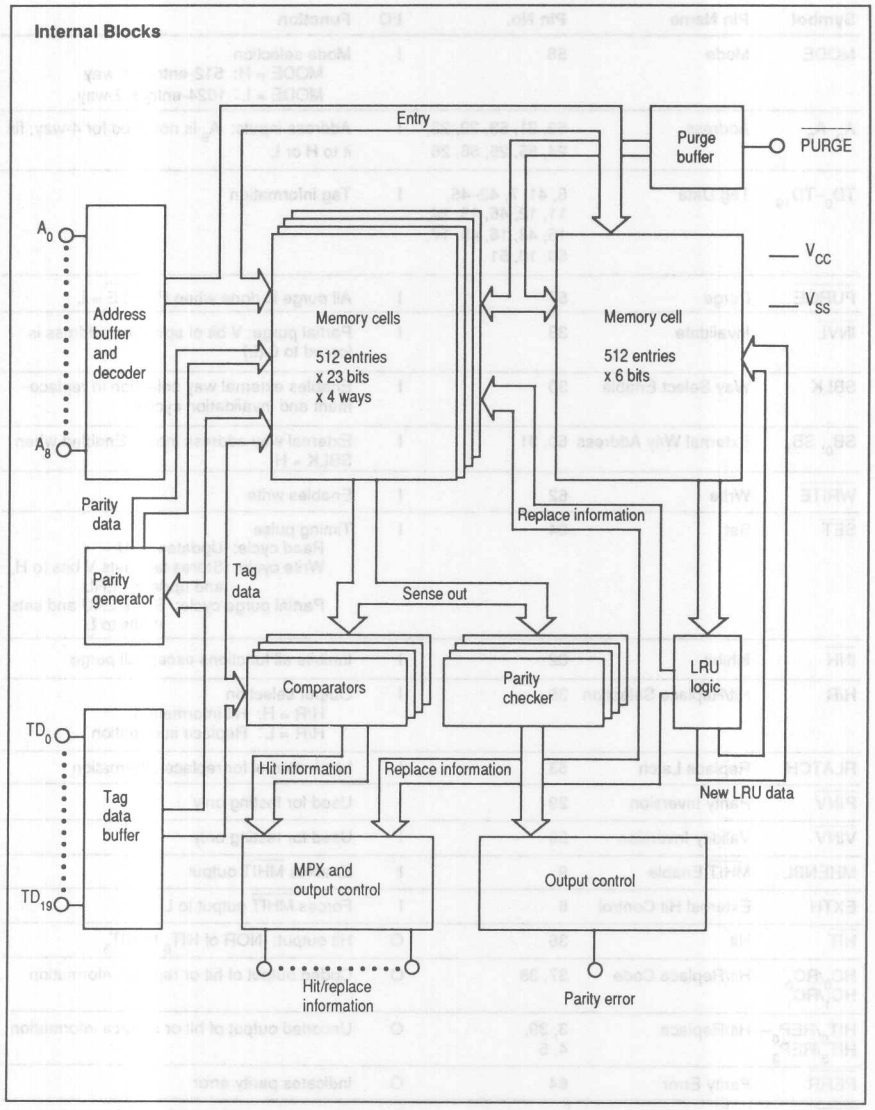


Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A_4	45	TD_6
2	$\overline{MHIT}$	24	A_5	46	TD_9
3	HIT_0/REP_0	25	A_7	47	V_{CC}
4	HIT_2/REP_2	26	A_9	48	TD_{13}
5	HIT_3/REP_3	27	N.C.	49	TD_{15}
6	TD_0	28	N.C.	50	TD_{17}
7	TD_2	29	$\overline{PINV}$	51	TD_{19}
8	EXTH	30	SBLK	52	A_0
9	MHENBL	31	SB_1	53	A_2
10	N.C.	32	$\overline{INH}$	54	V_{SS}
11	TD_7	33	$\overline{INVL}$	55	A_6
12	TD_8	34	$\overline{SET}$	56	A_8
13	TD_{10}	35	H/R	57	$\overline{PURGE}$
14	TD_{11}	36	$\overline{HIT}$	58	MODE
15	TD_{12}	37	HC_0/RC_0	59	$\overline{VINV}$
16	TD_{14}	38	HC_1/RC_1	60	SB_0
17	TD_{16}	39	HIT_1/REP_1	61	V_{CC}
18	TD_{18}	40	V_{SS}	62	$\overline{WRITE}$
19	N.C.	41	TD_1	63	RLATCH
20	N.C.	42	TD_3	64	$\overline{PERR}$
21	A_1	43	TD_4		
22	A_3	44	TD_5		

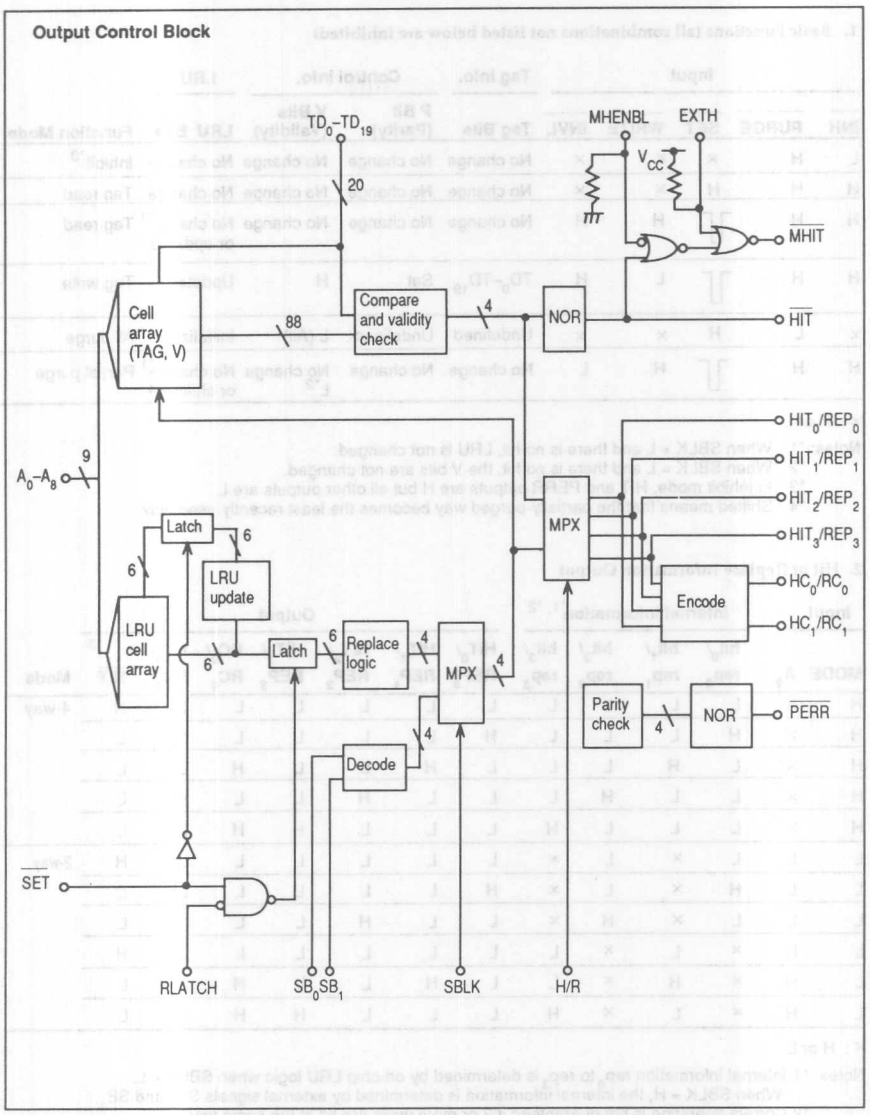
Pin Description

Symbol	Pin Name	Pin No.	I/O	Function
MODE	Mode	58	I	Mode selection MODE = H: 512-entry x 4-way MODE = L: 1024-entry x 2-way
A_0–A_9	Address	52, 21, 53, 22, 23, 24, 55, 25, 56, 26	I	Address inputs: A_9 is not used for 4-way; fix it to H or L
TD_0–TD_{19}	Tag Data	6, 41, 7, 42–45, 11, 12, 46, 13, 14, 15, 48, 16, 49, 17, 50, 18, 51	I	Tag information
$\overline{PURGE}$	Purge	57	I	All purge is done when $\overline{PURGE}$ = L
$\overline{INVL}$	Invalidate	33	I	Partial purge: V bit of specified address is forced to 0 (L)
SBLK	Way Select Enable	30	I	Enables external way selection in replacement and invalidation cycles
SB_0, SB_1	External Way Address	60, 31	I	External way address input: Enabled when SBLK = H
$\overline{WRITE}$	Write	62	I	Enables write
$\overline{SET}$	Set	34	I	Timing pulse Read cycle: Updates LRU Write cycle: Stores tag, sets V bits to H, and updates LRU Partial purge cycle: Shifts LRU and sets V bits to L
$\overline{INH}$	Inhibit	32	I	Inhibits all functions except all purge
H/R	Hit/Replace Selection	35	I	Output selection H/R = H: Hit information H/R = L: Replace information
RLATCH	Replace Latch	63	I	Latch control for replace information
$\overline{PINV}$	Parity Inversion	29	I	Used for testing only
$\overline{VINV}$	Validity Inversion	59	I	Used for testing only
MHENBL	$\overline{MHIT}$ Enable	9	I	Enables $\overline{MHIT}$ output
EXTH	External Hit Control	8	I	Forces $\overline{MHIT}$ output to L
$\overline{HIT}$	Hit	36	O	Hit output: NOR of HIT_0 to HIT_3
HC_0/RC_0 HC_1/RC_1	Hit/Replace Code	37, 38	O	Coded output of hit or replace information
HIT_0/REP_0– HIT_3/REP_3	Hit/Replace	3, 39, 4, 5	O	Uncoded output of hit or replace information
$\overline{PERR}$	Parity Error	64	O	Indicates parity error
$\overline{MHIT}$	Modified Hit	2	O	Hit output modified by MHENBL and EXTH
V_{CC}	Power	47, 61	I	Connects to + 5V power supply
V_{SS}	Ground	40, 54	I	Connects to ground

Block Diagrams



Output Control Block



Function Tables

1. Basic Functions (all combinations not listed below are inhibited)

Input					Tag Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	Tag Bits	P Bit (Parity)	V Bits (Validity)	LRU Bits	Function Mode
L	H	×	×	×	No change	No change	No change	No change	Inhibit*3
H	H	H	×	×	No change	No change	No change	No change	Tag read
H	H	⊓	H	H	No change	No change	No change	No change*1 or updated	Tag read
H	H	⊓	L	H	TD_0–TD_{19}	Set	H	Updated	Tag write
×	L	H	×	×	Undefined	Undefined	L (All)	Initialized	All purge
H	H	⊓	H	L	No change	No change	No change L*2	No change*1 or shifted*4	Partial purge

×: H or L

Notes: *1 When SBLK = L and there is no hit, LRU is not changed.
*2 When SBLK = L and there is no hit, the V bits are not changed.
*3 In inhibit mode, HIT and PERR outputs are H but all other outputs are L.
*4 Shifted means that the partially-purged way becomes the least recently used way.

2. Hit or Replace Information Output

Input		Internal Information*1, *2				Output							
MODE	A_9	hit_0/ rep_0	hit_1/ rep_1	hit_2/ rep_2	hit_3/ rep_3	HIT_0/ REP_0	HIT_1/ REP_1	HIT_2/ REP_2	HIT_3/ REP_3	HC_0/ RC_0	HC_1/ RC_1	$\overline{HIT}$*3	Mode
H	×	L	L	L	L	L	L	L	L	L	L	H	4-way
H	×	H	L	L	L	H	L	L	L	L	L	L	
H	×	L	H	L	L	L	H	L	L	H	L	L	
H	×	L	L	H	L	L	L	H	L	L	H	L	
H	×	L	L	L	H	L	L	L	H	H	H	L	
L	L	L	×	L	×	L	L	L	L	L	L	H	2-way
L	L	H	×	L	×	H	L	L	L	L	L	L	
L	L	L	×	H	×	L	L	H	L	L	H	L	
L	H	×	L	×	L	L	L	L	L	L	L	H	
L	H	×	H	×	L	L	H	L	L	H	L	L	
L	H	×	L	×	H	L	L	L	H	H	H	L	

×: H or L

Notes: *1 Internal information rep_0 to rep_3 is determined by on-chip LRU logic when SBLK = L.
When SBLK = H, the internal information is determined by external signals SB_0 and SB_1.
*2 Correct operation is not guaranteed if 2 or more ways are hit at the same time.
*3 $\overline{HIT}$ output is valid when H/R = H.

3. Partial Purge ($\overline{INVL}$ = L)

Input					Internal Info.				Purged Way				$\overline{SET}$	
MODE	A_9	SBLK	SB_0	SB_1	hit_0	hit_1	hit_2	hit_3	0	1	2	3	LRU	Mode
H	×	L	×	×	L	L	L	L	—	—	—	—	No change	4-way
H	×	L	×	×	H	L	L	L	Q	—	—	—	Shifted	
H	×	L	×	×	L	H	L	L	—	Q	—	—	Shifted	
H	×	L	×	×	L	L	H	L	—	—	Q	—	Shifted	
H	×	L	×	×	L	L	L	H	—	—	—	Q	Shifted	
H	×	H	L	L	×	×	×	×	Q	—	—	—	Shifted	
H	×	H	H	L	×	×	×	×	—	Q	—	—	Shifted	
H	×	H	L	H	×	×	×	×	—	—	Q	—	Shifted	
H	×	H	H	H	×	×	×	×	—	—	—	Q	Shifted	
L	L	L	×	×	L	×	L	×	—	—	—	—	No change	2-way
L	L	L	×	×	H	×	L	×	Q	—	—	—	Shifted	
L	L	L	×	×	L	×	H	×	—	—	Q	—	Shifted	
L	L	H	L	L	×	×	×	×	Q	—	—	—	Shifted	
L	L	H	L	H	×	×	×	×	—	—	Q	—	Shifted	
L	H	L	×	×	×	L	×	L	—	—	—	—	No change	
L	H	L	×	×	×	H	×	L	—	Q	—	—	Shifted	
L	H	L	×	×	×	L	×	H	—	—	—	Q	Shifted	
L	H	H	H	L	×	×	×	×	—	Q	—	—	Shifted	
L	H	H	H	H	×	×	×	×	—	—	—	Q	Shifted	

Note: Correct operation is not guaranteed if 2 or more ways are hit at the same time.

4. Parity Error and V Bits*1

(n: 0 to 3)

pen	vn_0	vn_1	PEn	Hit Info.*2
L	L	L	L	—
L	L	H	H	Hit
L	H	L	H	Hit
L	H	H	L	Hit
H	L	L	L	—
H	L	H	H	Hit
H	H	L	H	Hit
H	H	H	H	Hit

pen: Internal parity error in way n

vn_0/vn_1: Duplicate validity bits.

PEn: Determined by the following equation:

$$PEn = (vn_0 + vn_1) \cdot pen + (vn_0 \oplus vn_1)$$

Notes: *1 $\overline{PERR}$ is the NOR of PE0 to PE3.
*2 Output information when internal hit is valid.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage at Any Pin Relative to V_{SS}	V_{in}	–3.0 to +7.0	V
Output Voltage at Any Pin Relative to V_{SS}	V_{out}	–0.5 to +7.0	V
Output Current	I_{out}	±20	mA
Power Dissipation	P_T	1.5	W
Operating Temperature	T_{opr}	–10 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC} *1	4.5	5.0	5.5	V
Input Low Voltage	V_{IL} *1	–0.5 *2	—	0.8	V
Input High Voltage	V_{IH} *1	2.2	—	6.0	V

Notes: *1 All voltages are relative to V_{SS}.

*2 –3.0 V for pulse width of 20 ns or less.

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Power Supply Current	I_{CC}	Min. cycle, I_{out} = 0 mA	—	—	200	mA
		Cycle = 100 ns, I_{out} = 0 mA	—	—	180	mA
Input Leakage Current	I_{IL}	V_{in} = V_{SS} to V_{CC}	–10	—	10	µA
Output Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V

Capacitances (T_a = 25°C, f = 1 MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0 V	—	—	10	pF
Output Capacitance	C_{out}	V_{out} = 0 V	—	—	TBD	pF

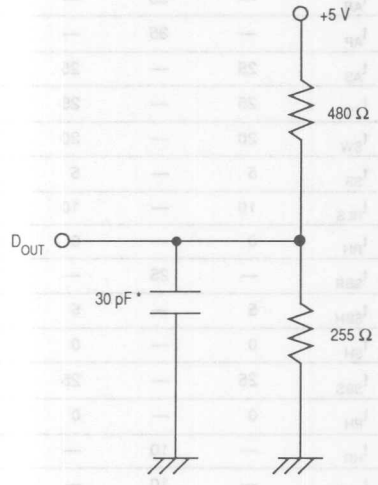
Note: These parameters are sampled, not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC}= 5 V ±10%, V_{SS}=0V, unless otherwise noted)

AC Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input pulse rise and fall times: 0 ns to 5 ns (time between 0.8 V and 2.2 V)
- Input and output timing reference levels: 1.5 V
- Output load: See figure.

Output Load



*Including scope and jig

1. **Tag Read Cycle (MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = H, $\overline{\text{INVL}}$ = H, $\overline{\text{PINV}}$ = H or L, $\overline{\text{VINV}}$ = H or L, $\overline{\text{INH}}$ = H)**

		HM644332G-25		HM644332G-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Read Cycle Time	t_{RC}	50	—	50	—	ns
Address Valid to $\overline{\text{HIT}}$, HC_n, HIT_n	t_{AH}	—	25	—	30	ns
Address Valid to $\overline{\text{MHIT}}$	t_{AMH}	—	27	—	32	ns
Tag Data Valid to $\overline{\text{HIT}}$, HC_n, HIT_n	t_{TH}	—	18	—	18	ns
Tag Data Valid to $\overline{\text{MHIT}}$	t_{TMH}	—	20	—	20	ns
$\overline{\text{HIT}}$, HC_n, HIT_n Hold Time	t_{HH}	0	—	0	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Valid to $\overline{\text{PERR}}$	t_{AP}	—	35	—	40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25	—	25	—	ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
RC_n, REP_n Hold Time for RLATCH	t_{RH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25	—	25	—	ns
$\overline{\text{PERR}}$ Hold Time	t_{PH}	0	—	0	—	ns
H/R to Multiplex Output Change	t_{HR}	—	10	—	12	ns
MHENBL, EXTH to $\overline{\text{MHIT}}$ Output	t_{MMH}	—	10	—	12	ns

2. Tag Write Cycle (MODE = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = L, $\overline{INVL}$ = H, H/$\overline{R}$ = L, $\overline{INH}$ = H)

		HM644332G-25		HM644332G-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Write Cycle Time	t_{WC}	50	—	50	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK Hold Time	t_{SBH}	5	—	5	—	ns
$\overline{PINV}$, $\overline{VINV}$ Setup Time for $\overline{SET}$	t_{IS}	25	—	25	—	ns
$\overline{PINV}$, $\overline{VINV}$ Recovery Time for $\overline{SET}$	t_{IR}	5	—	5	—	ns

3. Partial Purge (MODE = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = H, $\overline{INVL}$ = L, H/$\overline{R}$ = H or L, $\overline{INH}$ = H, RLATCH = L, $\overline{PINV}$ = H or L, $\overline{VINV}$ = H or L)

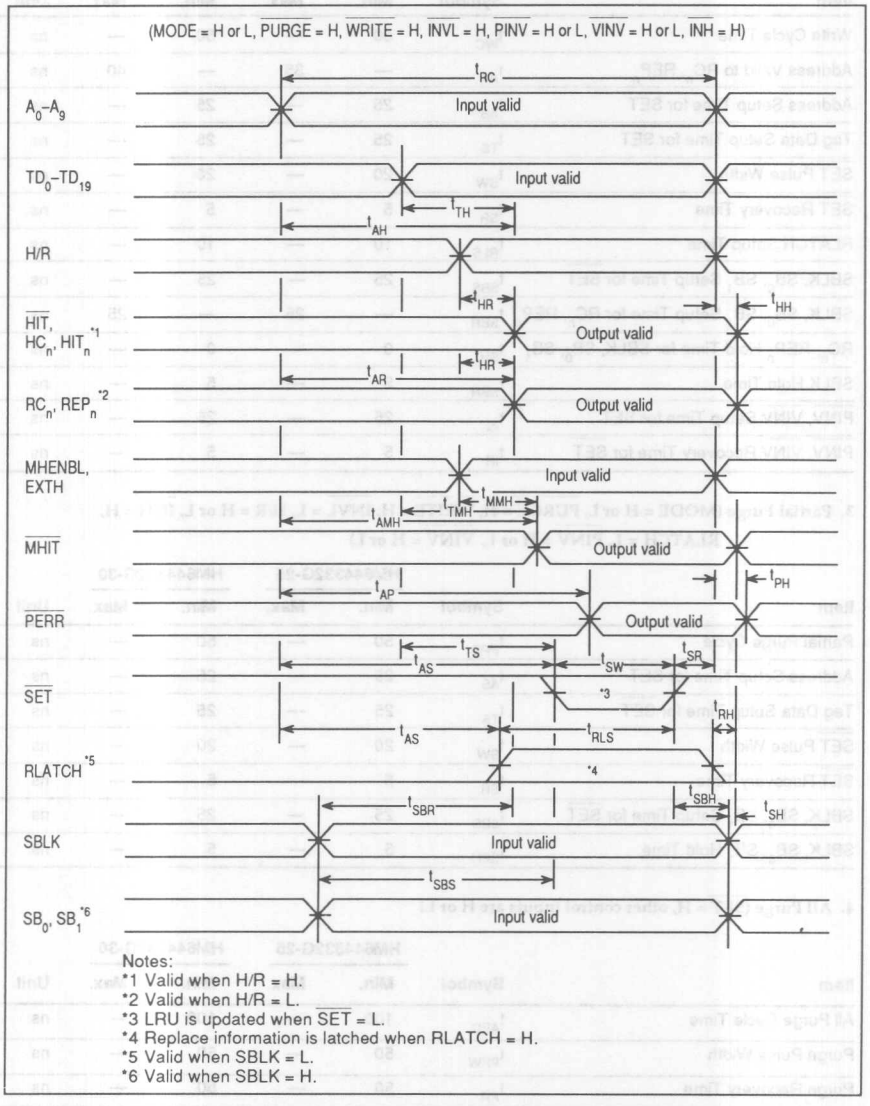
		HM644332G-25		HM644332G-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Partial Purge Cycle	t_{PPC}	50	—	50	—	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns

4. All Purge ($\overline{SET}$ = H, other control inputs are H or L)

		HM644332G-25		HM644332G-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
All Purge Cycle Time	t_{APC}	100	—	100	—	ns
Purge Pulse Width	t_{PPW}	50	—	50	—	ns
Purge Recovery Time	t_{PR}	50	—	50	—	ns

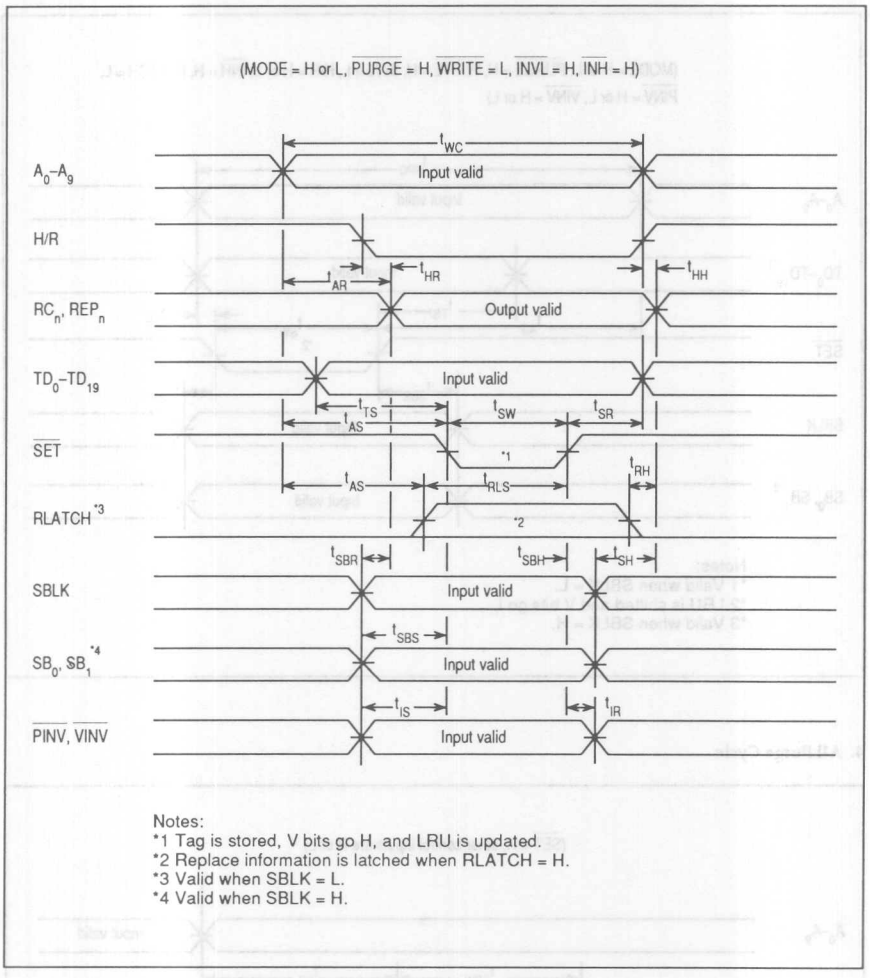
Timing Charts

1. Tag Read Cycle



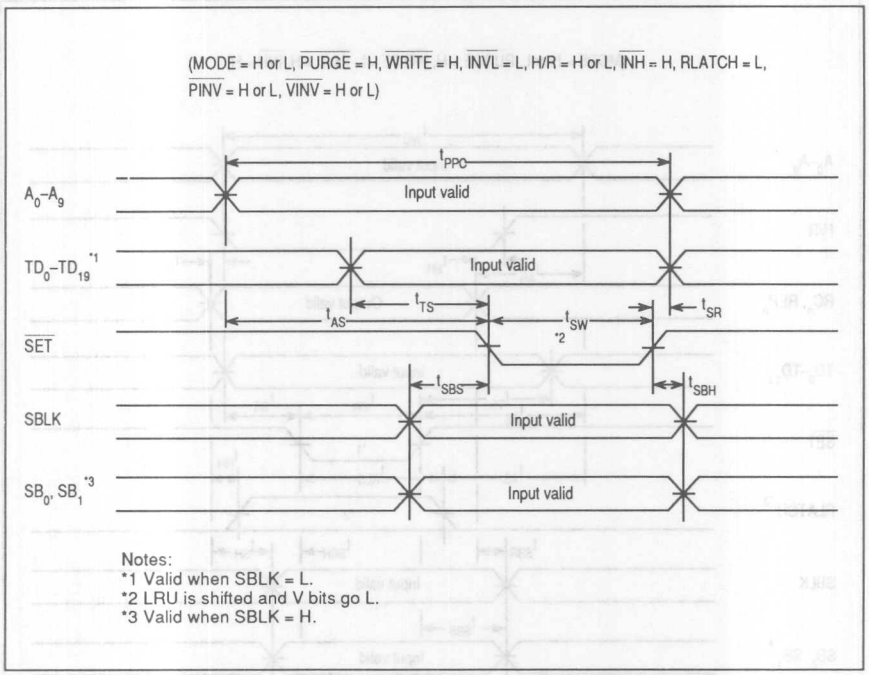
Notes:
*1 Valid when H/R = H.
*2 Valid when H/R = L.
*3 LRU is updated when $\overline{SET}$ = L.
*4 Replace information is latched when RLATCH = H.
*5 Valid when SBLK = L.
*6 Valid when SBLK = H.

2. Tag Write Cycle

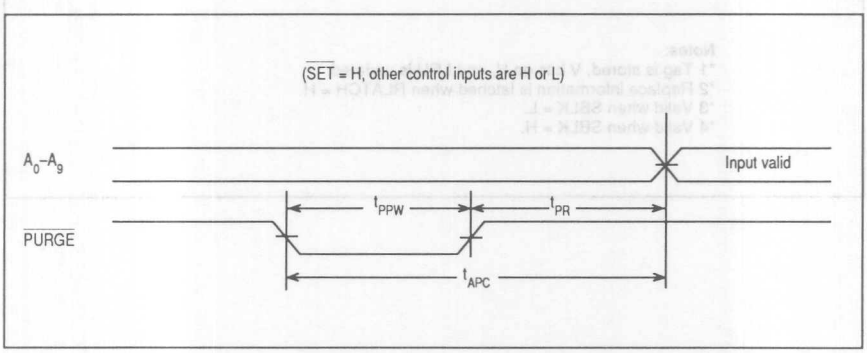


Notes:
*1 Tag is stored, V bits go H, and LRU is updated.
*2 Replace information is latched when RLATCH = H.
*3 Valid when SBLK = L.
*4 Valid when SBLK = H.

3. Partial Purge Cycle



4. All Purge Cycle



Function Description

Tag Read

The TAG input data (TD_0–TD_{19}) and the contents of the addressed location are compared. If they are the same, a hit is assumed. $\overline{HIT}$ goes low and the HCn and HITn outputs indicate the hit way associatively. If there is no hit, the LRU logic of the tag RAM automatically specifies which way is to be replaced.

The replacement information is presented at the RCn and REPn outputs by forcing the H/R input low. These signals will be latched and used for writing data into data memory.

Tag Write

If there is no hit, the tag RAM must be updated. A write operation is performed by setting $\overline{WRITE}$ low and inputting a $\overline{SET}$ pulse. The tag data will be written into the appropriate way by the internal LRU logic.

The way can be also specified externally by using SBLK, SB_0, and SB_1 inputs. In tag write mode, the V bits (validity bits) and the parity bit are set, and the LRU is updated.

All Purge

By asserting the $\overline{PURGE}$ input low, all the V bits are reset and LRU is initialized.

In this operation, the contents of each tag and its parity will not be identified.

Partial Purge

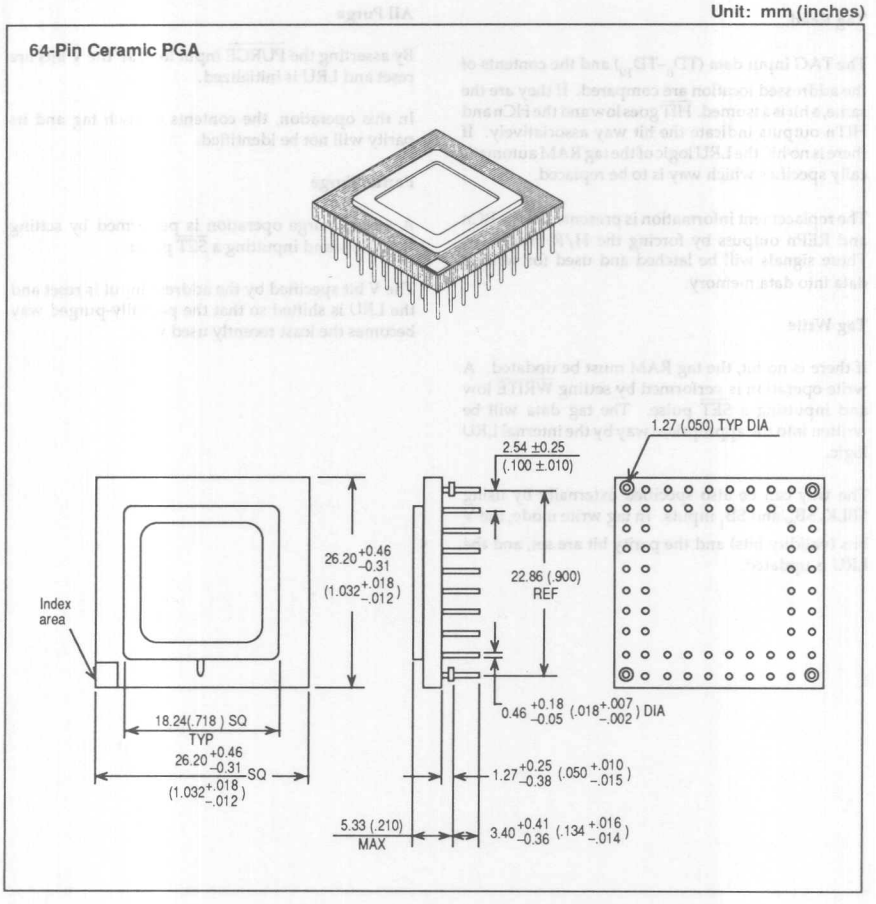
A partial purge operation is performed by setting $\overline{INVL}$ low and inputting a $\overline{SET}$ pulse.

The V bit specified by the address input is reset and the LRU is shifted so that the partially-purged way becomes the least recently used way.

Package Dimensions

Unit: mm (inches)

64-Pin Ceramic PGA



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3

Section 3
MOS Pseudo Static RAM

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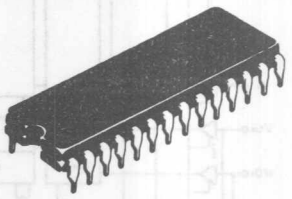
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

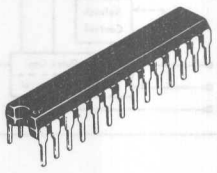
- Single 5V (±10%)
- High Speed
  Access Time
  $\overline{CE}$ Access Time 100/120/150/200ns
  Address Access Time 50/60/75/100ns
  (in Static Column Mode)
  Cycle Time
  Random Read/Write Cycle Time 160/190/235/310ns
  Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

HM65256BP Series



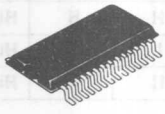
(DP-28)

HM65256BSP Series



(DP-28N)

HM65256BFP Series

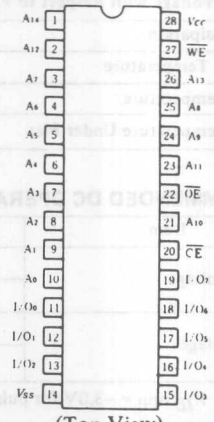


(FP-28DA)

■ ORDERING INFORMATION

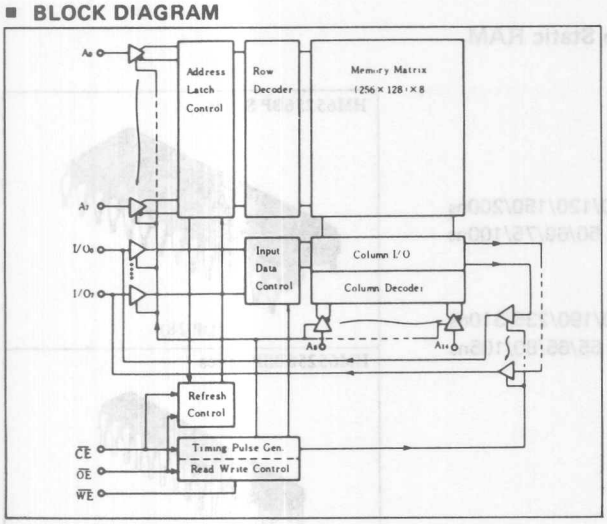
Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BSP-10	100ns	300 mil 28 pin Plastic DIP
HM65256BSP-12	120ns	
HM65256BSP-15	150ns	
HM65256BSP-20	200ns	
HM65256BLSP-10	100ns	
HM65256BLSP-12	120ns	
HM65256BLSP-15	150ns	
HM65256BLSP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	–
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA, t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$	–	–	–	–	50	100	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, Vin = V_{SS} to V_{CC}	–10	–	10	–10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	–10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = –1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

- AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

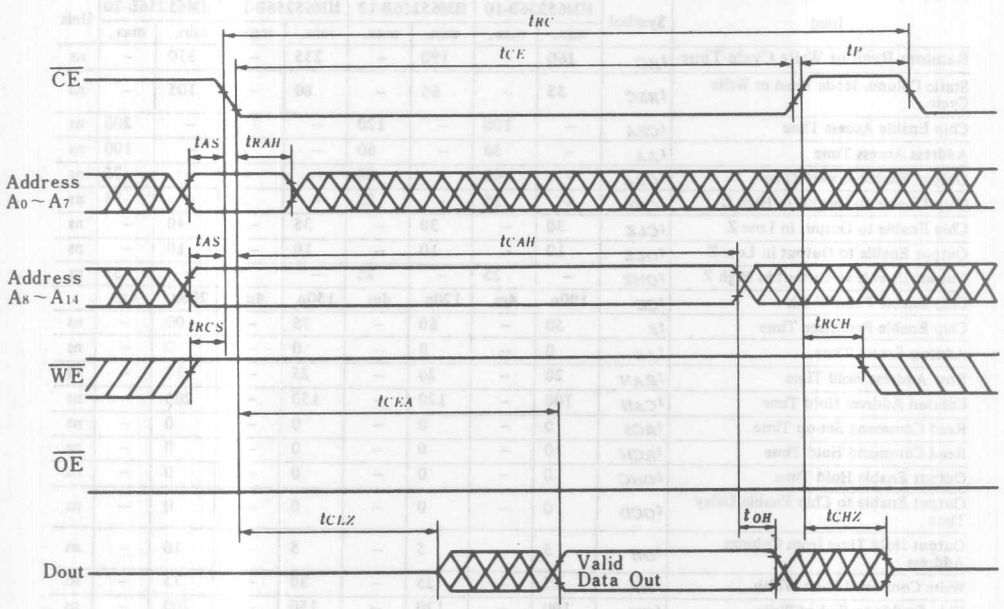
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

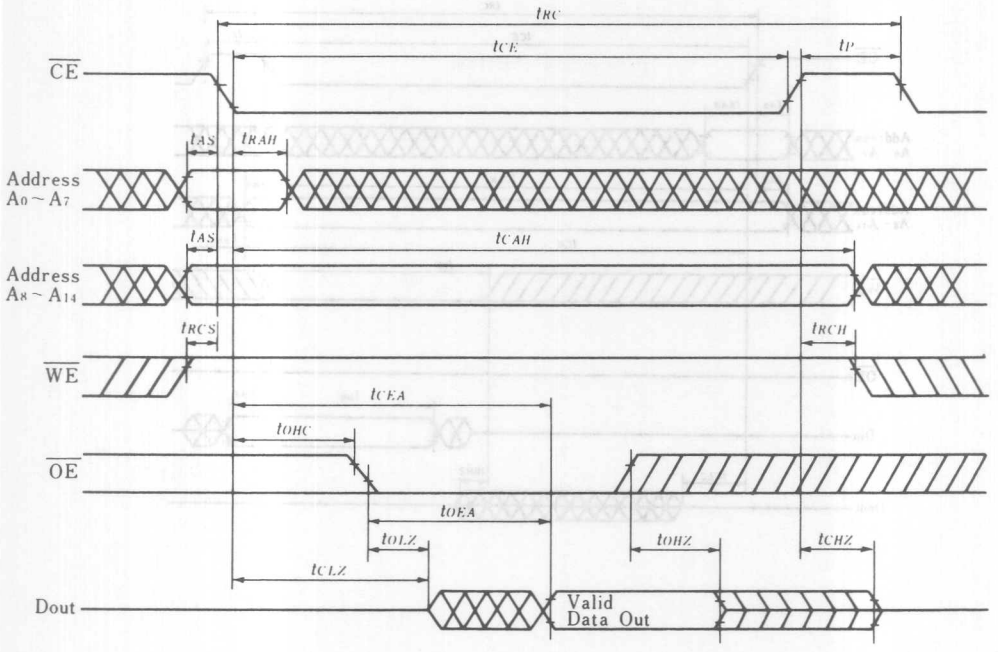
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

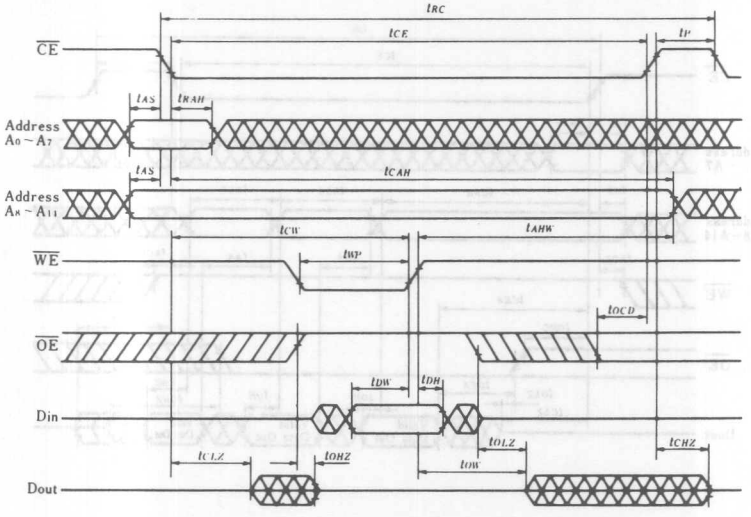
• Read Cycle No. 1 ($\overline{CE}$ controlled)



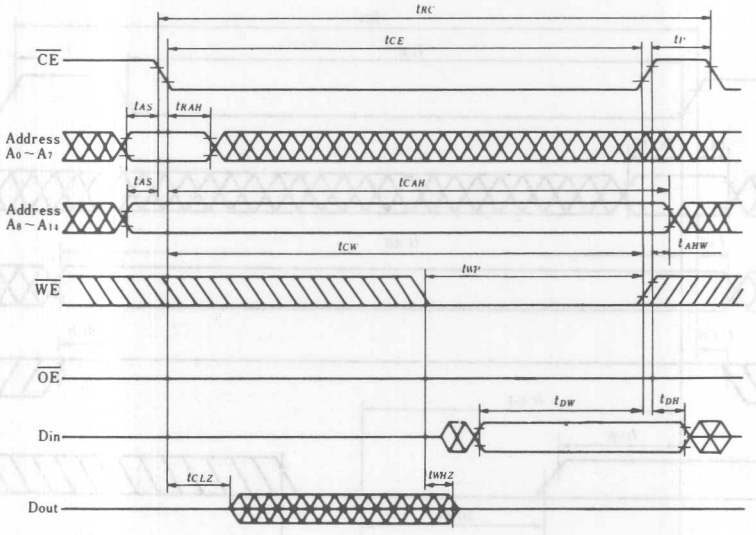
- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



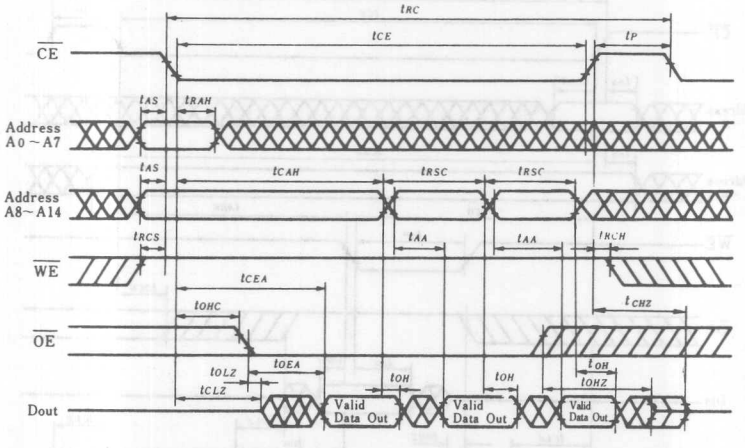
- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



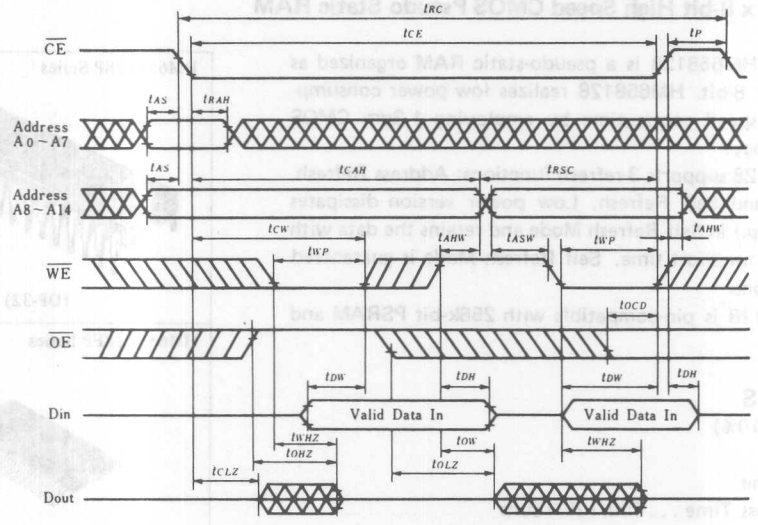
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



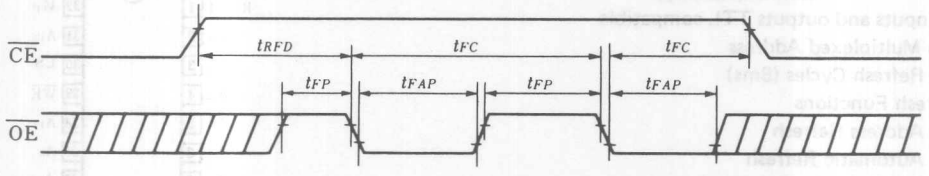
- **Static Column Mode Read Cycle**



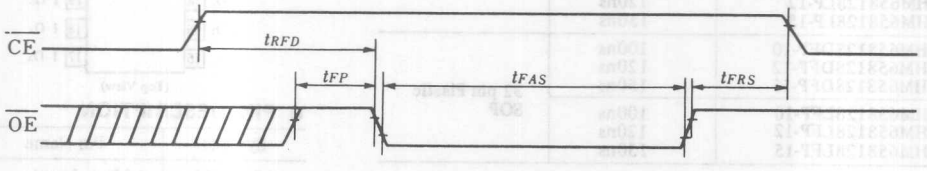
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



HM658128 Series

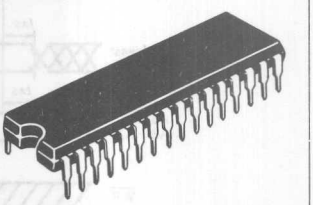
131072-word x 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128 is a pseudo-static RAM organized as 131,072-word x 8-bit. HM658128 realizes low power consumption and high speed access time by employing 1.3μm CMOS process technology.

The HM658128 supports 3 refresh functions: Address Refresh, Auto Refresh and Self Refresh. Low power version dissipates only 0.5mW (typ.) in Self Refresh Mode and retains the data with battery backup for short time. Self Refresh Mode is guaranteed only for L-version.

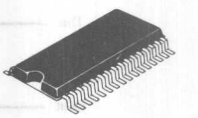
The HM658128 is pin-compatible with 256k-bit PSRAM and static RAM.

HM658128P Series



(DP-32)

HM658128FP Series



(FP-32D)

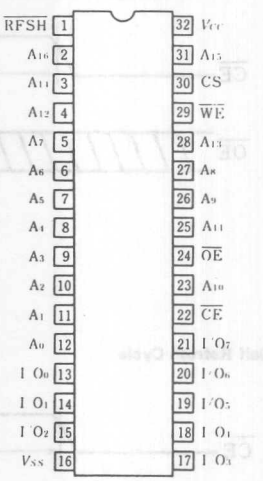
■ FEATURES

- Single 5V (±10%)
- High Speed
  - ○ Access Time
    $\overline{CE}$ Access Time . . . 100/120/150ns
  - ○ Cycle Time
    Random Read/Write Cycle Time . . . 180/210/250ns
- Low Power . . . 200mW typ. (Active)
  0.5mW (standby)
- All inputs and outputs TTL compatible
- Non Multiplexed Address
- 512 Refresh Cycles (8ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh (Only for L-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128DP-10 HM658128DP-12 HM658128DP-15	100ns 120ns 150ns	600 mil 32 pin Plastic DIP
HM658128LP-10 HM658128LP-12 HM658128LP-15	100ns 120ns 150ns	
HM658128DFP-10 HM658128DFP-12 HM658128DFP-15	100ns 120ns 150ns	32 pin Plastic SOP
HM658128LFP-10 HM658128LFP-12 HM658128LFP-15	100ns 120ns 150ns	

■ PIN ARRANGEMENT



(Top View)

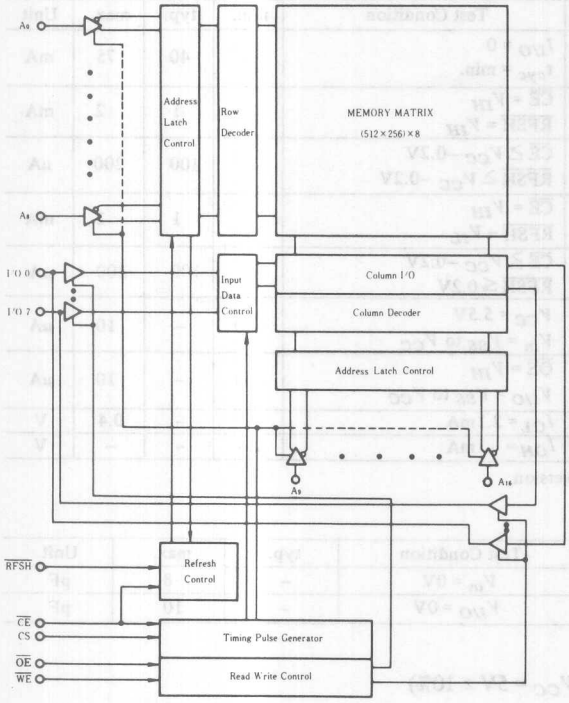
■ PIN DESCRIPTION

Symbol	Pin Name
A0 – A16	Address Inputs
I/O – I/O7	Data Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

HITACHI

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■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low Z	Read
L	H	X	X	L	High Z	Write
L	H	X	H	H	High Z	–
L	L	X	X	X	High Z	CS Standby
H	X	L	X	X	High Z	Refresh*1
H	X	H	X	X	High Z	Standby

Note) *1. Self refresh is guaranteed only for L-version.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	40	75	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2}	$\overline{CE} \geq V_{CC}$ –0.2V $\overline{RFSH} \geq V_{CC}$ –0.2V	–	100	200	µA
Operating Power Supply Current in Self Refresh Mode*1	I_{CC2}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	–	1	2	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}$ –0.2V $\overline{RFSH} \leq$ 0.2V	–	100	200	µA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	–10	–	10	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	µA
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = –1mA	2.4	–	–	V

Note) *1. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	10	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level ..... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load ..... 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	180	–	210	–	250	–	ns
Random Read Modify Write Cycle Time	t_{RWC}	240	–	280	–	330	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	ns
Output Enable Access Time	t_{OEA}	–	30	–	40	–	50	ns
Chip Disable to Output in High Z	t_{CHZ}	–	30	–	35	–	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	35	–	40	–	ns
Output Disable to Output in HighZ	t_{OHZ}	–	25	–	30	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Enable Pulse Width	t_{CE}	100n	1µ	120n	1µ	150n	1µ	s
Chip Enable Precharge Time	t_P	70	–	80	–	90	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	30	–	35	–	40	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	–	15	–	15	–	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	–	5	–	5	–	5	ns

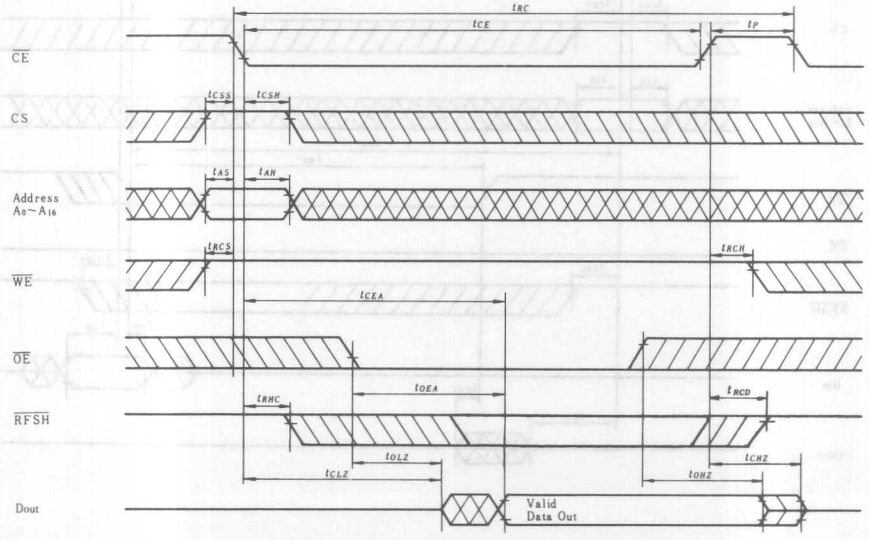
(to be continued)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Chip Select Set-up Time	t_{CSS}	0	–	0	–	0	–	ns
Chip Select Hold Time	t_{CSH}	30	–	35	–	40	–	ns
Write Command Pulse Width	t_{WP}	30	–	35	–	40	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	ns
Data In to End of Write	t_{DW}	25	–	30	–	35	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	70	–	80	–	90	–	ns
Refresh Precharge Time	t_{FP}	40	–	40	–	40	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	180	–	210	–	250	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}*9	8	–	8	–	8	–	μs
Refresh Reset Time for Self Refresh	t_{RFS}*9	180	–	210	–	250	–	ns
Refresh Reset Time for Automatic Refresh	t_{RFA}	0	–	0	–	0	–	ns
Refresh Period (512 cycles)	t_{REF}	–	8	–	8	–	8	ns

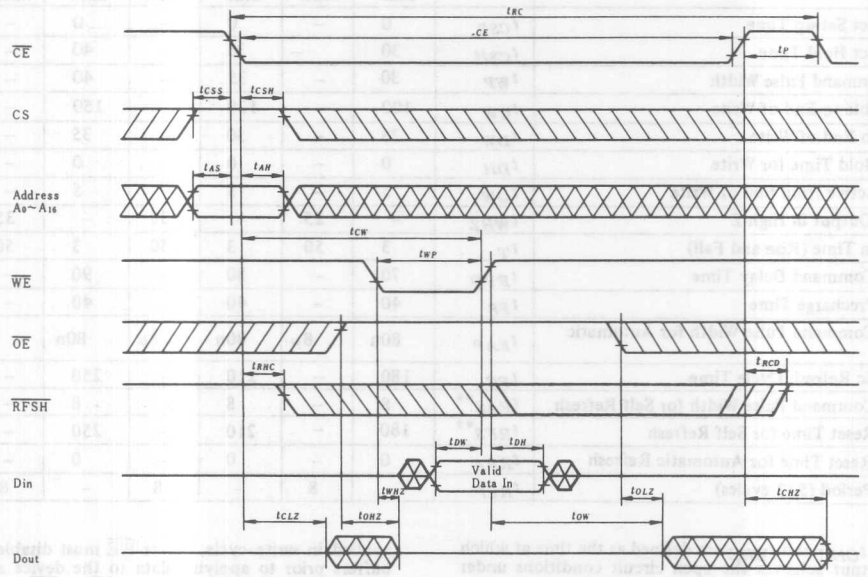
Notes:
(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions under the condition of t_T = 5ns and not 100% tested.
(2) t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5ns and not 100% tested.
(3) A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.
(8) After Self Refresh, Auto Refresh should be started within 15μs. (only for L-version)
(9) This characteristics is guaranteed only for L-version.

■ TIMING WAVEFORMS

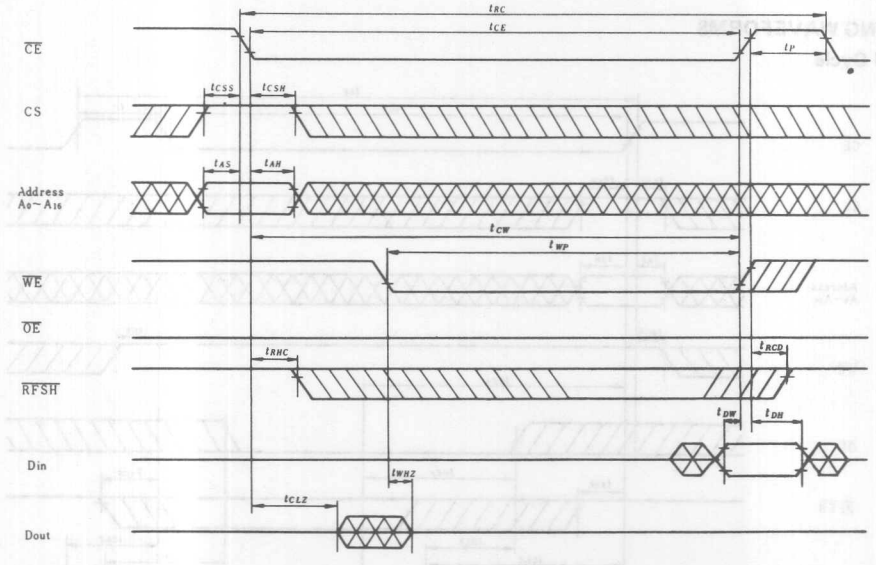
● Read Cycle



• Write Cycle-1 ($\overline{OE}$ Clock)

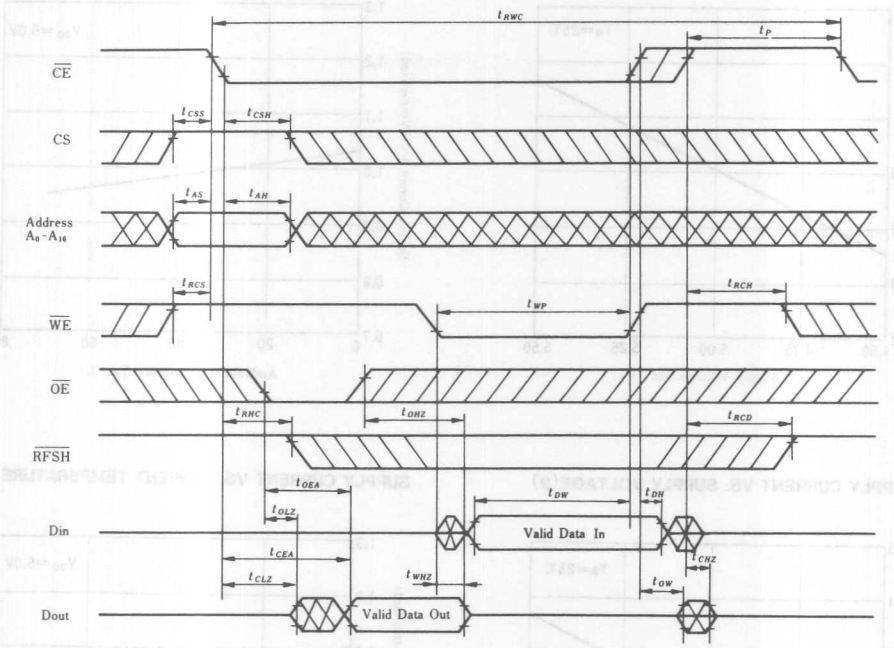


Write Cycle-2 ($\overline{OE}$ Low Fix)

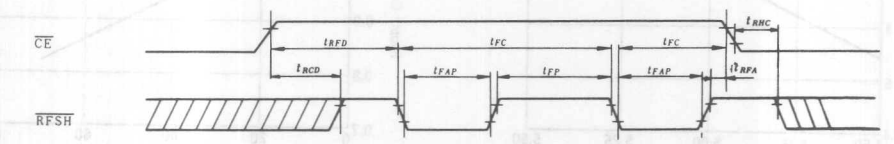


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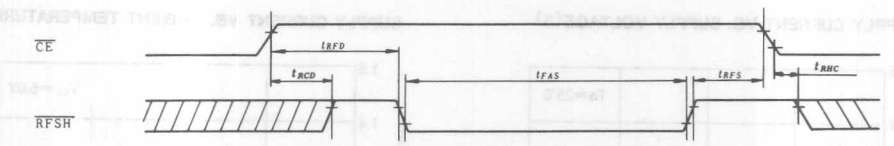
- **Read Modify Write Cycle**



- **Automatic Refresh Cycle**

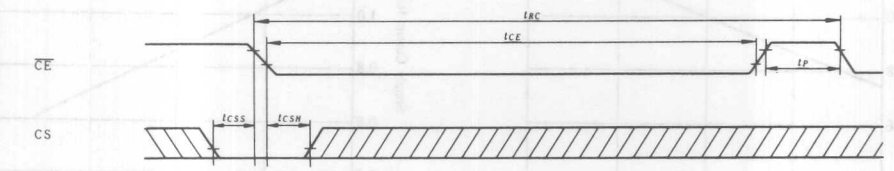


- **Self Refresh Cycle**

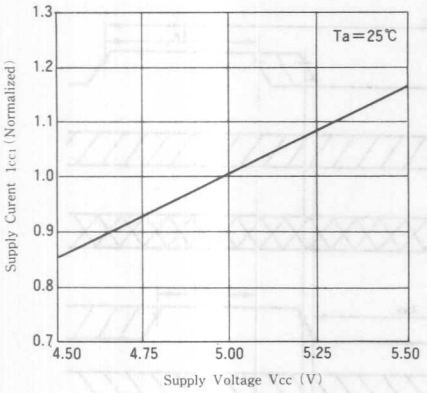


Note) Self refresh is guaranteed only for L-version.

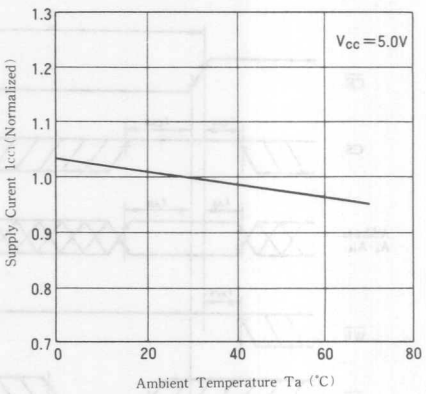
- **CS Standby Mode**



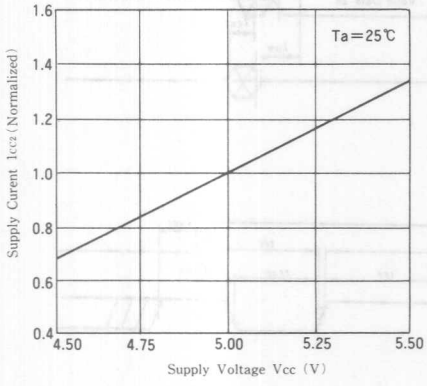
SUPPLY CURRENT VS. SUPPLY VOLTAGE(1)



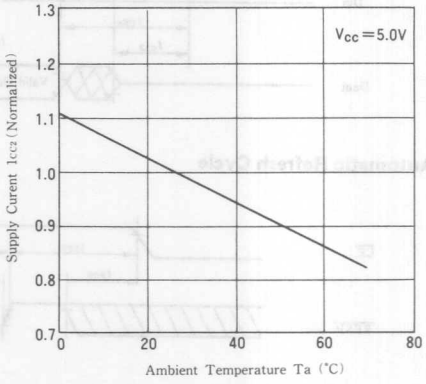
SUPPLY CURRENT VS. AMBIENT TEMPERATURE(1)



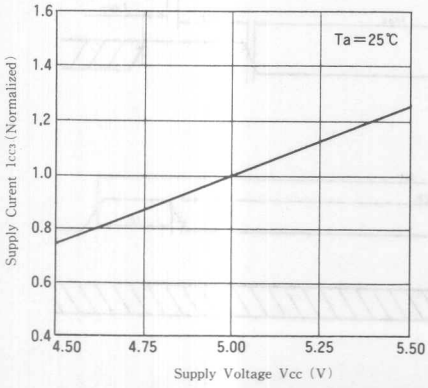
SUPPLY CURRENT VS. SUPPLY VOLTAGE(2)



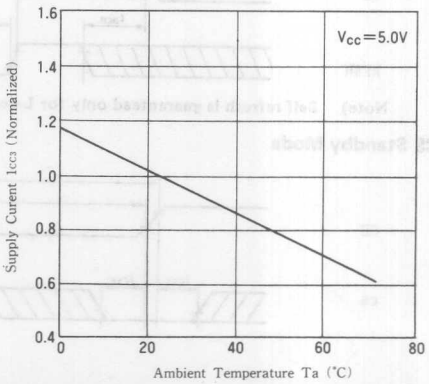
SUPPLY CURRENT VS. AMBIENT TEMPERATURE(2)



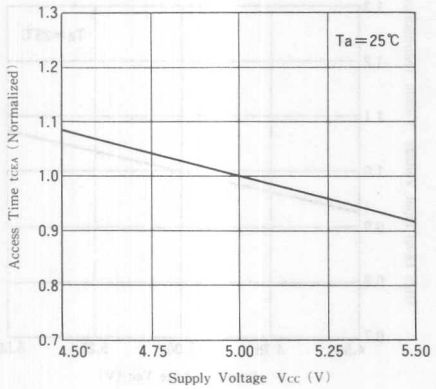
SUPPLY CURRENT VS. SUPPLY VOLTAGE(3)



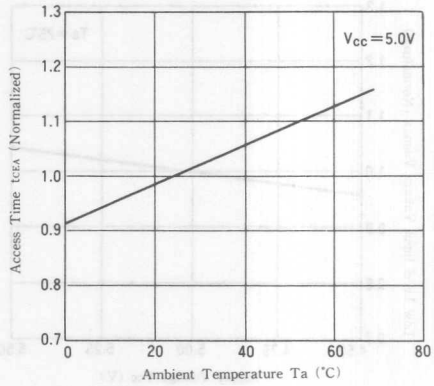
SUPPLY CURRENT VS. AMBIENT TEMPERATURE (3)



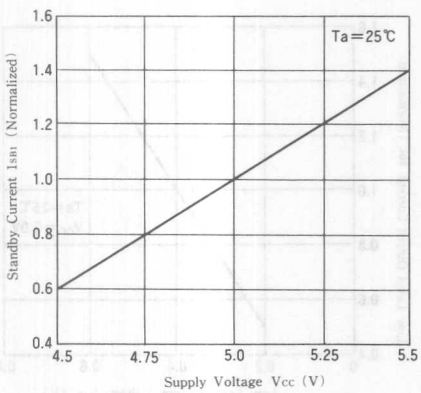
ACCESS TIME VS. SUPPLY VOLTAGE



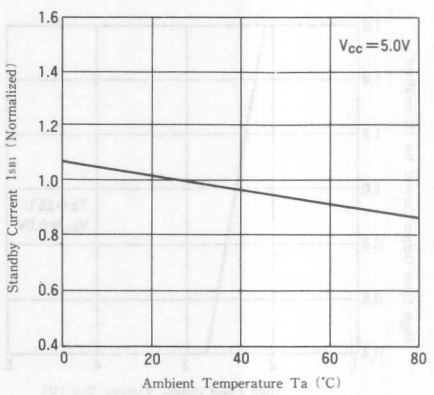
ACCESS TIME VS. AMBIENT TEMPERATURE



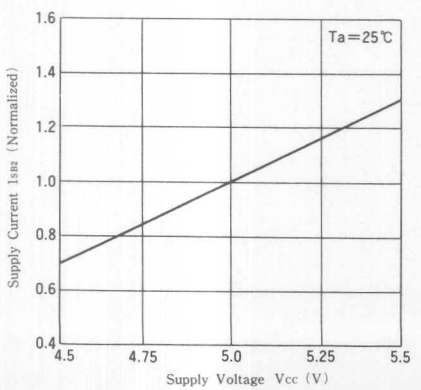
STANDBY CURRENT VS. SUPPLY VOLTAGE(1)



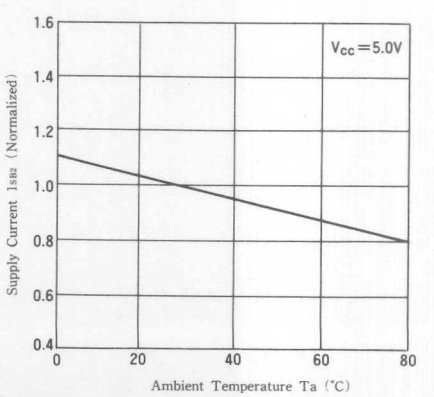
STANDBY CURRENT VS. AMBIENT TEMPERATURE (1)



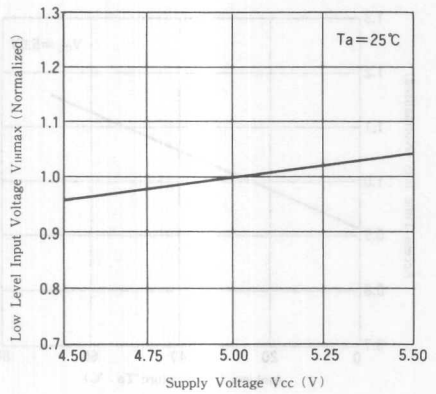
STANDBY CURRENT VS. SUPPLY VOLTAGE(2)



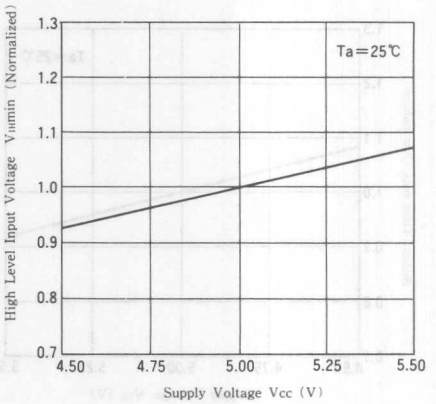
STANDBY CURRENT VS. AMBIENT TEMPERATURE(2)



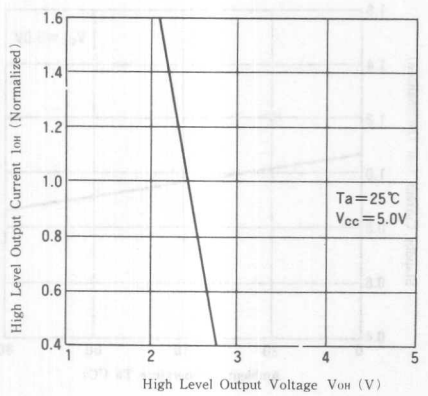
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



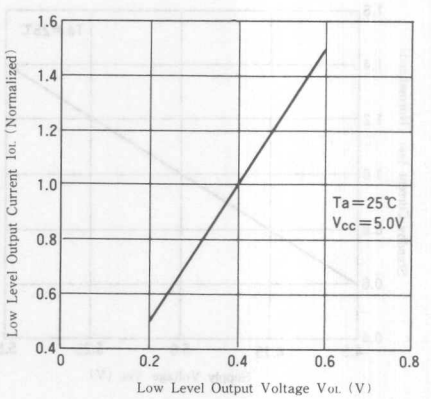
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



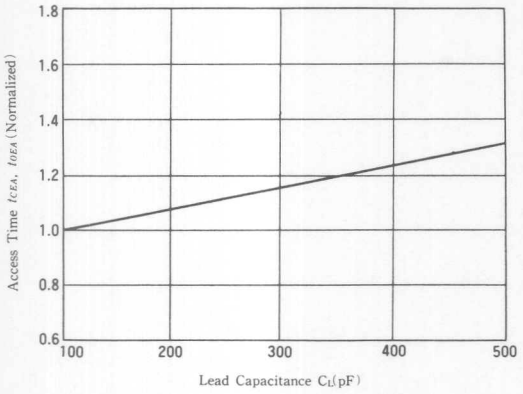
HIGH LEVEL OUTPUT CURRENT VS. OUTPUT VOLTAGE



LOW LEVEL OUTPUT CURRENT VS. OUTPUT VOLTAGE



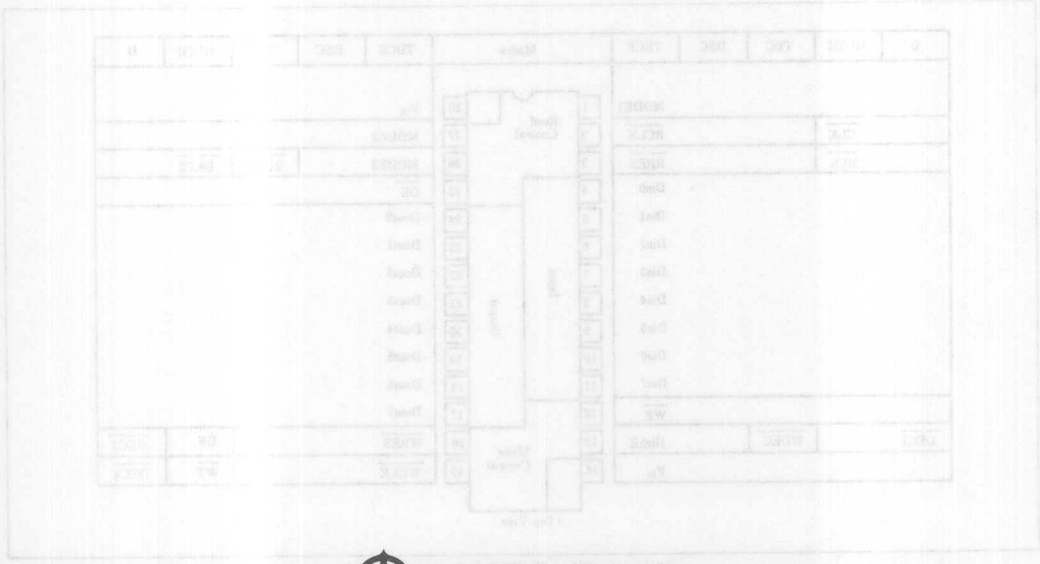
ACCESS TIME VS. LOAD CAPACITANCE



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Section 4
Video Memory

4

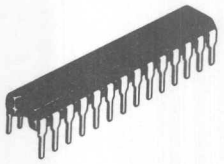


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HM63021 Series

2048-word x 8-bit Line Memory

HM63021 is a 2048-word x 8-bit static Serial Access Memory (SAM) with separate data inputs and outputs. Since it has an internal address counter, no external address signal is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memories, double-speed conversions, 1H delay lines and 1H/2H delay lines for digital TV signals. Its minimum cycle times are 28 ns and 34 ns each corresponding to 8 fsc of PAL TV signals and NTSC TV signals. All inputs and outputs are TTL-compartiable. This device is packaged in a 300-mil dual-in-line plastic package.



(DP-28N)

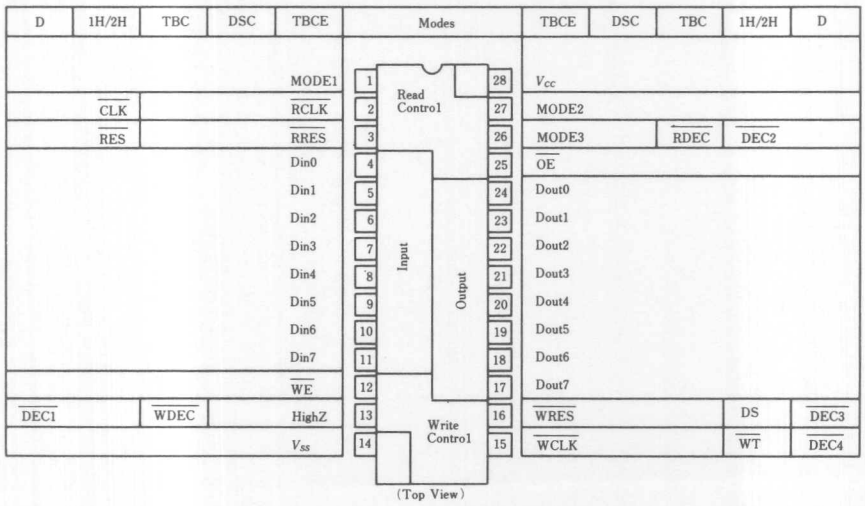
Features

- Five modes for various applications
- Corresponds to Digital TV system with 4 fsc sampling (PAL, NTSC)
- Decoder signal output pin; Fewer external circuits
- Asynchronous Read/Write operation;
  Separate address counters for Read/Write
  No Address Input required
- High Speed; Cycle Time 28/34/45 ns (min)
- Completely Static Memory; No refresh required
- 8-bit SAM with separate I/O
- Low Power; 250 mW typ. Active
- Single 5 V supply
- TTL compatible

Ordering Information

Type No.	Cycle Time	Package
HM63021P-28	28 ns	300-mil 28-pin Plastic DIP
HM63021P-34	34 ns	
HM63021P-45	45 ns	

Pin Arrangement



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Pin Description

Pin No.	Pin Name	Functions
1	MODE1	Mode Input 1 (All Modes)
2	$\overline{RCLK}/\overline{CLK}$	Read Clock Input (TBCE, DSC, TBC) Clock Input (1H/2H, D)
3	$\overline{RRES}/\overline{RES}$	Read Reset Input (TBCE, DSC, TBC) Reset Input (1H/2H, D)
4-11	Din 0 – Din 7	Data Inputs (All Modes)
12	$\overline{WE}$	Write Enable Input (All Modes)
13	High Z/$\overline{WDEC}/\overline{DEC1}$	High Impedance (TBCE, DSC) Write Decode Pulse Output (TBC) Decode Pulse Output 1 (1H/2H, D)
14	V_{SS}	Ground (All Modes)
15	$\overline{WCLK}/\overline{WT}/\overline{DEC4}$	Write Clock Input (TBCE, DSC, TBC) Write Timing Input (1H/2H) Decode Pulse Output 4 (D)
16	$\overline{WRES}/DS/\overline{DEC3}$	Write Reset Input (TBCE, DSC, TBC) Delay Select Input (1H/2H) Decode Pulse Output 3 (D)
17-24	Dout 0 – Dout 7	Data Outputs (All Modes)
25	$\overline{OE}$	Output Enable Input (All Modes)
26	MODE3/$\overline{RDEC}/\overline{DEC2}$	Mode Input 3 (TBCE) Read Decode Pulse Output (TBC) Decode Pulse Output 2 (1H/2H, D)
27	MODE2	Mode Input 2 (All Modes)
28	V_{CC}	Power Supply (+5V) (All Modes)

Mode Table

Mode Signals			Mode	Application Example
MODE1	MODE2	MODE3		
H	H	H	Time base compression/expansion (TBCE)	Picture in Picture
H	H	L	Double speed conversion (DSC)	Non interlace
H	L	– *1	Time base correction (TBC)	Time Base Corrector
L	H	– *1	1H/2H delay (1H/2H)	Vertical filter
L	L	– *1	Delay line (D)	Delay line

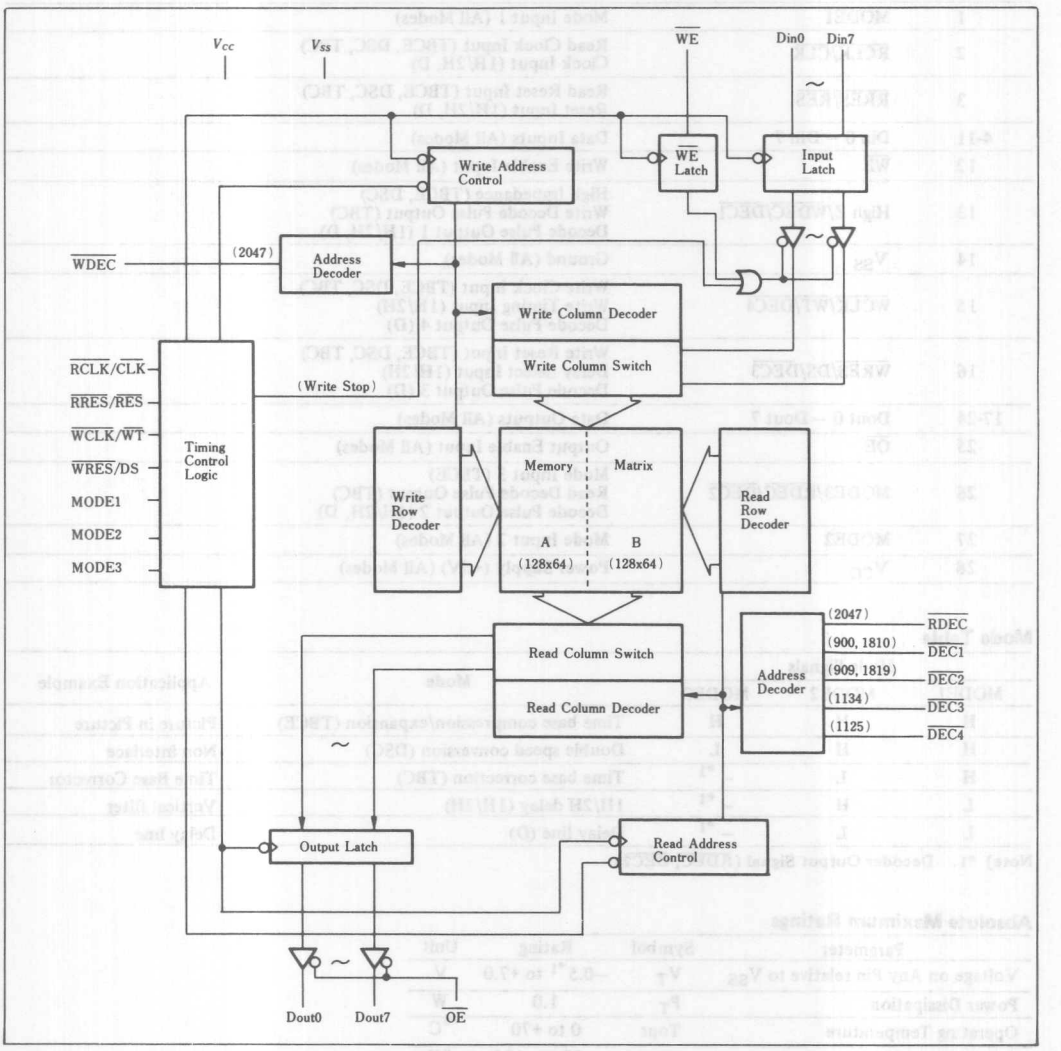
Note) *1. Decoder Output Signal ($\overline{RDEC}$, $\overline{DEC2}$)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

Note) *1. −3.5V for pulse width $\leqq$ 10 ns

Block Diagram



Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≤ 10 ns.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	10	μA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{OE}$ = V_{IH} V_{out} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	50	90	mA	Min. cycle, Iout = 0 mA
Output Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA*2, Dout 0 to Dout 7, $\overline{DEC}$ Output pin
	V_{OH}	2.4	–	–	V	I_{OH} = −4 mA, Dout 0 to Dout 7 pin
		2.4	–	–	V	I_{OH} = -1 mA, $\overline{DEC}$ Output pin

Notes) *1. Typical values are at V_{CC} = 5V, Ta = 25°C and for reference only.
*2. I_{OL} = 6mA for 45ns version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	min	typ	max	Unit	Conditions
Input Capacitance	Cin	–	–	6	pF	Vin = 0V
Output Capacitance*2	Cout	–	–	9	pF	Vout = 0V

Notes) *1. This parameter is sampled and not 100% tested.
*2. 13, 15 – 24, 26 pin

AC Characteristics (V_{CC} = 5V ± 10%, Ta = 0 to +70°C, unless otherwise noted.)

- AC Test Conditions

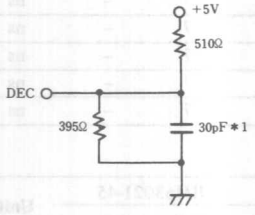
  Input and Output timing reference levels: 1.5V

  Input pulse levels: V_{SS} to 3V

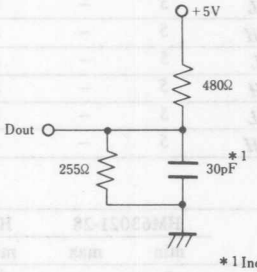
  Input rise and fall times: 5 ns

HM63021-28/34

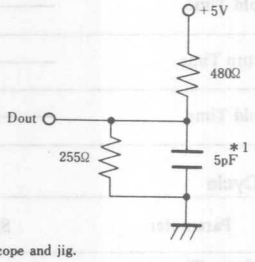
DEC Output Load



Dout Output Load (A)



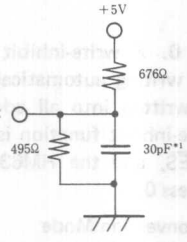
Dout Output Load (B)
(t_{OLZ}, t_{OHZ})



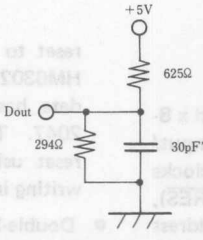
*1 Including scope and jig.

HM63021-45

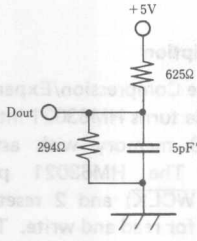
DEC Output Load



Dout Output Load (A)



Dout Output Load (B)
(t_{OLZ}, t_{OHZ})



*1 Including scope and jig

Read Cycle

Parameter		Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	28	–	34	–	45	–	ns
Read Clock Width		t_{RWL}	10	–	10	–	15	–	ns
		t_{RWH}	10	–	10	–	15	–	ns
Access Time		t_{AC}	–	20	–	25	–	30	ns
Decode Output Access Time	(fall)	t_{DA1}	–	20	–	25	–	30	ns
	(rise)	t_{DA2}	–	40	–	50	–	60	ns
Output Hold Time		t_{OH}	5	–	5	–	5	–	ns
Decode Output Hold Time	(fall)	t_{DOH1}	5	–	5	–	5	–	ns
	(rise)	t_{DOH2}	5	–	5	–	5	–	ns
Output Enable Access Time		t_{OE}	–	20	–	25	–	30	ns
Output Disable to Output in High Z		t_{OHZ}	0	15	0	20	0	25	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns

Write Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	28	–	34	–	45	–	ns
	t_{WC}(1H/2H Mode)	56	–	68	–	90	–	ns
Write Clock Width	t_{WWL}	10	–	10	–	15	–	ns
	t_{WWH}	10	–	10	–	15	–	ns
Input Data Setup Time	t_{DS}	5	–	5	–	7	–	ns
Input Data Hold Time	t_{DH}	5	–	5	–	7	–	ns
$\overline{WE}$ Setup Time	t_{WESL}	5	–	5	–	7	–	ns
	t_{WESH}	5	–	5	–	7	–	ns
$\overline{WE}$ Hold Time	t_{WEHL}	5	–	5	–	7	–	ns
	t_{WEHH}	5	–	5	–	7	–	ns
$\overline{WT}$ Setup Time	t_{WTSL}	5	–	5	–	7	–	ns
	t_{WTSH}	5	–	5	–	7	–	ns
$\overline{WT}$ Hold Time	t_{WTHL}	5	–	5	–	7	–	ns
	t_{WTHH}	5	–	5	–	7	–	ns

Reset Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		min	max	min	max	min	max	
Reset Setup Time	t_{RES}	8	–	9	–	10	–	ns
Reset Hold Time	t_{REH}	5	–	5	–	7	–	ns
Clock Setup Time Before Reset	t_{REPS}	8	–	9	–	10	–	ns
Clock Hold Time Before Reset	t_{REPH}	5	–	5	–	7	–	ns

Mode Description

- Time Base Compression/Expansion Mode
  This mode turns HM63021 into a 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address clock and are reset to address 0. A write-inhibit function of HM63021 stops writing automatically after the data has been written into all addresses 0 to 2047. The write-inhibit function is released by reset using $\overline{WRES}$, and the HM63021 restarts writing into address 0.
- Double-Speed Conversion Mode
  This mode turns HM63021 into a 1024-word x

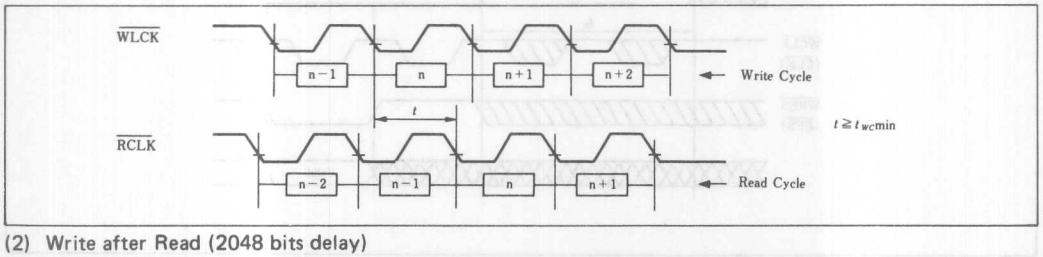
8-bit x 2 memory with asynchronous input/output. It is used for generating non-interlaced TV signals. When the original signal and the interpolated signal (1 field delay) of interlaced signals are input to the HM63021, multiplexed per dot, it outputs non-interlaced signals for each line. 8 fsc should be input to $\overline{RCLK}$ and $\overline{WCLK}$. A standard H synchronizing signal and a non-interlace H synchronizing signal are input to $\overline{WRES}$ and $\overline{RRES}$ respectively. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135-1024 = 111 bits) is ignored.

- TBC Mode
  This mode turns HM63021 into 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address at each clock and are reset to address 0. The internal address counters return to address 0 after they reach address 2047. The HM63021 outputs a write decode pulse from $\overline{WDEC}$, synchronizing it with address 2047 in the write address counter, and read a decode pulse from $\overline{RDEC}$, synchronizing with address 2047 in the read address counter. Using these pulses, the memory area can be extended easily (multiple-HM63021s can be used with ease).
- 1H/2H Delay Mode
  This mode turns HM63021 into a 1024-word x 8-bit x 2 delay line with synchronous input/output. Delay time is defined by the reset period of $\overline{RES}$. Since the HM63021 outputs a 901 decode pulse ($\overline{DEC1}$) and a 910 decode pulse ($\overline{DEC2}$), connecting $\overline{DEC2}$ to $\overline{RES}$, for example, outputs 1H- and 2H- delayed signals alternately at a 8- fsc cycle when the original signal is input at a 4- fsc cycle. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135-1024 = 111 bits) is ignored.
- Delay Line Mode
  This mode turns HM63021 into a 2048-word x 8-bit delay line with synchronous input/output. Delay time (3 to 2048 bits) is defined by the reset period of $\overline{RES}$. The delay is 2048 bits when $\overline{RES}$ is fixed High. Signals delayed by 910 bits to 1135 bits for example, can be easily obtained without external circuits by just connecting selected decoded pulses on $\overline{DEC1}$ – $\overline{DEC4}$ to $\overline{RES}$.

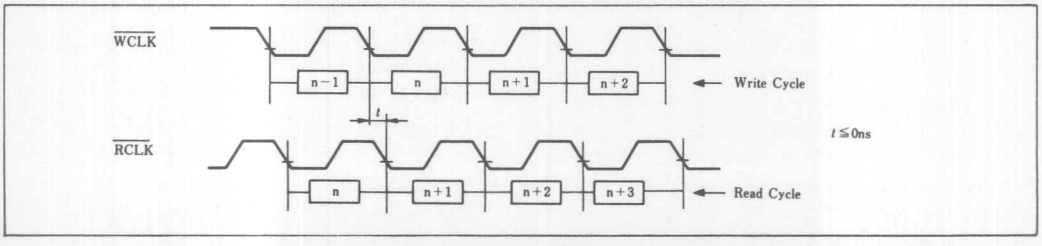
Notes on Using HM63021

- Hitachi recommends that pin 13 (high impedance) should be fixed by pulling up or down with a resistor (of several kΩ) in TBC or DSC mode.
- Hitachi recommends that the mode signal input pins and DS pin should be fixed by pulling them up or down with a resistor (of several kΩ).
- Data integrity cannot be guaranteed when mode is changed during operation.
- When a read address coincides with a write address in TBCE, TBC or DSC mode, the data is written correctly but it is not always read correctly.

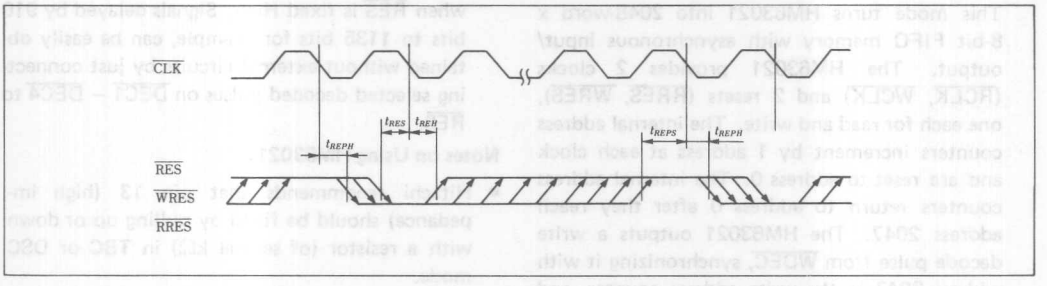
(1) Read after Write (3 bits delay)



(2) Write after Read (2048 bits delay)

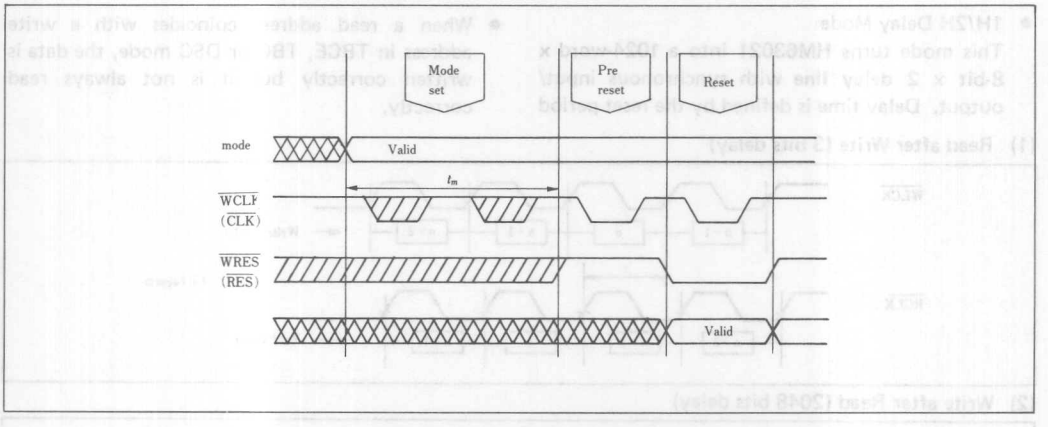


- At power on, the output of the address counter is not defined. Therefore, operations before the system is reset cannot be guaranteed, and decode signal output is not defined until after the first reset cycle.
- The decode signal is latched by a decode output latch circuit at the previous address of the internal counter address and is output synchronized with the next address. For example, $\overline{WDEC}$ in TBC mode is latched at write address 2046 and is output at write address 2047. If a write reset is performed on address 2047 at this time, the write address becomes 0 and $\overline{WDEC}$ is output.
  The same operation is performed in other modes.
- In the reset cycle, the input levels of $\overline{WRES}$, $\overline{RRES}$, $\overline{RES}$ are raised to satisfy t_{REH}, and are fixed high until t_{REPH} in the next pre-reset cycle is satisfied. The rise timings of the reset signals ($\overline{RES}$, $\overline{WRES}$, $\overline{RRES}$) are optionals provided that the t_{REPS} specification is satisfied. The timings at which $\overline{RES}$, $\overline{WRES}$, and $\overline{RRES}$ fall after pre-reset are also optional, provided that the t_{REPH} and t_{RES} specifications are satisfied.

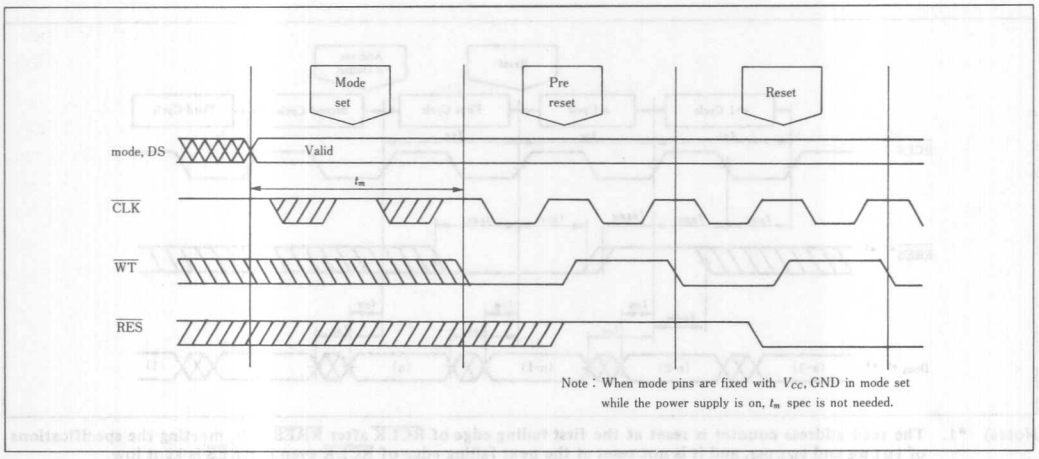


- Hitachi recommends that t_m (time between mode set and the first cycle (Pre-reset)) should be kept for 2 cycle time (56ns / 68ns / 90ns) or more while the power supply is on.

(1) TBCE, TBC, DSC and Delay Line Mode



(2) 1H / 2H Delay Mode



Decode Signal

When internal address counter reaches the specified address as shown below, decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address counter	Timing of the Output Signal	Operation
TBC	13	$\overline{\text{WDEC}}$	Write 2047	After Write 2047	Completion of Writing on all bits is detected.
	26	$\overline{\text{RDEC}}$	Read 2047	Output of 2046	Completion of Reading from all bits is detected.
1H/2H	13	$\overline{\text{DEC1}}$	Read 900 (2H)	Output of 900 (1H)	By inputting this signal to pin #3, 901/1802-bit delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909 (2H)	Output of 909 (1H)	By inputting this signal to pin #3, 910/1820-bit delay output is obtained.
Delay line	13	$\overline{\text{DEC1}}$	Read 900	Output of 899	By inputting this signal to pin #3, 901-bit delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC1}}$ is devided into two, 1811-bit delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909	Output of 908	By inputting this signal to pin #3, 910-bit delay output is obtained.
			Read 1819	Output of 1818	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC2}}$ is devided into two, 1820-bit delay output is obtained.
	16	$\overline{\text{DEC3}}$	Read 1134	Output of 1133	By inputting this signal to pin #3, 1135-bit delay output is obtained.
	15	$\overline{\text{DEC4}}$	Read 1125	Output of 1124	By inputting this signal to pin #3, 1126-bit delay output is obtained.

Note) When counter is reset by Reset Signal ($\overline{\text{RRES}}$, $\overline{\text{RES}}$, $\overline{\text{WRES}}$), address becomes 0.

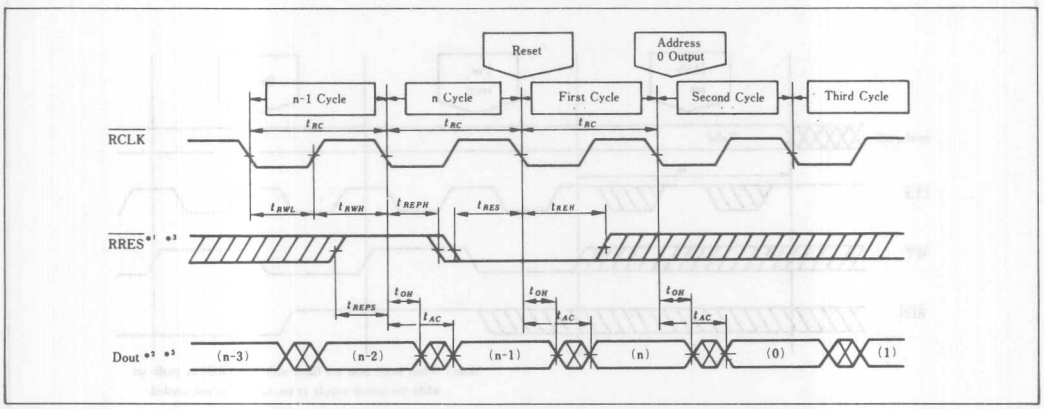
Write-inhibit Function

When internal address counter is as follows, writing is inhibited automatically for the next cycle. The write-inhibit function is cancelled by reset through $\overline{\text{WRES}}$ or $\overline{\text{RES}}$.

Mode	Write-inhibit Function (internal counter address)
TBCE	Write-inhibit after address 2047
DSC	Write-inhibit after address 1023 x 2
TBC	No function
1H/2H	Write-inhibit after address 1023
D	No function

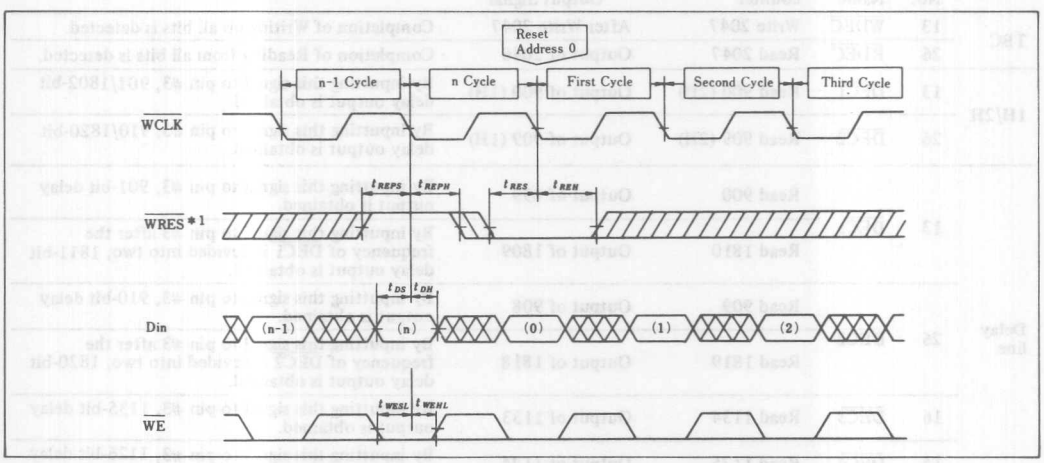
Note) When address counter is reset by $\overline{\text{WRES}}$ or $\overline{\text{RES}}$, address becomes 0.

Read Reset Cycle (TBCE, TBC Modes)



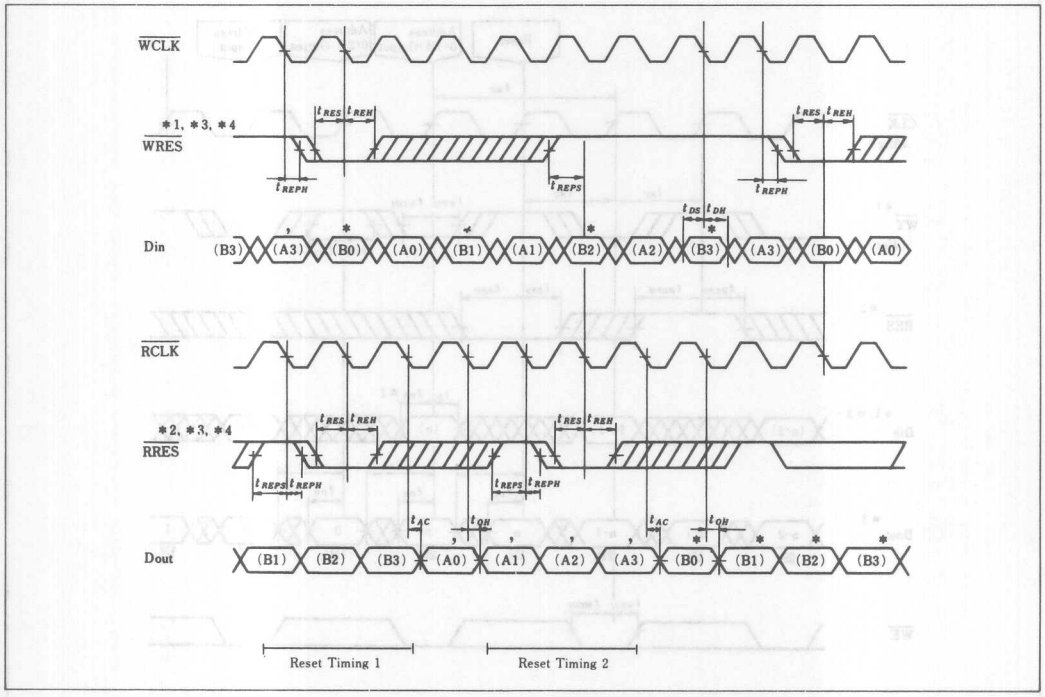
Notes) *1. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
*2. Output is from the read address of the previous cycle.
*3. When $\overline{RRES}$ is fixed high, the data at the read address counter is reset after the data of address 2047 is output, and the same operation restarts.

Write Reset Cycle (TBCE, TBC Modes)



Note) The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

Reset Cycle (DSC Mode)



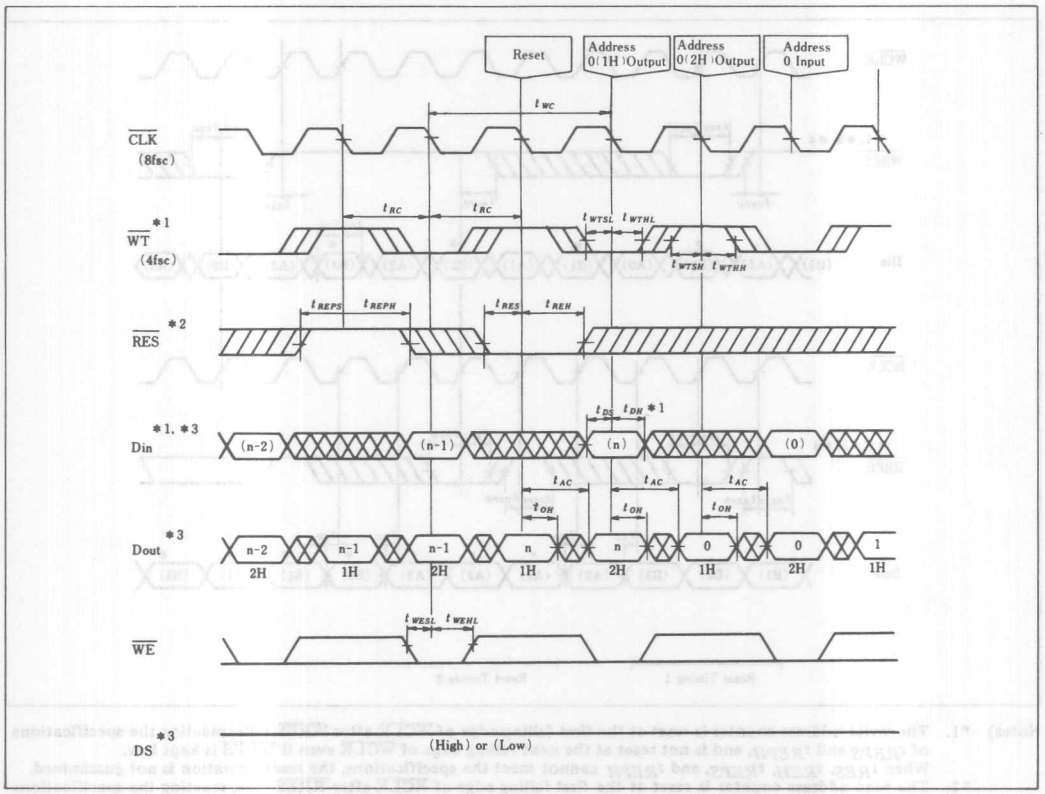
Notes) *1. The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

*2. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} cannot meet the specifications, reset operation is not guaranteed.

*3. When t_{REPH}, t_{RES}, t_{REH} ($\overline{WRES}$ to $\overline{WCLK}$), or t_{REPS}, t_{REPH}, t_{RES}, t_{REH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the output of video signal A is not guaranteed. (Reset Timing I).

*4. When t_{REPS} ($\overline{WRES}$ to $\overline{RCLK}$), or t_{RES}, t_{REH}, t_{REPS}, t_{REPH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the interpolation signal B is not guaranteed. (Reset Timing II).

Reset Cycle (1H/2H Mode)

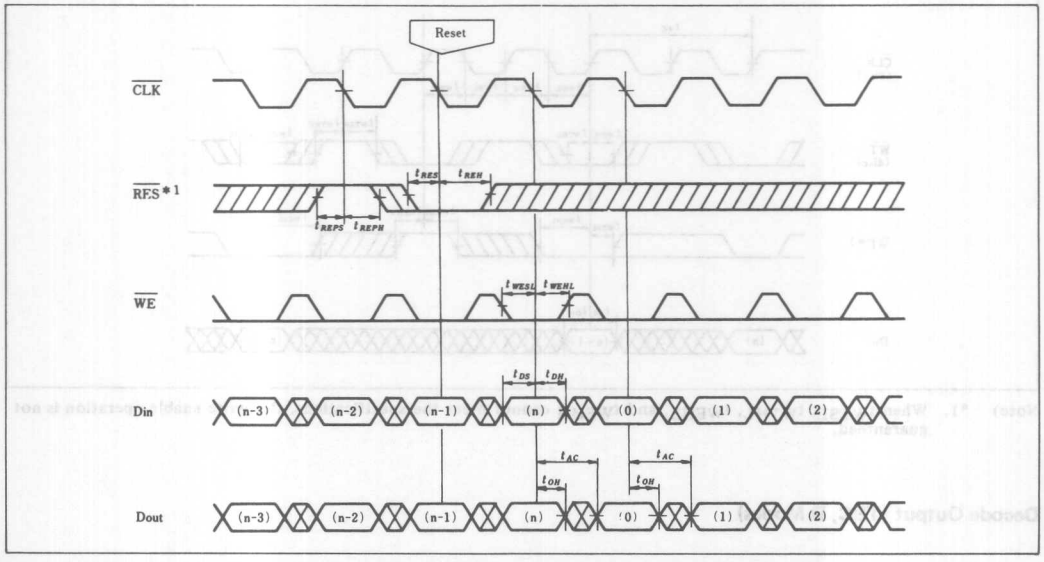


Notes) *1. $\overline{WT}$ is the input during half cycle of $\overline{CLK}$, meeting the specifications of t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH}. Data is written when $\overline{WT}$ is low. Reset is possible when $\overline{WT}$ is high.

*2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

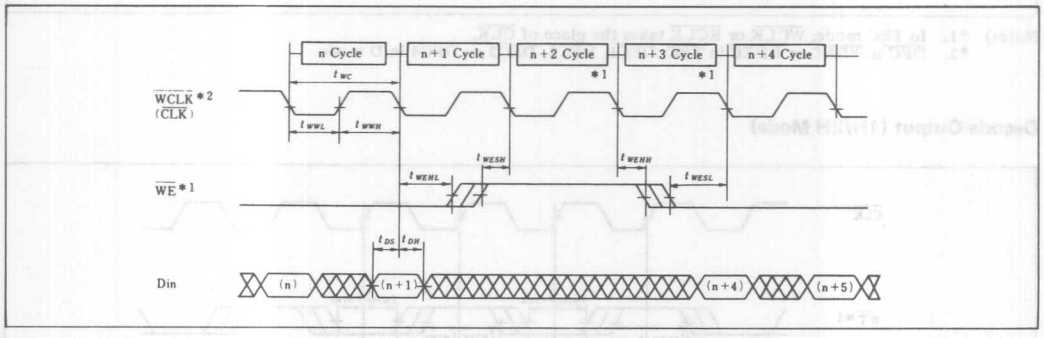
*3. When DS is fixed high, 1H output data is delayed by n bits and 2H output data is delayed by 2n bits where 2n is the reset cycle of $\overline{RES}$.
When DS is fixed low, 1H output data is delayed by n-5 bits and 2H output data is delayed by 2n-5 bits.

Reset Cycle (D Mode)



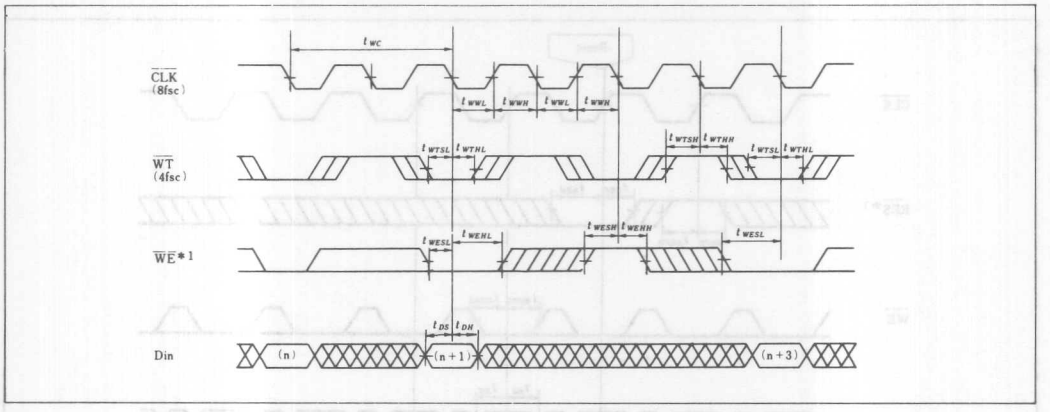
Note) *1. The read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

Write Enable (TBCE, DSC, TBC, D Modes)



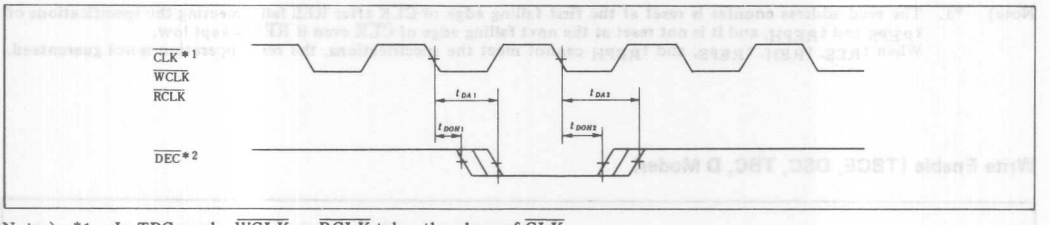
Notes) *1. When t_{WEHL}, t_{WESH}, t_{WEHH}, and t_{WESL} cannot meet this specifications, the write enable operation is not guaranteed.
*2. In the delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



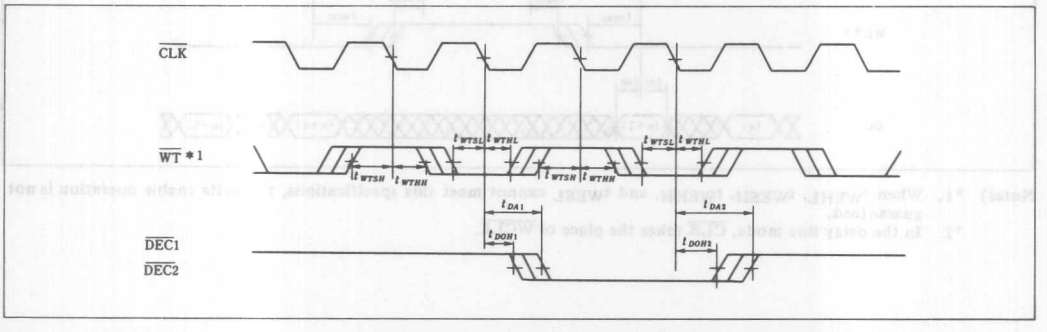
Note) *1. When t_{WTSL}, t_{WTHL}, t_{WEHL}, and t_{WEHH} cannot meet the specifications, the write enable operation is not guaranteed.

Decode Output (TBC, D Modes)



Notes) *1. In TBC mode, $\overline{WCLK}$ or $\overline{RCLK}$ takes the place of $\overline{CLK}$.
*2. $\overline{DEC}$ is $\overline{WDEC}$ or $\overline{RDEC}$ in $\overline{TBC}$, $\overline{DEC1}$, $\overline{DEC2}$, $\overline{DEC3}$ or $\overline{DEC4}$ in D mode.

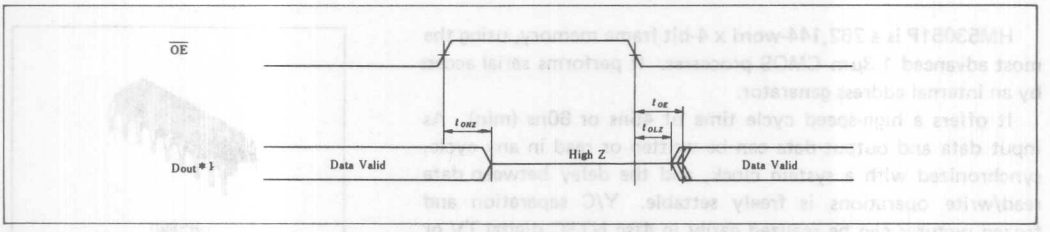
Decode Output (1H/2H Mode)



Note) *1. When t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH} cannot meet the specifications, the decode output operation is not guaranteed.

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Output Enable (All Modes)



Note) *1. Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with Output Load B. This parameter is sampled and not 100% tested.

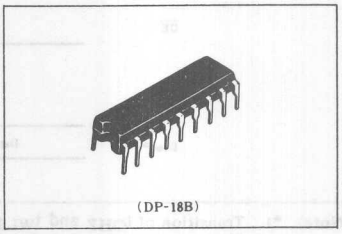
HM53051P*

* An Application Note is available for this device, contact your local Hitachi representative.

262144-word x 4-bit Frame Memory

HM53051P is a 262,144-word x 4-bit frame memory, using the most advanced 1.3μm CMOS processes. It performs serial access by an internal address generator.

It offers a high-speed cycle time of 45ns or 60ns (min). As input data and output data can be written or read in any cycle, synchronized with a system clock, and the delay between data read/write operations is freely settable. Y/C separation and frozen pictures can be realized easily in 4fsc NTSC digital TV or VCR systems. Also, it enables random access in 32-word x 4-bit data block. With this function, picture in picture or a multiplexed picture can be displayed with ease.

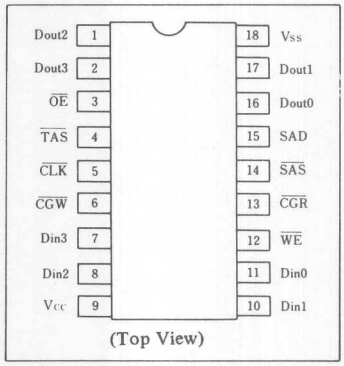


(DP-18B)

Features

- 262,144-word x 4-bit serial access memory
- Organized with dual ports
  - Serial input x 4-bit
  - Serial output x 4-bit
- High Speed
  - Read/Write Cycle Time: 45ns/60ns (min)
  - Access Time: 35ns/40ns (max)
- Semi-synchronous Read/Write Cycle
- Low Power
  - Active: 200mW (typ)
- Random Access in 32-word x 4-bit blocks
- External Refresh Control is unnecessary

Pin Arrangement



(Top View)

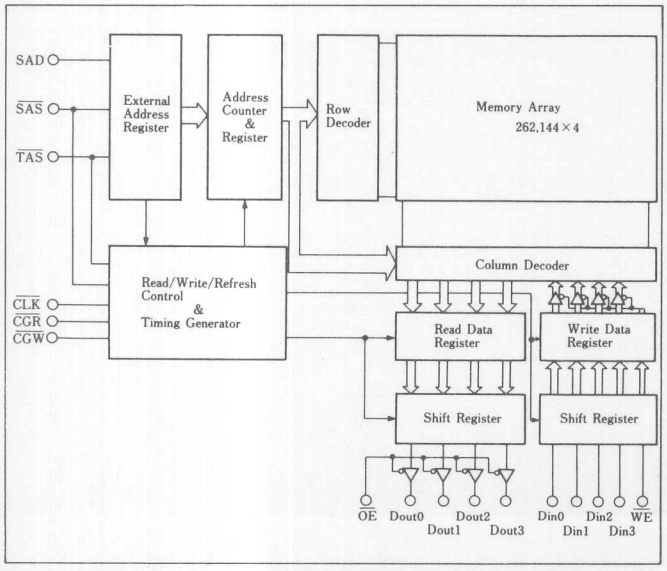
Ordering Information

Type No.	Cycle Time	Package
HM53051P-45	45ns	300 mil 18-pin
HM53051P-60	60ns	Plastic DIP

Pin Description

Pin Name	Function
Din	Data Input
Dout	Data Output
$\overline{OE}$	Output Enable
$\overline{TAS}$	Transfer Address Strobe
$\overline{CLK}$	System Clock
$\overline{CGW}$	Clock Gate (Write)
$\overline{CGR}$	Clock Gate (Read)
SAD	Serial Address
$\overline{SAS}$	Serial Address Strobe
$\overline{WE}$	Write Enable

Block Diagram



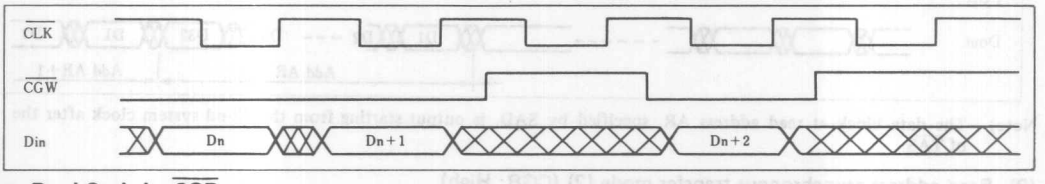
Functional Description

Serial access memory with I/O separated

Read cycle and write cycle of HM53051 can be operated independently synchronized with a system clock. It realizes time compression or expansion for picture in picture in digital TV, for example.

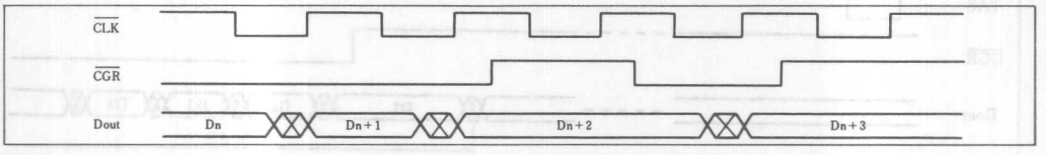
- **Write cycle by $\overline{CGW}$**

Write data are taken in at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter write cycle (cycle time is defined by system clock cycle time). Time is compressed easily with $\overline{CGW}$.



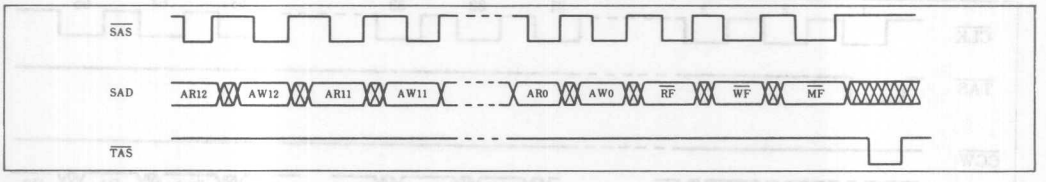
- **Read Cycle by $\overline{CGR}$**

Read data is output at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter read cycle (cycle time is defined by system clock time). Time is expanded is realized easily with $\overline{CGR}$.



Random Access

The HM53051 is also capable of random access by serial address input, SAD. Random access by the unit of 32-word x 4-bit is performed, when $\overline{TAS}$ is low after read address (AR0 – AR12), write address (AW0 – AW12) and mode setting flags, $\overline{RF}$ (Read Flag), $\overline{WF}$ (Write Flag) and $\overline{MF}$ (Mode Flag) are read into by $\overline{SAD}$ with synchronous $\overline{SAS}$. In order to output data continuously, the address specified by $\overline{SAD}$ increments automatically.



Mode Programming

Operation mode in HM53051 is programmed by the combination of SAD 5-bit.

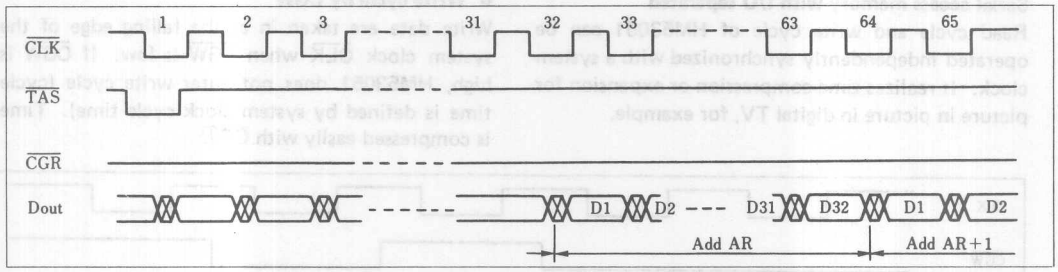
$\overline{MF}$	$\overline{WF}$	$\overline{RF}$	AW0	AR0	Mode
0	0	0	x	x	Write/read address asynchronous transfer
0	0	1	x	x	Write address asynchronous transfer
0	1	0	x	x	Read address asynchronous transfer
0	1	1	x	x	–
1	0	0	x	x	Write/read address synchronous transfer
1	0	1	x	x	Write address synchronous transfer
1	1	0	x	x	Read address synchronous transfer
1	1	1	1	1	System reset
1	1	1	0	0	Inhibit
1	1	1	0	1	
1	1	1	1	0	

Note) x means Don't care.

Read/Write Address Asynchronous Transfer Mode

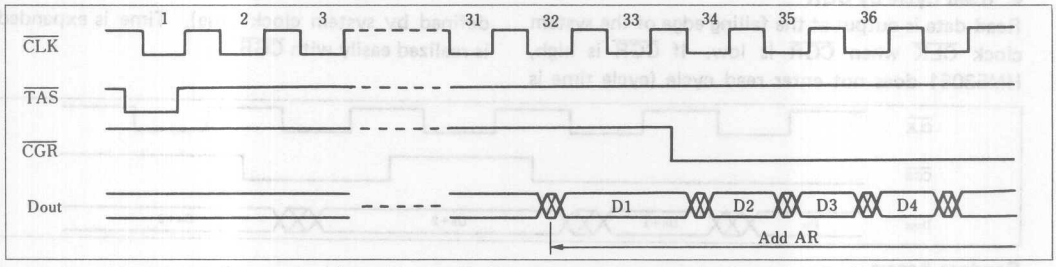
- **Read address asynchronous transfer mode**

(1) Read address asynchronous transfer mode (1) ($\overline{CGR}$: Low)



Note) The data block at read address AR, specified by SAD, is output starting from the 32-nd system clock after the of $\overline{TAS}$.

(2) Read address asynchronous transfer mode (2) ($\overline{CGR}$: High)

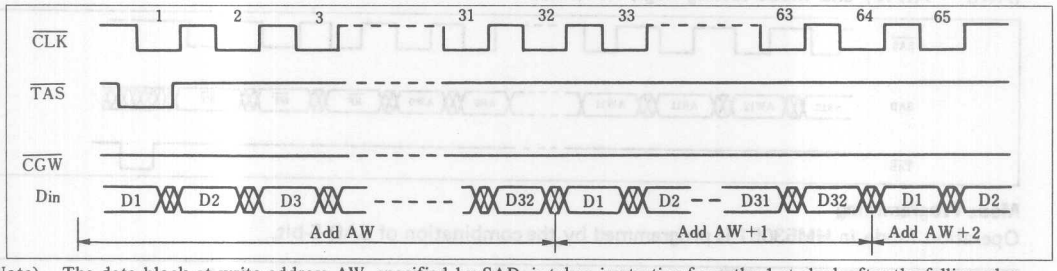


Notes) *1. The data block at read address AR, specified by SAD, is output starting from the 32-nd system clock after the falling of $\overline{TAS}$.

*2. If $\overline{CGR}$ is turned to low after 33-rd clock from the falling edge of $\overline{TAS}$, the data at read address AR (D2, D3, D4 . . .) is output with synchronous $\overline{CLK}$ while $\overline{CGR}$ is low.

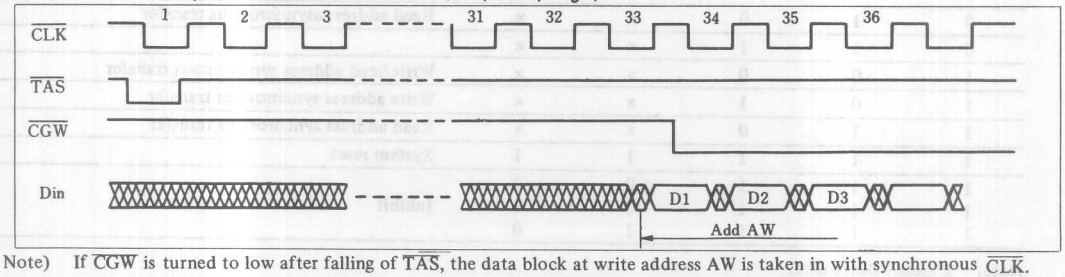
- **Write address asynchronous transfer mode**

(1) Write address asynchronous transfer mode (1) ($\overline{CGW}$: Low)



Note) The data block at write address AW, specified by SAD, is taken in starting from the 1-st clock after the falling edge of $\overline{TAS}$.

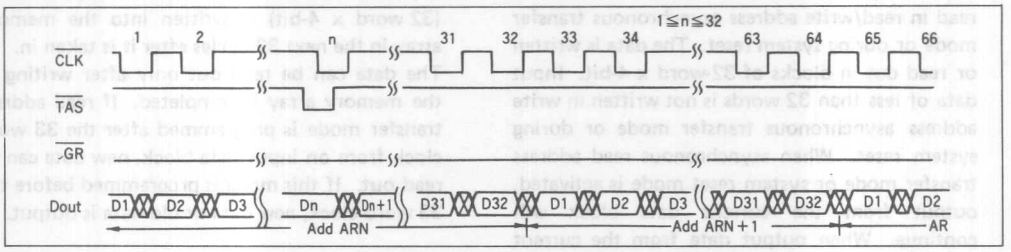
(2) Write address asynchronous transfer mode (2) ($\overline{CGW}$; High)



Note) If $\overline{CGW}$ is turned to low after falling of $\overline{TAS}$, the data block at write address AW is taken in with synchronous $\overline{CLK}$.

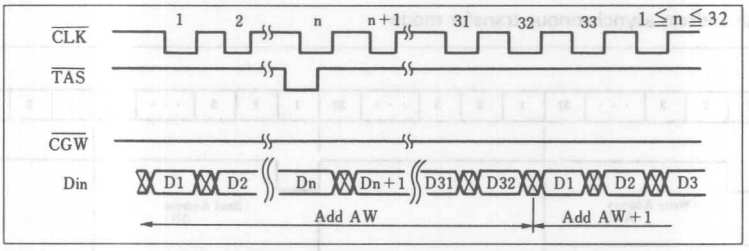
Read/Write Address Synchronous Transfer Mode

- Read address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block at read address AR, specified by SAD, is output after the data block at the present read address ARN, and the next address ARN+1 is put out.

- Write address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block being written is taken into write address AW.

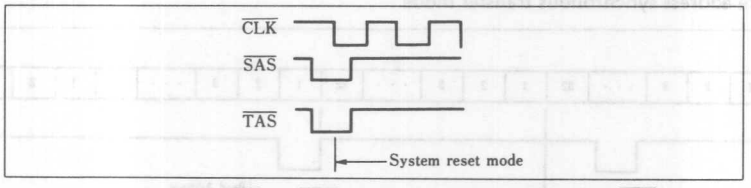
System Reset Mode

System reset mode is the same as read/write address asynchronous transfer mode except that read/write address are reset to 0.

- System reset by SAD

Note) System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0, and AR0 are all high.

- System reset by $\overline{SAS}$ and $\overline{TAS}$



Note) System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of the $\overline{CLK}$.

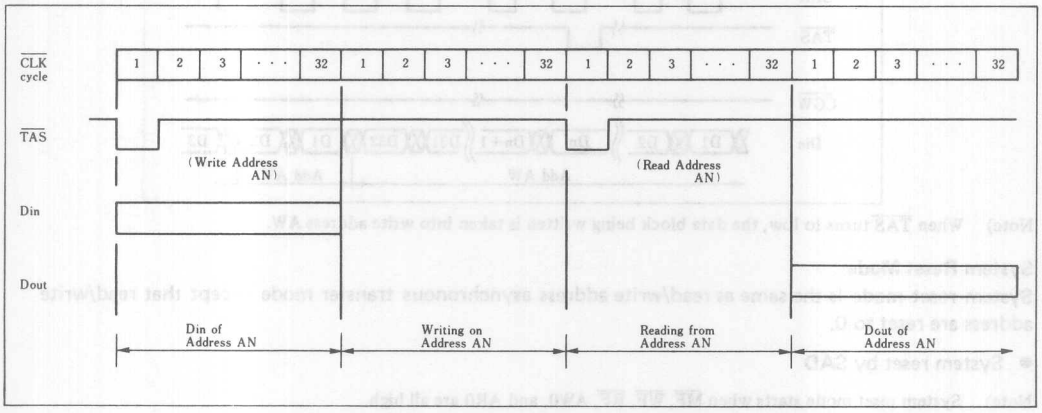
- 1 field delay

Note) Field-delayed data is output, when $\overline{CGR}$ and $\overline{CGW}$ turn to high before the system reset at the beginning of every field, and turn to low simultaneously after the 33rd clock from the system reset.

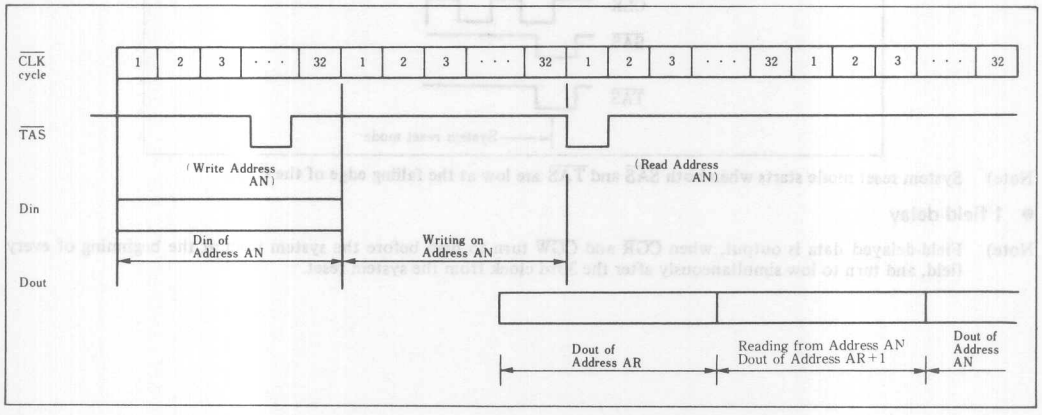
Notes on Using HM53051

- Input/output data of 32 words is not written or read in read/write address asynchronous transfer mode or during system reset. The data is written or read out in blocks of 32-word x 4-bit. Input data of less than 32 words is not written in write address asynchronous transfer mode or during system reset. When asynchronous read address transfer mode or system reset mode is activated, output from the current data block will continue. When output data from the current data block is finished, the next data block is not read out if it has less than 32 words.
- Input data is not read out immediately. The data (32 word x 4-bit) is written into the memory array in the next 32 cycles after it is taken in. The data can be read out only after writing to the memory array is completed. If read address transfer mode is programmed after the 33 word clock from on input data block, new data can be read out. If this mode is programmed before the 33 word clock, new data or old data is output.

(1) Read/write address asynchronous transfer mode



(2) Read/write address synchronous transfer mode



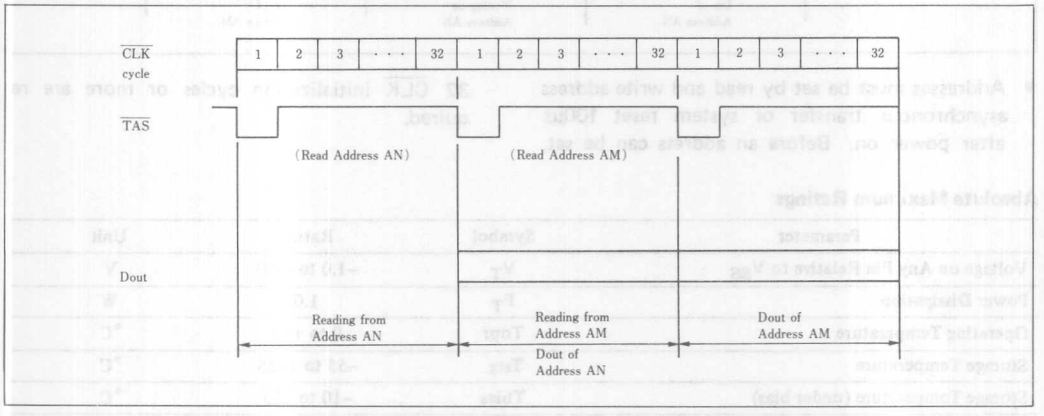
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- **Mode programming**

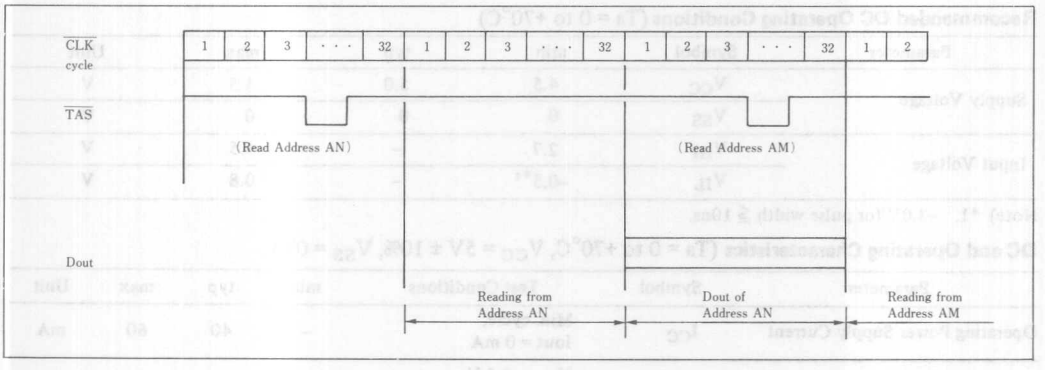
Do not reprogram read address transfer mode before a read operation of the previous read address transfer mode or system reset mode is completed. If it is reprogrammed during a read operation, address becomes invalid, and the device may malfunction.

Do not reprogram write address transfer mode or system reset mode before a write operation of the previous write address transfer mode or system reset mode is completed. If it is reprogrammed during a write operation, address become invalid, and the device may malfunction.

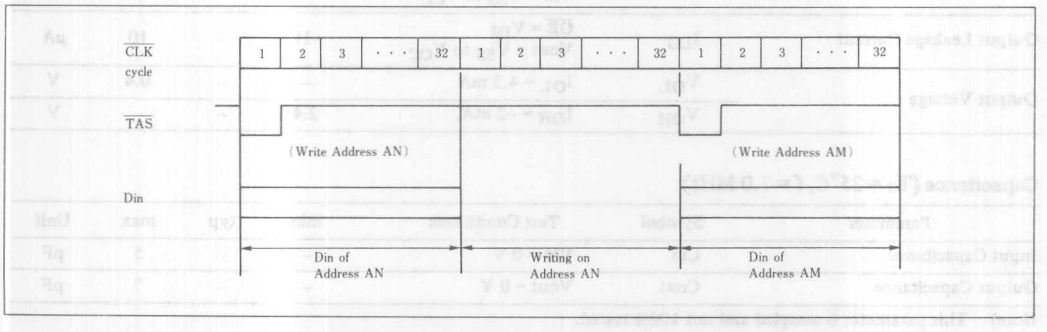
(1) Read address asynchronous transfer mode



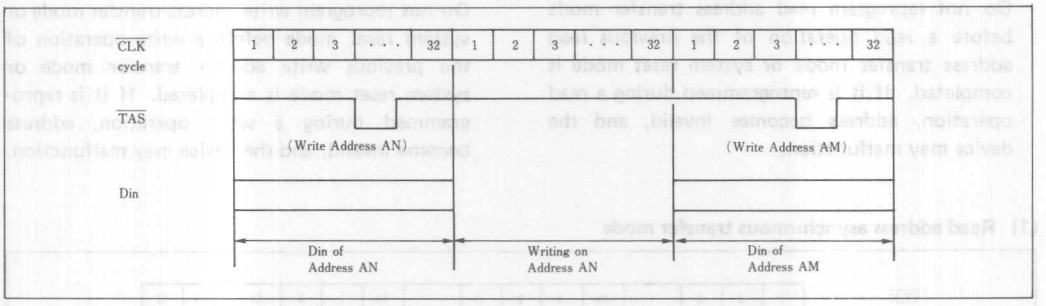
(2) Read address synchronous transfer mode



(3) Write address asynchronous transfer mode



(4) Write address synchronous transfer mode



- Addresses must be set by read and write address asynchronous transfer or system reset 100μs after power on. Before an address can be set, 32 $\overline{CLK}$ initialization cycles or more are required.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature (under bias)	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.7	–	6.5	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 10ns.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Operating Power Supply Current	I_{CC}	Min. cycle, Iout = 0 mA	–	40	60	mA
Input Leakage Current	I_{LI}	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, Vout = V_{SS} to V_{CC}	−10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 4.2 mA	–	–	0.4	V
	V_{OH}	I_{OH} = −2 mA,	2.4	–	–	V

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	Cin	Vin = 0 V	–	–	5	pF
Output Capacitance	Cout	Vout = 0 V	–	–	7	pF

Note) This parameter is sampled and not 100% tested.

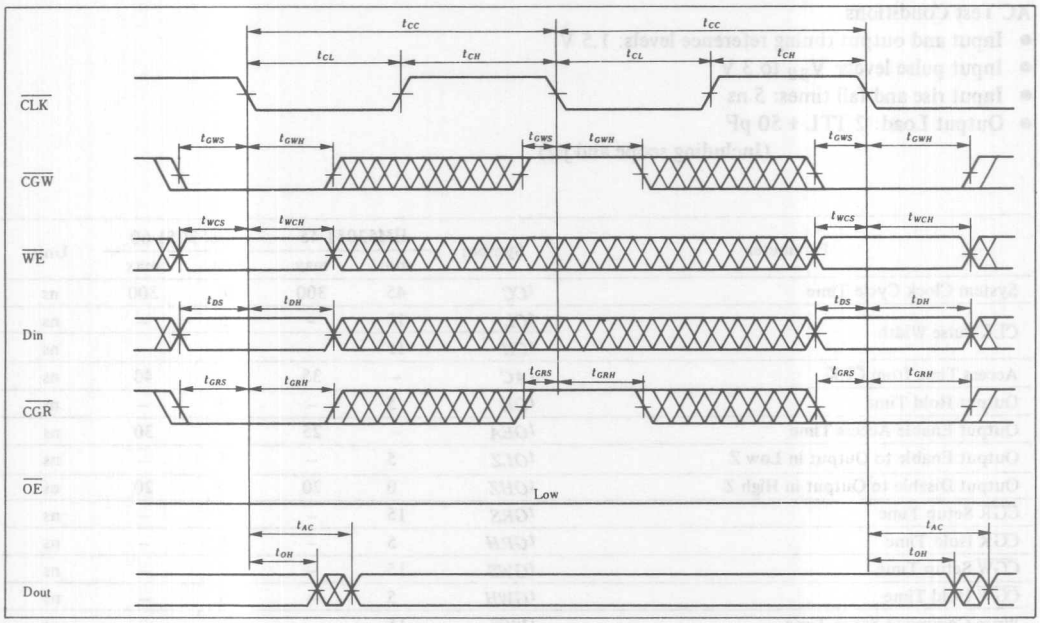
AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 5 ns
- Output Load: 2 TTL + 50 pF
  (Including scope and jig)

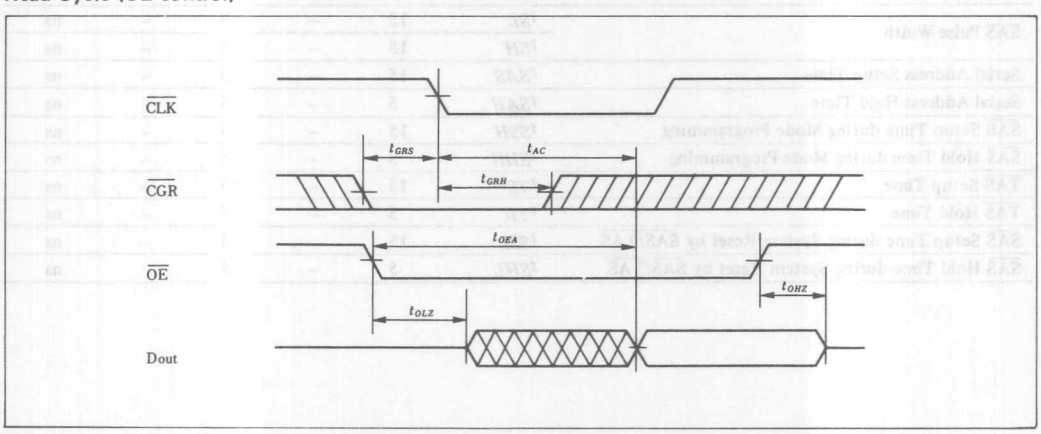
Parameter	Symbol	HM53051-45		HM53051-60		Unit
		min	max	min	max	
System Clock Cycle Time	t_{CC}	45	300	60	300	ns
$\overline{CLK}$ Pulse Width	t_{CL}	15	–	15	–	ns
	t_{CH}	15	–	15	–	ns
Access Time from $\overline{CLK}$	t_{AC}	–	35	–	40	ns
Output Hold Time	t_{OH}	5	–	8	–	ns
Output Enable Access Time	t_{OEA}	–	25	–	30	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	20	0	20	ns
$\overline{CGR}$ Setup Time	t_{GRS}	15	–	15	–	ns
$\overline{CGR}$ Hold Time	t_{GRH}	5	–	5	–	ns
$\overline{CGW}$ Setup Time	t_{GWS}	15	–	15	–	ns
$\overline{CGW}$ Hold Time	t_{GWH}	5	–	5	–	ns
Write Command Setup Time	t_{WCS}	15	–	15	–	ns
Write Command Hold Time	t_{WCH}	5	–	5	–	ns
Data Input Setup Time	t_{DS}	15	–	15	–	ns
Data Input Hold Time	t_{DH}	5	–	5	–	ns
$\overline{SAS}$ Cycle Time	t_{SC}	45	–	60	–	ns
$\overline{SAS}$ Pulse Width	t_{SL}	15	–	15	–	ns
	t_{SH}	15	–	15	–	ns
Serial Address Setup Time	t_{SAS}	15	–	15	–	ns
Serial Address Hold Time	t_{SAH}	5	–	5	–	ns
$\overline{SAS}$ Setup Time during Mode Programming	t_{SSH}	15	–	15	–	ns
$\overline{SAS}$ Hold Time during Mode Programming	t_{SHH}	5	–	5	–	ns
$\overline{TAS}$ Setup Time	t_{TS}	15	–	15	–	ns
$\overline{TAS}$ Hold Time	t_{TH}	5	–	5	–	ns
$\overline{SAS}$ Setup Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SSL}	15	–	15	–	ns
$\overline{SAS}$ Hold Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SHL}	5	–	5	–	ns

Read/Write Cycle



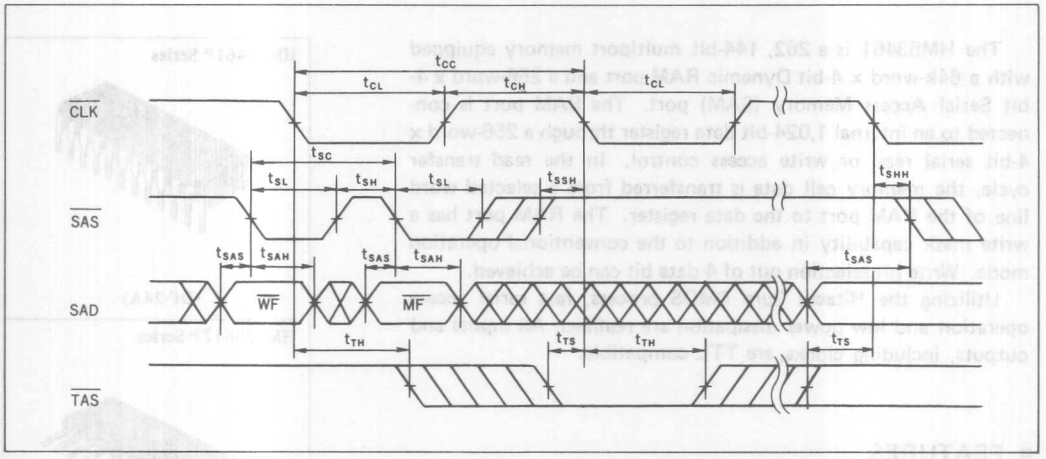
Notes) *1. Write Cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data are not written when $\overline{WE}$ is high. Time-compression mode is realized by controlling $\overline{CGW}$.
*2. Read cycle starts when $\overline{CGR}$ is low. Time-expansion mode is realized by controlling $\overline{CGR}$.

Read Cycle ($\overline{OE}$ control)



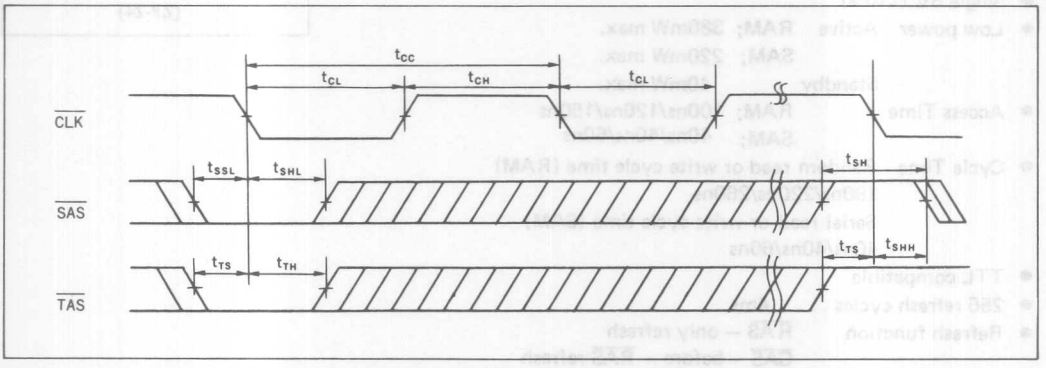
Notes) *1. t_{OHZ} is defined by the time at which the output achieves the open circuit condition.
*2. t_{OLZ} and t_{OHZ} are sampled and not 100% tested.

Mode Selection



Note) $\overline{SAS}$ operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of the $\overline{CLK}$, the address transfer cycle starts. $\overline{SAS}$ should be high during the address transfer cycle.

$\overline{SAS}$, $\overline{TAS}$ Reset Mode



Note) The mode which was selected by SAD before $\overline{SAS}$ and $\overline{TAS}$ reset, if $\overline{SAS}$ and $\overline{TAS}$ are reset, should be changed because SAD is newly taken into by SAS. The mode should be reselected by SAD after $\overline{SAS}$ and $\overline{TAS}$ reset.

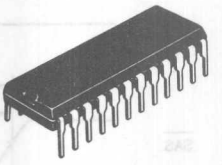
HM53461 Series

65,536-word x 4-bit Multiport CMOS Video RAM

The HM53461 is a 262, 144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

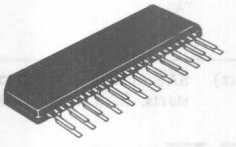
Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53461P Series



(DP-24A)

HM53461ZP Series



(ZP-24)

■ FEATURES

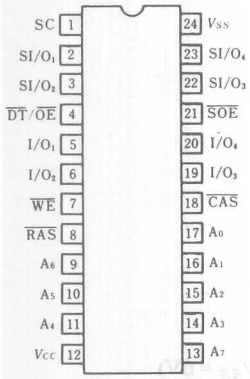
- Multiport organization
  (RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low power Active RAM; 380mW max.
  SAM; 220mW max.
  Standby 40mW max.
- Access Time RAM; 100ns/120ns/150ns
  SAM; 40ns/40ns/60ns
- Cycle Time Random read or write cycle time (RAM)
  190ns/220ns/260ns
  Serial read or write cycle time (SAM)
  40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles 4ms
- Refresh function $\overline{RAS}$ – only refresh
  $\overline{CAS}$ – before – $\overline{RAS}$ refresh
  Hidden refresh
- Data transfer operation (RAM⇄SAM)
- Fast serial access operation asynchronized with RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM53461P-10	100ns	400 mil 24-pin Plastic DIP
HM53461P-12	120ns	
HM53461P-15	150ns	
HM53461ZP-10	100ns	24-pin Plastic ZIP
HM53461ZP-12	120ns	
HM53461ZP-15	150ns	

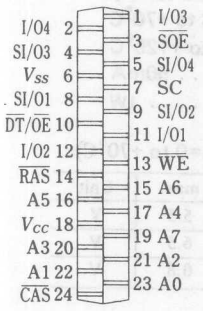
■ PIN ARRANGEMENT

● HM53461P Series



(Top View)

● HM53461ZP Series

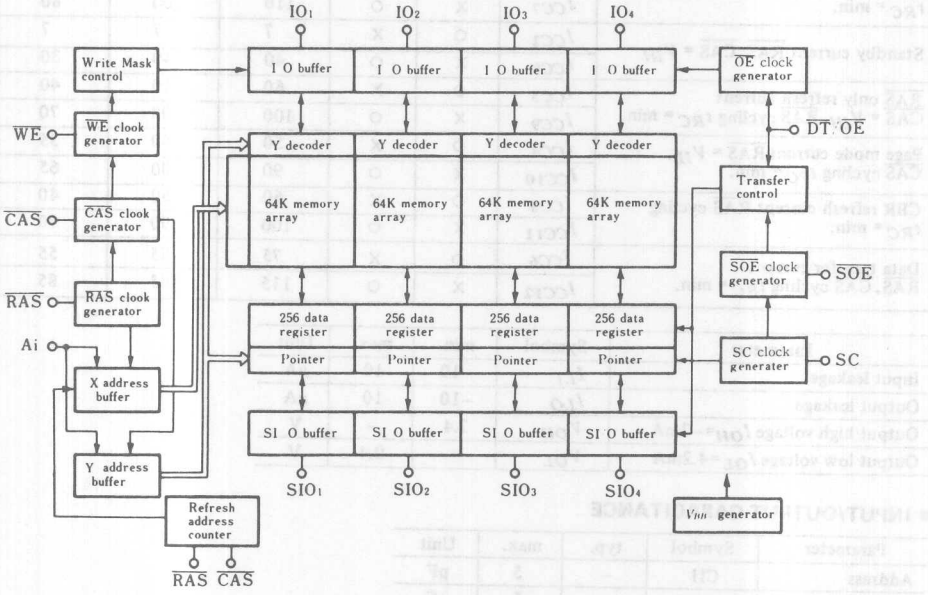


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	-0.5*2	–	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. -3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT		HM53461 -10	HM53461 -12	HM53461 -15	Unit
		Standby	Active				
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	O	X	70	60	50	mA
	I_{CC7}	X	O	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	O	X	7	7	7	mA
	I_{CC8}	X	O	40	40	30	mA
$\overline{RAS}$ only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	O	X	60	50	40	mA
	I_{CC9}	X	O	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	O	X	50	40	35	mA
	I_{CC10}	X	O	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	O	X	60	50	40	mA
	I_{CC11}	X	O	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	O	X	75	65	55	mA
	I_{CC12}	X	O	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	-10	10	μA
Output leakage	I_{LO}	-10	10	μA
Output high voltage I_{OH}=-2mA	V_{OH}	2.4	–	V
Output low voltage I_{OL}=4.2mA	V_{OL}	–	0.4	V

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI1	–	5	pF
Clocks	CI2	–	5	pF
I/O, SI/O	$C_{I/O}$	–	7	pF

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■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10), 11)]

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	

(to be continued)

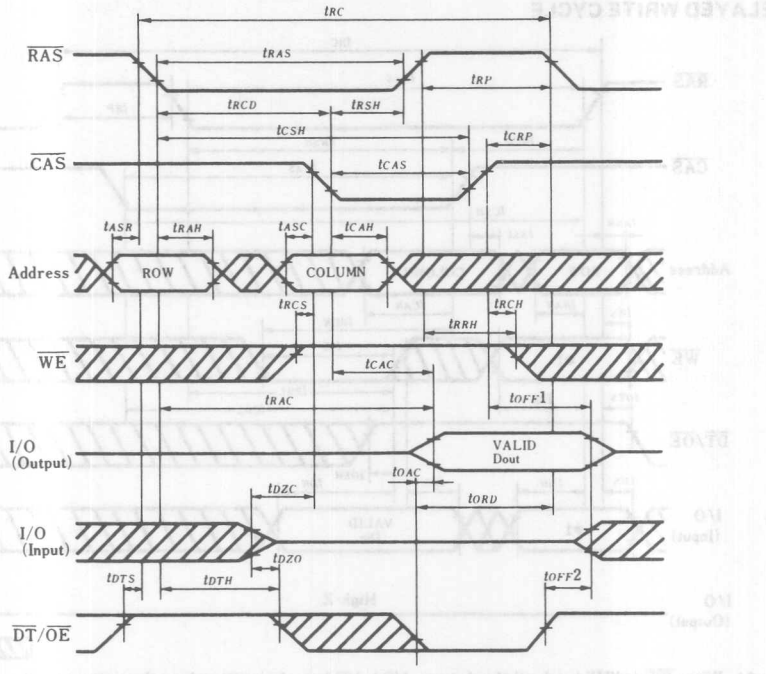
Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time(Read Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ms	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Setup Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

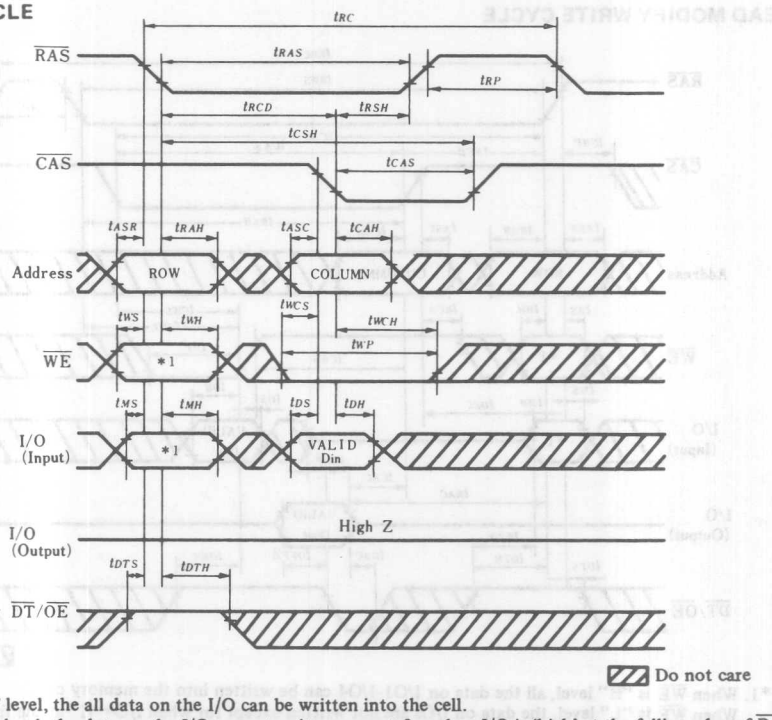
1. AC measurements assume t_T=5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC} (max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50pF.
11. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

■ WAVE FORMS

• READ CYCLE

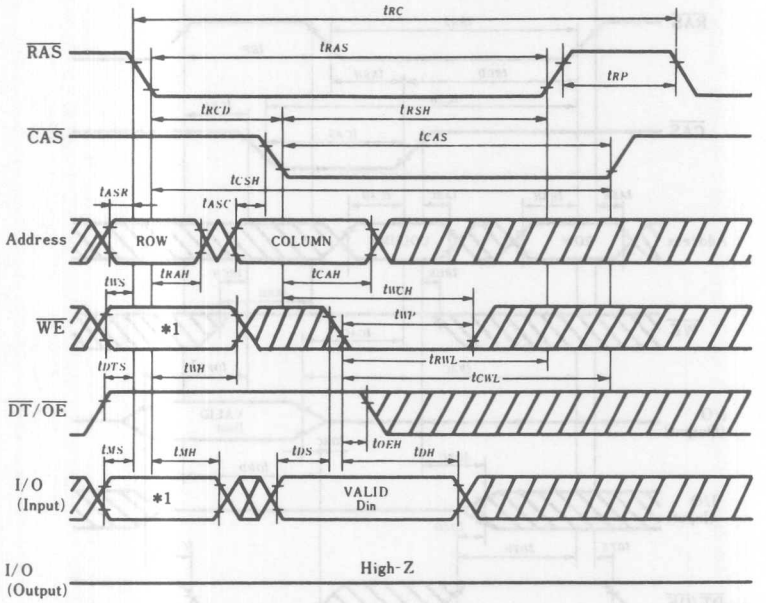


• EARLY WRITE CYCLE



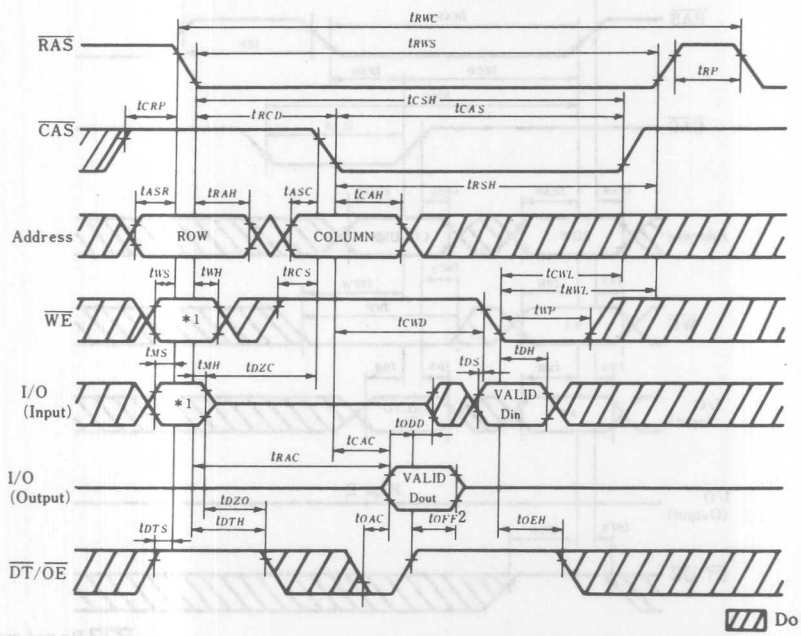
Note) *1. When $\overline{WE}$ is "H" level, the all data on the I/O can be written into the cell.
When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

• DELAYED WRITE CYCLE



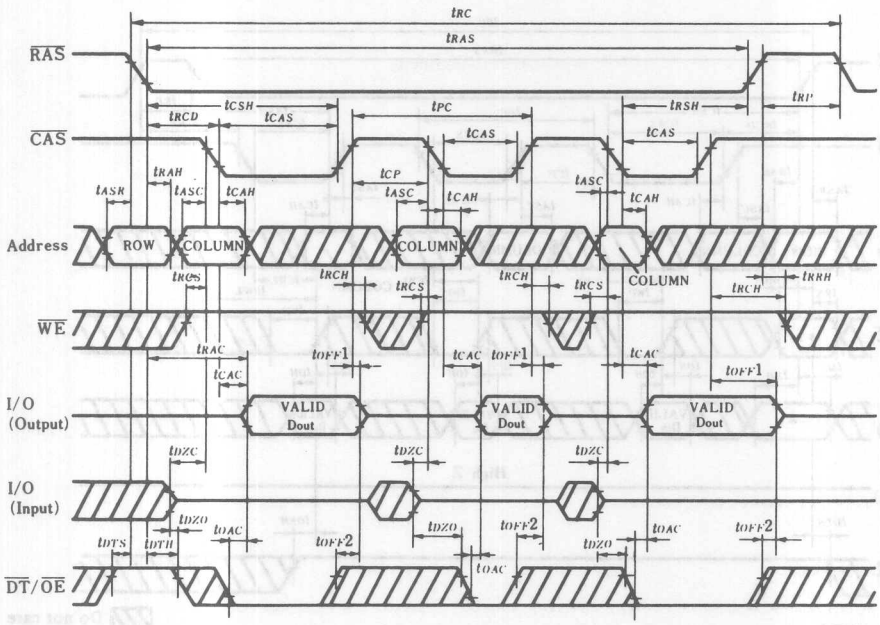
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written exept for when I/O="H" at the falling edge of $\overline{RAS}$.

• READ MODIFY WRITE CYCLE

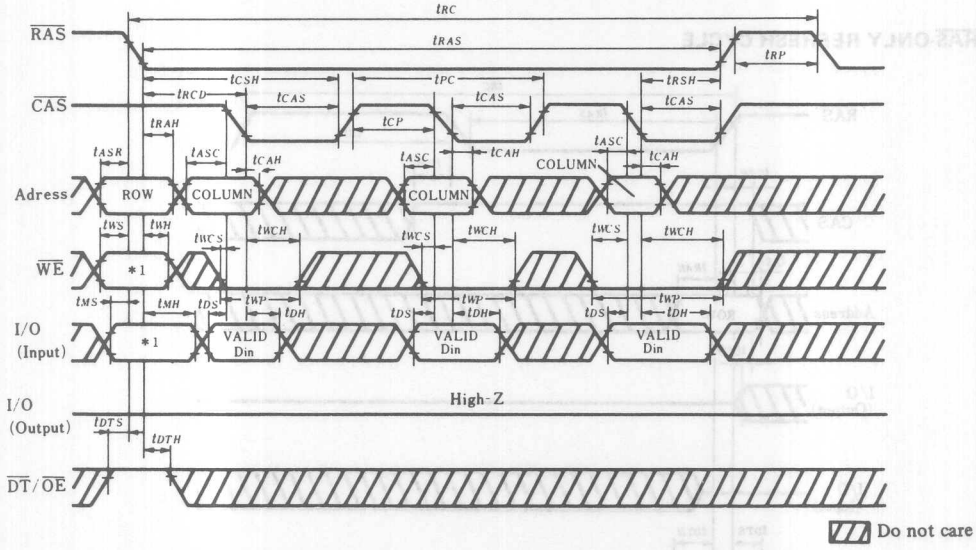


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE READ CYCLE

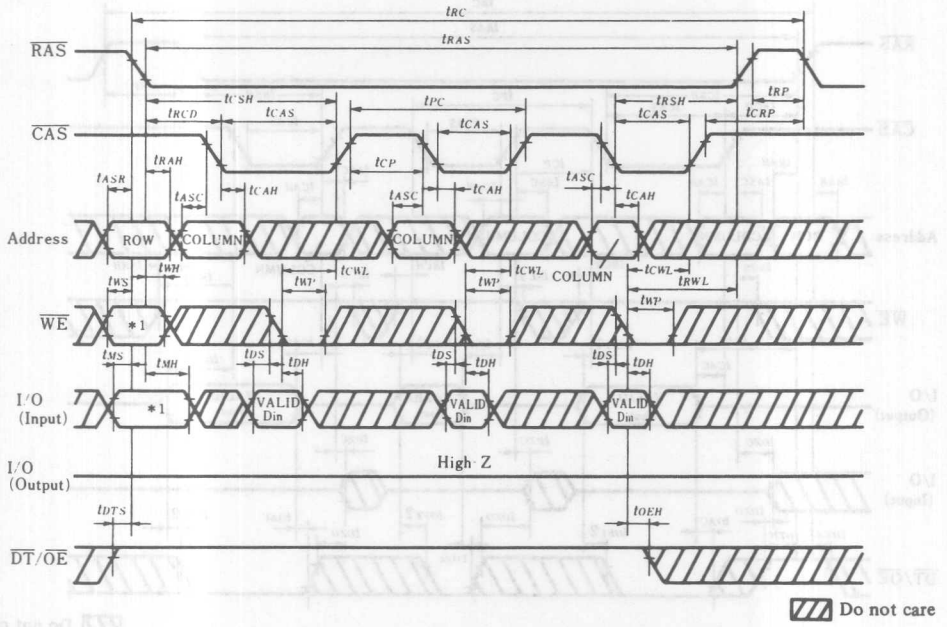


• PAGE MODE WRITE CYCLE (Early Write)



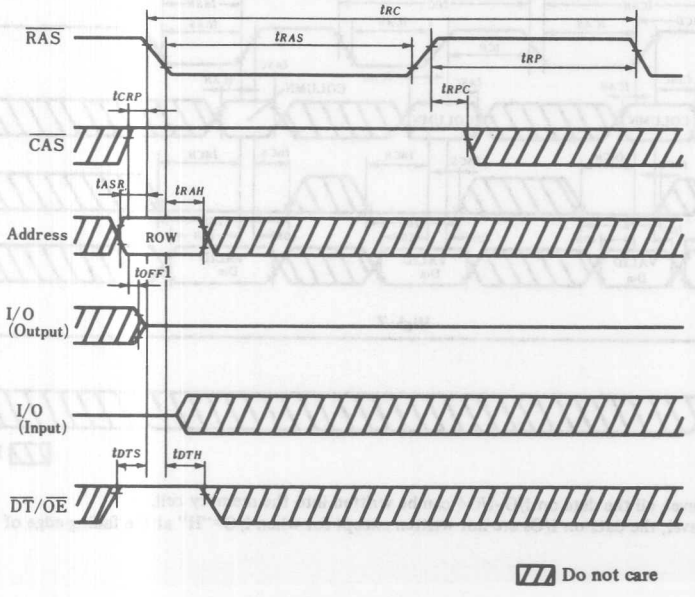
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Delayed Write)

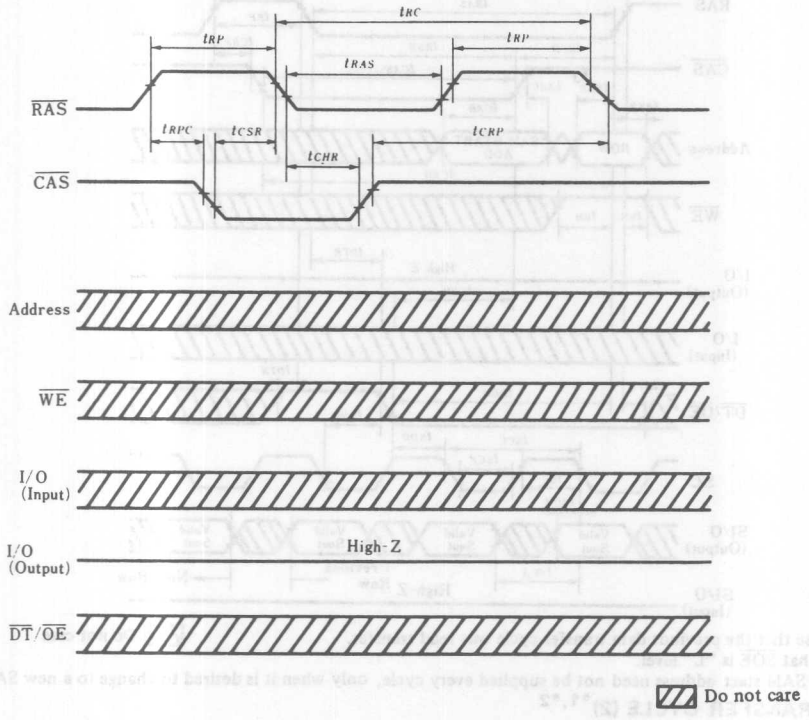


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

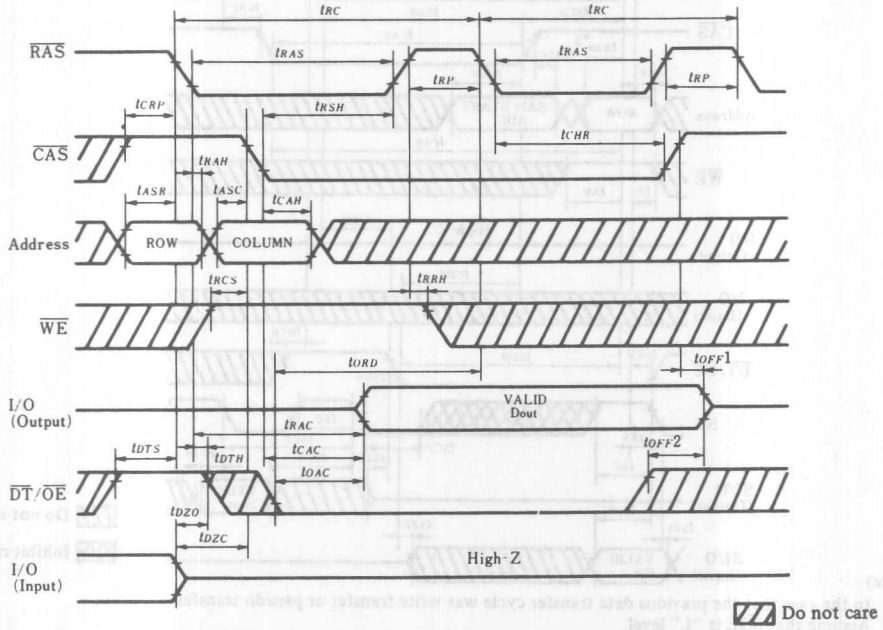
• $\overline{RAS}$-ONLY REFRESH CYCLE



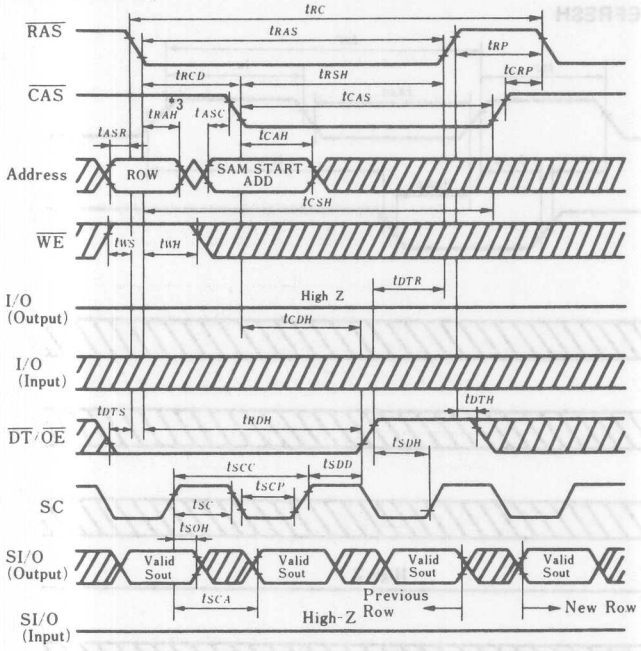
• $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH



• HIDDEN REFRESH CYCLE



• READ TRANSFER CYCLE (1)*1,*2



Note

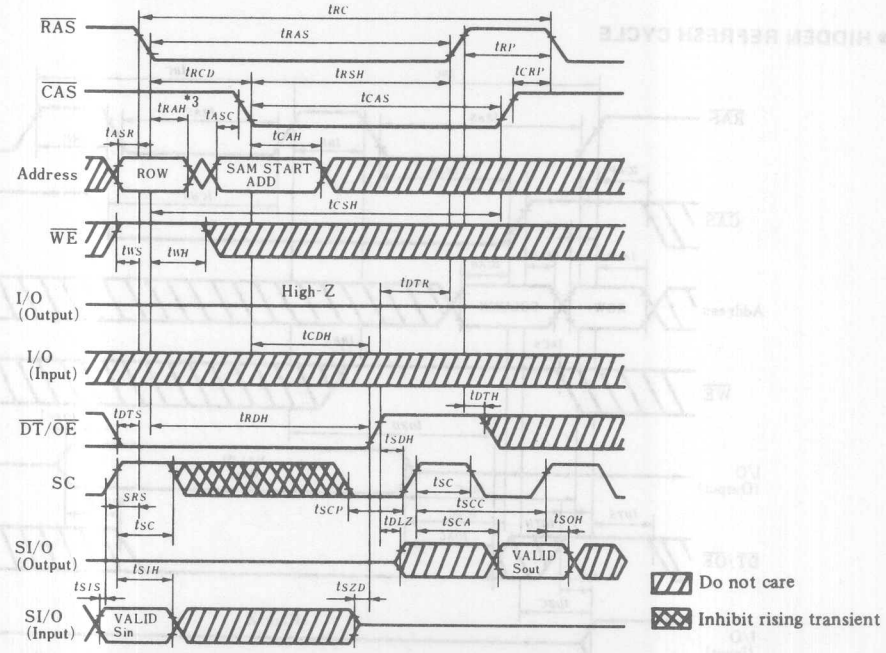
*1) In the case that the previous data transfer cycle was read transfer.

*2) Assume that $\overline{SOE}$ is "L" level.

*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Do not care

• READ TRANSFER CYCLE (2)*1,*2



Do not care

Inhibit rising transient

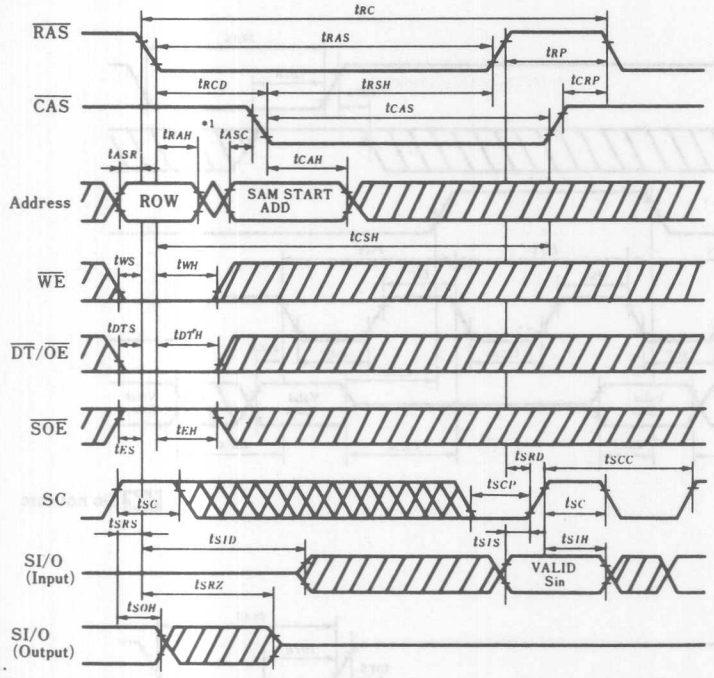
Note)

*1) In the case that the previous data transfer cycle was write transfer or pseudo transfer.

*2) Assume that $\overline{SOE}$ is "L" level,

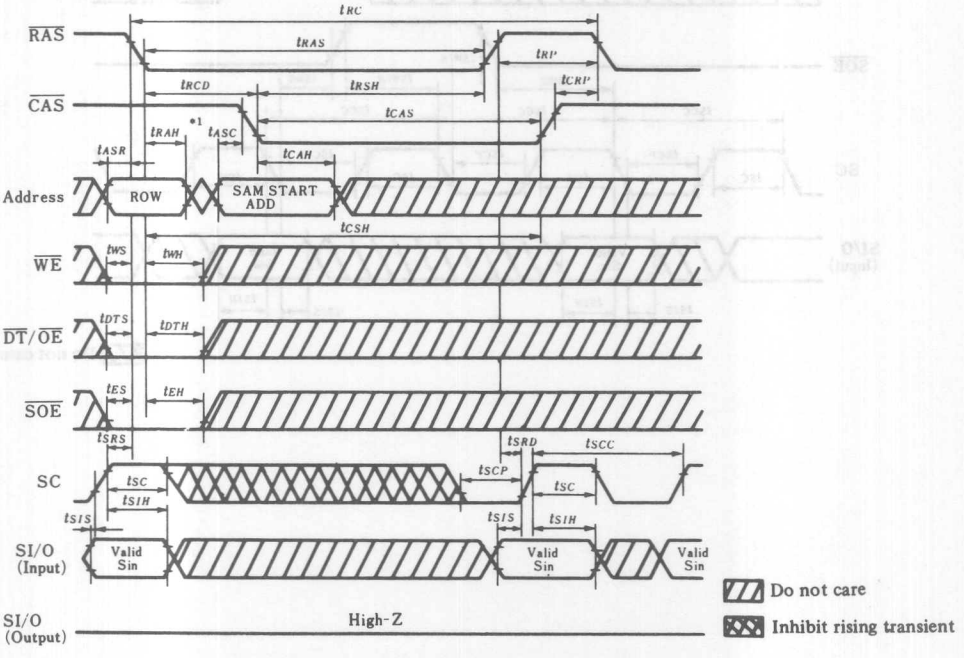
*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• PSEUDO TRANSFER CYCLE



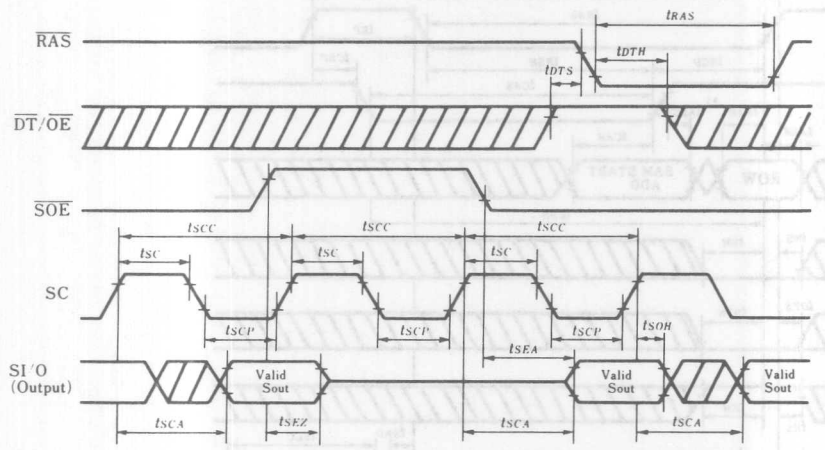
Note) *1.
$\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE TRANSFER CYCLE

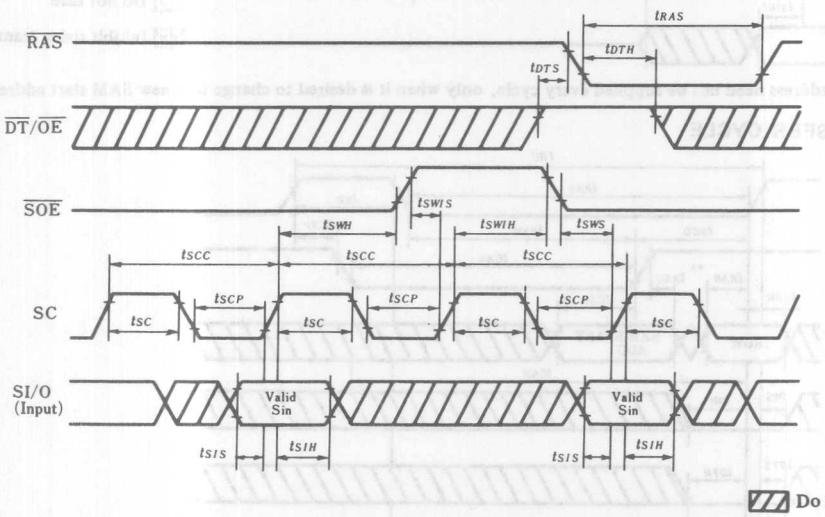


Note) *1.
$\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• SERIAL READ CYCLE



• SERIAL WRITE CYCLE

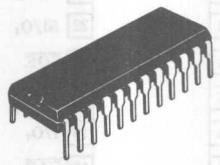


HM53462 Series

65,536-word x 4 bits Multiport CMOS Video RAM (with Logic operation mode)

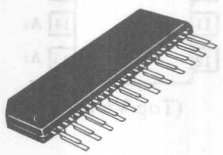
The HM53462 is a 262, 144 bit multiport memory equipped with a 64k-word x 4 bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53462P Series



(DP-24A)

HM53462ZP Seires



(ZP-24)

■ FEATURES

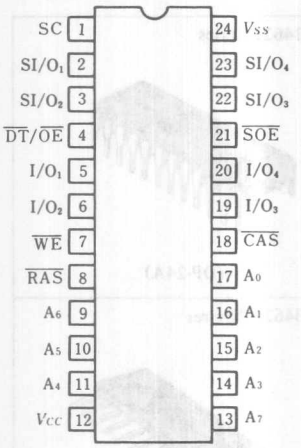
- Multiport organization
  (RAM; 64k-word x 4 bit and SAM; 256-word x 4 bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low powr Active RAM; 380 mW max.
  SAM; 220 mW max.
  Standby 40 mW max.
- Access Time RAM; 100ns/120ns/150ns
  SAM; 40ns/40ns/60ns
- Cycle Time Random read or write cycle time (RAM)
  190ns/220ns/260ns
  Serial read or write cycle time (SAM)
  40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles . . 4ms
- Refresh function $\overline{RAS}$ – only refresh
  $\overline{CAS}$ – before – $\overline{RAS}$ refresh
  Hidden refresh
- Bidirectional data transfer operation (RAM ⇄ SAM)
- Fast serial access operation asynchronized with RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability
- Logic operation capability between Din and Dout
- SAM organization can be changed to 1024 x 1

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM53462P-10 HM53462P-12 HM53462P-15	100ns 120ns 150ns	400 mil 24 pin Plastic DIP
HM53462ZP-10 HM53462ZP-12 HM53462ZP-15	100ns 120ns 150ns	24 pin Plastic ZIP

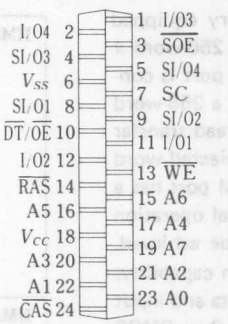
■ PIN ARRANGEMENT

● HM53462P Series



(Top View)

● HM53462ZP Series

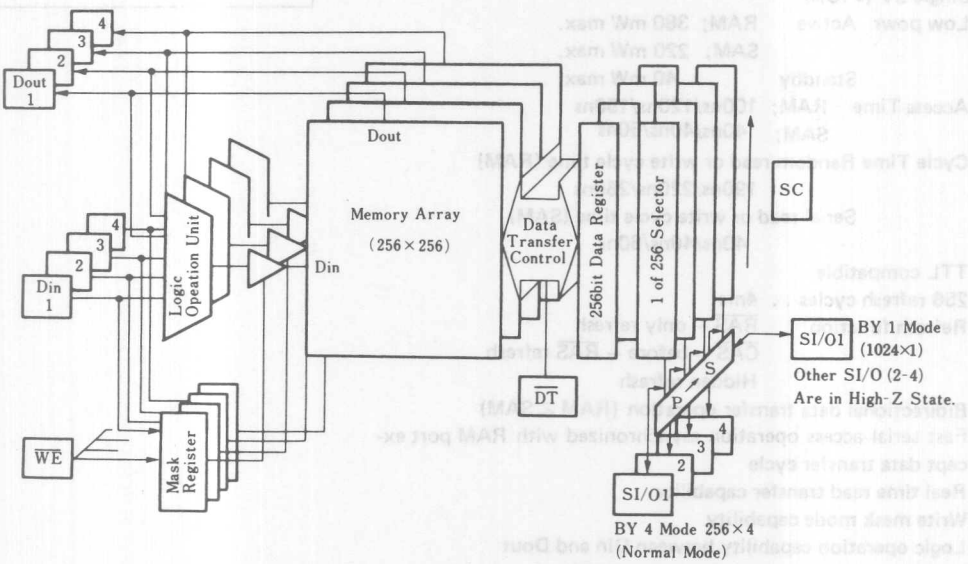


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI_1	–	5	pF
Clocks	CI_2	–	5	pF
I/O, SI/O	$C_{I/O}$	–	7	pF

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	-0.5*2	–	0.8	V

Notes) 1. All voltages referenced to V_{SS}.
2. -3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT Standby	SAM PORT Active	HM53462 -10	HM53462 -12	HM53462 -15	Unit
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	○	×	70	60	50	mA
	I_{CC7}	×	○	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	○	×	7	7	7	mA
	I_{CC8}	×	○	40	40	30	mA
RAS only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	○	×	60	50	40	mA
	I_{CC9}	×	○	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	○	×	50	40	35	mA
	I_{CC10}	×	○	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	○	×	60	50	40	mA
	I_{CC11}	×	○	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	○	×	75	65	55	mA
	I_{CC12}	×	○	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	-10	10	μA
Output leakage	I_{LO}	-10	10	μA
Output high voltage I_{OH} = -2 mA	V_{OH}	2.4	–	V
Output low voltage I_{OL} = 4.2 mA	V_{OL}	–	0.4	V

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1), 10), 11)]

Parameter	Symbol	HM53462 −10		HM53462 −12		HM53462 −15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ – before – $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ – before – $\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	

(to be continued)

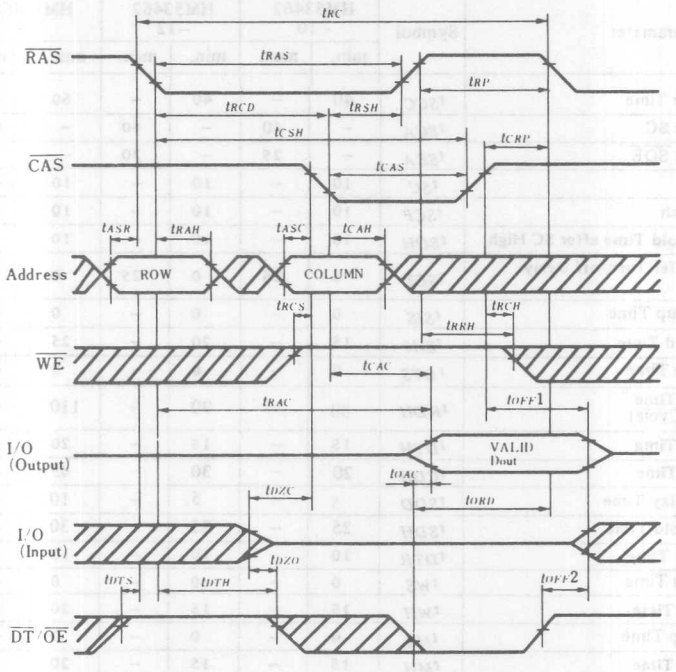
Parameter	Symbol	HM53462 -10		HM53462 -12		HM53462 -15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ns	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Setup Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

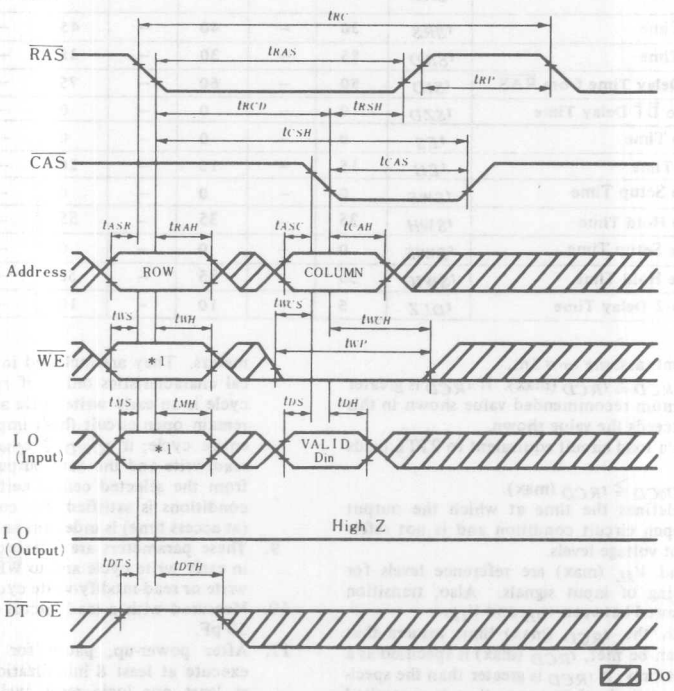
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50 pF.
11. After power-up, pause for more than 100μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = "Low" and I/O1 – I/O = "High"), and execute one or more transport cycle for initiation of SAM port.

■ WAVE FORMS

● READ CYCLE

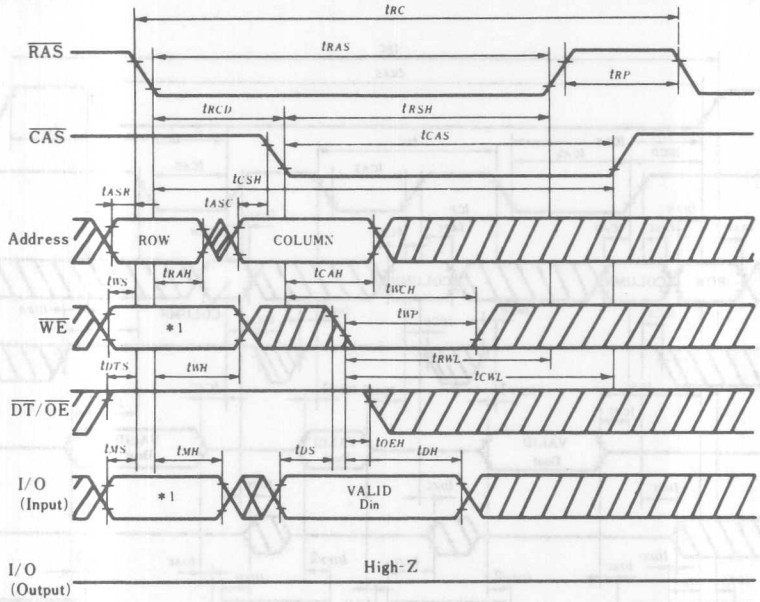


● EARLY WRITE CYCLE



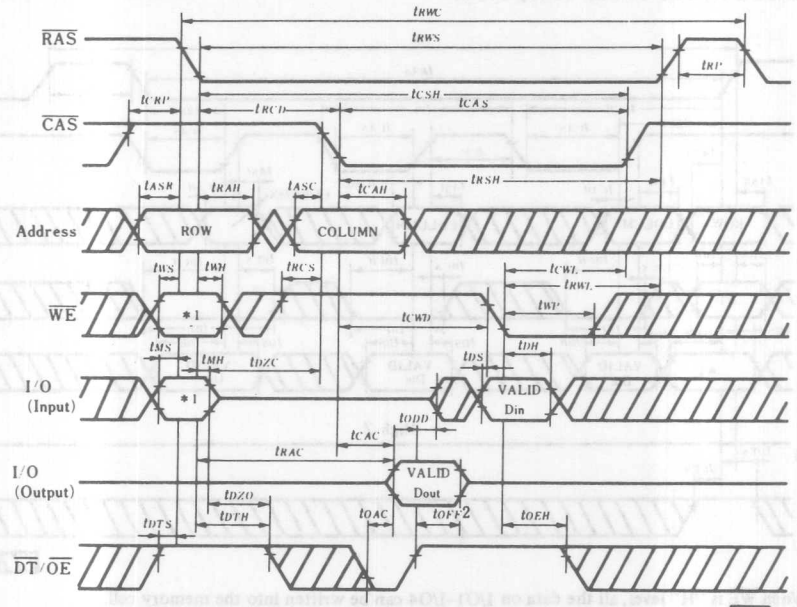
Note) *1. When $\overline{WE}$ is "H" level, the all data on the I/O can be written into the cell. When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of $\overline{RAS}$.

• DELAYED WRITE CYCLE



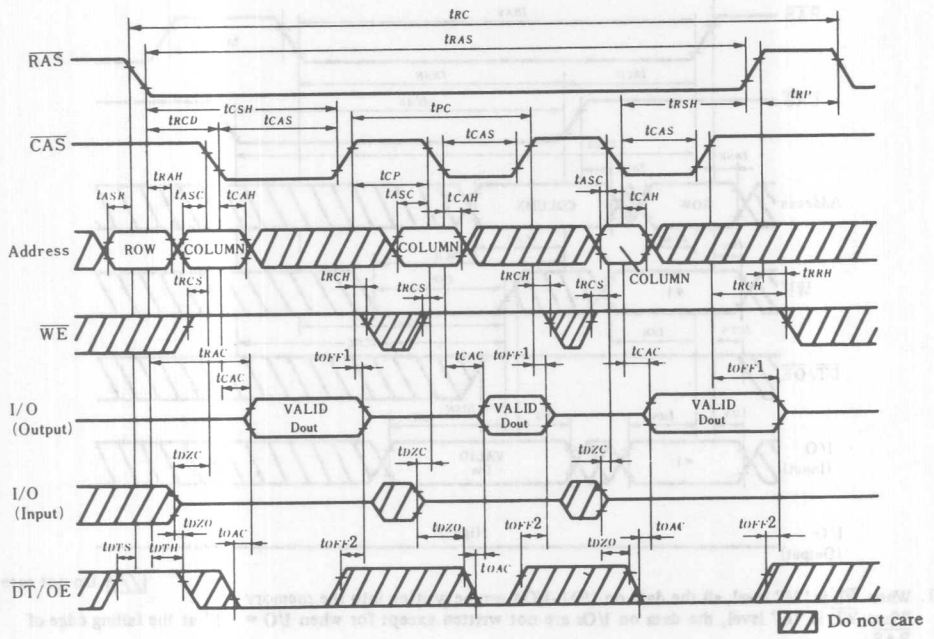
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• READ MODIFY WRITE CYCLE

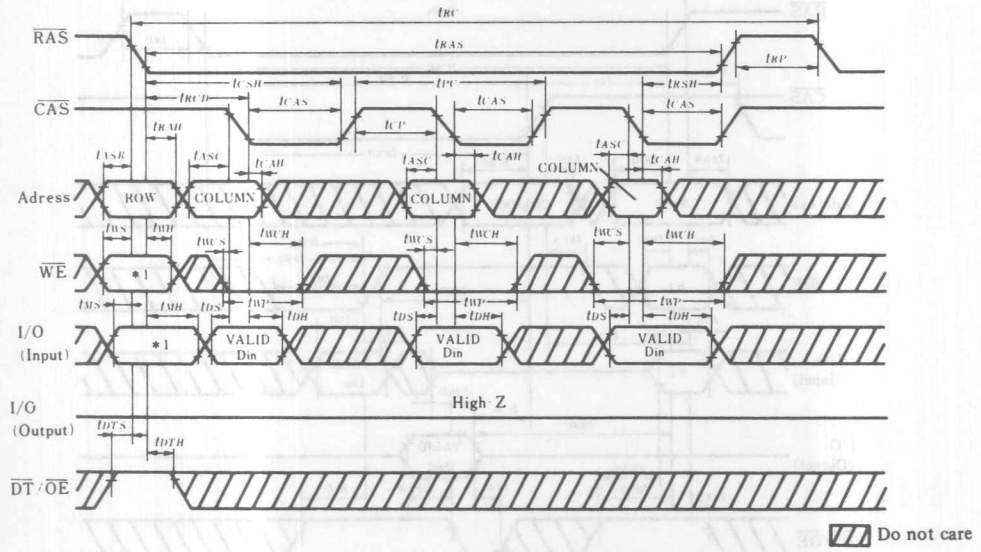


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• PAGE MODE READ CYCLE

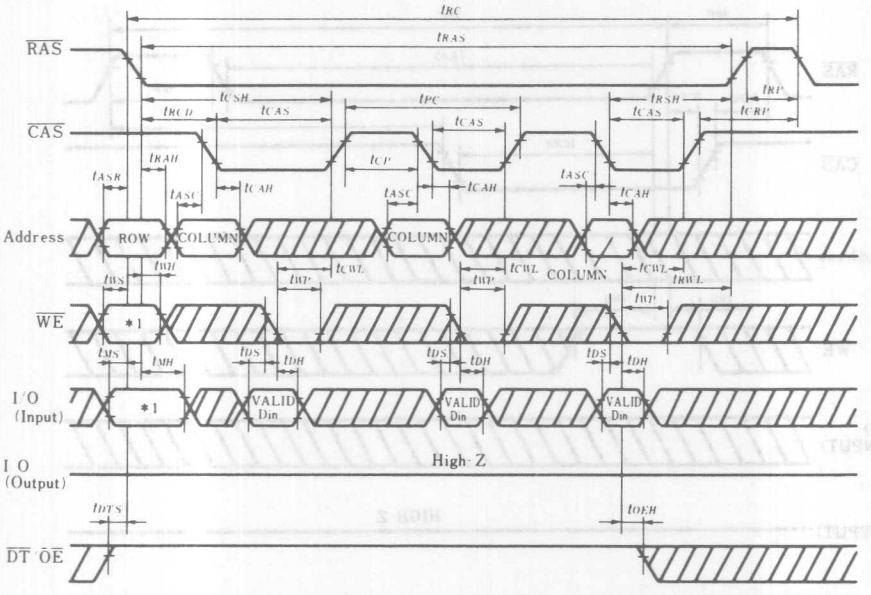


• PAGE MODE WRITE CYCLE (Early Write)



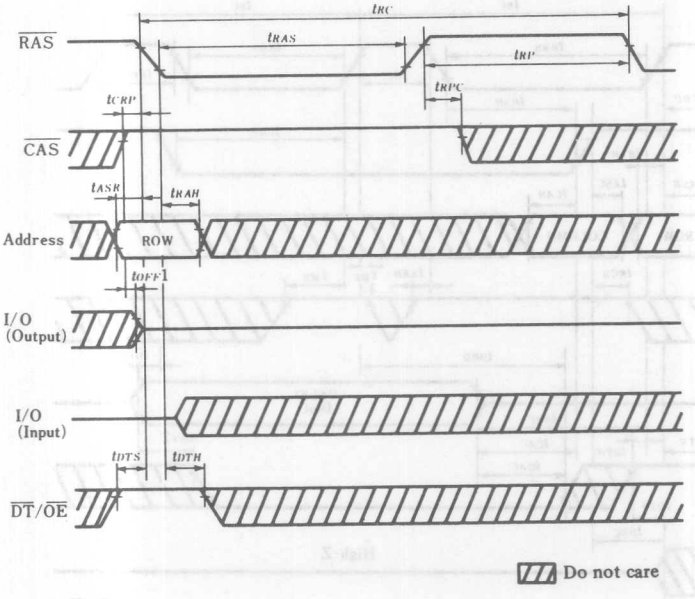
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Delayed Write)

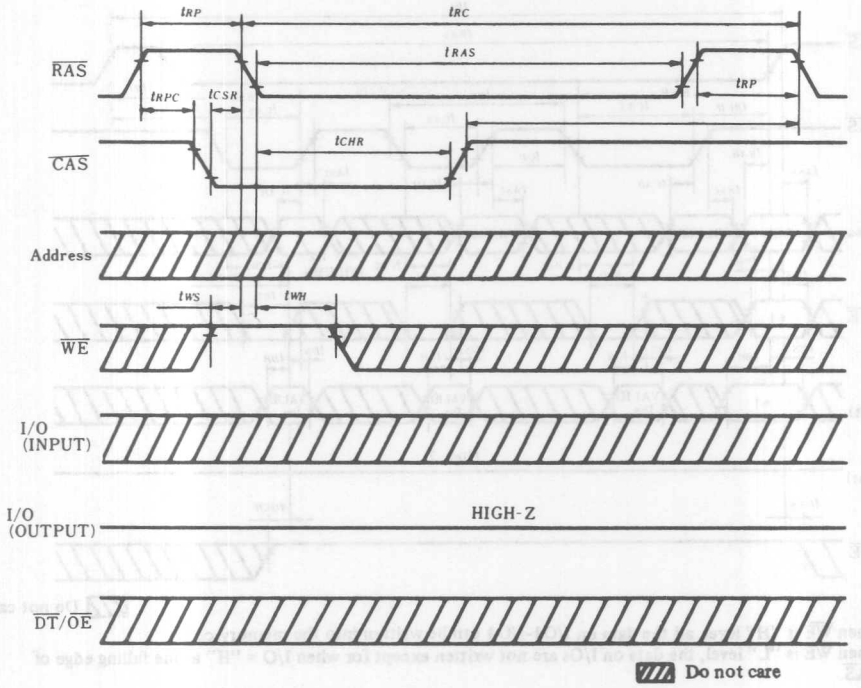


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

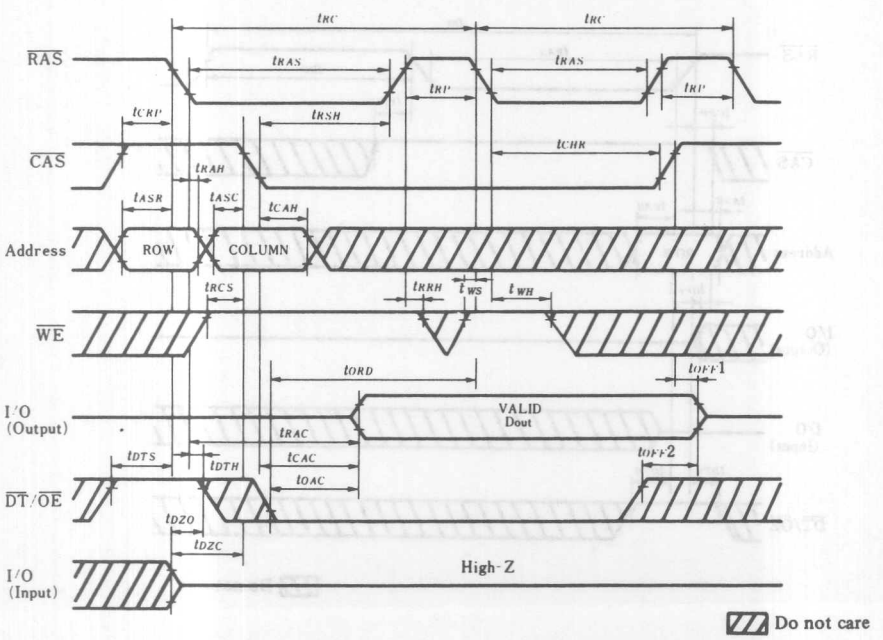
• $\overline{RAS}$-ONLY REFRESH CYCLE



• $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

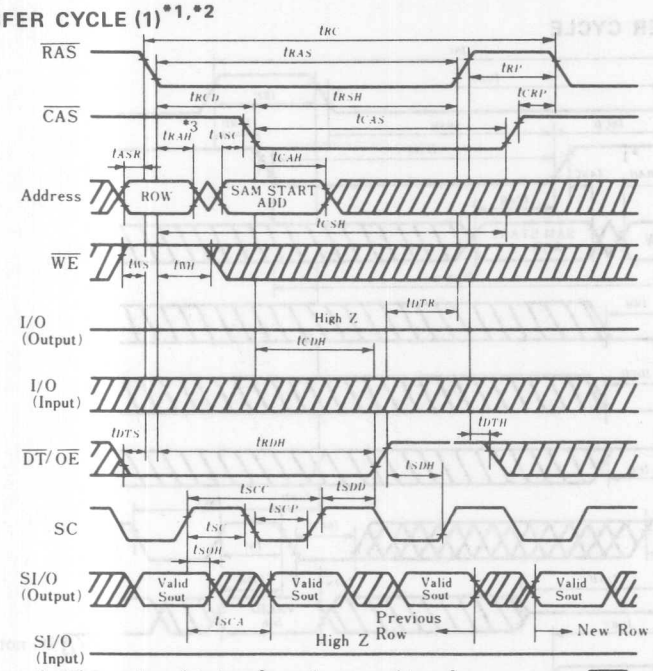


• HIDDEN REFRESH CYCLE



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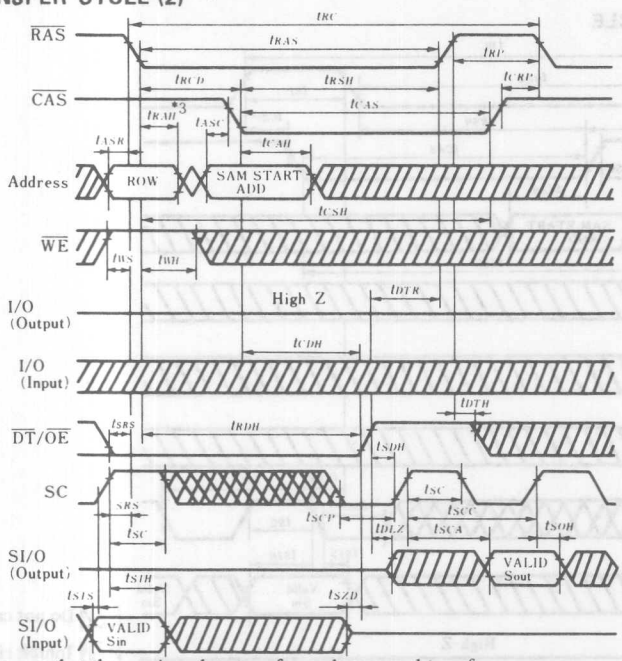
• READ TRANSFER CYCLE (1)*1,*2



NOTE *1) In the case that the previous data transfer cycle was read transfer.
*2) Assume that $\overline{SOE}$ is "Low".
*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

Do not care

• READ TRANSFER CYCLE (2)*1,*2

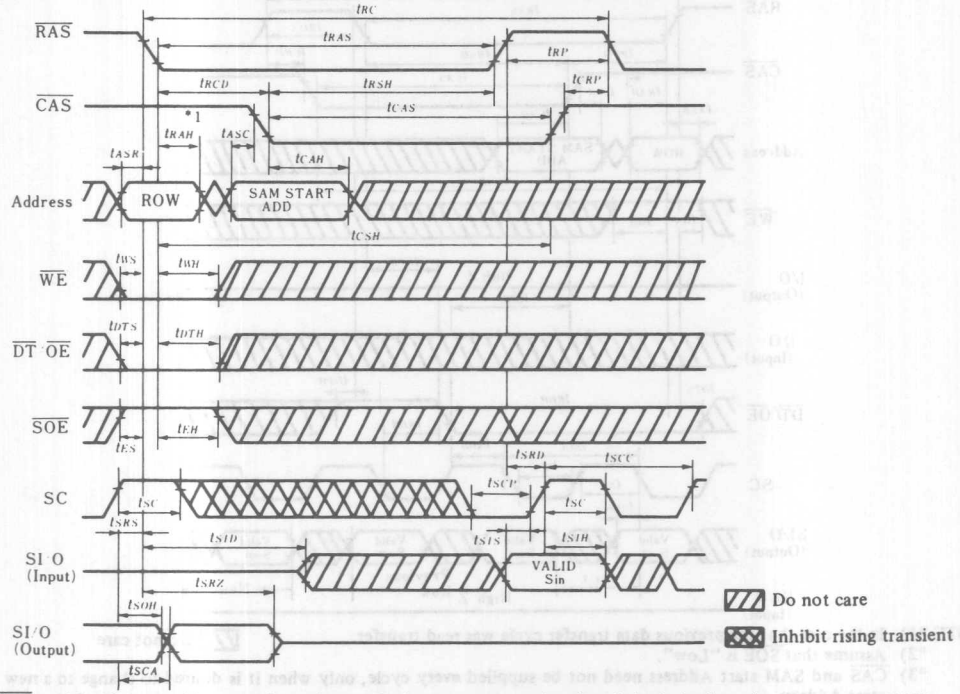


Do not care

Inhibit rising transient

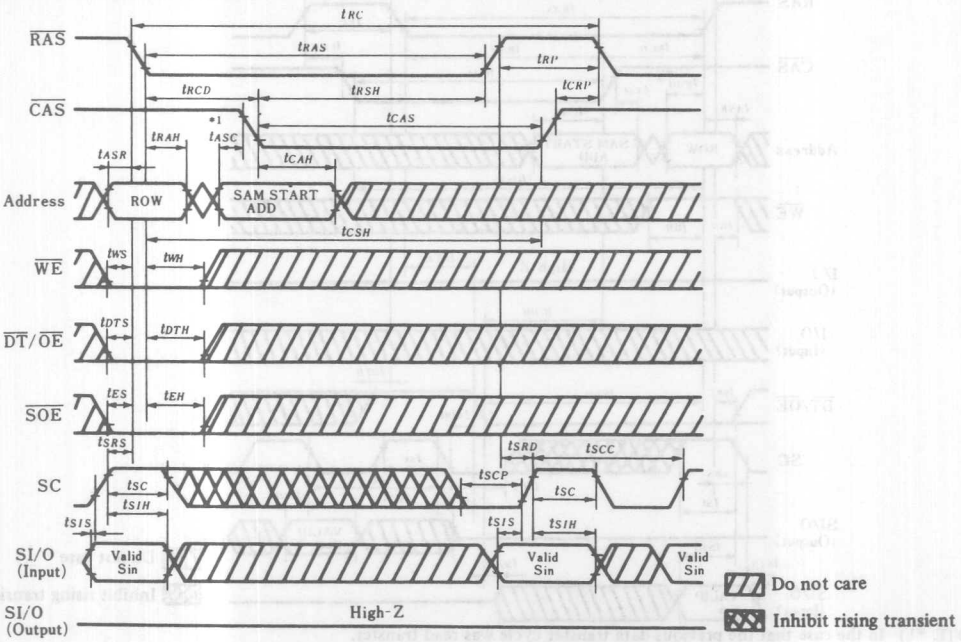
NOTE *1) In the case that the previous data transfer cycle was read transfer.
*2) Assume that $\overline{SOE}$ is "Low"
*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new $\overline{SAM}$ start Address.

• PSEUDO TRANSFER CYCLE



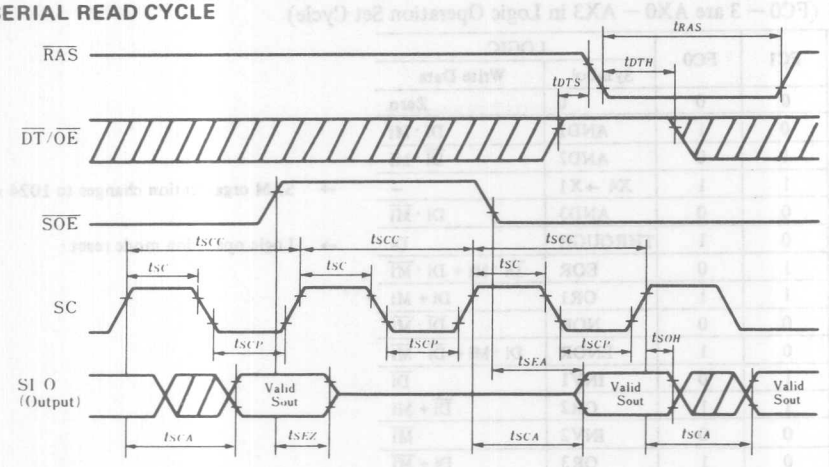
*1) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE TRANSFER CYCLE

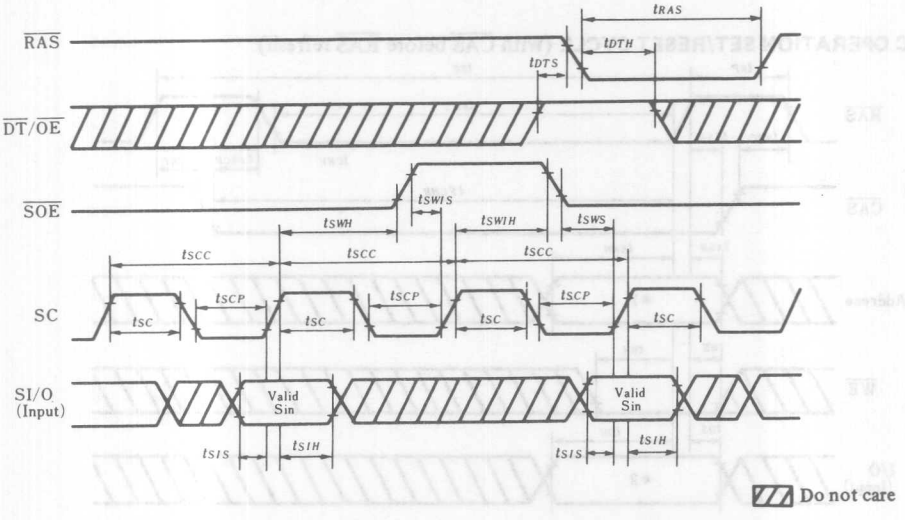


*1) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• SERIAL READ CYCLE



• SERIAL WRITE CYCLE



■ ELECTRICAL AC CHARACTERISTICS (Logic operation mode)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{FRC}	230	–	265	–	310	–	ns
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	165	10000	200	10000	ns
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	80	10000	95	10000	105	10000	ns
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	–	165	–	200	–	ns
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	80	–	95	–	105	–	ns
Page mode cycle time (Write cycle)	t_{FPC}	100	–	120	–	135	–	ns
$\overline{CAS}$ hold time (Logic operation set/reset cycle)	t_{FCHR}	90	–	100	–	120	–	ns
$\overline{CAS}$ hold time from $\overline{RAS}$ precharge (x4 → x1 set cycle)	t_{PSCH}	10	–	10	–	10	–	ns

■ LOGIC CODE (FC0 – 3 are AX0 – AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 → X1	–
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

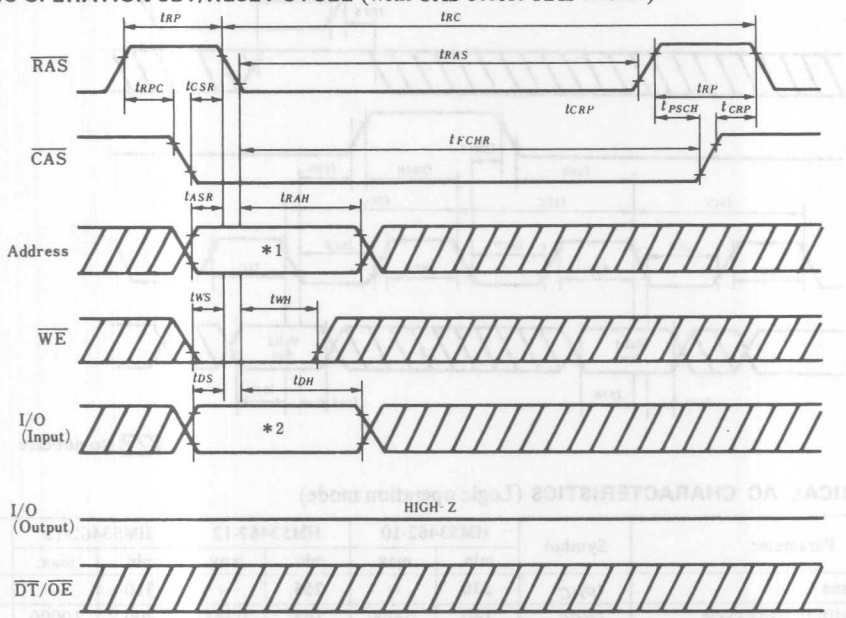
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

Di : External Data-in

Mi : The data of the memory cell

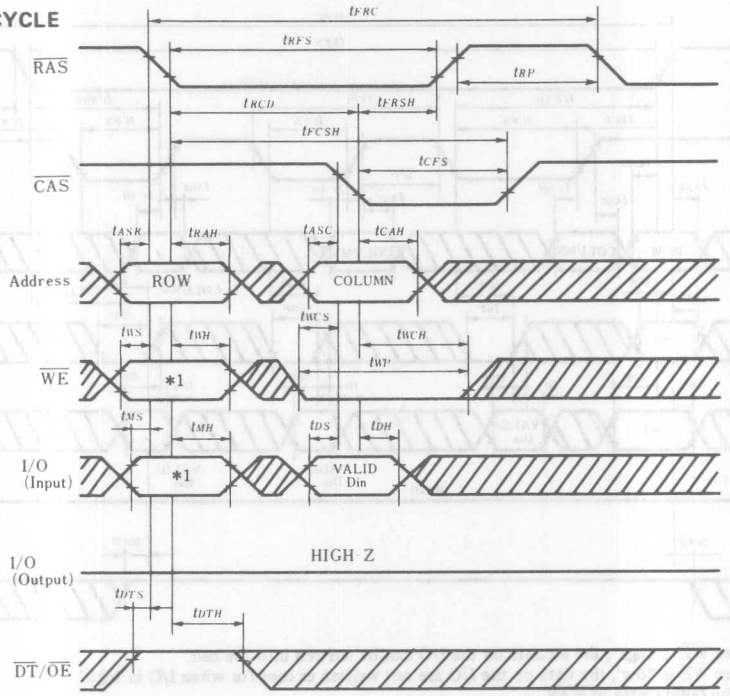
● LOGIC OPERATION SET/RESET CYCLE (With $\overline{CAS}$ before $\overline{RAS}$ refresh)



*1) Logic code A0-A3 (A4-A7: don't care)
*2) Write mask data

■ LOGIC OPERATION MODE

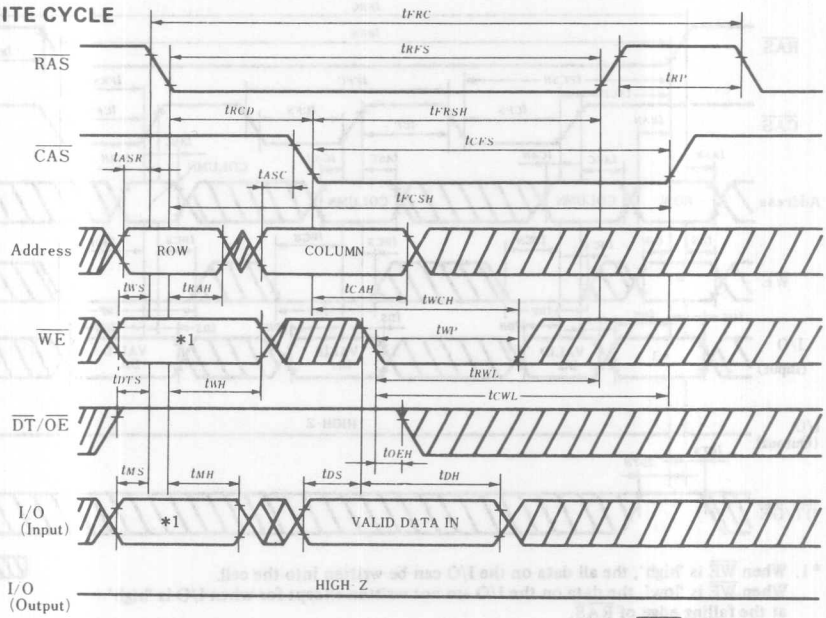
• EARLY WRITE CYCLE



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

▨ Do not care

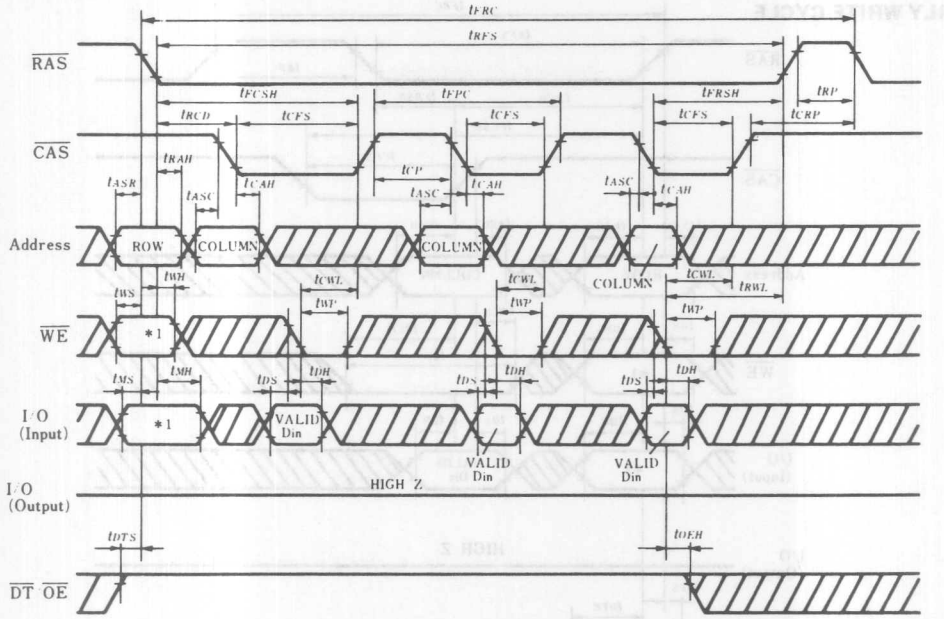
• DELAYED WRITE CYCLE



NOTE 1) When $\overline{WE}$ is "H" level, all the data on I/O1-4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

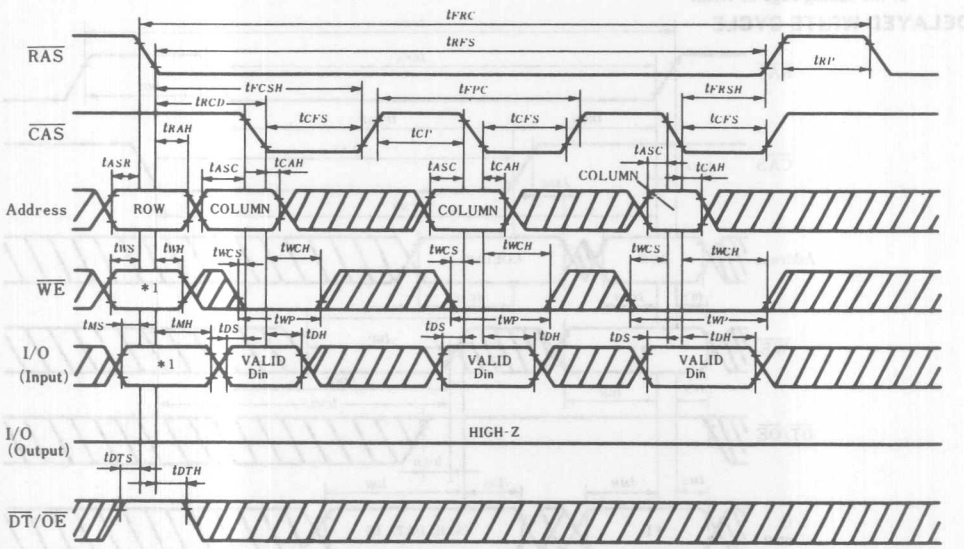
▨ Do not care

• PAGE MODE WRITE CYCLE (Delayed Write)



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Early Write)



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

■ DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between Din and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by Ax0-3 state and I/01-4 state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ – before – $\overline{RAS}$ refresh operation is executed, too. In the case of executing the conventional $\overline{CAS}$ – before – $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1. Logic code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is (Ax3, Ax2, Ax1, Ax0) = (0, 0, 1, 1), the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1,024 x 1, one data transfer cycle is needed to initialie the SAM selector.

Once the SAM organization is changed to 1024 x 1, this code is maintained unless power is turned off.

2.2. Write mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

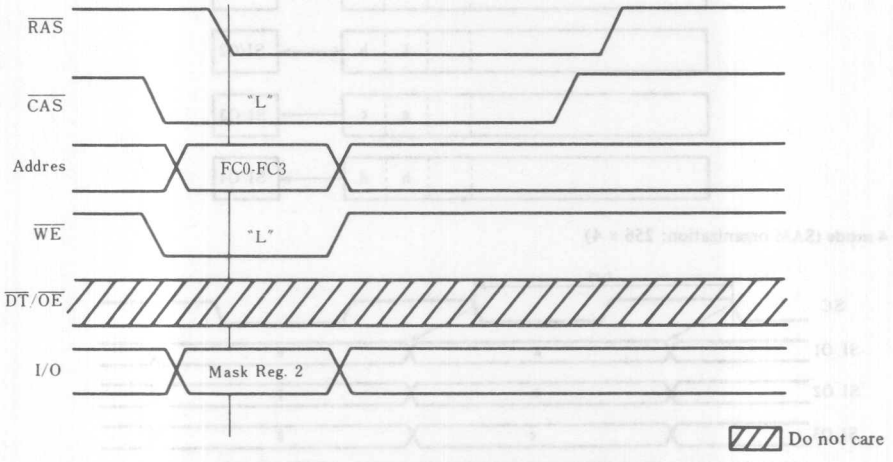


Fig. 1 LOGIC OPERATION SET/RESET CYCLE

Table 1. LOGIC CODE (FC0 – FC3 are AX0 – AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 →X1	–
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

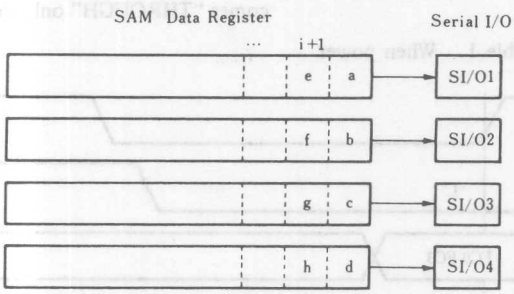
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

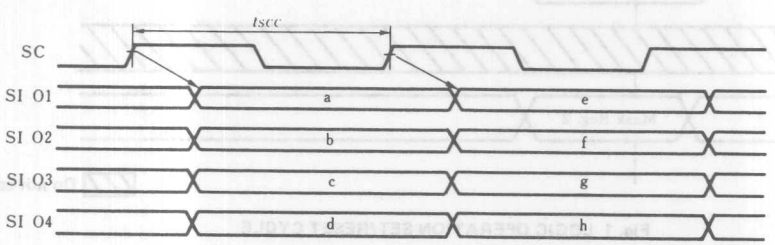
Di : External Data-in

Mi : The data of the memory cell

Fig. 2 THE SHIFT WAY OF SAM DATA



1) By 4 mode (SAM organization: 256 x 4)



2) By 1 mode (SAM organization: 1024 x 1)

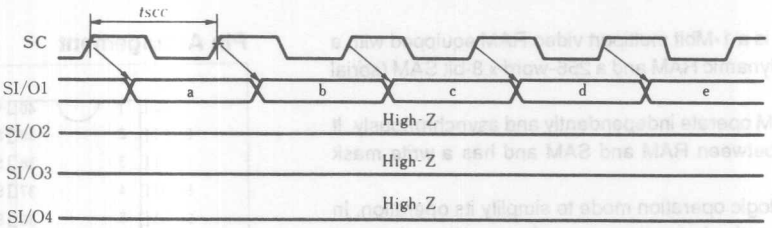


Fig. 3 EXAMPLE OF LOGIC OPERATION MODE

	Logic operation set/reset cycle	Write cycle	Write cycle	Write cycle	Write cycle
$\overline{RAS}$					
$\overline{CAS}$	"L"	"H"	"H"	"H"	"H"
$\overline{WE}$	"L"	"H"	"L"	"H"	"H"
I/O1		"0" Write	Masked	"1" Write	"0" Write
I/O2		Masked	"1" Write	Masked	Masked
I/O3		Masked	"0" Write	Masked	Masked
I/O4		"1" Write	Masked	"0" Write	"1" Write
Logic	—	AND1	THROUGH	AND1	AND1
	Mask reg.2 is set I/O2,3 :Masked Assume that the logic is set to "AND1".		Mask reg.1 is set, and valid only in this cycle. I/O1,4:Masked		

HM538122 Series — Preliminary

131072-Word × 8-Bit Multiport CMOS Video RAM

The HM538122 is a 1-Mbit multiport video RAM equipped with a 128-kword x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function.

It also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

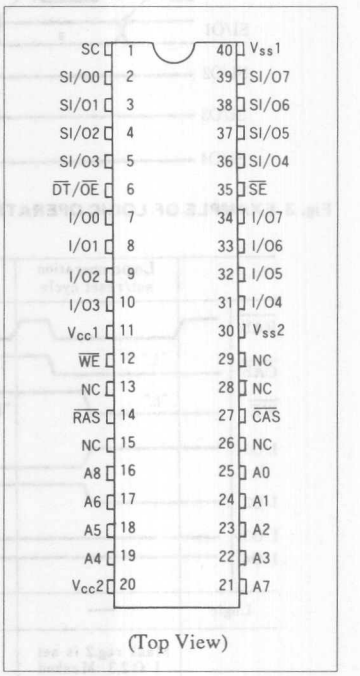
Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 128-kword x 8-bit and SAM: 256-word x 8-bit
- Access time — RAM: 100 ns/120 ns/150 ns max; SAM: 30 ns/ 40 ns/ 50 ns max
- Cycle time — RAM: 190 ns/220 ns/260 ns min; SAM: 30 ns/ 40 ns/ 60 ns min
- Low power
  - Active — RAM: 385 mW max; SAM: 275 mW max
  - Standby — 40 mW max
- High-speed page mode capability
- Logic operation mode capability
- 2 types of mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM538122JP-10	100 ns	400-mil
HM538122JP-12	120 ns	40-pin
HM538122JP-15	150 ns	Plastic SOJ (CP-40D)

Pin Arrangement



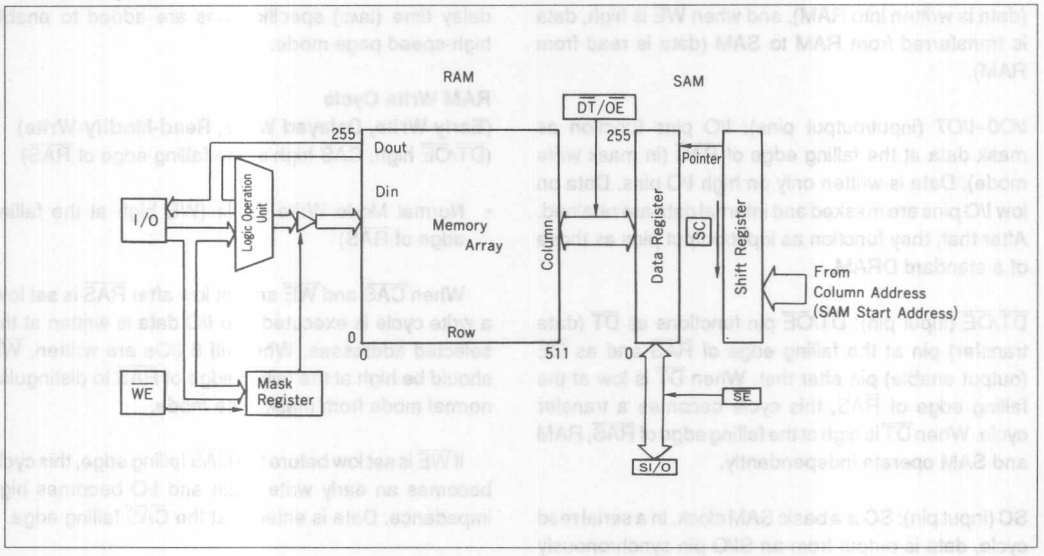
(Top View)

Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O–I/O7	RAM port data inputs/ outputs
SI/O0–SI/O7	SAM port data inputs/ outputs
$\overline{RAS}$	Row adress strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT}/\overline{OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
Vcc	Power supply
Vss	Ground
NC	No connection

This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Block Diagram



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538122.

Table 1. Operation Cycles of the HM538122

Input Level at the Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	×	RAM read/write
H	H	L	×	Mask write
H	L	H	×	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	×	H	×	CBR refresh
L	×	L	×	Logic operation set/reset

Note: ×; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0–A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538122 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$.

When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM538122

Operation of RAM Port

RAM Read Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle

(Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle

($\overline{DT}/\overline{OE}$ high, CAS high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page

mode cycle by 70–80%. This product is based on static column mode, therefore address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 µs).

Transfer Operation

The HM538122 provides the transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
(2) Determine direction of data transfer
  (a) Read transfer cycle: RAM → SAM
  (b) Write transfer cycle: RAM ← SAM
(3) Determine input or output of SAM I/O pin (SI/O)
  Read transfer cycle: SI/O output
  Pseudo transfer cycle, write transfer cycle: SI/O input
(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and WE high at the falling edge of $\overline{RAS}$. The row address data (256 x 8 bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can access SAM serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH}(min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

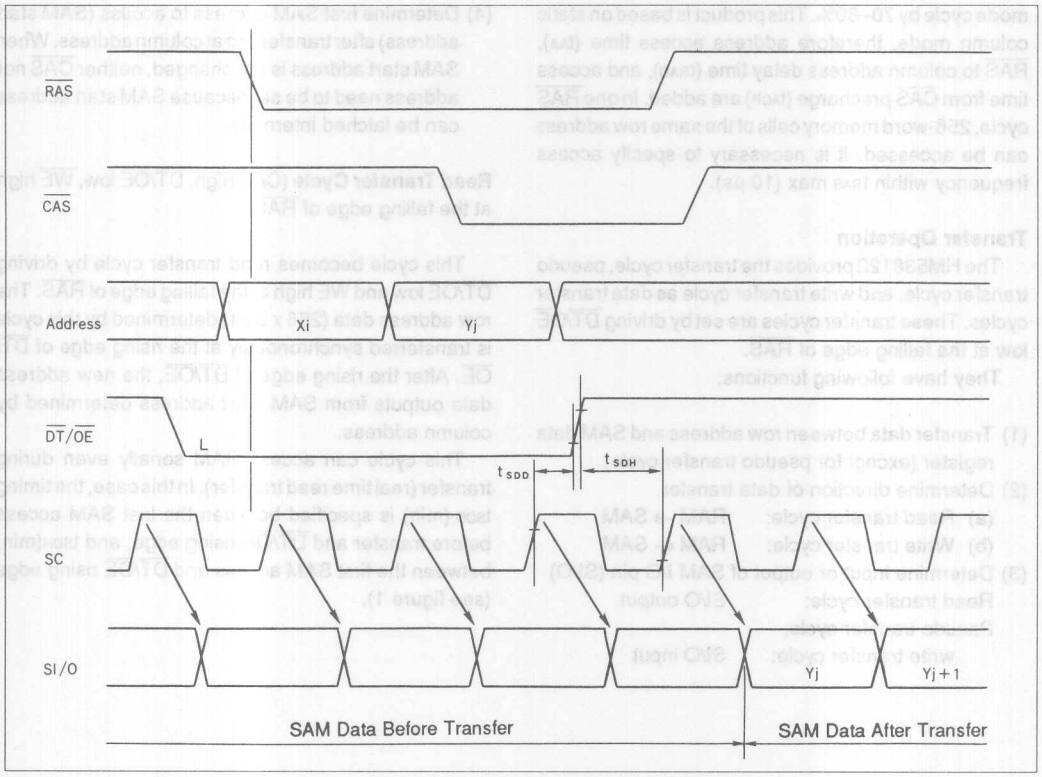


Figure 1. Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ}(min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of RAS. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$-only refresh cycles because $\overline{CAS}$ circuits don't operate. To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode

The HM538122 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle
($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0–A3 levels at the falling edge of $\overline{RAS}$. (A4–A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0,1,0,1) resets the logic operation mode. When write cycle is performed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2)Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

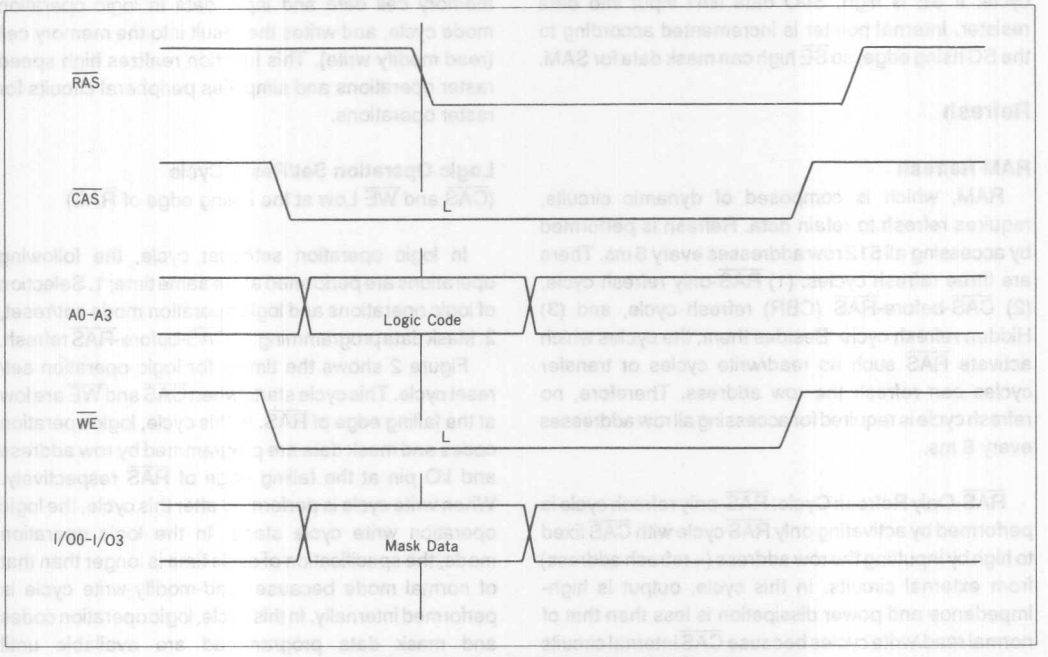


Figure 2. Logic Operation Set/Reset

Table 2. Logic Code

Logic Code						
A3	A2	A1	A0	Symbol	Write Data	Notes
0	0	0	0	Zero	0	
0	0	0	1	AND1	Di·Mi	
0	0	1	0	AND2	$\overline{Di}$·Mi	Logic operation mode set
0	0	1	1	—	Mi	
0	1	0	0	AND3	Di·$\overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	$\overline{Di}$·Mi+Di·$\overline{Mi}$	
0	1	1	1	OR1	Di+Mi	
1	0	0	0	NOR	$\overline{Di}$·$\overline{Mi}$	
1	0	0	1	ENOR	Di·Mi+$\overline{Di}$·$\overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	Logic operation mode set
1	0	1	1	OR2	$\overline{Di}$+Mi	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	Di+$\overline{Mi}$	
1	1	1	0	NAND	$\overline{Di}$+$\overline{Mi}$	
1	1	1	1	One	1	

Notes: Di; External data-in
Mi; The data of the memory cell

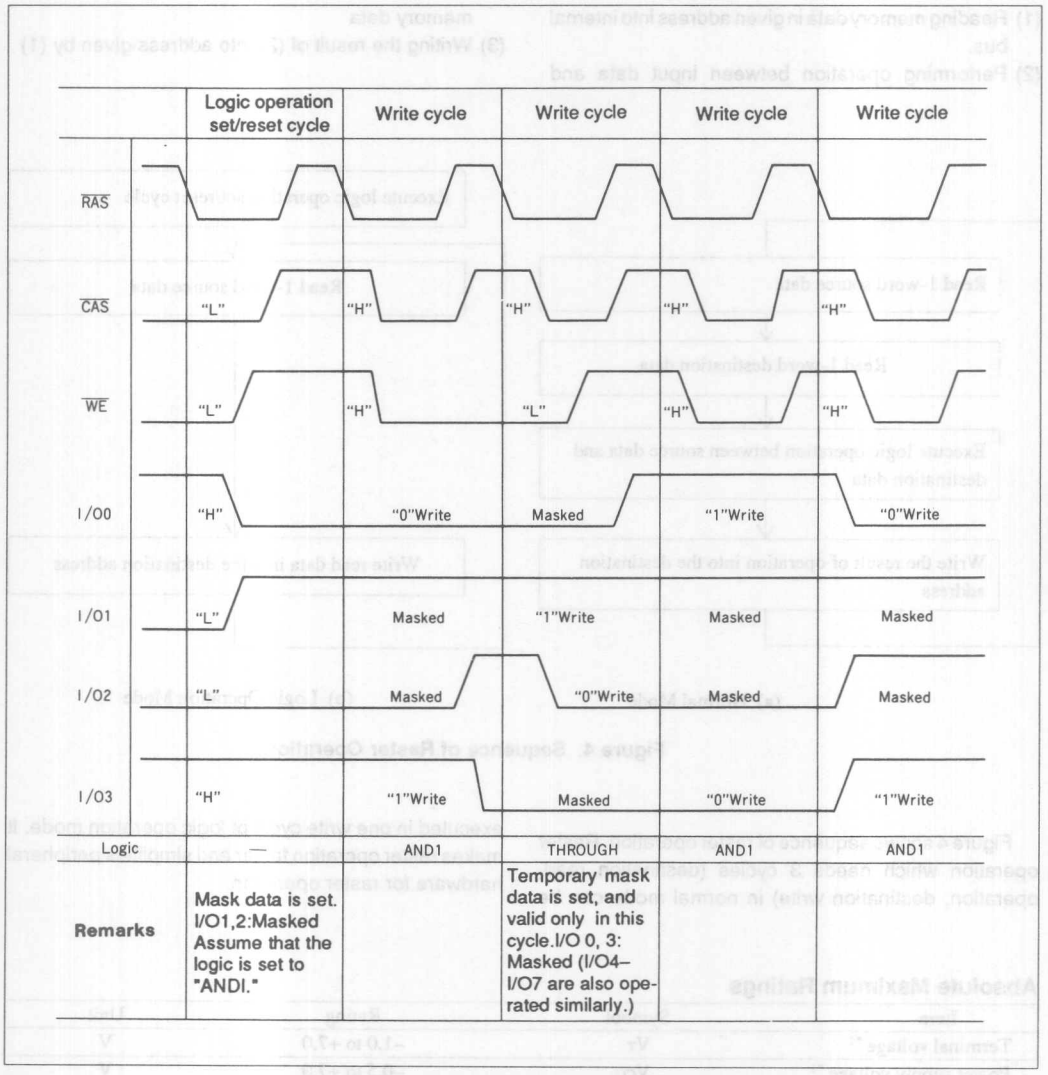


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

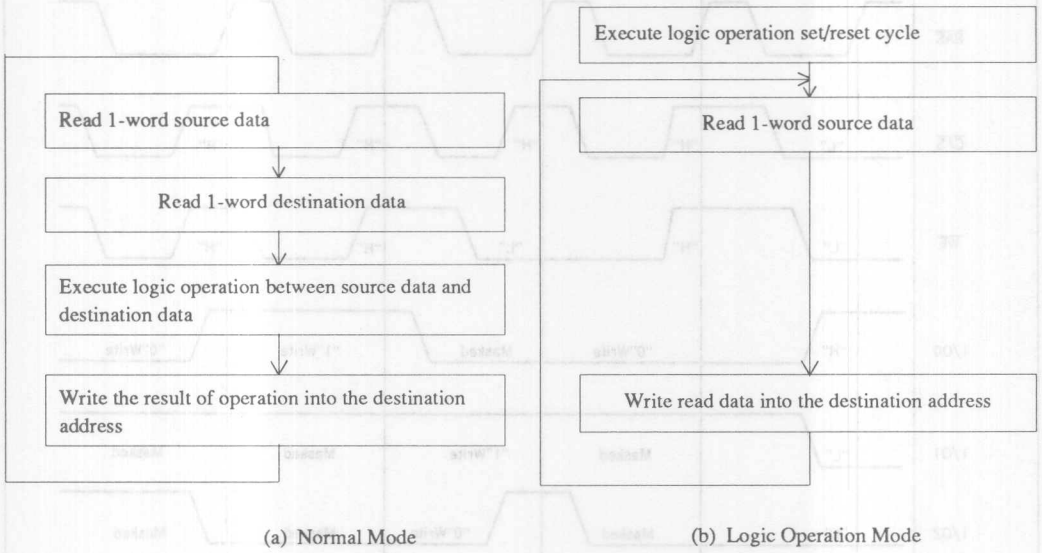
Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is devided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed Internally.

(1) Reading memory data in given address into internal bus.
(2) Performing operation between input data and memory data
(3) Writing the result of (2) into address given by (1)



(a) Normal Mode (b) Logic Operation Mode

Figure 4. Sequence of Raster Operation

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	–1.0 to +7.0	V
Power supply voltage *1	V_{CC}	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: *1. Relative to Vss.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	—	6.5	V
Input low voltage *1	V_{IL}	–0.5*2	—	0.8	V

Notes: *1. All voltages referenced to Vss.
*2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Item	Symbol	HM538122 -10		HM538122 -12		HM538122 -15		Unit	Test Conditions	
		Min	Max	Min	Max	Min	Max		RAM port	SAM port
Operating current	I_{CC1}	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	120	—	100	—	80	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$=V_{IH}
	I_{CC8}	—	50	—	40	—	30	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{RAS}$-only refresh current	I_{CC3}	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}	SC = V_{IL},$\overline{SE}$ = V_{IH}
	I_{CC9}	—	110	—	90	—	70	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Page mode current	I_{CC4}	—	65	—	55	—	45	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	115	—	95	—	75	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Data transfer current	I_{CC6}	—	90	—	90	—	90	mA	$\overline{RAS}$,$\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	125	—	125	—	125	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

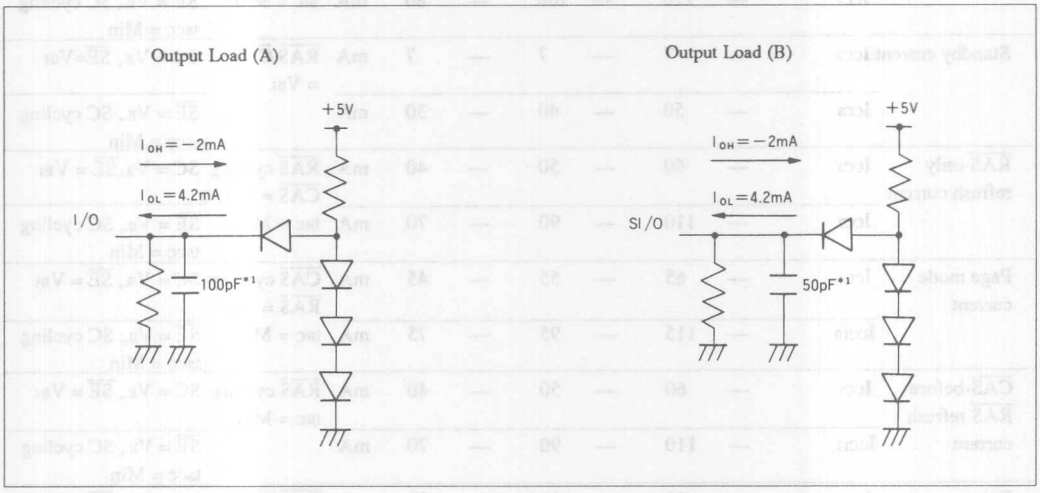
Capacitance (Ta = 25°C, V_{CC} =5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)[*1, *11]

Test Conditions

Input rise and fall time: 5 ns
Output load: See Figures
Input timing reference levels: 0.8 V, 2.4 V
Output timing reference levels: 0.4 V, 2.4 V



Note: *1. Including scope & jig.

Common Parameter

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	30	10000	35	10000	40	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	70	25	85	30	110	ns	*5,*6
$\overline{RAS}$ hold time	t_{RSH}	30	—	35	—	40	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	*8
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	55	—	70	ns	*3, *6
Output buffer turn off delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	*7
Output buffer turn off delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	*7
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	*12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	*12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	65	25	80	ns	*5, *6
Page mode cycle time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	*9
Write command hold time	t_{WCH}	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read modify write cycle time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	75	—	90	—	ns	*9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	95	—	120	—	ns	*9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{AC}	—	100	—	120	—	150	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	55	—	70	ns	*3,*6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	65	25	80	ns	*5,*6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Transfer Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{RAS}$ setup time	t_{RS}	30	—	40	—	45	—	ns	
$\overline{DT}$ hold time from $\overline{RAS}$	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{DT}$ hold time from $\overline{CAS}$	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ hold time	t_{SDH}	TBD	—	TBD	—	TBD	—	ns	
$\overline{DT}$ to $\overline{RAS}$ lead time	t_{DTL}	50	—	50	—	50	—	ns	
$\overline{DT}$ hold time referenced to $\overline{RAS}$ high	t_{DTHH}	20	—	25	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	30	—	35	—	40	—	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	—	10	—	10	—	10	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	*7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	–	30	–	40	—	50	ns	*4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	

Serial Read Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	40	—	50	ns	*4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	40	ns	*4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	0	25	0	25	0	30	ns	*7

Serial Write Cycle

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	30	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	50	—	ns	

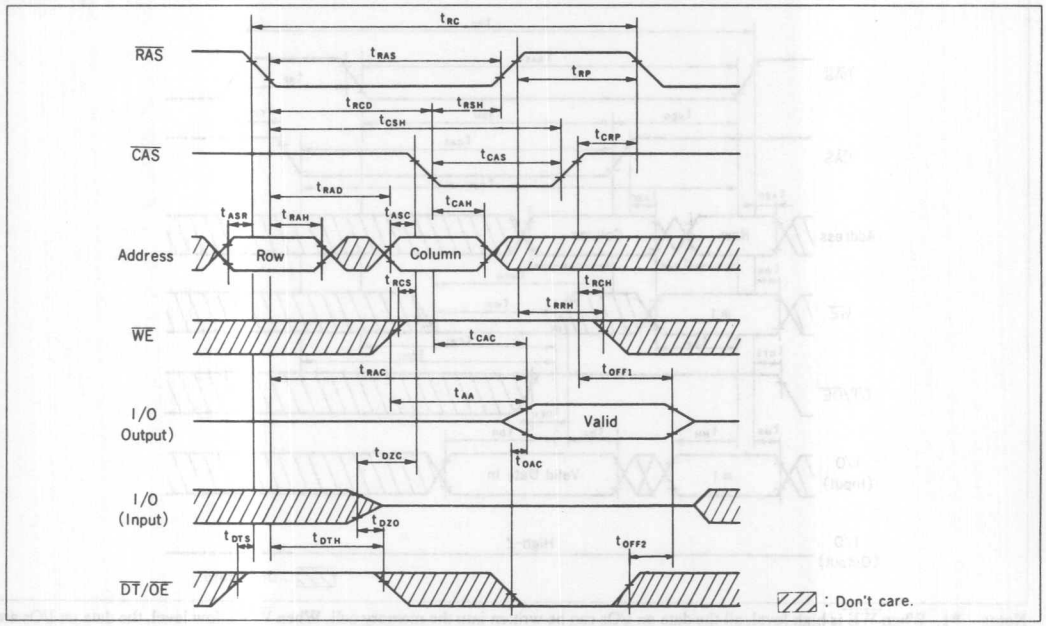
Logic Operation Mode

Item	Symbol	HM538122-10		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ hold time (logic operation set/reset cycle)	t_{FCHR}	90	—	100	—	120	—	ns	
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	60	—	70	—	80	—	ns	
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	—	165	—	200	—	ns	
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	60	—	70	—	80	—	ns	
Write cycle time	t_{FRC}	230	—	265	—	310	—	ns	
Page mode cycle time (write cycle)	t_{FPC}	85	—	100	—	120	—	ns	

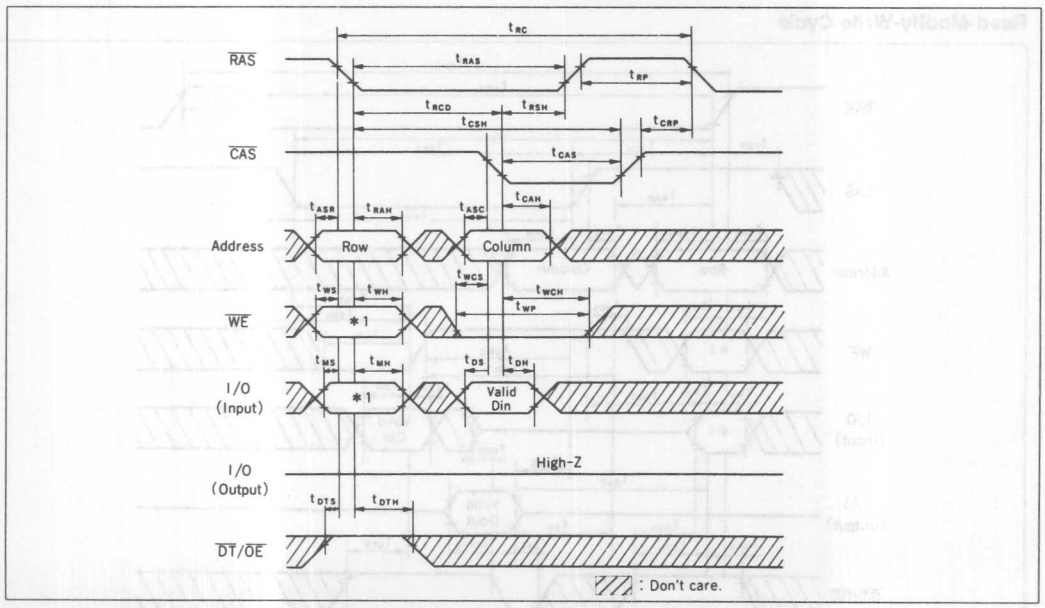
Notes:
*1. AC measurements assume t_T = 5 ns.
*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
*6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200 mV, V_{OL} + 200 mV).
*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
*11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

Timing Waveforms

Read Cycle

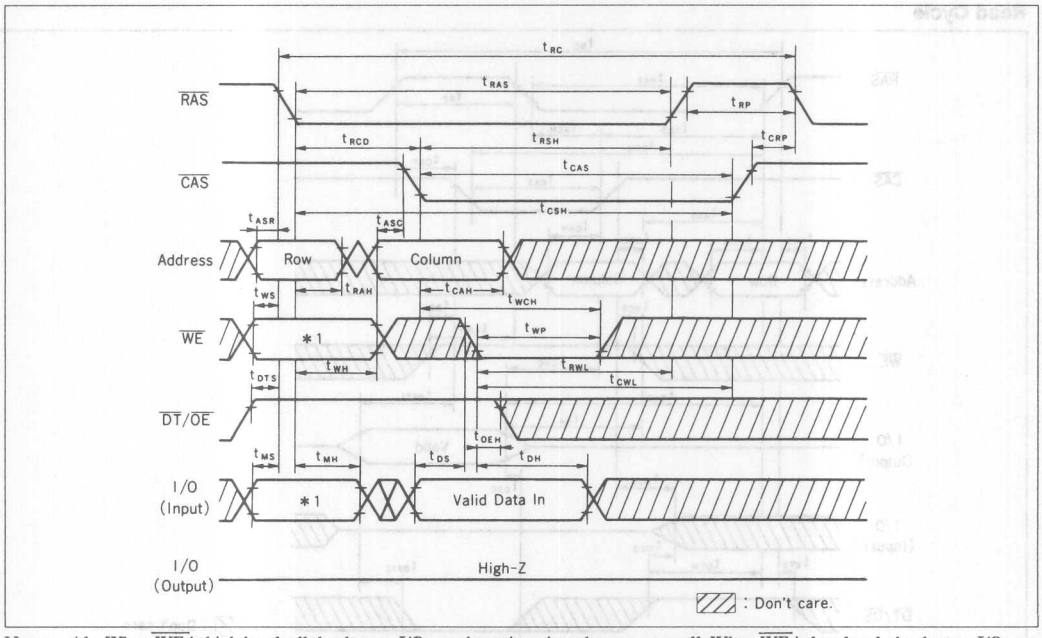


Early Write Cycle



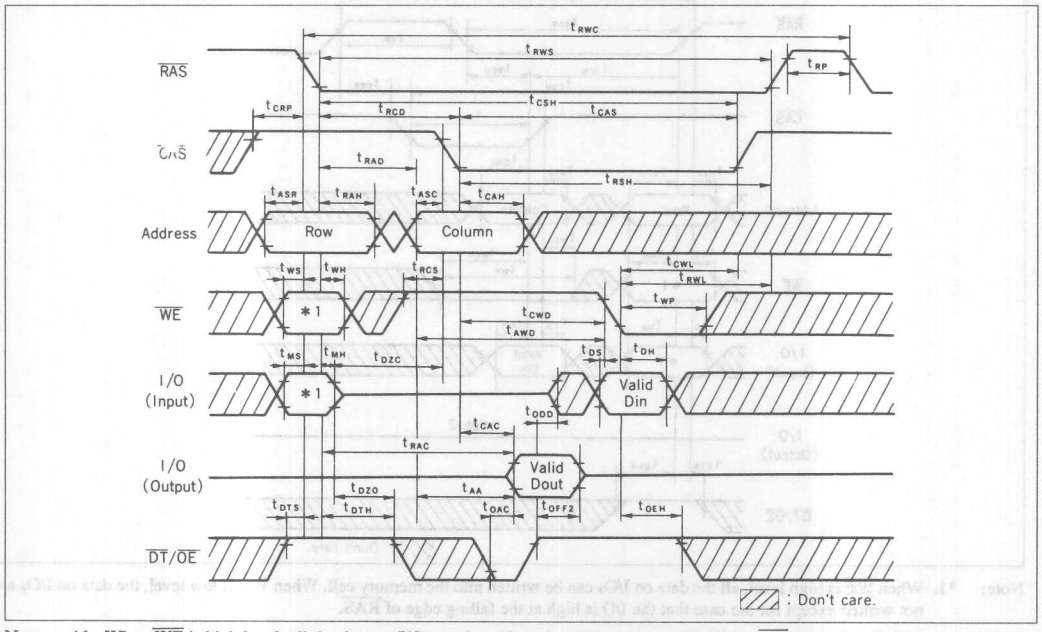
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

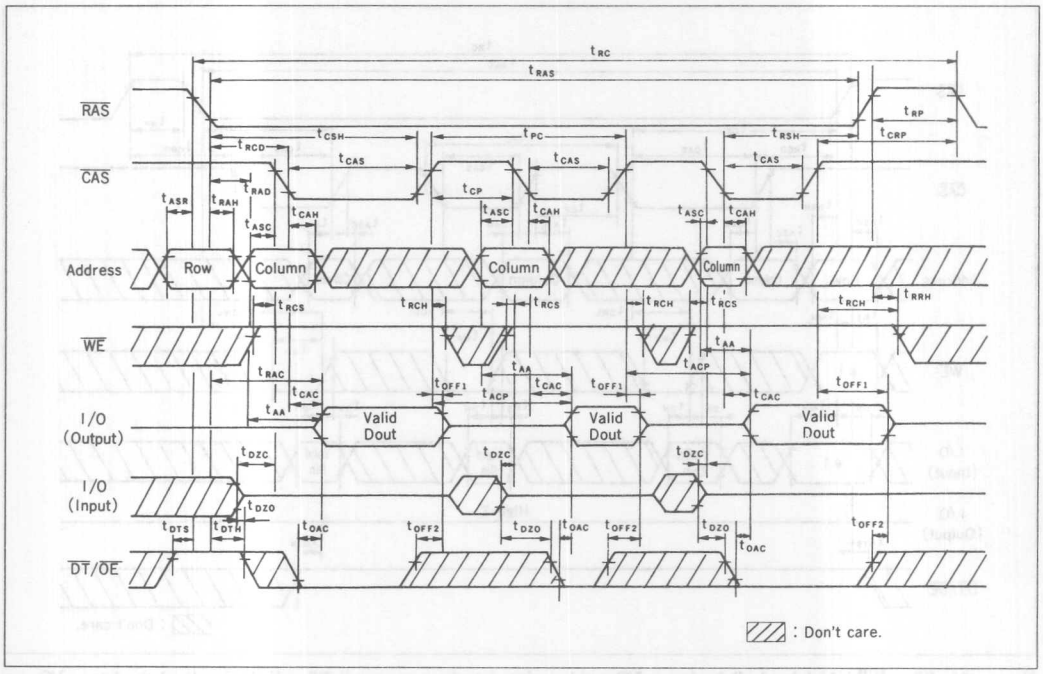
Read-Modify-Write Cycle



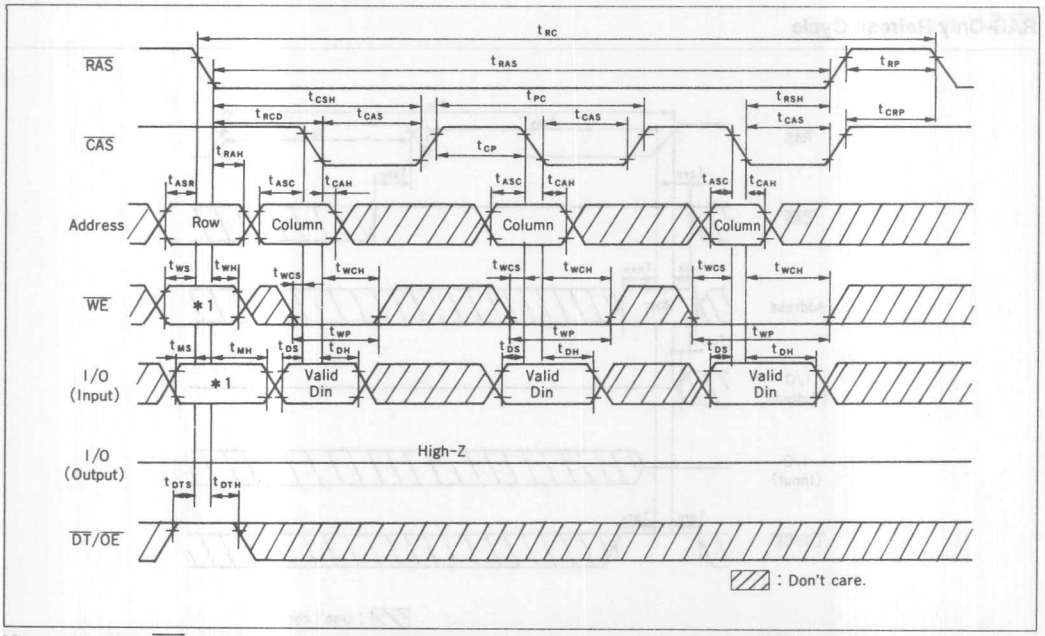
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

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Page Mode Read Cycle

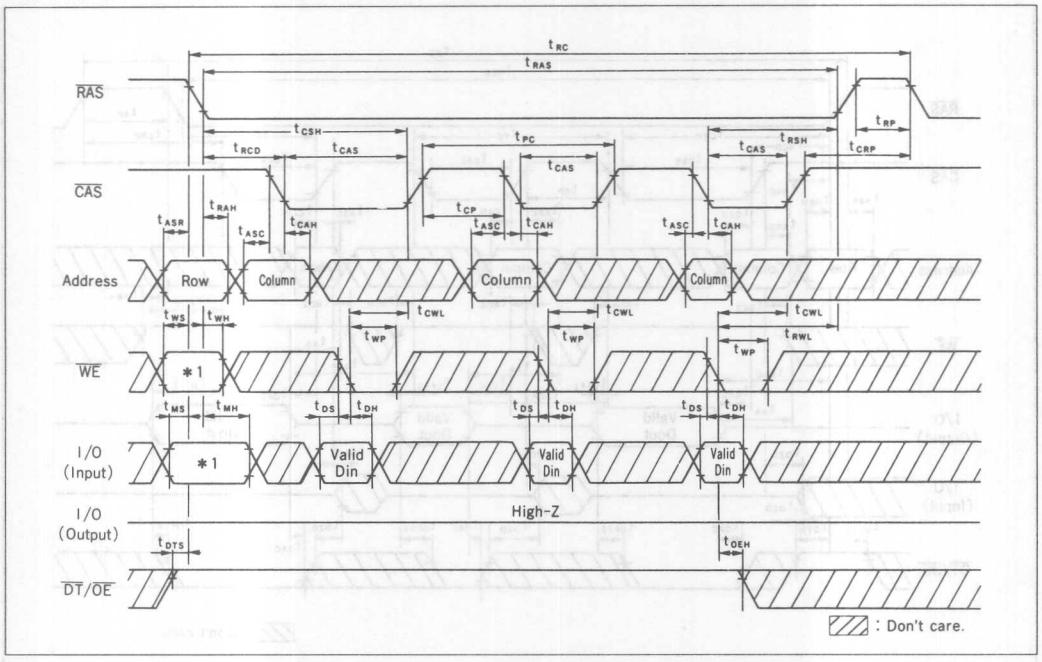


Page Mode Write Cycle (Early Write)



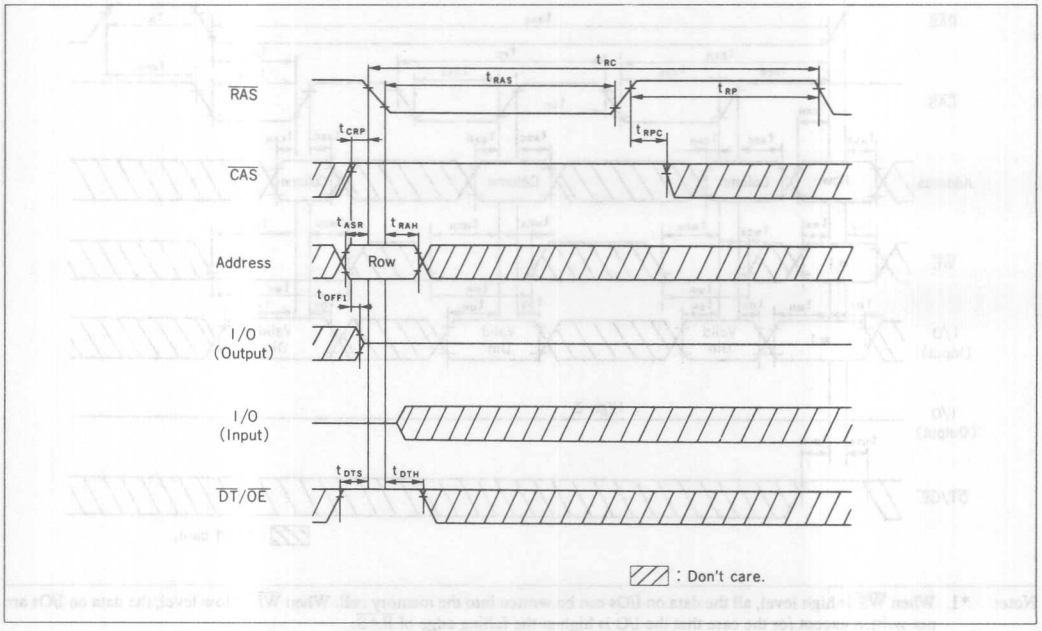
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

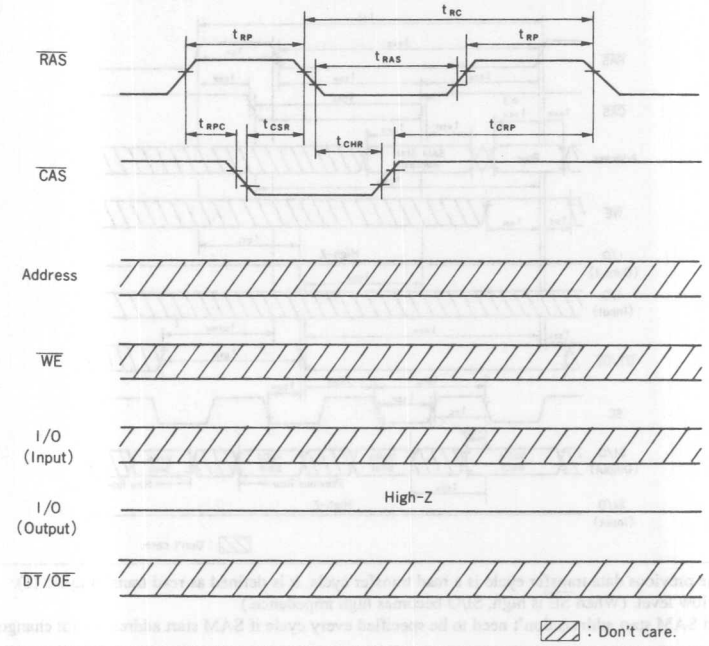


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

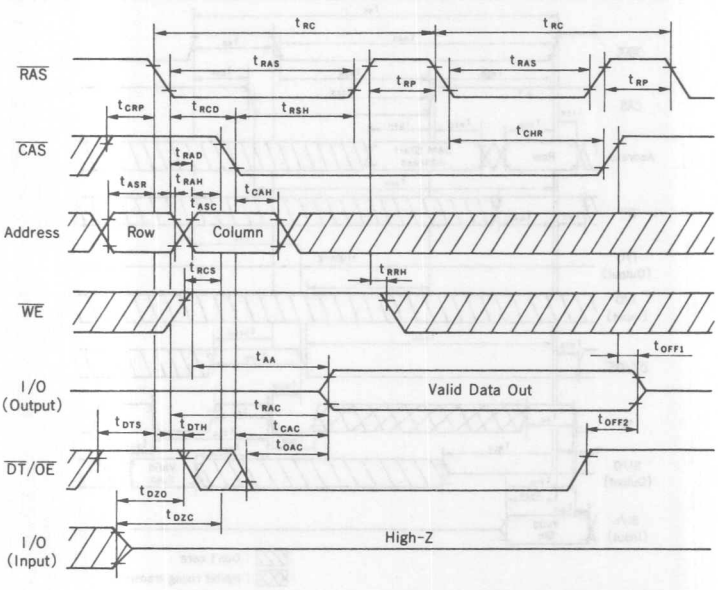
$\overline{RAS}$-Only Refresh Cycle



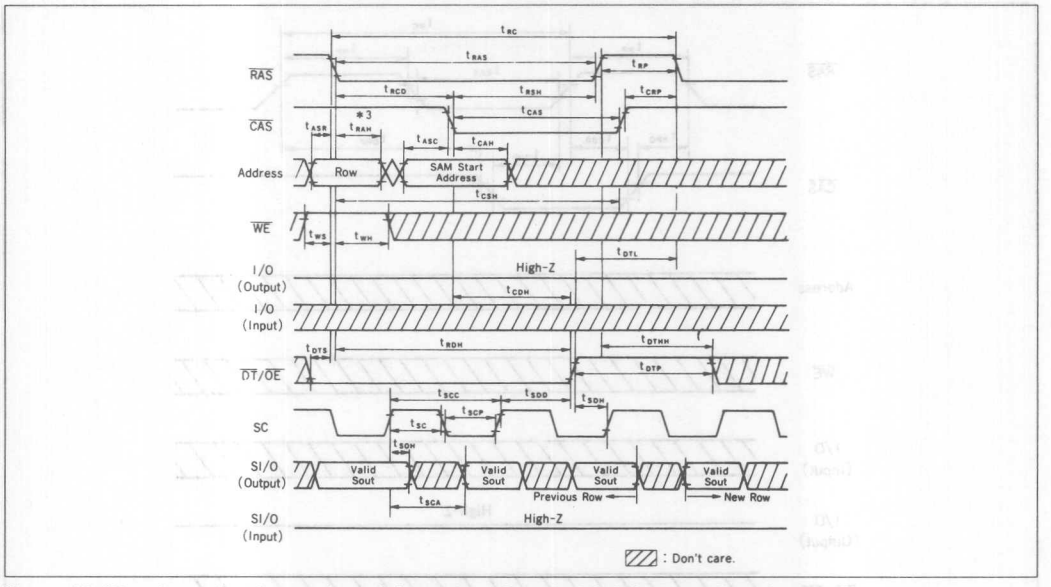
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle

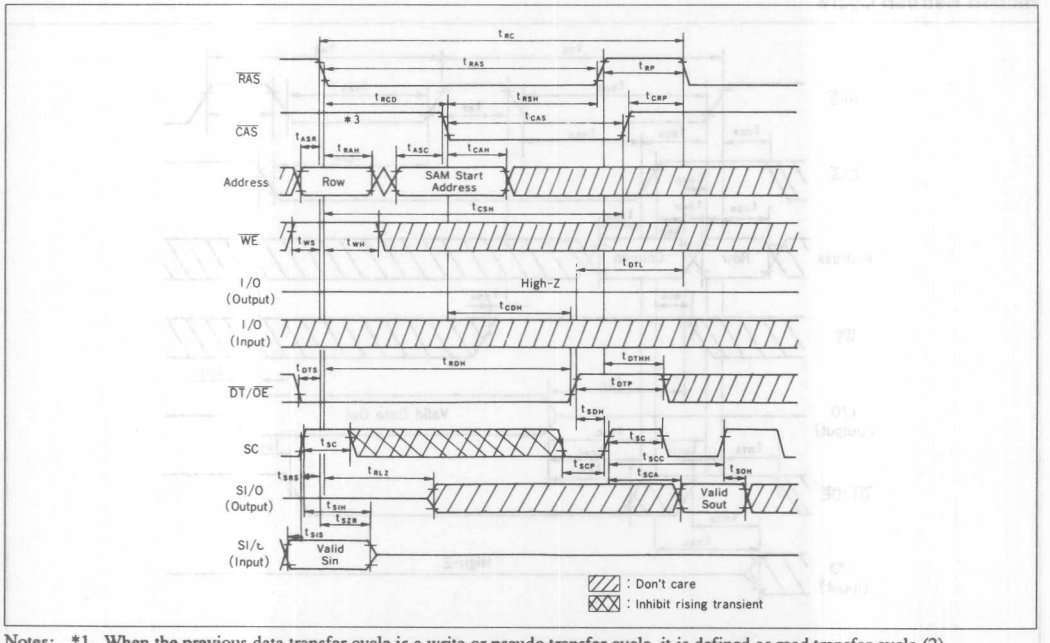


Read Transfer Cycle (1) *1, *2



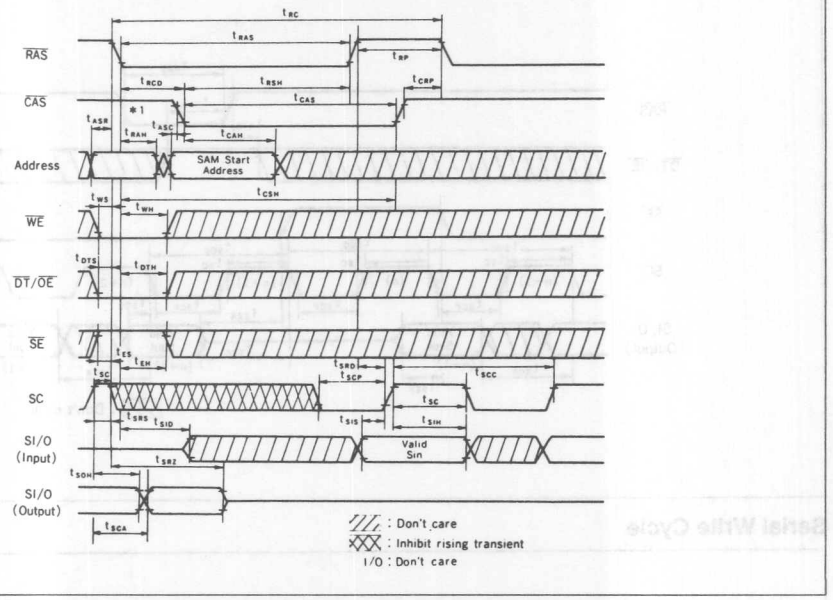
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle if SAM start address is not changed.

Read Transfer Cycle (2) *1, *2



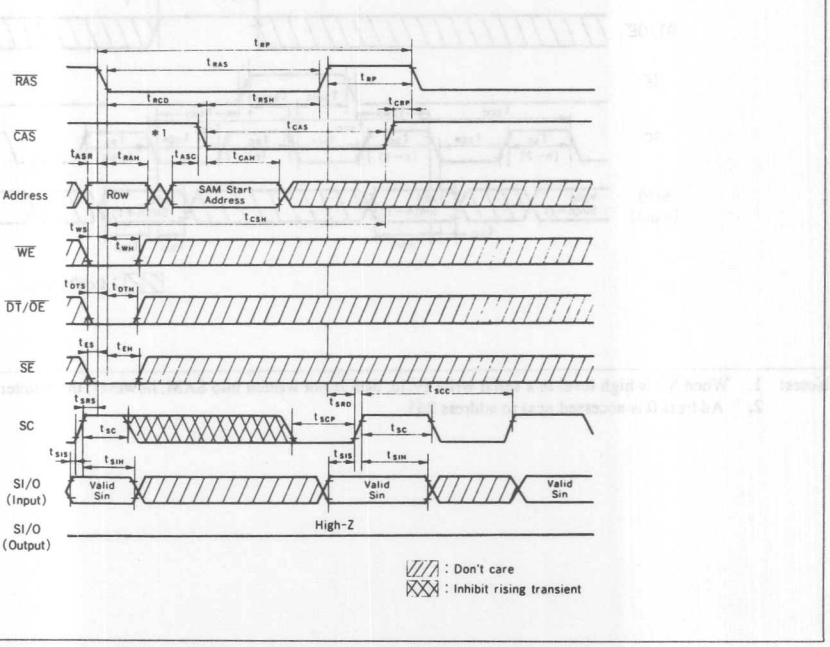
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle if SAM start address is not changed.

Pseudo Transfer Cycle



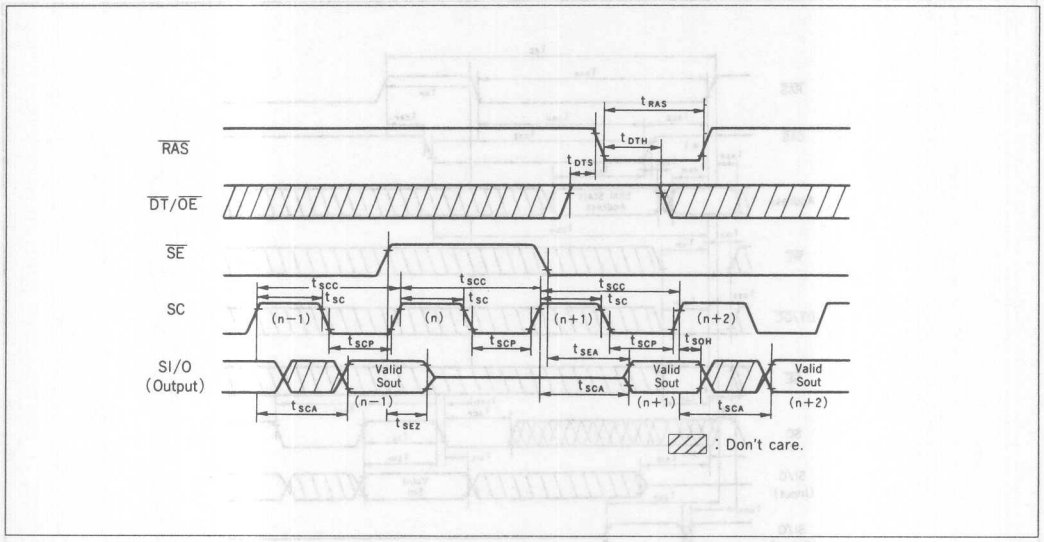
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Write Transfer Cycle

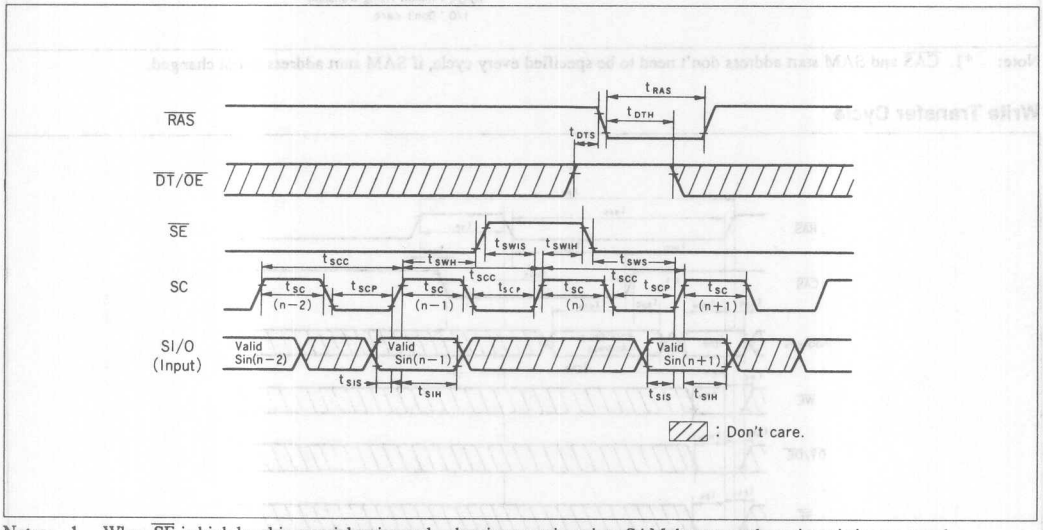


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Serial Read Cycle

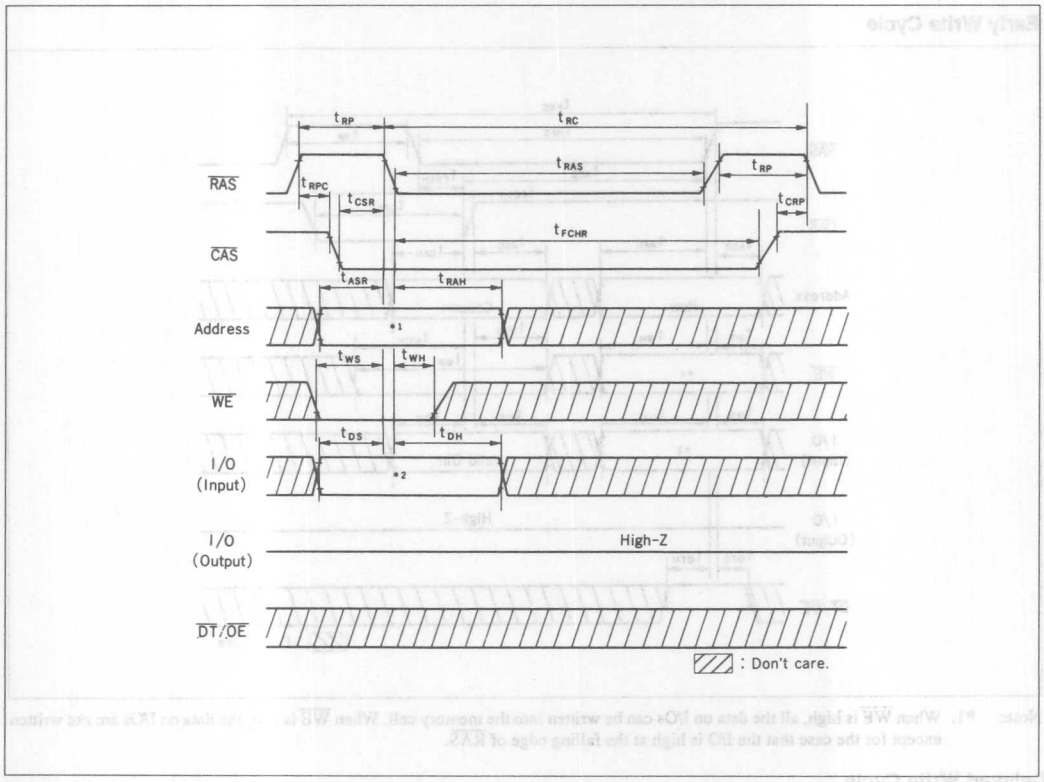


Serial Write Cycle



Notes: 1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
2. Address 0 is accessed next to address 255.

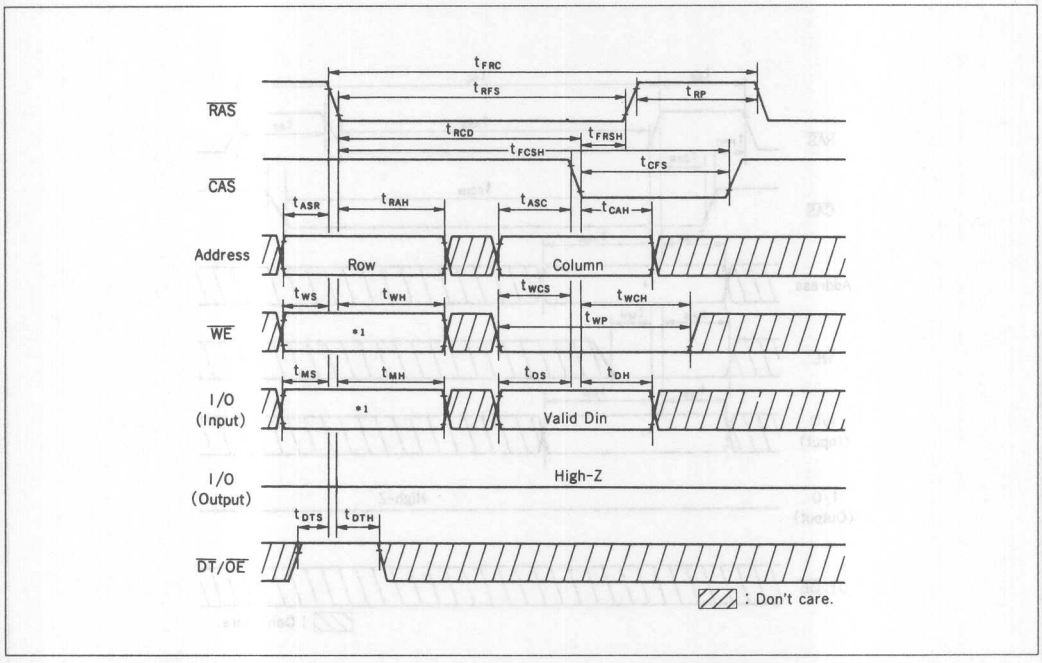
Logic Operation Set/Reset Cycle



Notes: 1. Logic code A0–A3
2. Write mask data

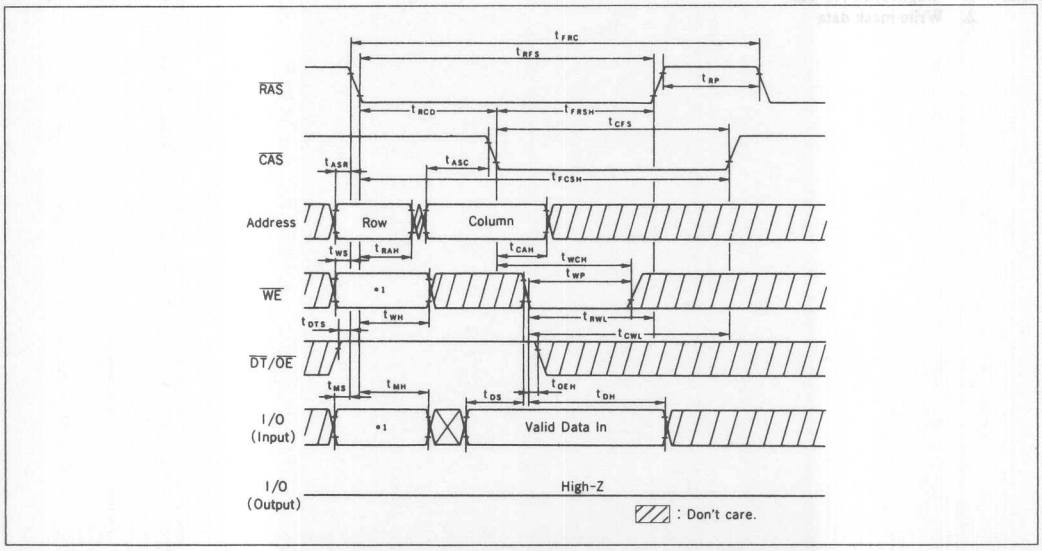
Logic Operation Mode Timing Waveforms

Early Write Cycle



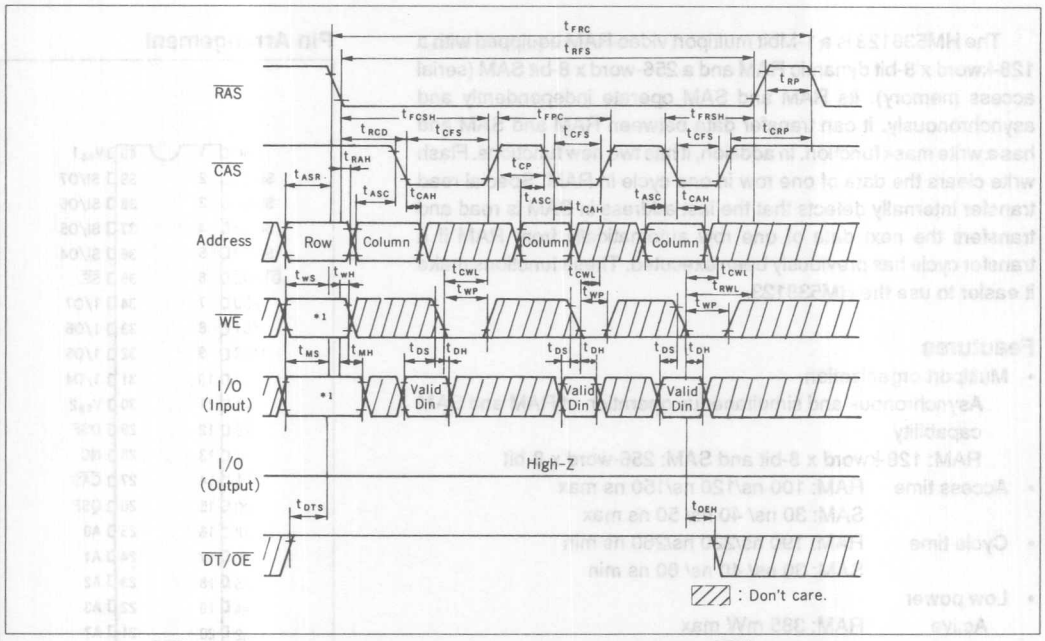
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



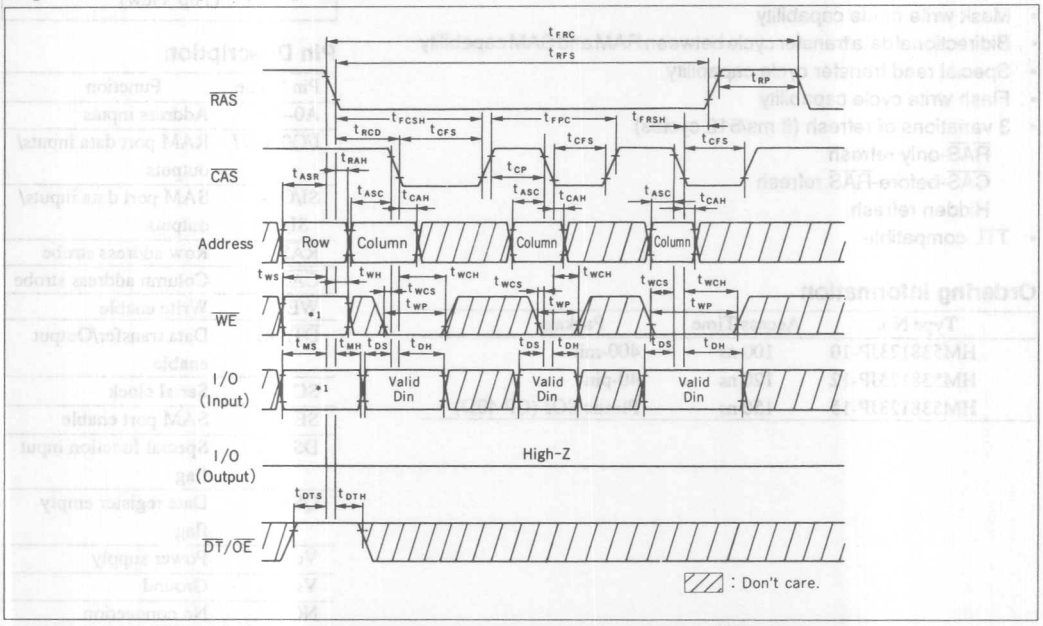
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write)



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

HM538123 Series — Preliminary

131072-Word × 8-Bit Multiport CMOS Video RAM

The HM538123 is a 1-Mbit multiport video RAM equipped with a 128-kword x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. In addition, it has two new functions. Flash write clears the data of one row in one cycle in RAM. Special read transfer internally detects that the last address in SAM is read and transfers the next data of one row automatically from RAM if a transfer cycle has previously been executed. These functions make it easier to use the HM538123.

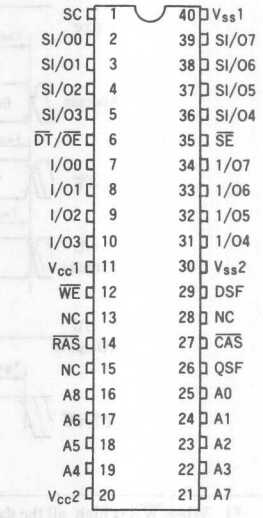
Feautures

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 128-kword x 8-bit and SAM: 256-word x 8-bit
- Access time — RAM: 100 ns/120 ns/150 ns max; SAM: 30 ns/ 40 ns/ 50 ns max
- Cycle time — RAM: 190 ns/220 ns/260 ns min; SAM: 30 ns/ 40 ns/ 60 ns min
- Low power
  - Active — RAM: 385 mW max; SAM: 275 mW max
  - Standby — 40 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Special read transfer cycle capability
- Flash write cycle capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM538123JP-10	100 ns	400-mil
HM538123JP-12	120 ns	40-pin
HM538123JP-15	150 ns	Plastic SOJ (CP-40D)

Pin Arrangement



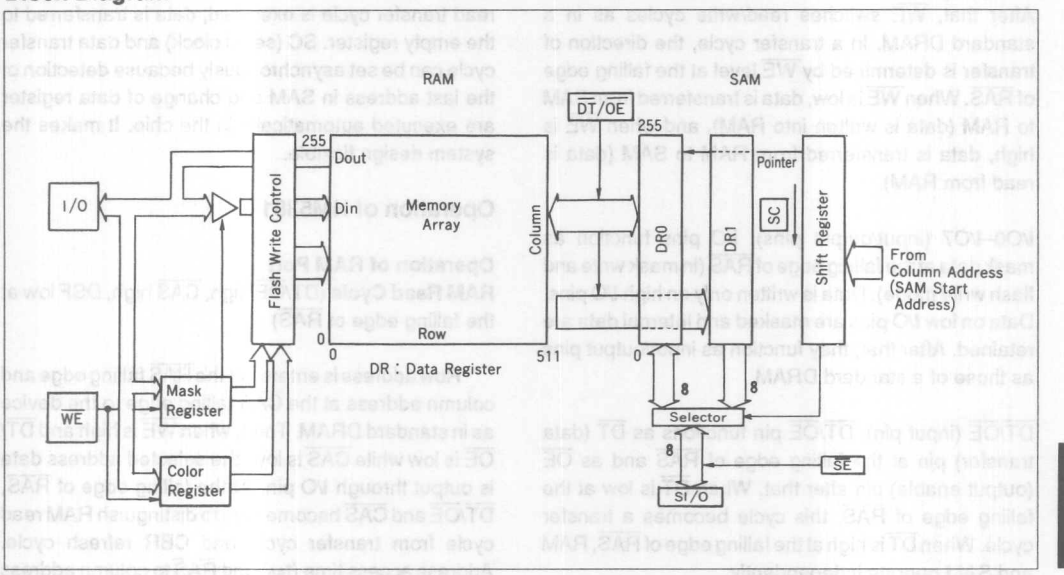
(Top View)

Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O7	RAM port data inputs/ outputs
SI/O0–SI/07	SAM port data inputs/ outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF	Special function input flag
QSF	Data register empty flag
Vcc	Power supply
Vss	Ground
NC	No connection

This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Block Diagram



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538123.

Table 1. Operation Cycles of the HM538123

Input Level at the Falling edge of $\overline{RAS}$					Operation Cycle
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	DSF	
H	H	H	×	L	RAM read/write
H	H	H	×	H	Color register set
H	H	L	×	L	Mask write
H	H	L	×	H	Flash write
H	L	H	×	L	Special read initialization
H	L	H	×	H	Special read transfer
H	L	L	H	×	Pseudo transfer
H	L	L	L	×	Write transfer
L	×	×	×	×	CBR refresh

Note: ×; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0–A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538123 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the

falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write and flash write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a special read transfer cycle or special read initialization cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special data input flag pin. It is set to high when new functions such as color register set, special read transfer, and flash write, are used.

QSF (output pin): The HM538123 has a double buffer organization which includes two SAM data registers to relax the restriction on timings of $\overline{DT}/\overline{OE}$ and SC in real time transfer cycle. QSF flag turns high when output from one of SAM data registers finished (data register empty flag). If the condition is detected and special read transfer cycle is executed, data is transferred to the empty register. SC (serial clock) and data transfer cycle can be set asynchronously because detection of the last address in SAM and change of data register are executed automatically in the chip. It makes the system design flexible.

Operation of HM538123

Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle
(Early Write, Delayed Write, Read Modify Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle
  ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read modify write cycle and enables read/write to execute in the

same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode
  ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80 %. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 µs).

Flash Write Function (See figure. 1)

- Color Register Set Cycle ($\overline{CAS}$·$\overline{DT}/\overline{OE}$·$\overline{WE}$ high, DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it preserves the data until reset. The data set is just as same as in the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and early write and delayed write cycle can be executed. In this cycle, memory array access is not executed, so it is unnecessary to give row and column addresses.

- Flash Write Cycle ($\overline{CAS}$·$\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256 x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also possible to mask I/O in this cycle. When $\overline{CAS}$·$\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is preserved. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time.

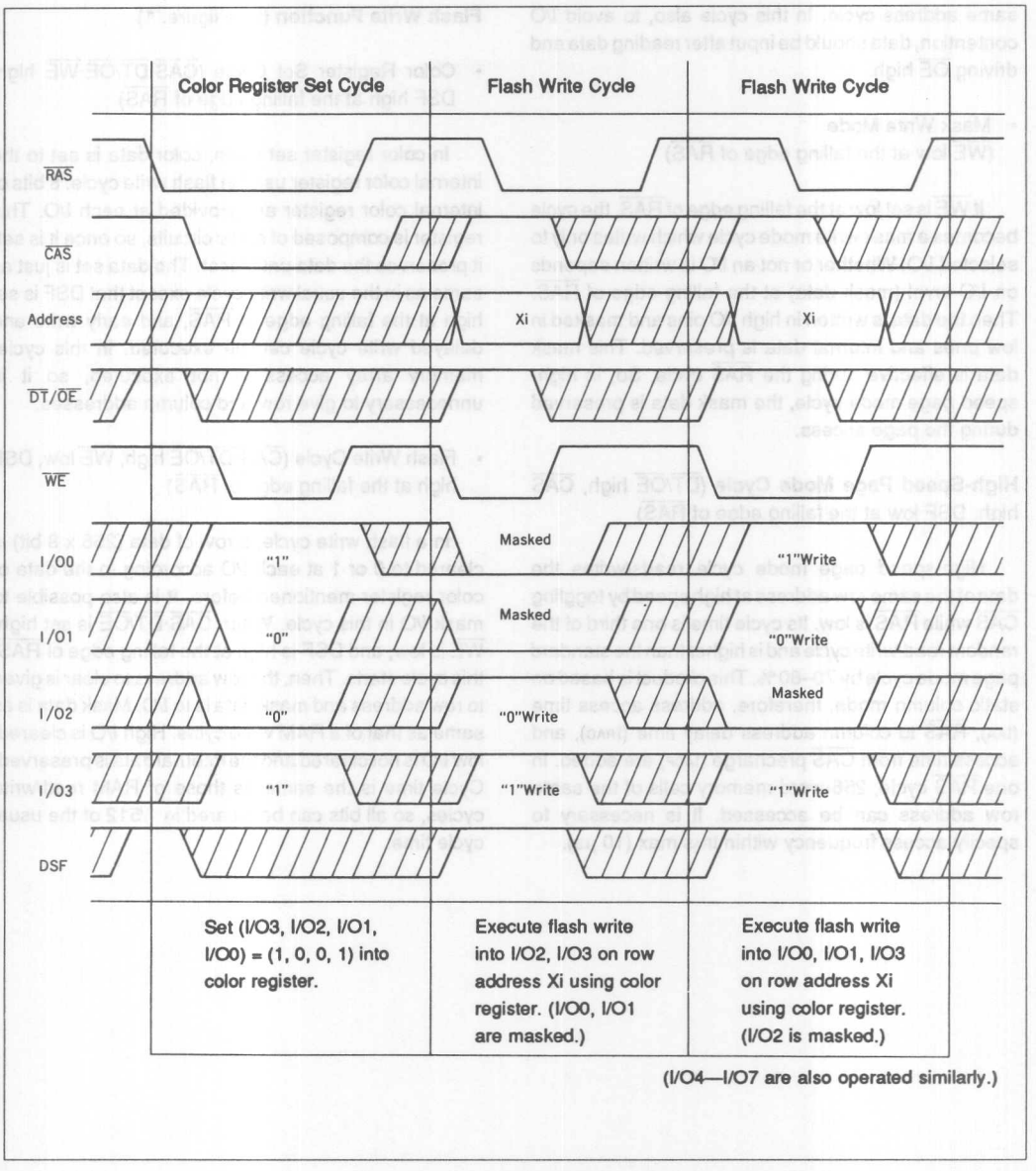


Figure 1. Use of Flash Write

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Transfer Operation

The HM538123 provides the special read initialization cycle, special read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
  (a) Special read initialization cycle,
  Special read transfer cycle: RAM → SAM
  (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
  Special read initialization cycle: SI/O output
  Pseudo transfer cycle,
  write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Special Read Initialization Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high, DSF low at the falling edge of $\overline{RAS}$)

If $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ high, and DSF low at the falling edge of $\overline{RAS}$, this cycle becomes a special read initialization cycle. Special read initialization is used (1) to start special read transfer operation and (2) to switch SAM input/output pin (SI/O) set in input state by pseudo transfer cycle or write transfer cycle, to output state.

If the clock is set as mentioned before, address of SAM transfer word line is set to row address and first SAM address to access (SAM start address) to column address, it becomes possible to execute SAM read after t_{SRD} (min) after $\overline{RAS}$ is high. In this cycle, SI/O outputs uncertain data after the $\overline{RAS}$ falling edge. So when SAM is in input state before executing this cycle, it is necessary to stop input before the $\overline{RAS}$ falling edge.

SAM access is inhibited while $\overline{RAS}$ is low in this cycle. SC should not be raised during $\overline{RAS}$ low.

Special Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high, DSF high at the falling edge of $\overline{RAS}$)

Ordinary multiport video RAM has some problems; (1) severe limitation on timings between processor clock $\overline{DT/OE}$ and CRT clock SC, (2) complicated external control circuit to detect SAM last address externally and to insert transfer cycle synchronously. Special read transfer cycle makes it possible to relax the timing limitations and to set serial clock (SC) and transfer cycle perfectly synchronously.

Figure 2 shows the block diagram for a special read transfer. SAM double buffers are composed of two data registers (DR). When data is read out from DR0 serially, special read transfer cycle transfers a row of RAM data, which will be read from SAM next, to DR1.

The end of data read from DR0 is detected internally and data register switching circuit automatically switches to DR1 output. So data can be output continuously.

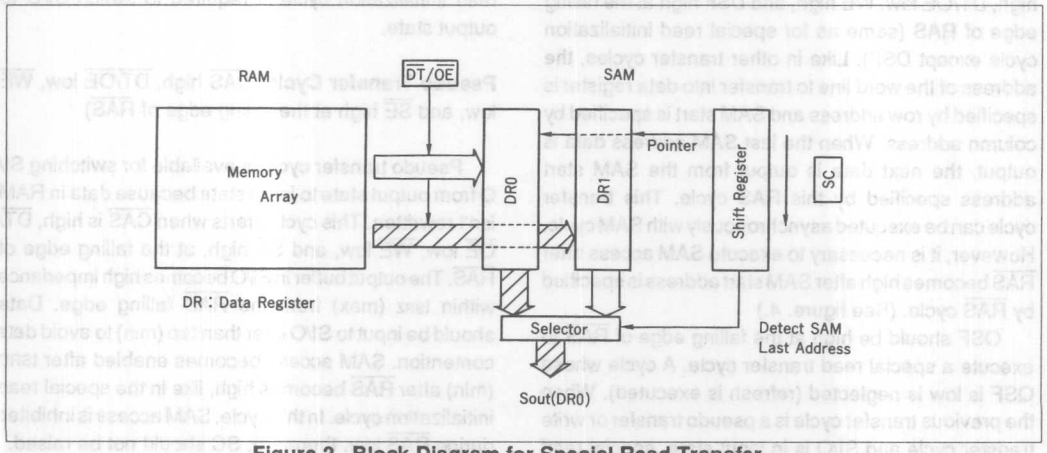


Figure 2. Block Diagram for Special Read Transfer

Figure 3 shows special read transfer operation sequence. QSF flag indicates that reading out from data resister has finished (data register empty flag), and special read transfer can be executed while QSF is high. At first, special read operation starts by executing an special read initialization cycle. So QSF becomes high, the processor gives row address and SAM start address, which is needed next, to the memory, and inserts a special read transfer cycle. Data register becomes full after a special read transfer cycle, so QSF becomes low during the cycle. When the last SAM address is accessed, QSF becomes high and the data register, which outputs from the next SAM address, changes, and serial access can be executed.

By executing these handshakes, serial clock and transfer cycle can be executed perfectly asynchronously, and flexibility of the system design is improved.

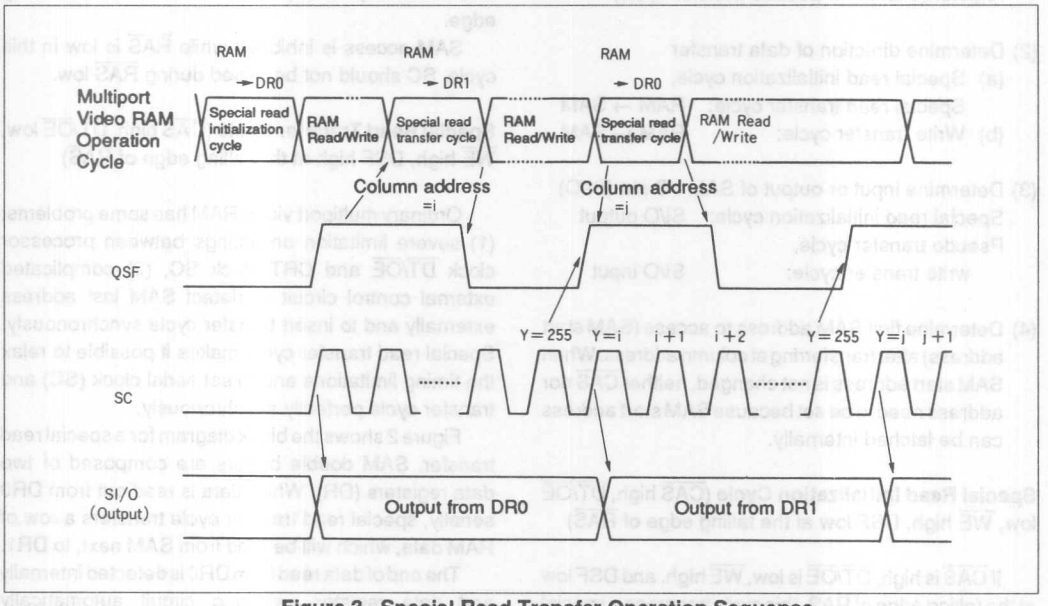


Figure 3. Special Read Transfer Operation Sequence

Special read transfer cycle is set by making $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high, and DSF high at the falling edge of RAS (same as for special read initialization cycle except DSF). Like in other transfer cycles, the address of the word line to transfer into data register is specified by row address and SAM start is specified by column address. When the last SAM address data is output, the next data is output from the SAM start address specified by this RAS cycle. This transfer cycle can be executed asynchronously with SAM cycle. However, it is necessary to execute SAM access after $\overline{RAS}$ becomes high after SAM start address is specified by $\overline{RAS}$ cycle. (See figure. 4.)

QSF should be high at the falling edge of $\overline{RAS}$ to execute a special read transfer cycle. A cycle whose QSF is low is neglected (refresh is executed). When the previous transfer cycle is a pseudo transfer or write transfer cycle and SI/O is in input state, special read transfer cycle cannot be used (neglected). Special read initialization cycle is required to switch SI/O to output state.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high, like in the special read initialization cycle. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

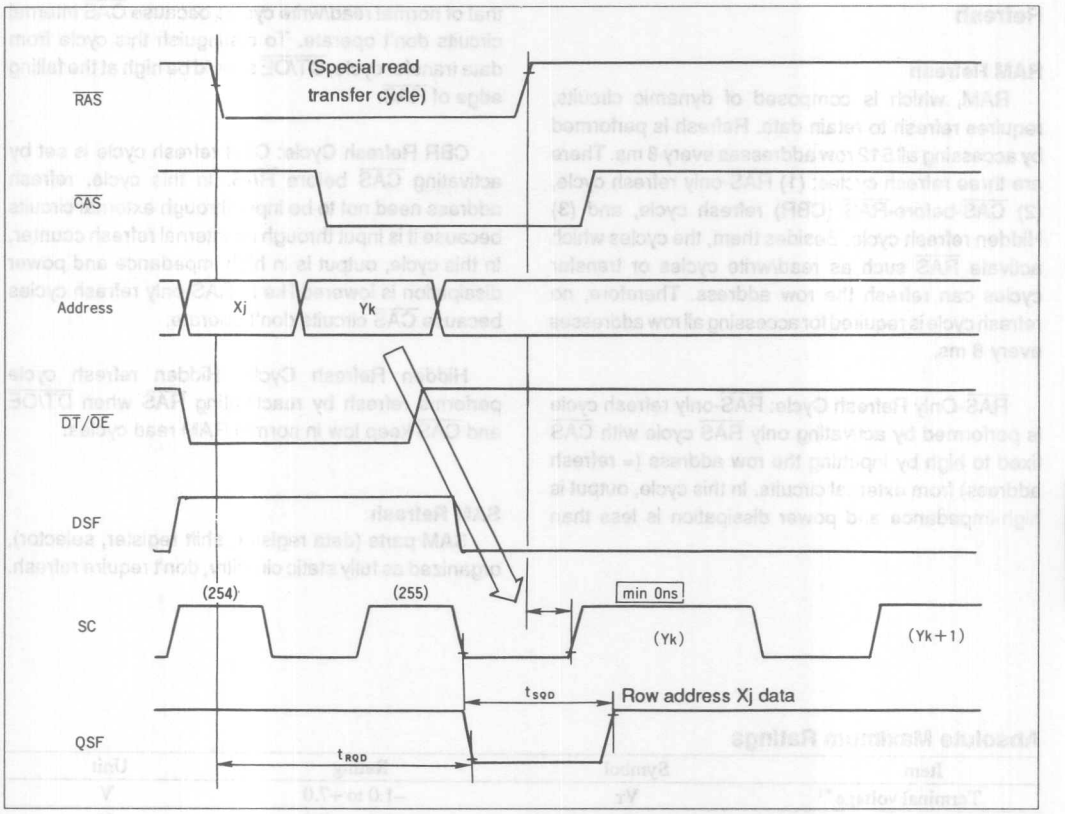


Figure 4. The Restriction of Special Read Transfer

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is special read initialization cycle or special read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When the last address is accessed at the state of QSF low (data register is full), it is signaled to external circuits that special read transfer is enabled by making QSF high. Next, after SAM access, output data register is switched, then the row address data given by previous special read transfer cycle is output from the SAM start address. If special read transfer isn't performed (QSF high), the column address 0 of the same row address is accessed after the last address is accessed.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so SE high can be used to mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$-only refresh cycles because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	–1.0 to +7.0	V
Power supply voltage *1	V_{CC}	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: *1. Relative to V_{SS}.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	—	6.5	V
Input low voltage *1	V_{IL}	–0.5*2	—	0.8	V

Notes: *1. All voltages referenced to V_{SS}.
*2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM538123 -10 Min	HM538123 -10 Max	HM538123 -12 Min	HM538123 -12 Max	HM538123 -15 Min	HM538123 -15 Max	Unit	Test Conditions RAM port	Test Conditions SAM port
Operating current	I_{CC1}	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	120	—	100	—	80	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	40	—	30	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{RAS}$-only refresh current	I_{CC3}	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	110	—	90	—	70	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Page mode	I_{CC4}	—	65	—	55	—	45	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	115	—	95	—	75	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling t_{RC} =Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Data transfer current	I_{CC6}	—	90	—	90	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	125	—	125	—	125	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

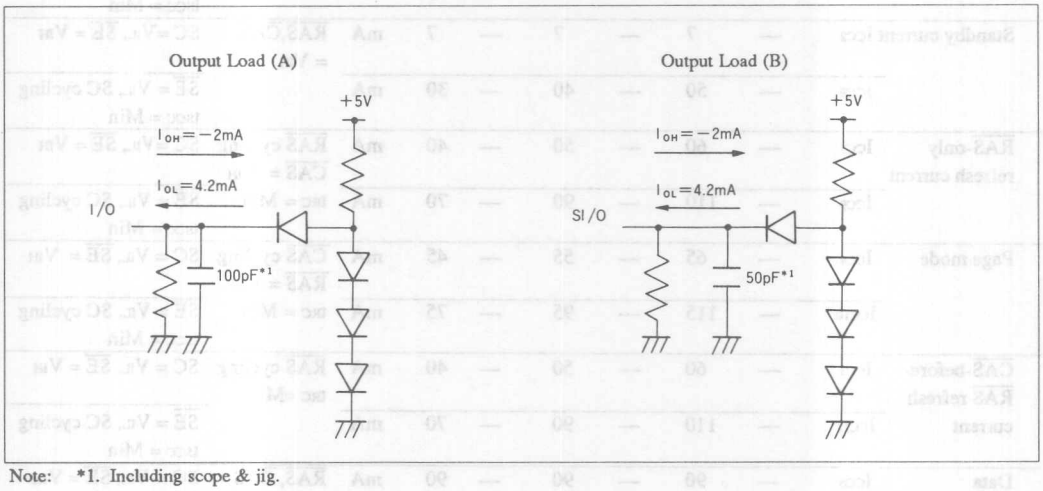
Capacitance (Ta = 25°C, V_{CC} =5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V) *1, *11

Test Conditions

Input rise and fall time : 5 ns
Output load : See figures
Input timing reference levels : 0.8 V, 2.4 V
Output timing reference levels : 0.4 V, 2.4 V



Note: *1. Including scope & jig.

Common Parameter

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	190	—	220	—	260	—	ns	
$\overline{RAS}$ precharge time	tRP	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	tRAS	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width	tCAS	30	10000	35	10000	40	10000	ns	
Row address setup time	tASR	0	—	0	—	0	—	ns	
Row address hold time	tRAH	15	—	15	—	20	—	ns	
Column address setup time	tASC	0	—	0	—	0	—	ns	
Column address hold time	tCAH	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	25	70	25	85	30	110	ns	*5,*6
$\overline{RAS}$ hold time	tRSH	30	—	35	—	40	—	ns	
$\overline{CAS}$ hold time	tCSH	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10	—	10	—	10	—	ns	
Transition time (rise to fall)	tT	3	50	3	50	3	50	ns	*8
Refresh period	tREF	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	tDTS	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	tDTH	15	—	15	—	20	—	ns	
DSF to $\overline{RAS}$ setup time	tSFS	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ hold time	tSFH	25	—	25	—	30	—	ns	
Data-in to $\overline{OE}$ delay time	tDZO	0	—	0	—	0	—	ns	
Data–in to $\overline{CAS}$ delay time	tDZC	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	55	—	70	ns	*3, *6
Output buffer turn off delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	*7
Output buffer turn off delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	*7
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	*12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	*12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	65	25	80	ns	*5, *6
Page mode cycle time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	*9
Write command hold time	t_{WCH}	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	75	—	90	—	ns	*9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	95	—	120	—	ns	*9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	55	—	70	ns	*3,*6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	65	25	80	ns	*5,*6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Transfer Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	100	–	120	–	150	ns	*4
$\overline{RAS}$ to QSF (high) delay time	t_{RQH}	—	TBD	–	TBD	–	TBD	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	—	10	–	10	–	10	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	*7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	–	40	–	50	ns	*4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	

Serial Read Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	40	—	50	ns	*4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	40	ns	*4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	0	25	0	25	0	30	ns	*7
Last SC to QSF delay time	t_{SQD}	—	TBD	—	TBD	—	TBD	ns	*4

Serial Write Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wite enable hold time	t_{SWH}	30	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	50	—	ns	

Flash Write Cycle

Item	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Flash write cycle time	t_{RCFW}	230	—	265	—	310	—	ns	
$\overline{RAS}$ pulse width	t_{RCSFW}	140	—	165	—	200	—	ns	
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{CAS}$ high level hold time referenced to $\overline{RAS}$	t_{CHHR}	20	—	25	—	30	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	

Notes: *1. AC measurements assume $t_T = 5$ ns.

*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.

*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.

*6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.

*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200 mV, V_{OL} + 200 mV).

*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data out pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.

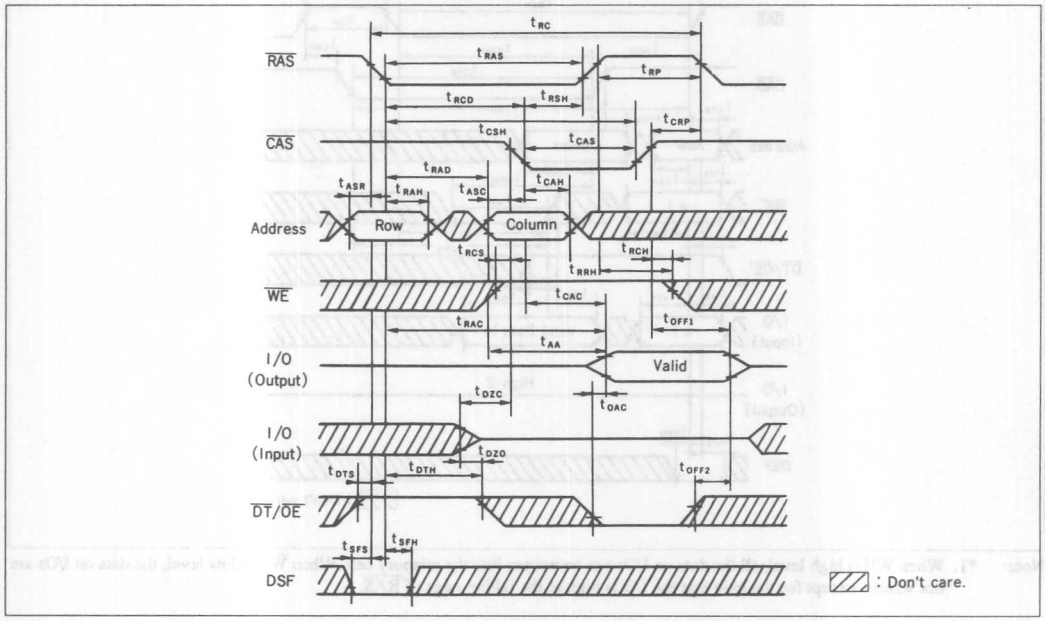
*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.

*11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.

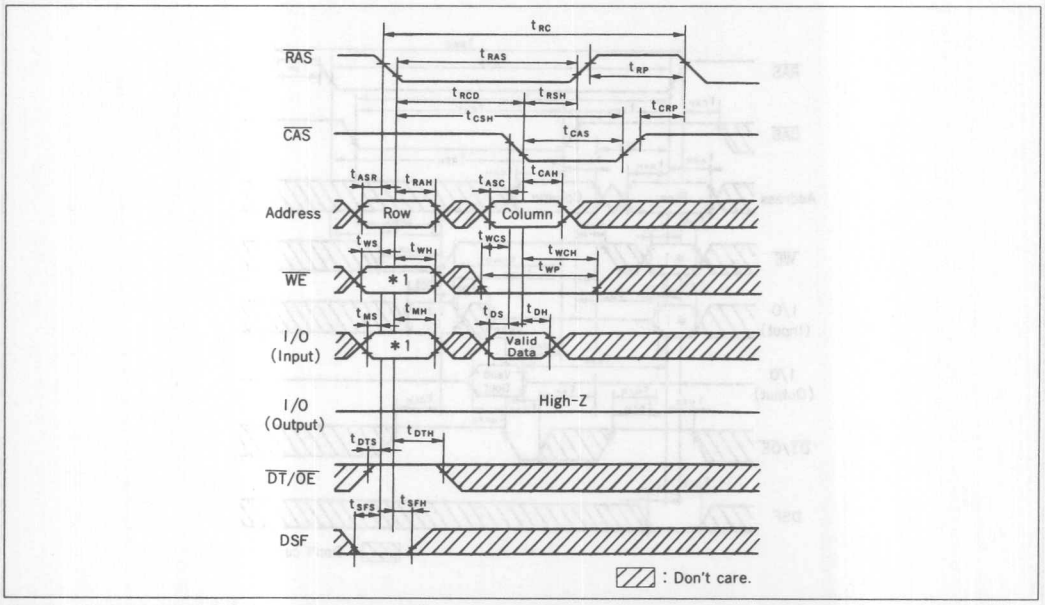
*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

Timing Waveforms

Read Cycle

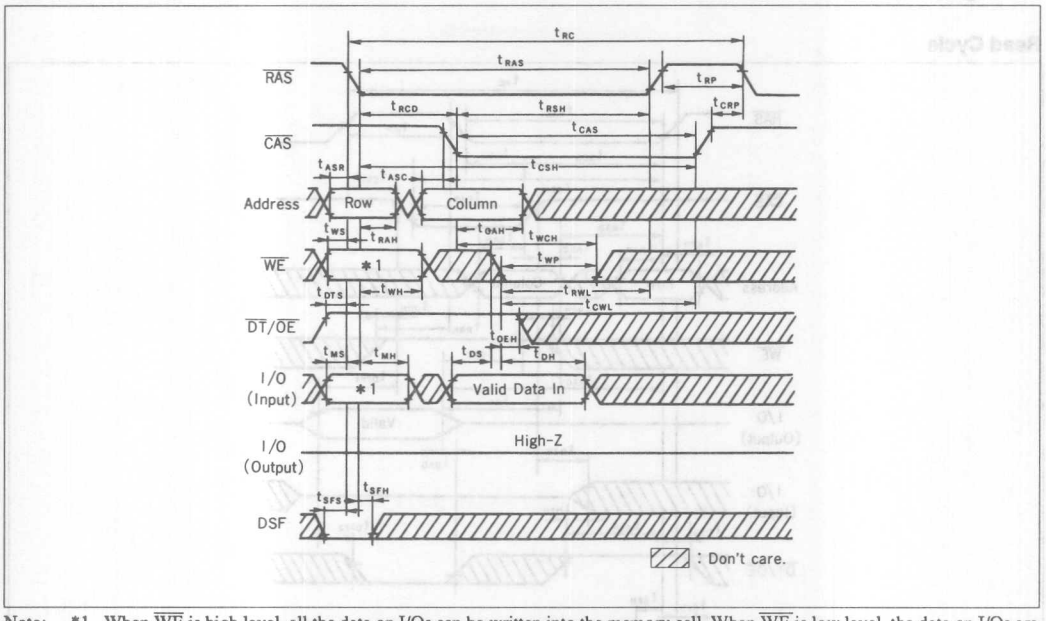


Early Write Cycle



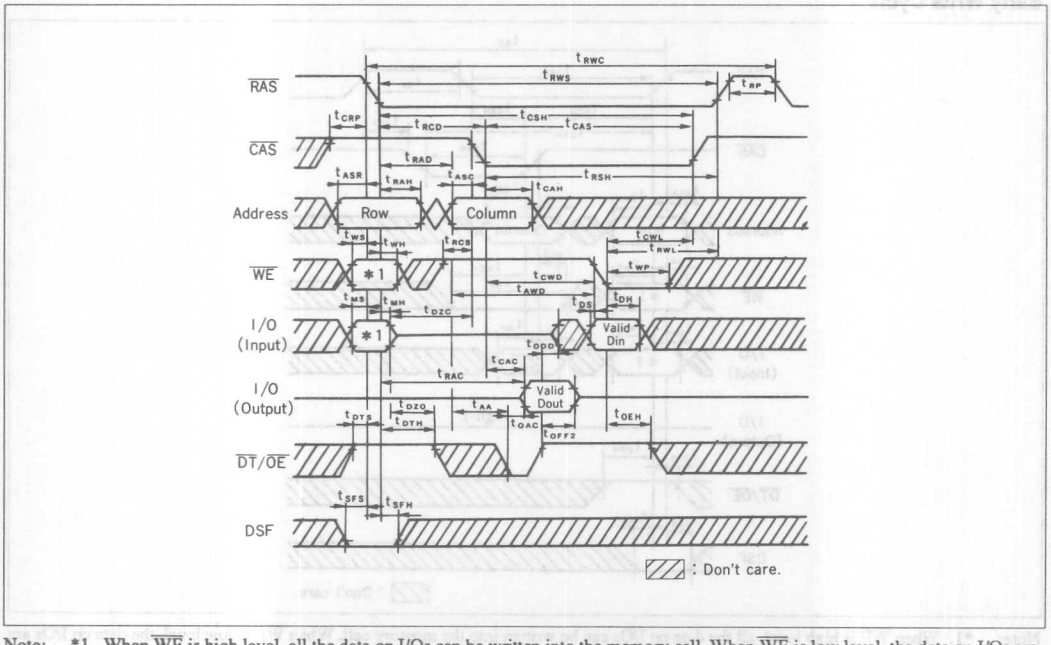
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



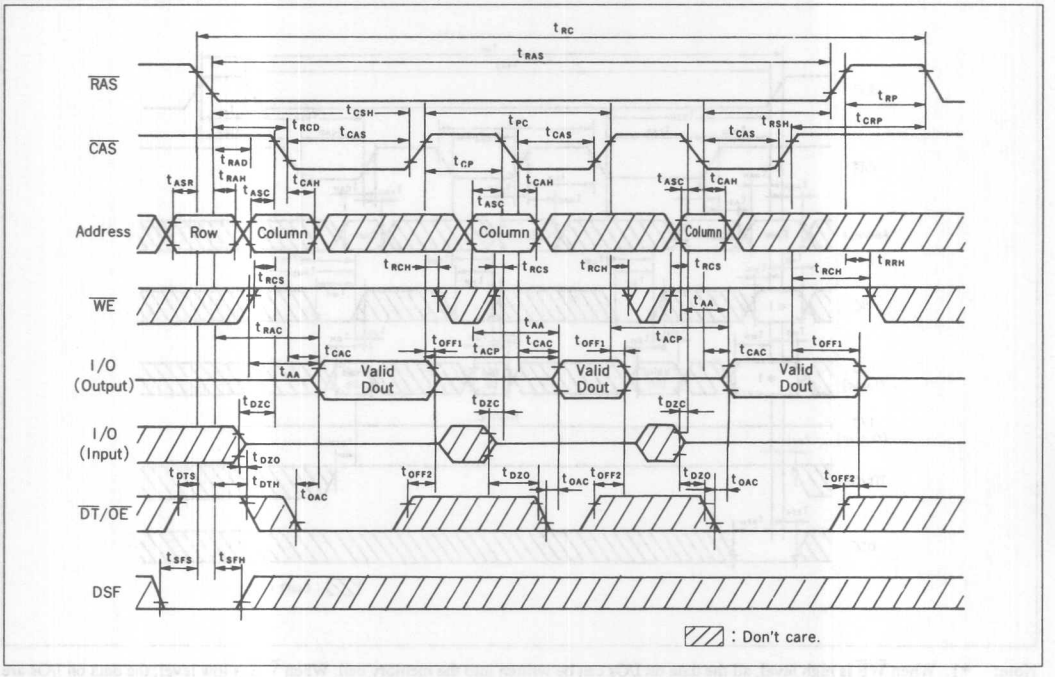
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

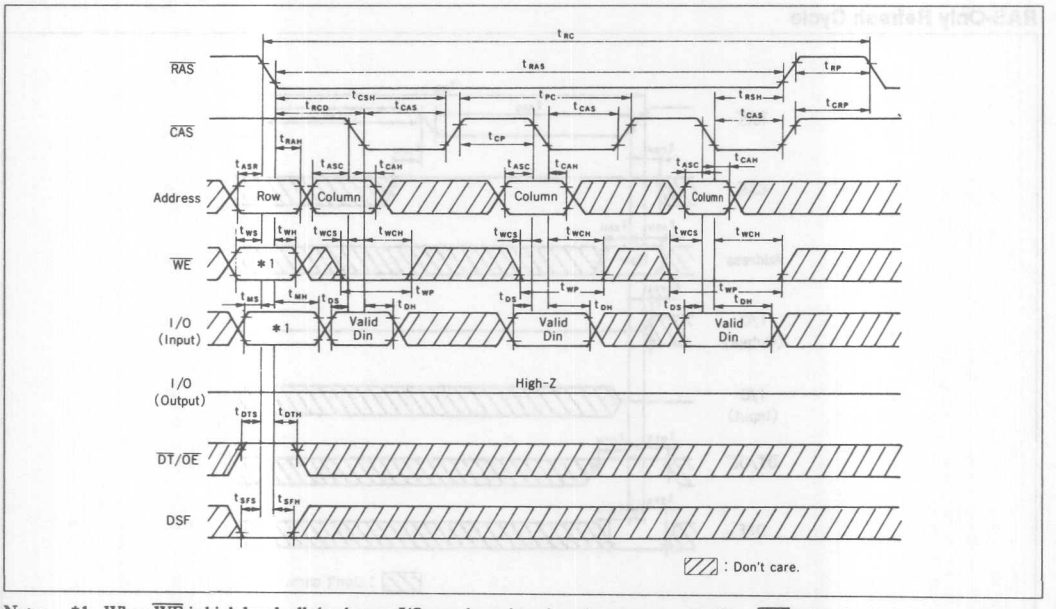


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

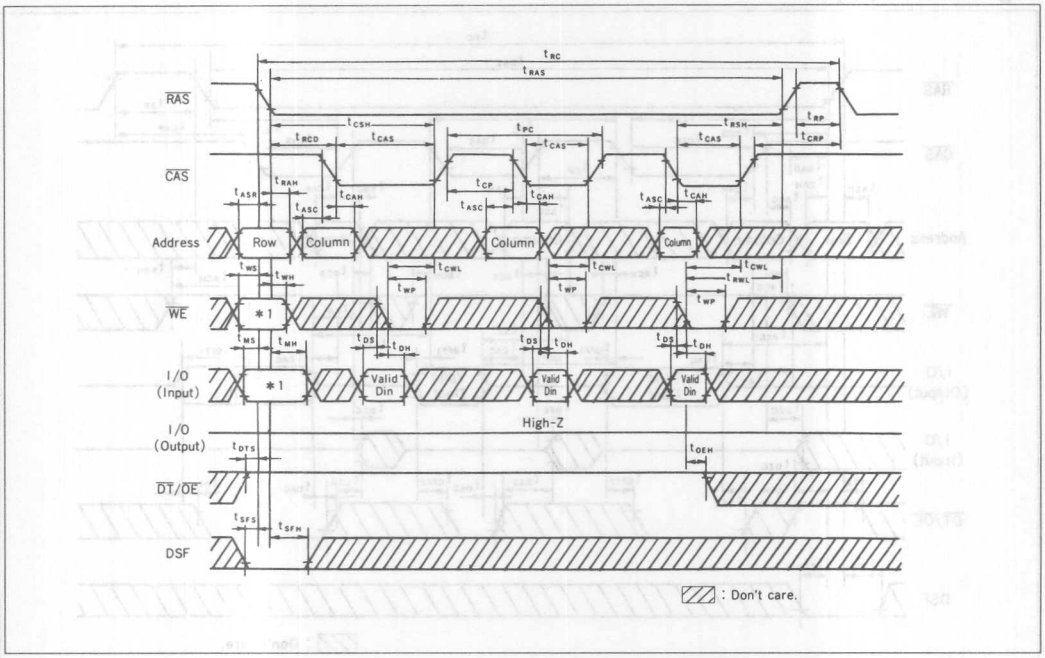


Page Mode Write Cycle (Early Write)



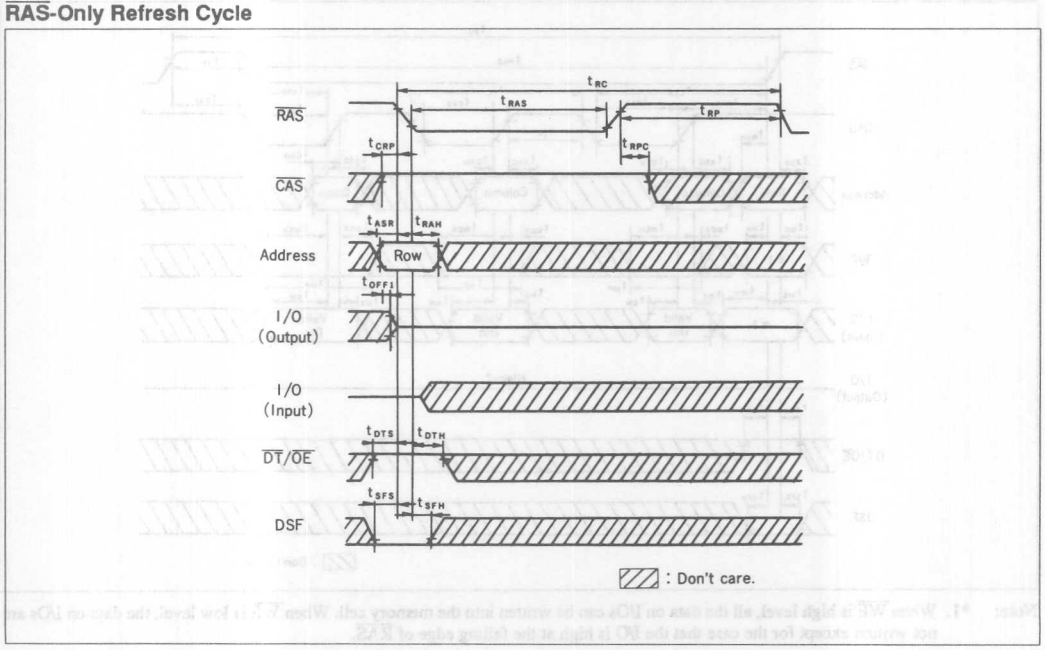
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

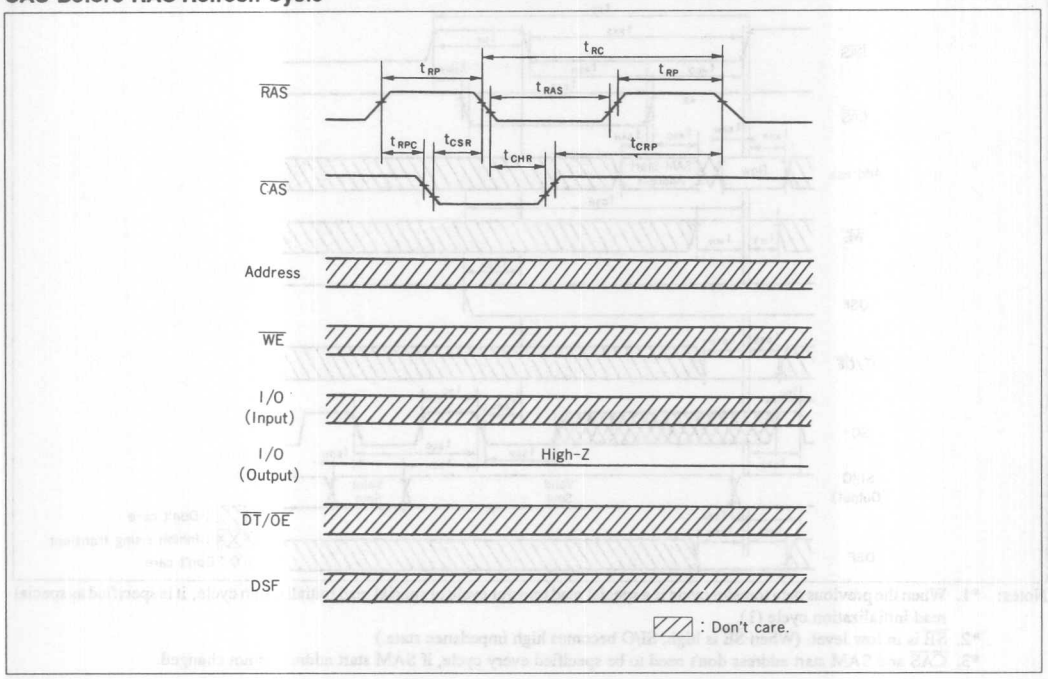


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

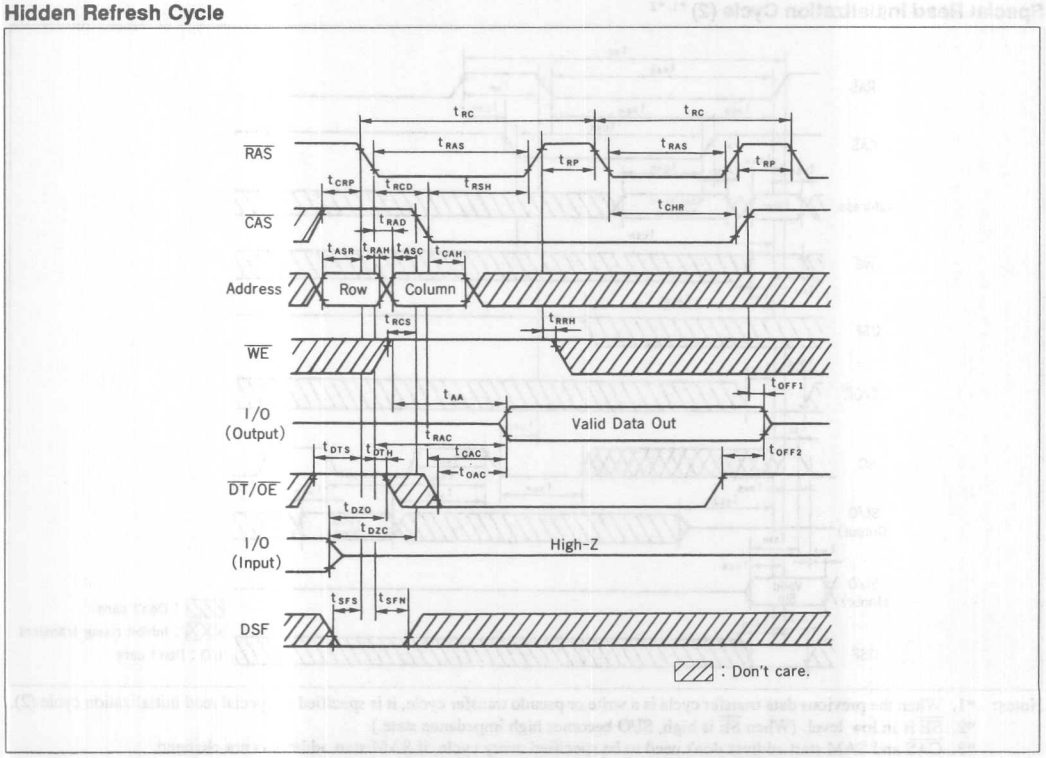
$\overline{RAS}$-Only Refresh Cycle



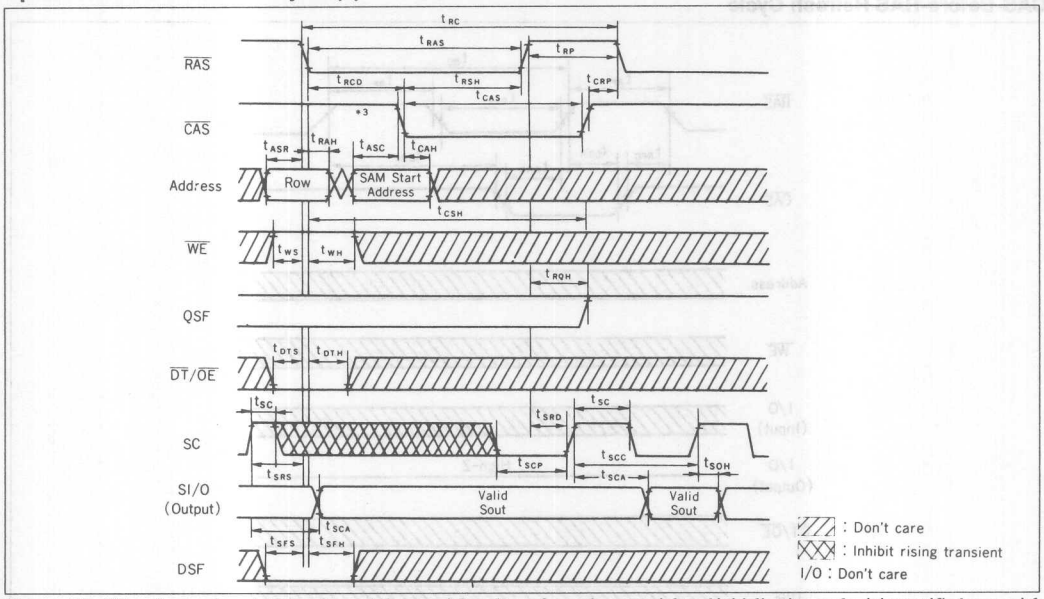
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle

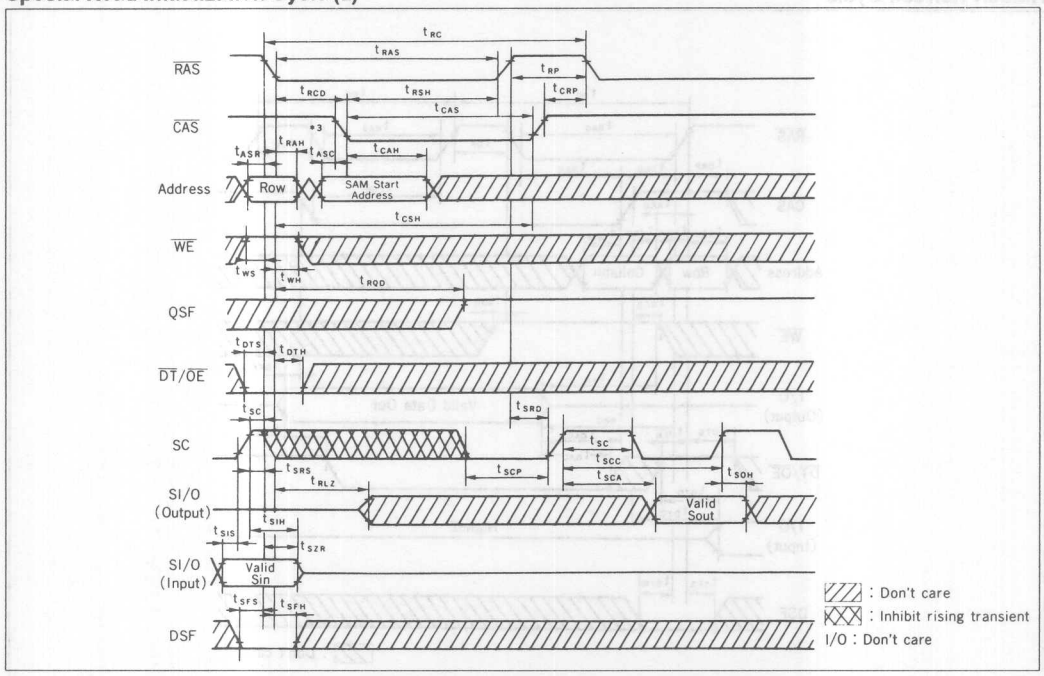


Special Read Initialization Cycle (1)*1, *2



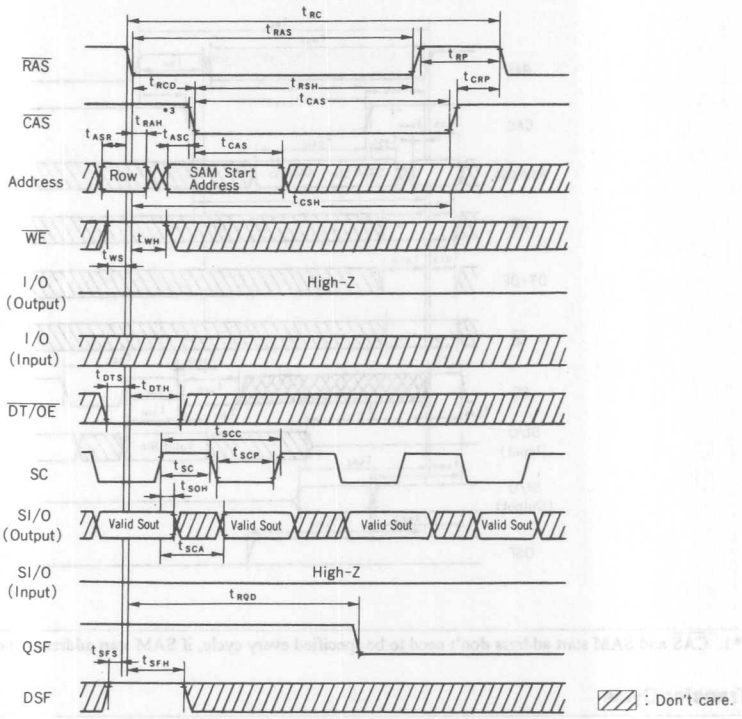
Notes: *1. When the previous data transfer cycle is a special read transfer cycle or special read initialization cycle, it is specified as special read initialization cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Special Read Initialization Cycle (2) *1, *2



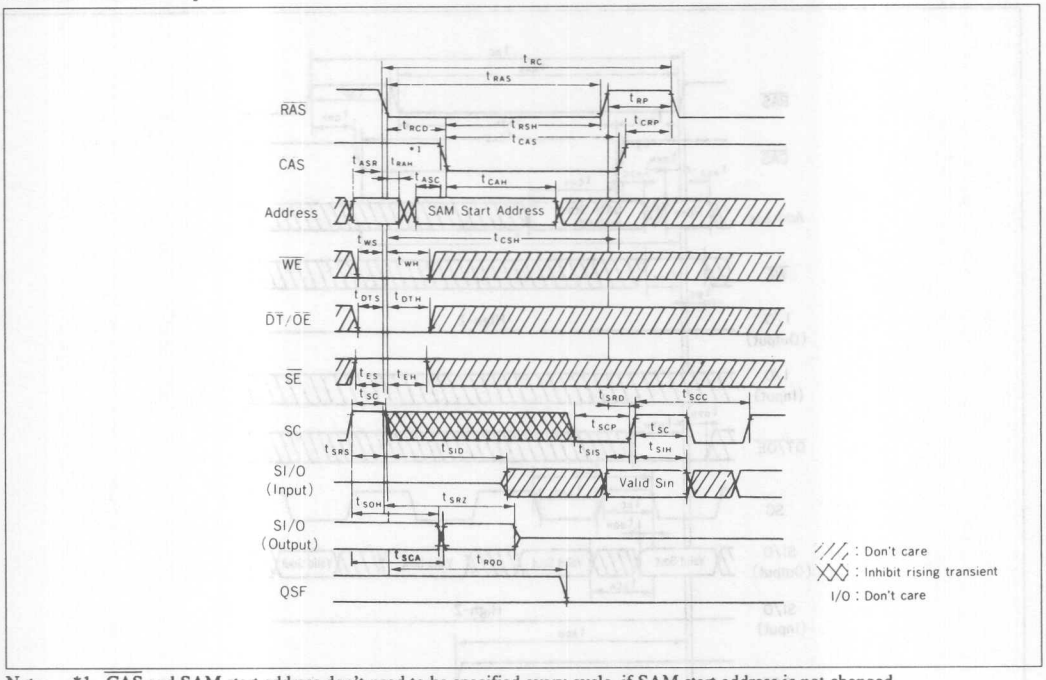
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is specified as special read initialization cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Special Read Transfer Cycle *1, *2



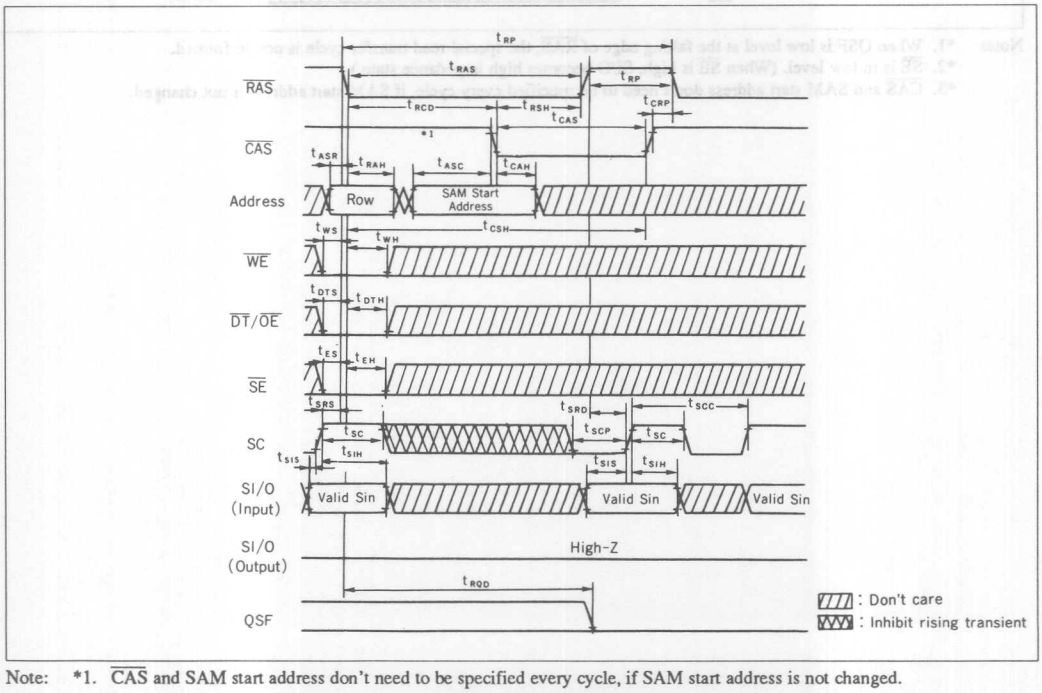
Notes: *1. When QSF is low level at the falling edge of $\overline{RAS}$, the special read transfer cycle is not performed.
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Pseudo Transfer Cycle



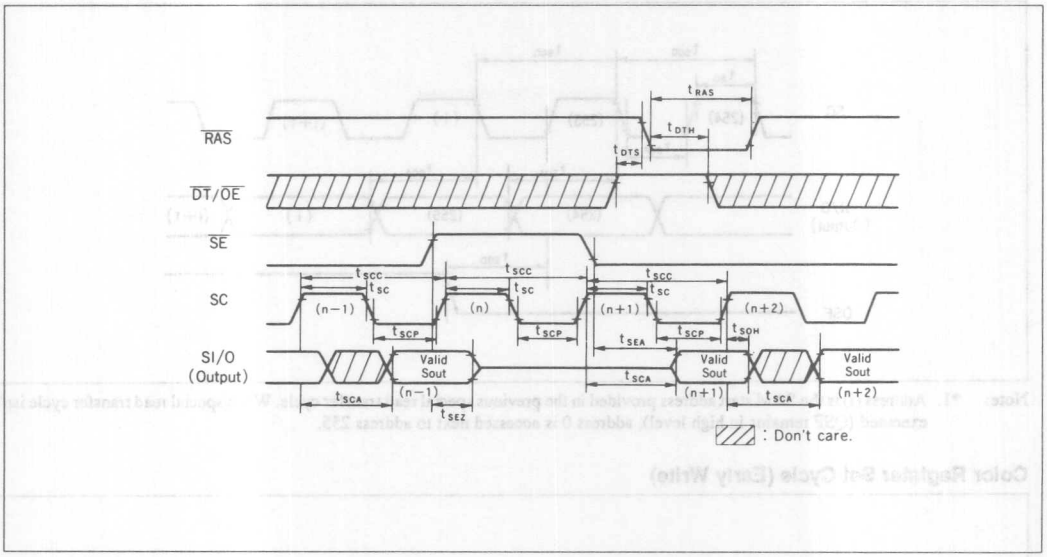
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Write Transfer Cycle

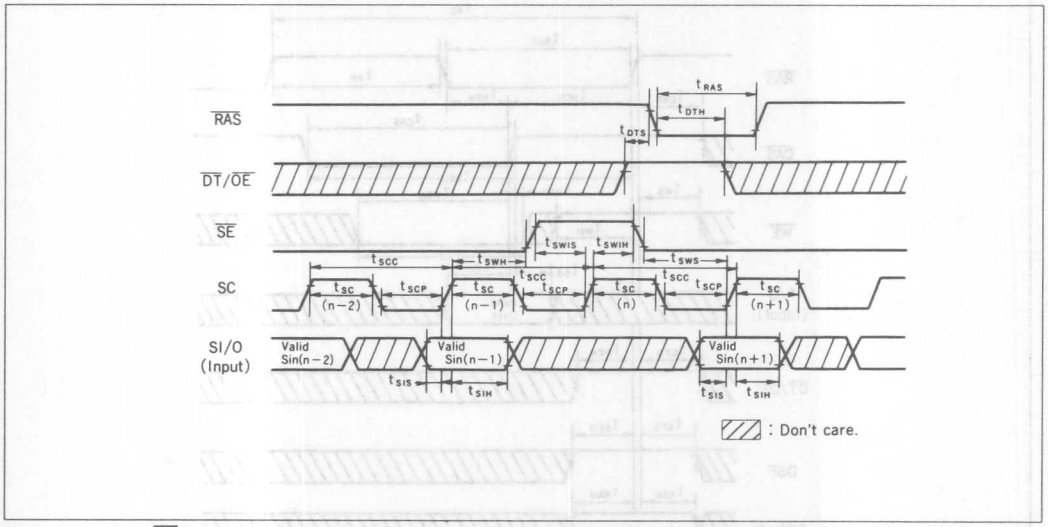


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Serial Read Cycle

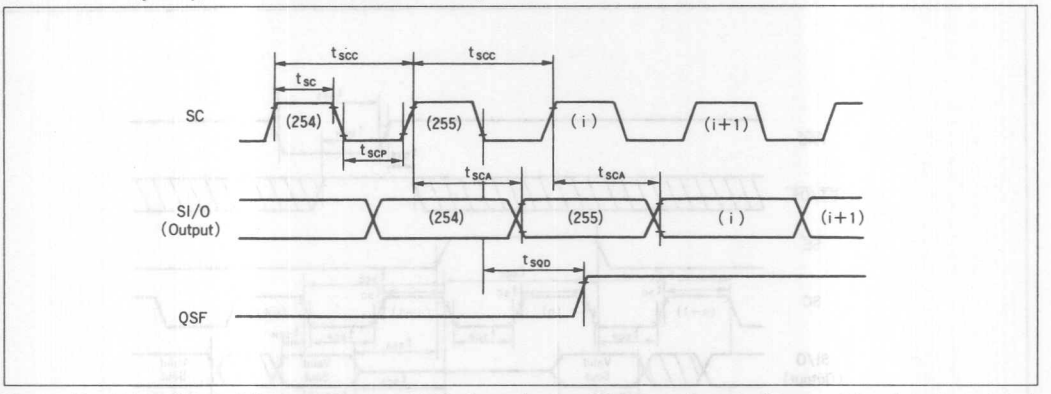


Serial Write Cycle *1,*2



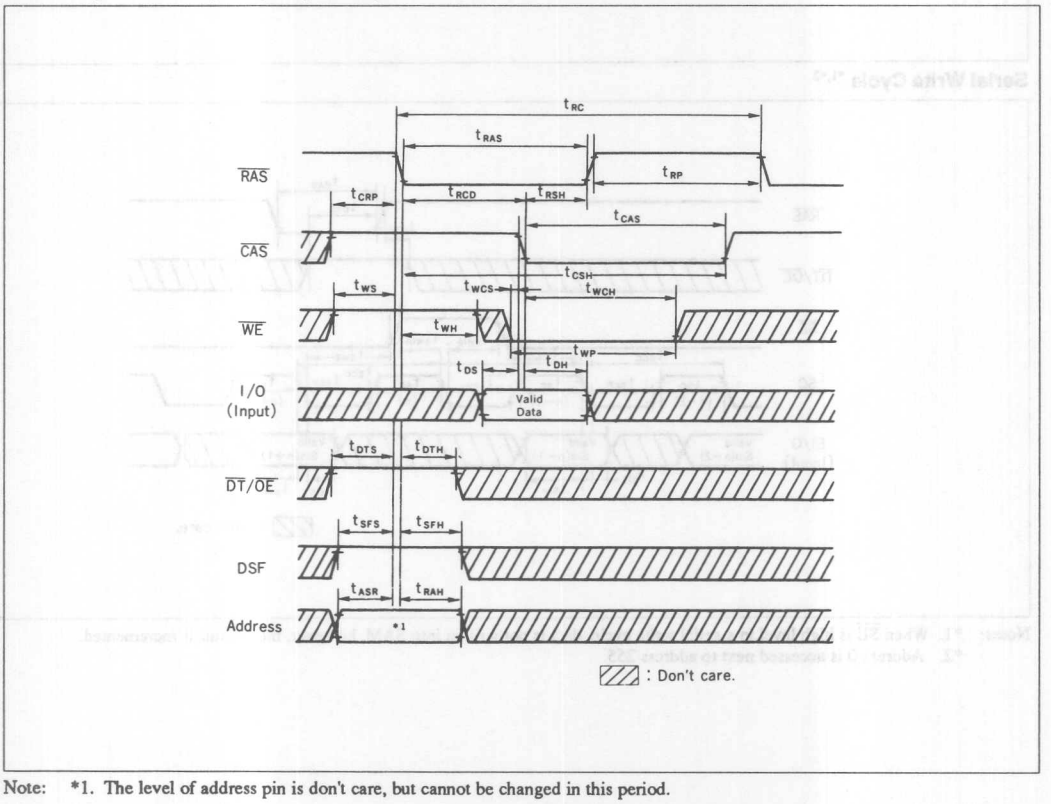
Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 255.

Serial Read Cycle (Around Address 255 in SAM)



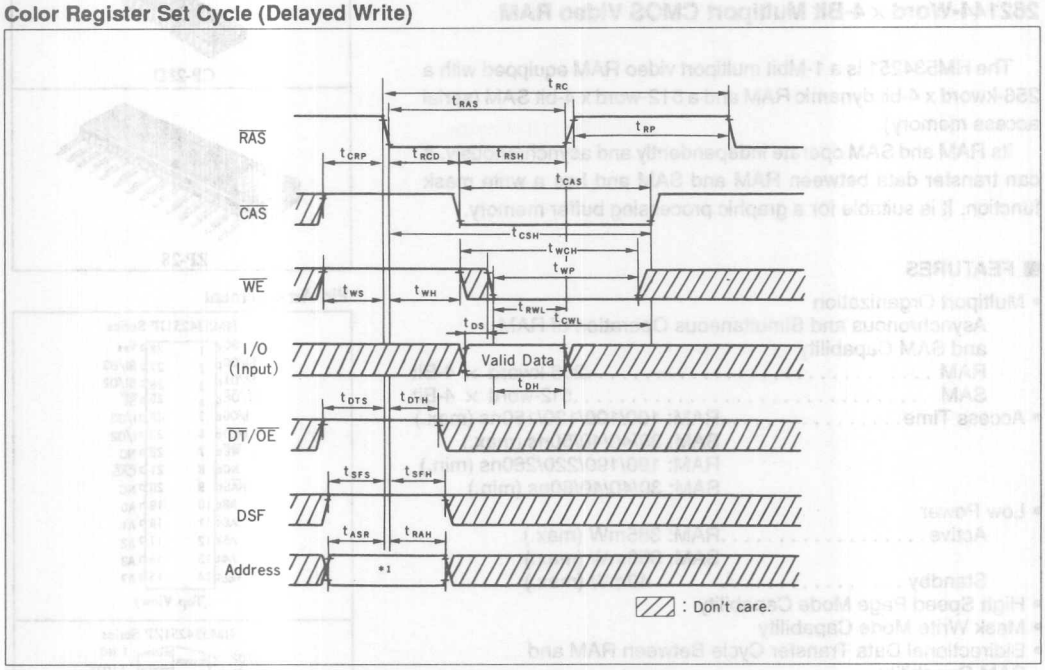
Note: *1. Address (i) is the SAM start address provided in the previous special read transfer cycle. When special read transfer cycle isn't executed (QSF remains in high level), address 0 is accessed next to address 255.

Color Register Set Cycle (Early Write)



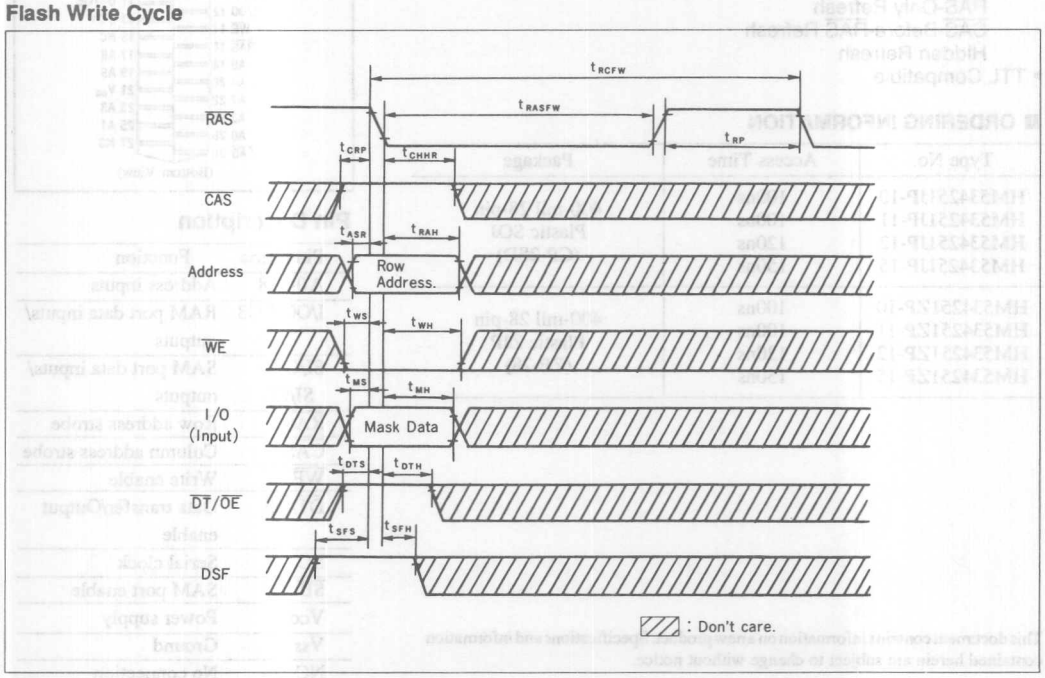
Note: *1. The level of address pin is don't care, but cannot be changed in this period.

Color Register Set Cycle (Delayed Write)



Note: *1. The level of address pin is don't care, but cannot be changed in this period.

Flash Write Cycle



HM534251 Series — Preliminary

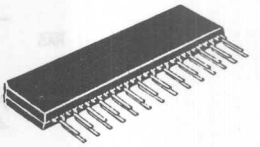
262144-Word × 4-Bit Multiport CMOS Video RAM

The HM534251 is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory.



CP-28D



ZP-28

■ FEATURES

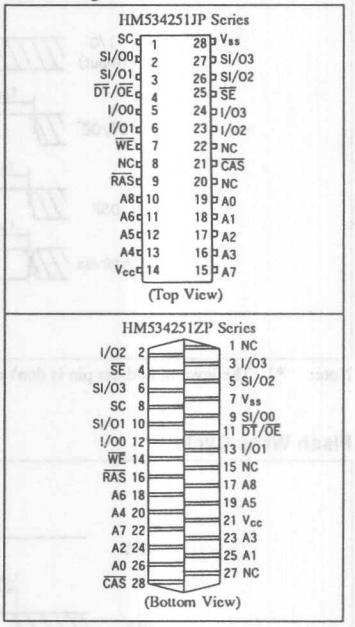
- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM . . . . . .256-kword × 4-Bit
  - SAM . . . . . .512-word × 4-Bit
- Access Time. . . . . .RAM: 100/100/120/150ns (max.)
  - SAM: 30/40/40/50ns (max.)
  - RAM: 190/190/220/260ns (min.)
  - SAM: 30/40/40/60ns (min.)
- Low Power
  - Active. . . . . .RAM: 385mW (max.)
  - SAM: 358mW (max.)
  - Standby . . . . . 40mW (max.)
- High Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle Between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8ms/512 Cycles)
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM534251JP-10	100ns	400-mil 28-pin Plastic SOJ (CP-28D)
HM534251JP-11	100ns	
HM534251JP-12	120ns	
HM534251JP-15	150ns	
HM534251ZP-10	100ns	400-mil 28-pin Plastic ZIP (ZP-28)
HM534251ZP-11	100ns	
HM534251ZP-12	120ns	
HM534251ZP-15	150ns	

This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

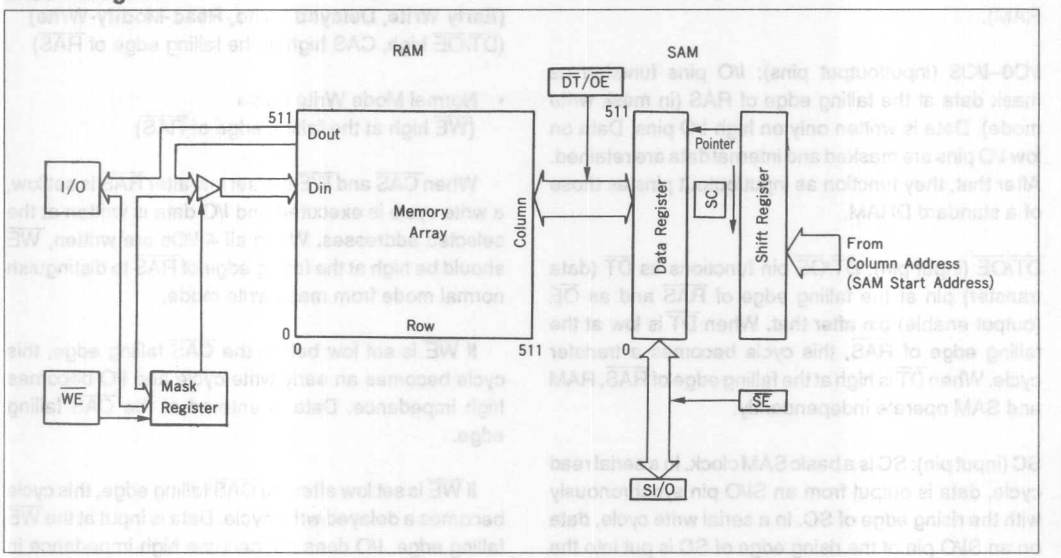
Pin Arrangement



Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O3	RAM port data inputs/outputs
SI/O0–SI/O3	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
Vcc	Power supply
Vss	Ground
NC	No connection

Block Diagram



Pin Function

RAS (input pin): RAS is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of RAS. The input level of those signals determine the operation cycle of the HM534251.

Table 1. Operation Cycles of the HM534251

Input level at the falling edge of RAS				Operation Cycle
CAS	DT/OE	WE	SE	
H	H	H	×	RAM read/write
H	H	L	×	Mask write
H	L	H	×	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	×	×	×	CBR refresh

Note: ×; Don't care.

CAS (input pin): Column address is put into chip at the falling edge of CAS. CAS controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of RAS. Column address is determined by A0–A8 level at the falling edge of CAS. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

WE (input pin): WE pin has two functions at the falling edge of RAS and after. When WE is low at the falling edge of RAS, the HM534251 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. (WE level at the falling edge of RAS is don't care in read cycle.) When WE is high at the falling edge of RAS, a normal write cycle is executed. After that, WE switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by WE level at the falling edge of RAS. When WE is low, data is transferred from SAM to RAM (data is written into RAM), and when WE is high, data

is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of RAS (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251

Operation of RAM Port

RAM Read Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle

(Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, CAS high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle
  ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time

(t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 µs).

Transfer Operation

The HM534251 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
- (a) Read transfer cycle: RAM → SAM
- (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
- Read transfer cycle: SI/O output
- Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by setting $\overline{DT/OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512x4 bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge, and t_{SDH}(min) between the first SAM access and $\overline{DT/OE}$ rising edge (see figure 1).

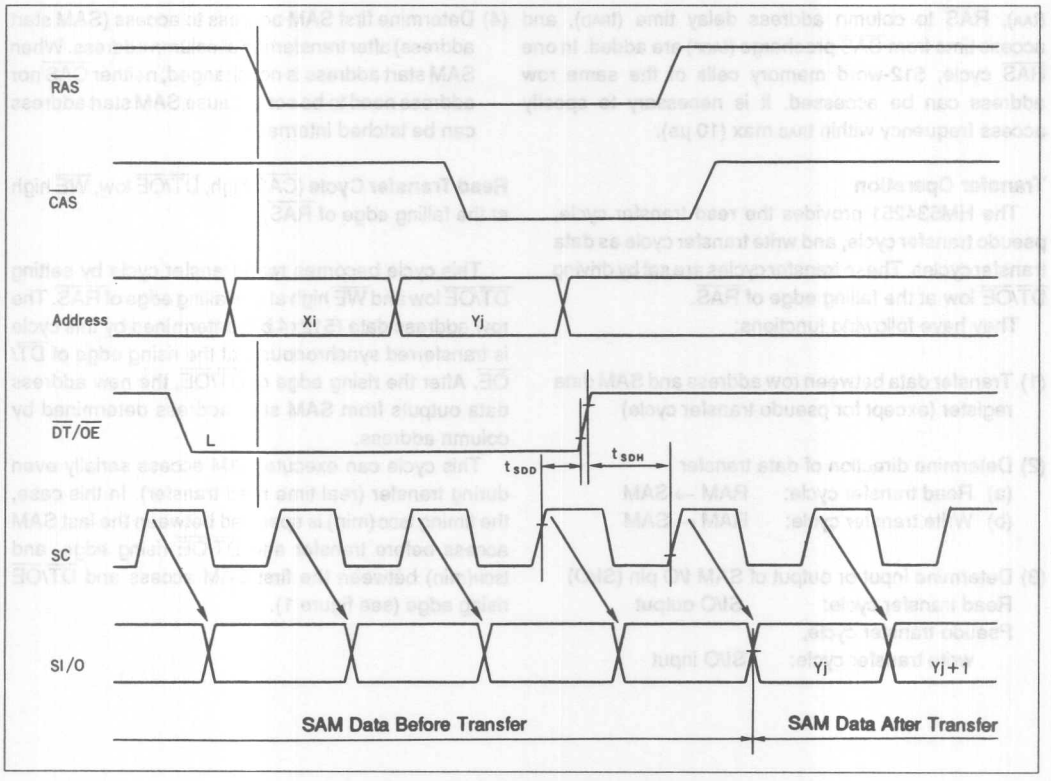


Figure 1. Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of RAS. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$-only refresh cycles because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	–1.0 to +7.0	V
Power supply voltage *1	V_{CC}	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: *1. Relative to Vss.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	–	6.5	V
Input low voltage *1	V_{IL}	–0.5*2	–	0.8	V

Notes: *1. All voltages referenced to Vss.
*2. –3.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	Test Conditions		HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		RAM Port	SAM Port	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	$\overline{SE}$ = V_{IH}, SC = V_{IL}	—	70	—	70	—	60	—	55	mA	1, 2
	I_{CC7}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	120	—	120	—	100	—	85	mA	
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC = V_{IL}	—	7	—	7	—	7	—	7	mA	1
	I_{CC8}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	65	—	55	—	55	—	40	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	$\overline{SE}$ = V_{IH}, SC = V_{IL}	—	70	—	70	—	60	—	55	mA	2
	I_{CC9}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	120	—	120	—	100	—	85	mA	
Page Mode Current	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min.	$\overline{SE}$ = V_{IH}, SC = V_{IL}	—	80	—	80	—	70	—	60	mA	1, 3
	I_{CC10}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	130	—	130	—	110	—	90	mA	
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC5}	$\overline{RAS}$ Cycling t_{RC} = Min.	$\overline{SE}$ = V_{IH}, SC = V_{IL}	—	60	—	60	—	50	—	40	mA	
	I_{CC11}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	110	—	110	—	90	—	70	mA	
Data Transfer Current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	$\overline{SE}$ = V_{IH}, SC = V_{IL}	—	95	—	95	—	90	—	85	mA	2
	I_{CC12}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	135	—	135	—	125	—	115	mA	
Input Leakage Current	I_{LI}			-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}			-10	10	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4	—	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA		—	0.4	—	0.4	—	0.4	—	0.4	V	

NOTES: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.

2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

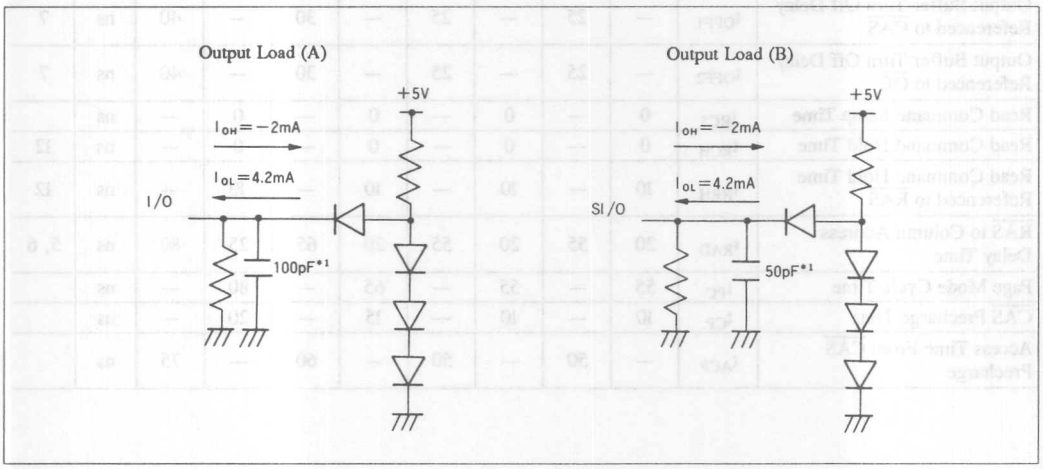
Capacitance (T_a = 25°C, V_{CC} = 5 V, f = 1MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *11

Test Conditions

Input rise and fall time:	5 ns
Output load:	See figures
Input timing reference levels:	0.8 V, 2.4 V
Output timing reference levels:	0.4 V, 2.4 V



Note: *1. Including scope & jig.

• Common Parameter

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-In to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-In to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

• Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn Off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn Off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	

• Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-In Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	

• Read-Modify-Write Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Modify Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-In Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time From $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-Off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-In Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

• Refresh Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

• Transfer Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
DT Hold Time From $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
DT Hold Time From $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to DT Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to DT Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
DT to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
DT Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
DT Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-Off Delay From $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time From SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Serial Data Out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-In Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-In Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

• Serial Read Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time From SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Access Time From $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-Out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-Off Delay From $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

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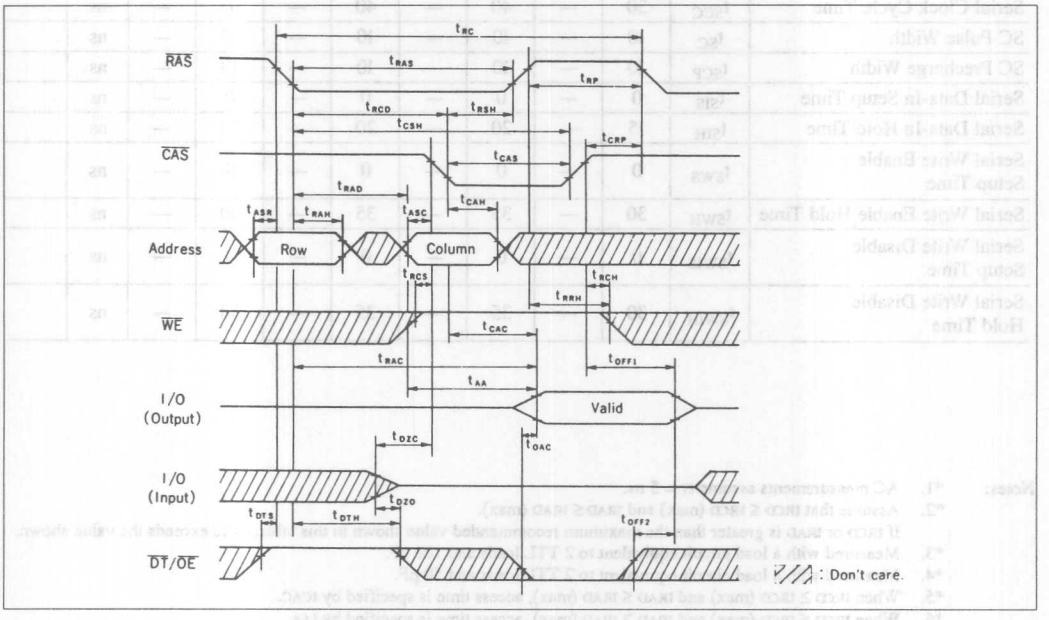
• Serial Write Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-In Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-In Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

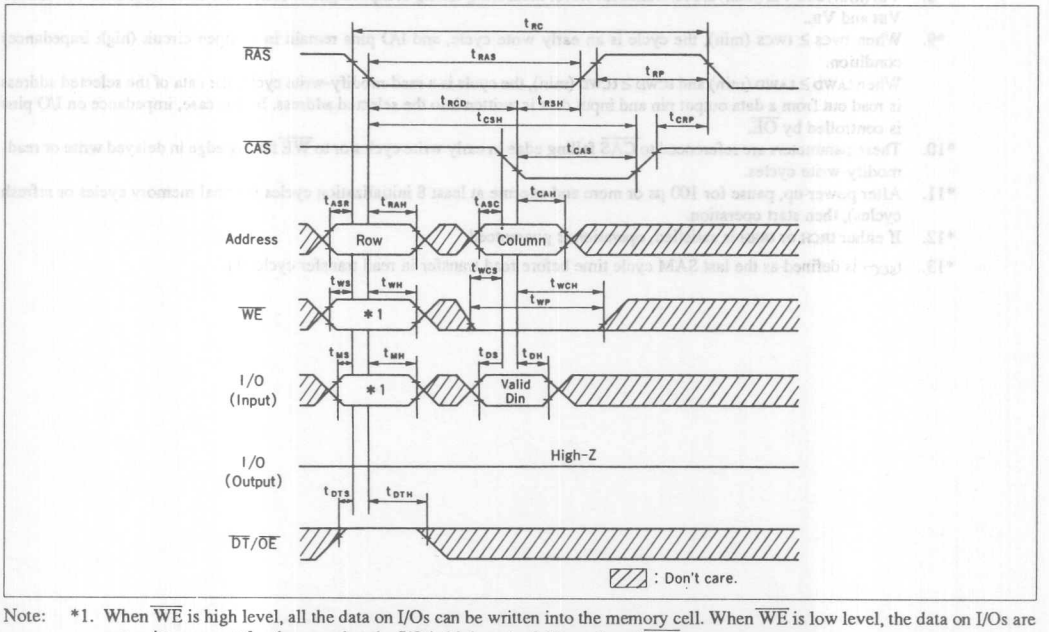
Notes:
*1. AC measurements assume t_T = 5 ns.
*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
*6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200 mV, V_{OL} + 200 mV).
*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
*11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
*13. t_{SCC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).

Timing Waveforms

Read Cycle



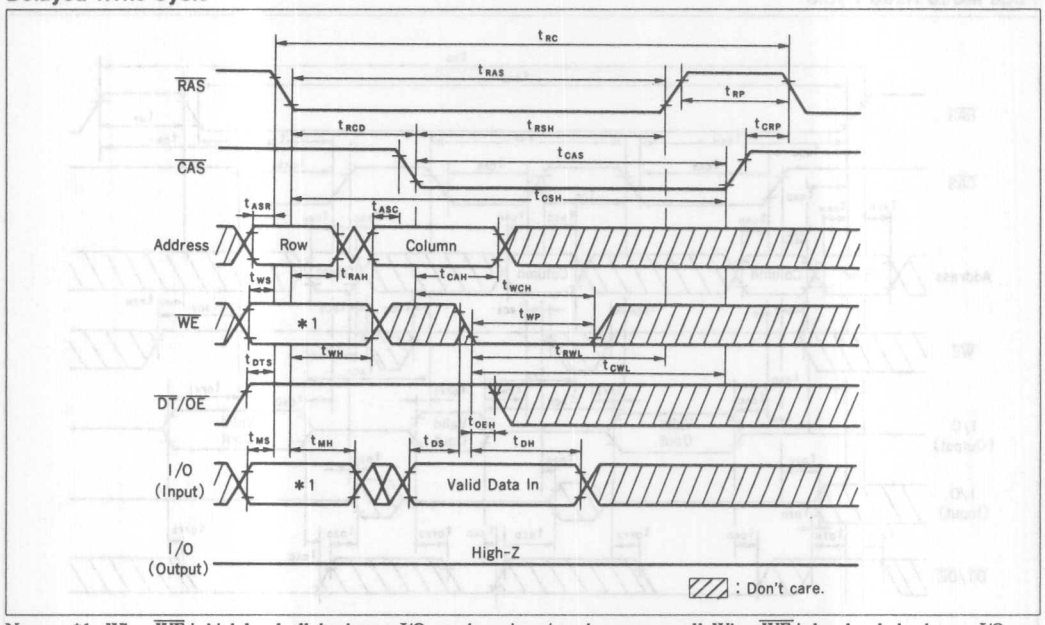
Early Write Cycle



Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

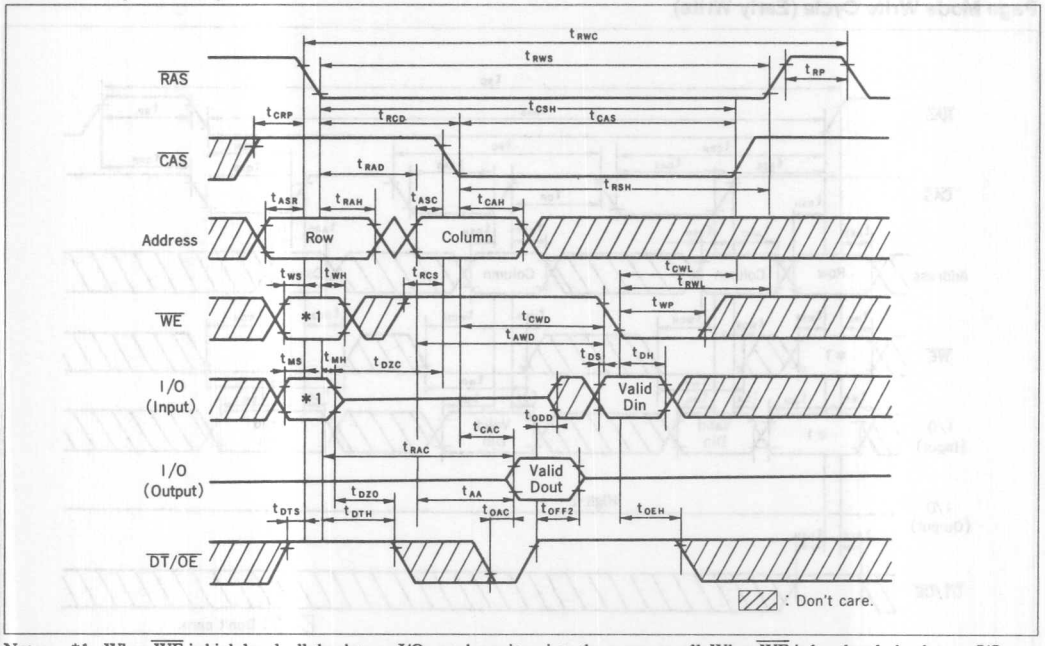
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Delayed Write Cycle



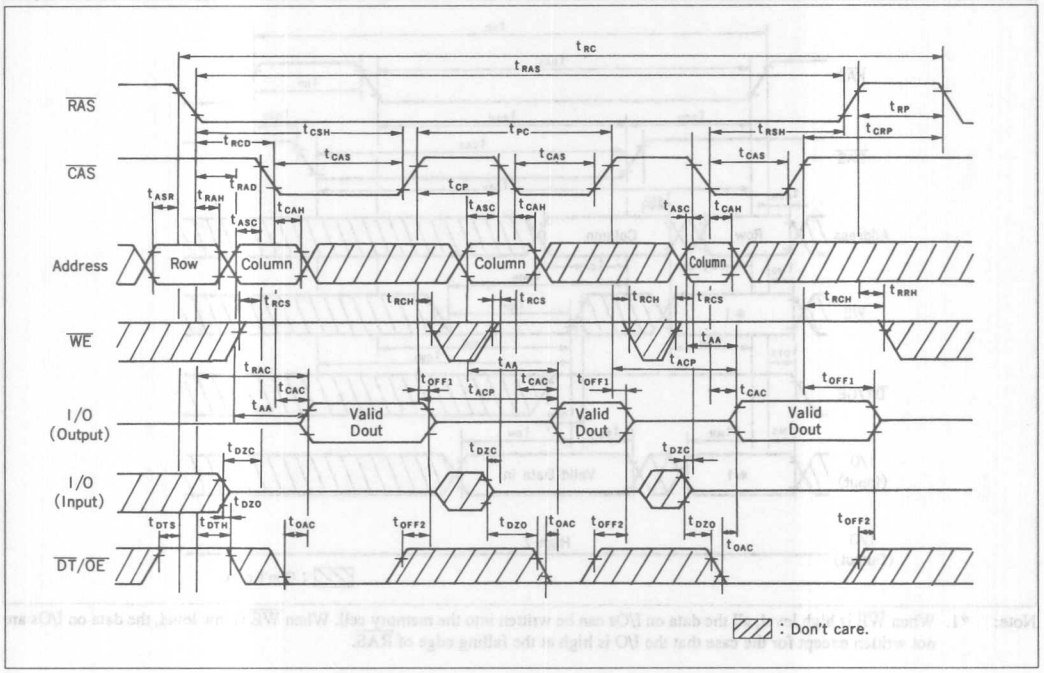
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

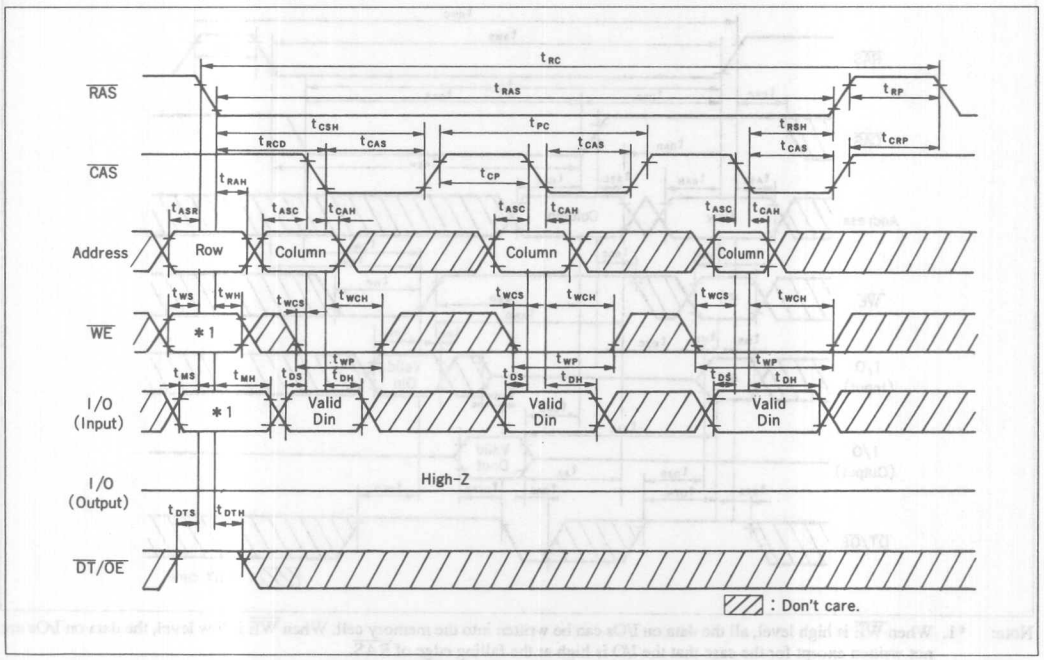


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle



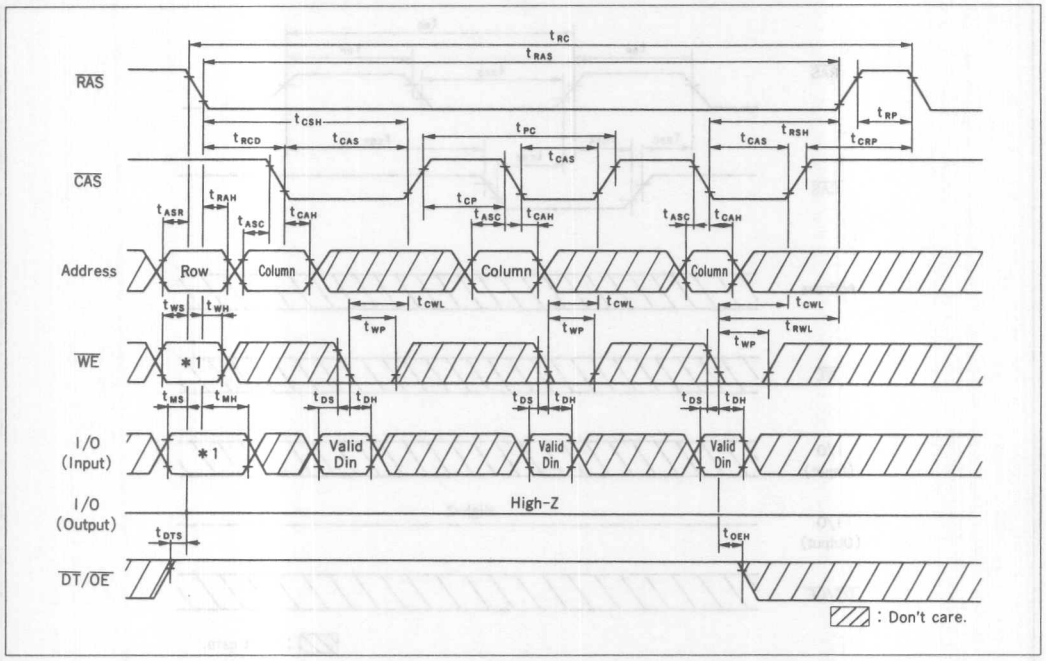
Page Mode Write Cycle (Early Write)



Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

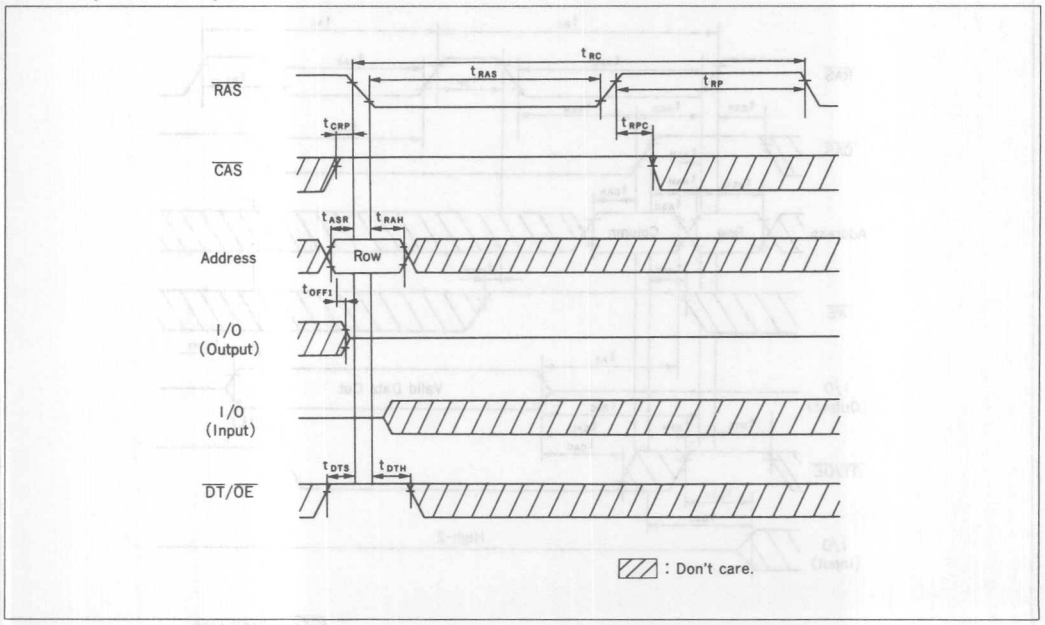
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Page Mode Write Cycle (Delayed Write)

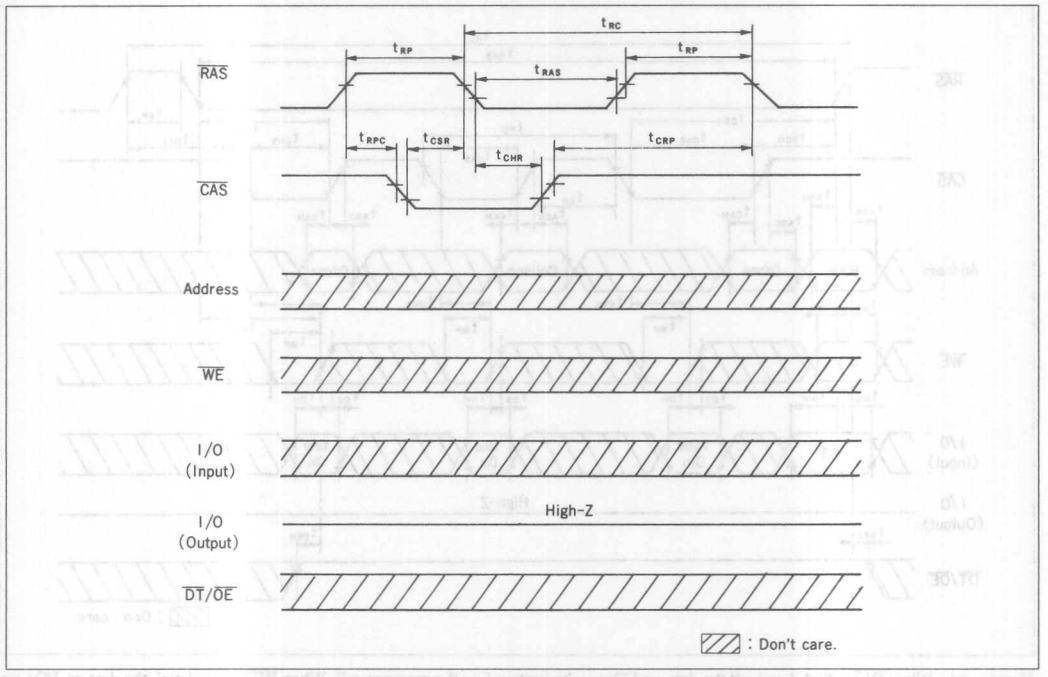


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

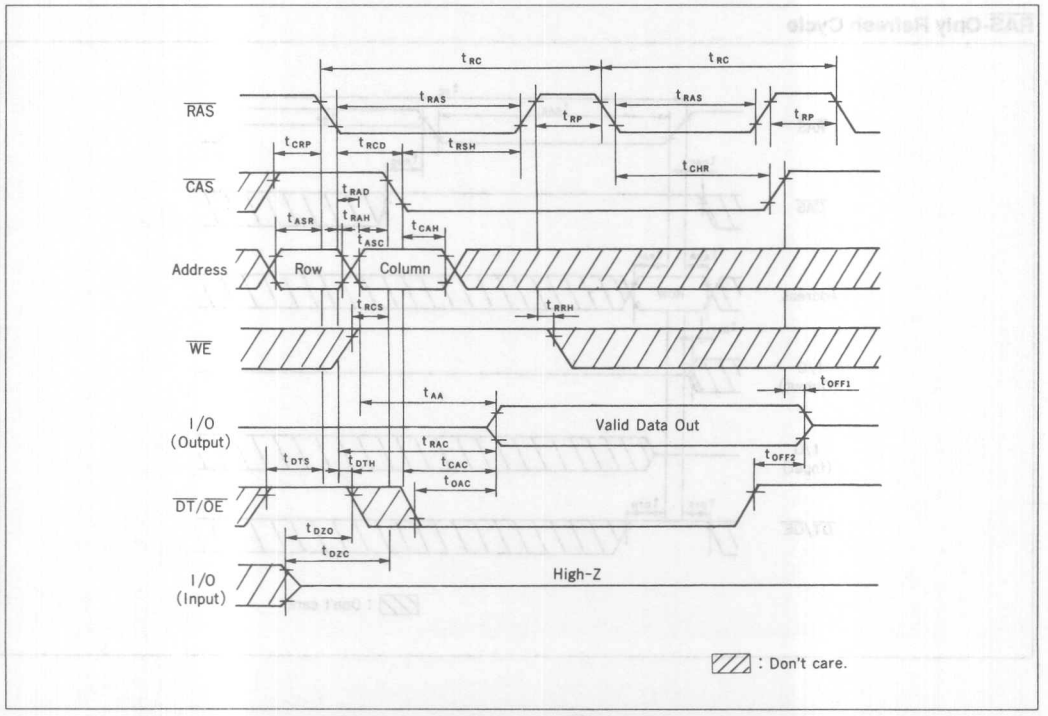
$\overline{RAS}$-Only Refresh Cycle



CAS-Before-RAS Refresh Cycle

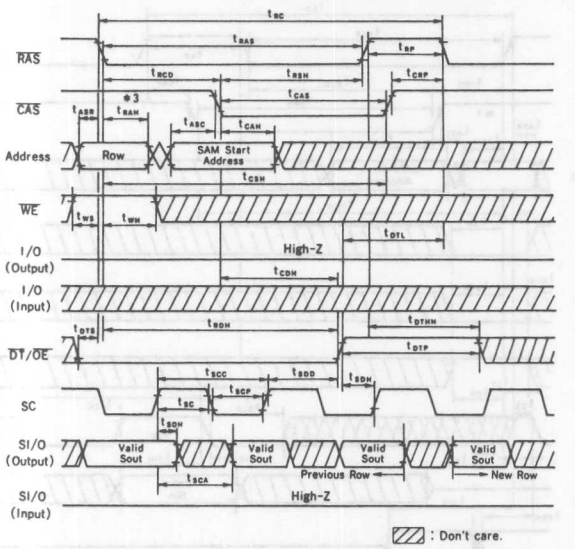


Hidden Refresh Cycle



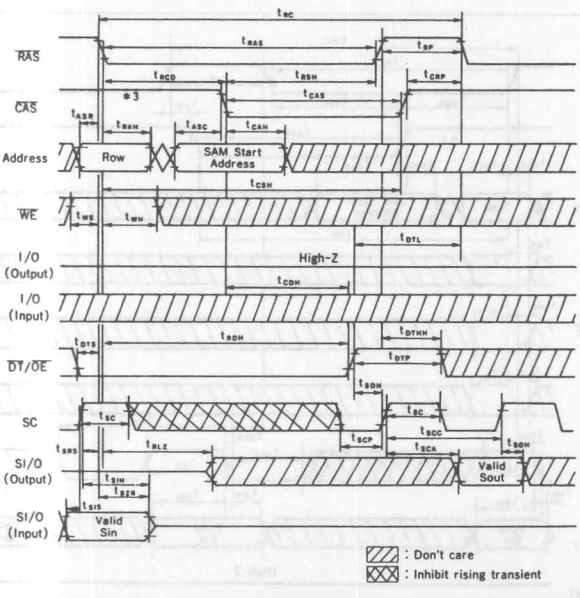
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Read Transfer Cycle (1)*1,*2



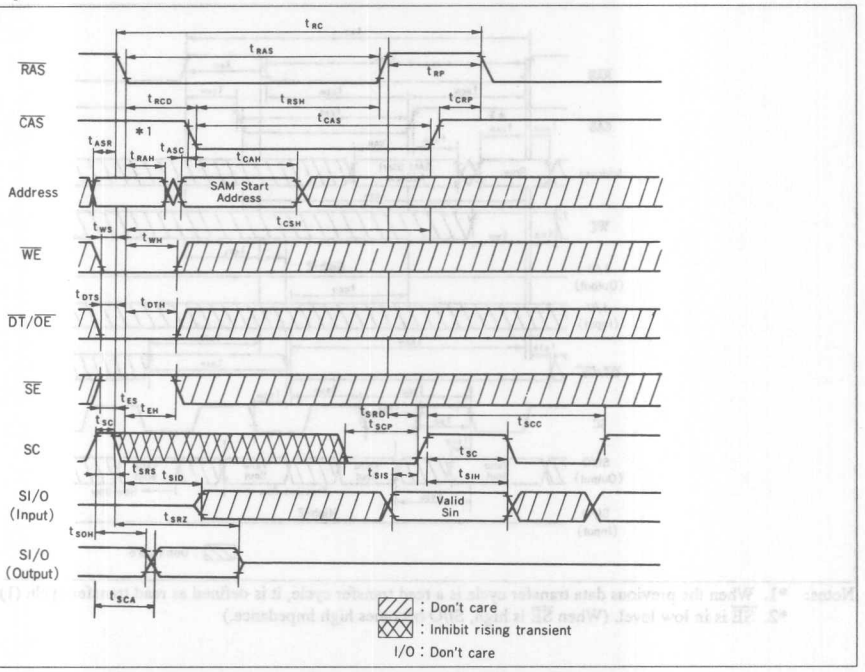
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

Read Transfer Cycle (2)*1,*2



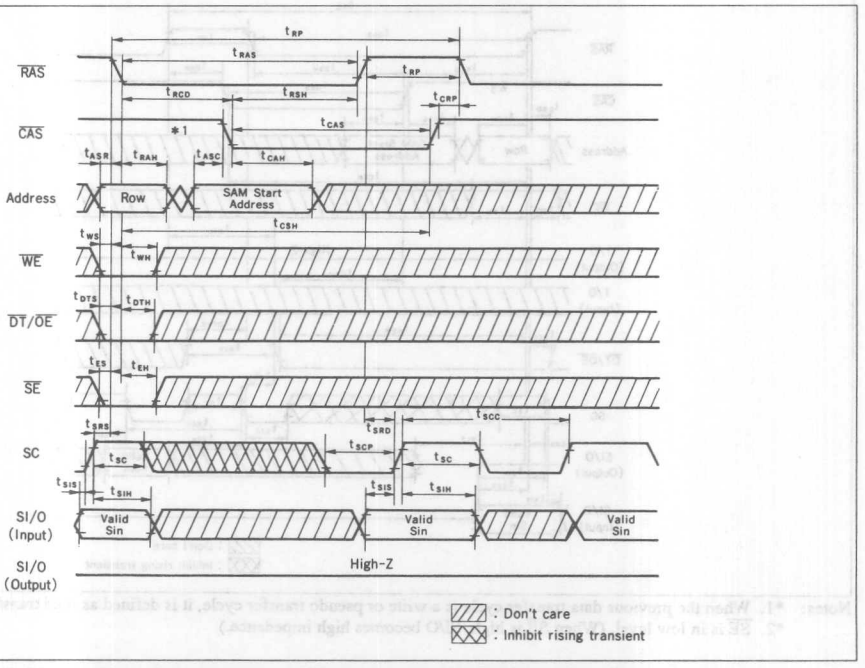
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

Pseudo Transfer Cycle



Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

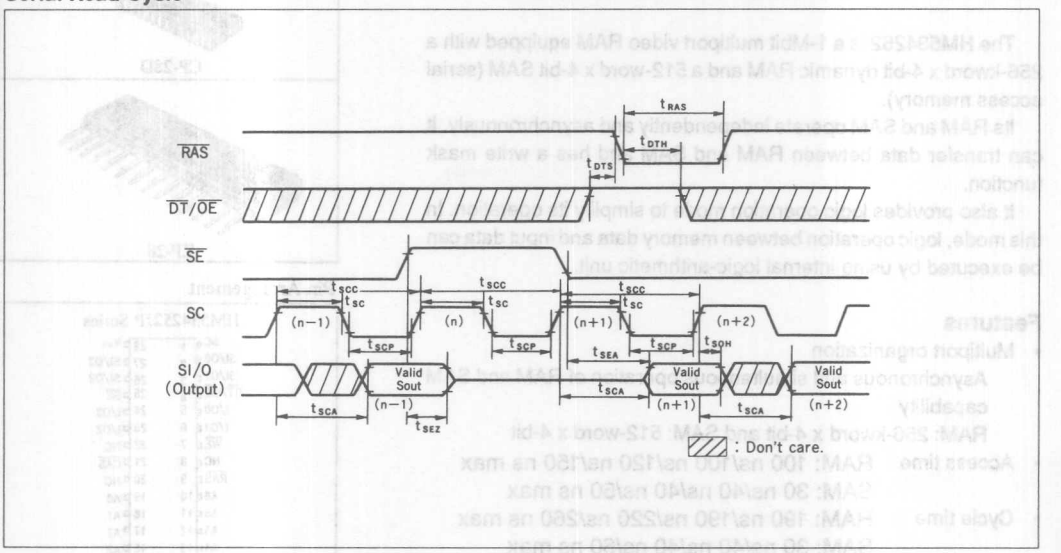
Write Transfer Cycle



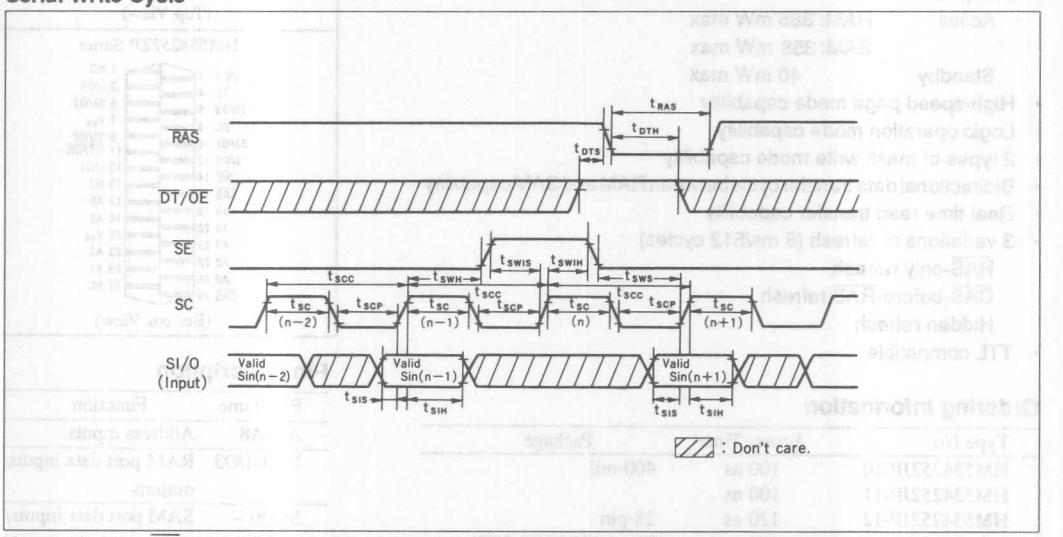
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

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Serial Read Cycle



Serial Write Cycle



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

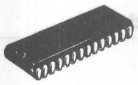
HM534252 Series — Preliminary

262144-Word × 4-Bit Multiport CMOS Video RAM

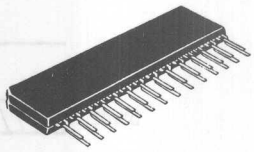
The HM534252 is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function.

It also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.



CP-28D



ZP-28

Features

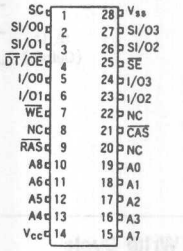
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 256-kword x 4-bit and SAM: 512-word x 4-bit
- Access time RAM: 100 ns/100 ns/120 ns/150 ns max
  SAM: 30 ns/40 ns/40 ns/50 ns max
- Cycle time RAM: 190 ns/190 ns/220 ns/260 ns max
  SAM: 30 ns/40 ns/40 ns/60 ns max
- Low power
  - Active RAM: 385 mW max
    SAM: 358 mW max
  - Standby 40 mW max
- High-speed page mode capability
- Logic operation mode capability
- 2 types of mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM534252JP-10	100 ns	400-mil
HM534252JP-11	100 ns	
HM534252JP-12	120 ns	28-pin
HM534252JP-15	150 ns	Plastic SOJ (CP-28D)
HM534252ZP-10	100 ns	400-mil
HM534252ZP-11	100 ns	
HM534252ZP-12	120 ns	28-pin
HM534252ZP-15	150 ns	Plastic ZIP (ZP-28)

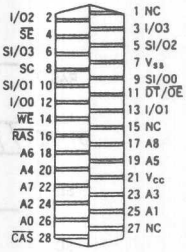
Pin Arrangement

HM534252JP Series



(Top View)

HM534252ZP Series



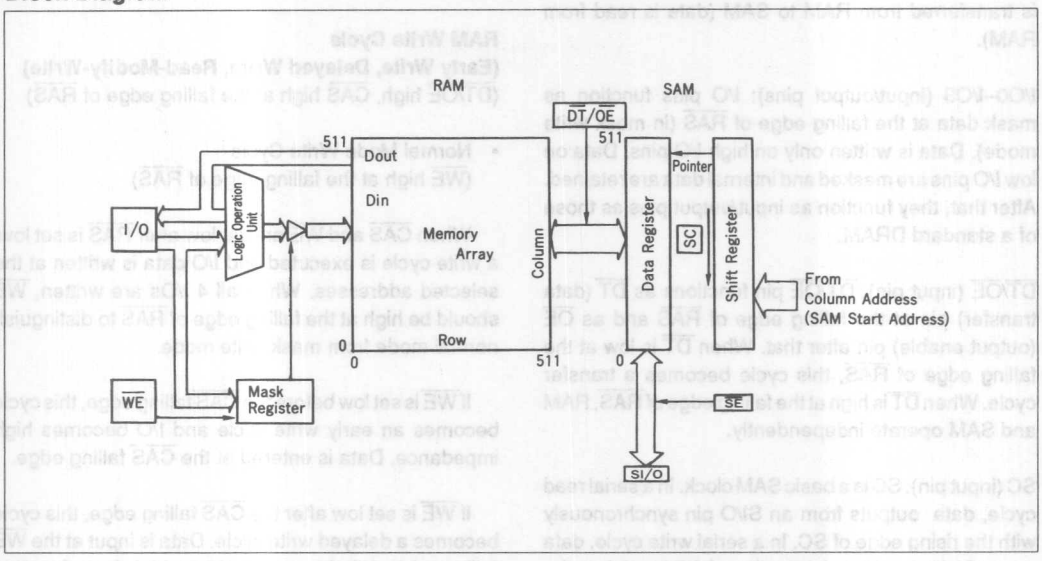
(Bottom View)

Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O3	RAM port data inputs/ outputs
SI/O0 – SI/O3	SAM port data inputs/ outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
Vcc	Power supply
Vss	Ground
NC	No connection

This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Block Diagram



Pin Function

RAS (input pin): RAS is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of RAS. The input level of those signals determine the operation cycle of the HM534252.

Table 1. Operation Cycles of the HM534252

Input level at the falling edge of RAS				Operation Cycle
CAS	DT/OE	WE	SE	
H	H	H	×	RAM read/write
H	H	L	×	Mask write
H	L	H	×	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	×	H	×	CBR refresh
L	×	L	×	Logic operation set/reset

Note: ×; Don't care.

CAS (input pin): Column address is put into chip at the falling edge of CAS. CAS controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of RAS. Column address is determined by A0–A8 level at the falling edge of CAS. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

WE (input pin): WE pin has two functions at the falling edge of RAS and after. When WE is low at the falling edge of RAS, the HM534252 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. (WE level at the falling edge of RAS is don't care in read cycle.) When WE is high at the falling edge of RAS, a normal write cycle is executed. After that, WE switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by WE level at the falling edge of RAS. When WE is low, data is transferred from SAM to RAM

(data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534252

Operation of RAM Port

RAM Read Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of RAS, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle
(Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle
  ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore address access time (t_{AA}), $\overline{RAS}$

to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 µs).

Transfer Operation

The HM534252 provides the transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
   (a) Read transfer cycle: RAM → SAM
   (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
   Read transfer cycle: SI/O output
   Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither CAS nor address need to be set because SAM start address can be latched internally.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, WE high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT/OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512x4 bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can access SAM serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge, and t_{SDH}(min) between the first SAM access and $\overline{DT/OE}$ rising edge (see figure 1).

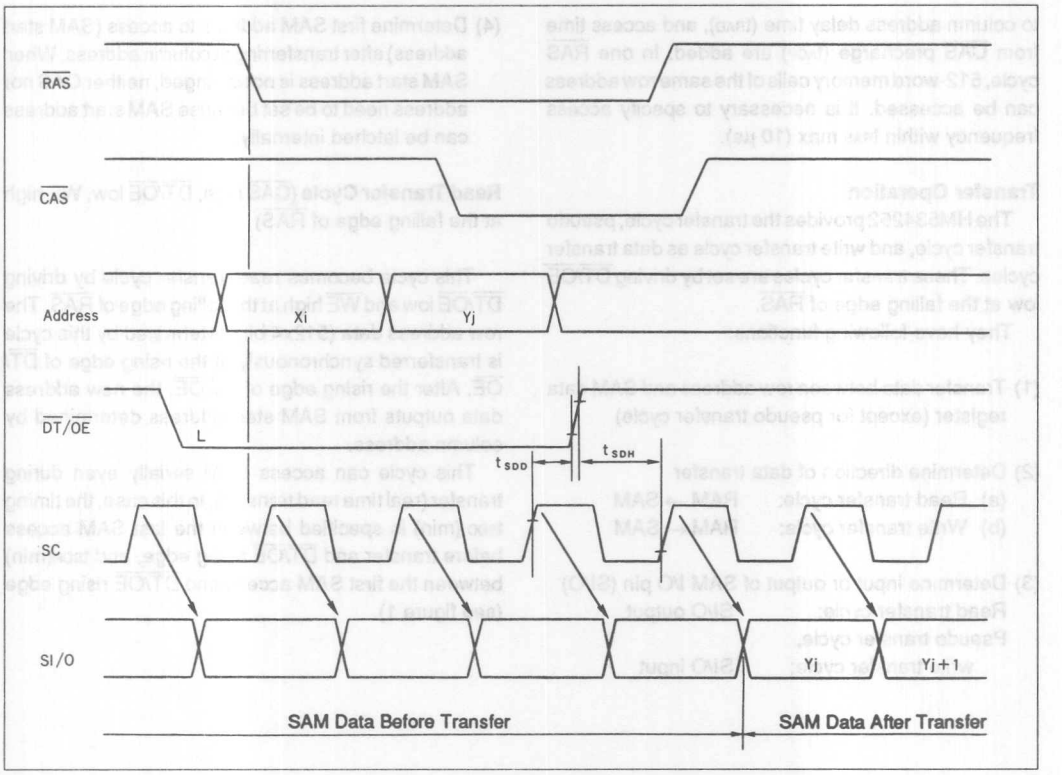


Figure 1. Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$-only refresh cycles because $\overline{CAS}$ circuits don't operate. To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating RAS when DT/OE and CAS keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode

The HM534252 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0-A3 levels at the falling edge of $\overline{RAS}$. (A4–A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0,1,0,1) resets the logic operation mode. When write cycle is performed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2)Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

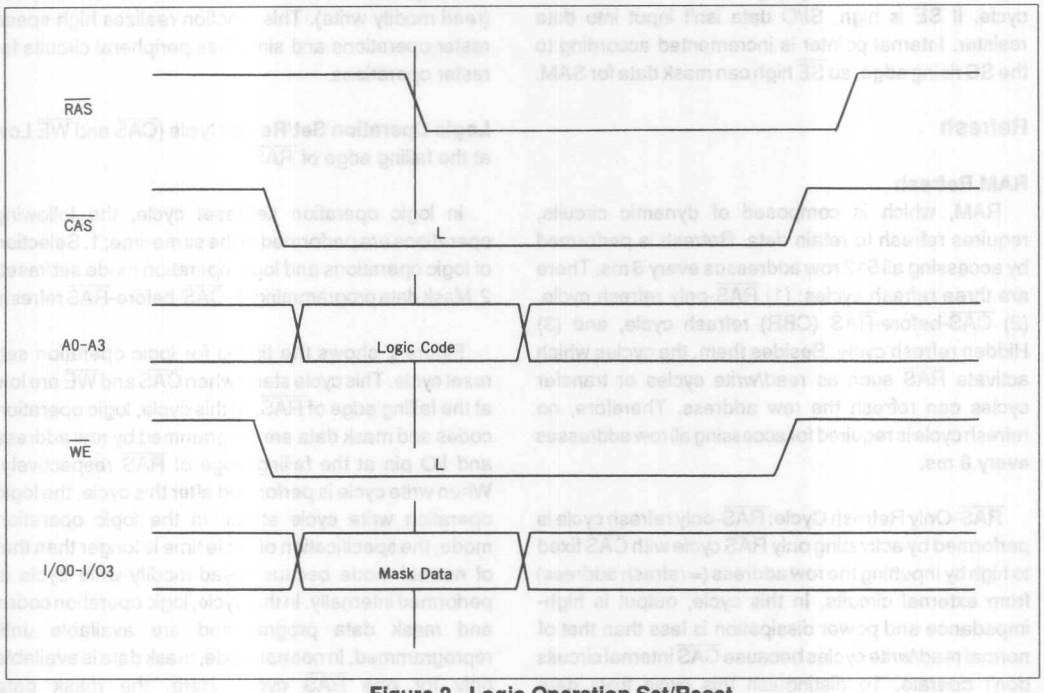


Figure 2. Logic Operation Set/Reset

Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A3	A2	A1	A0			
0	0	0	0	Zero	0	
0	0	0	1	AND1	$Di \cdot Mi$	
0	0	1	0	AND2	$\overline{Di} \cdot Mi$	Logic operation mode set
0	0	1	1	—	Mi	
0	1	0	0	AND3	$Di \cdot \overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$	
0	1	1	1	OR1	$Di + Mi$	
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$	
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	Logic operation mode set
1	0	1	1	OR2	$\overline{Di} + Mi$	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	$Di + \overline{Mi}$	
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$	
1	1	1	1	One	1	

Notes: Di; External data-in
Mi; The data of the memory cell

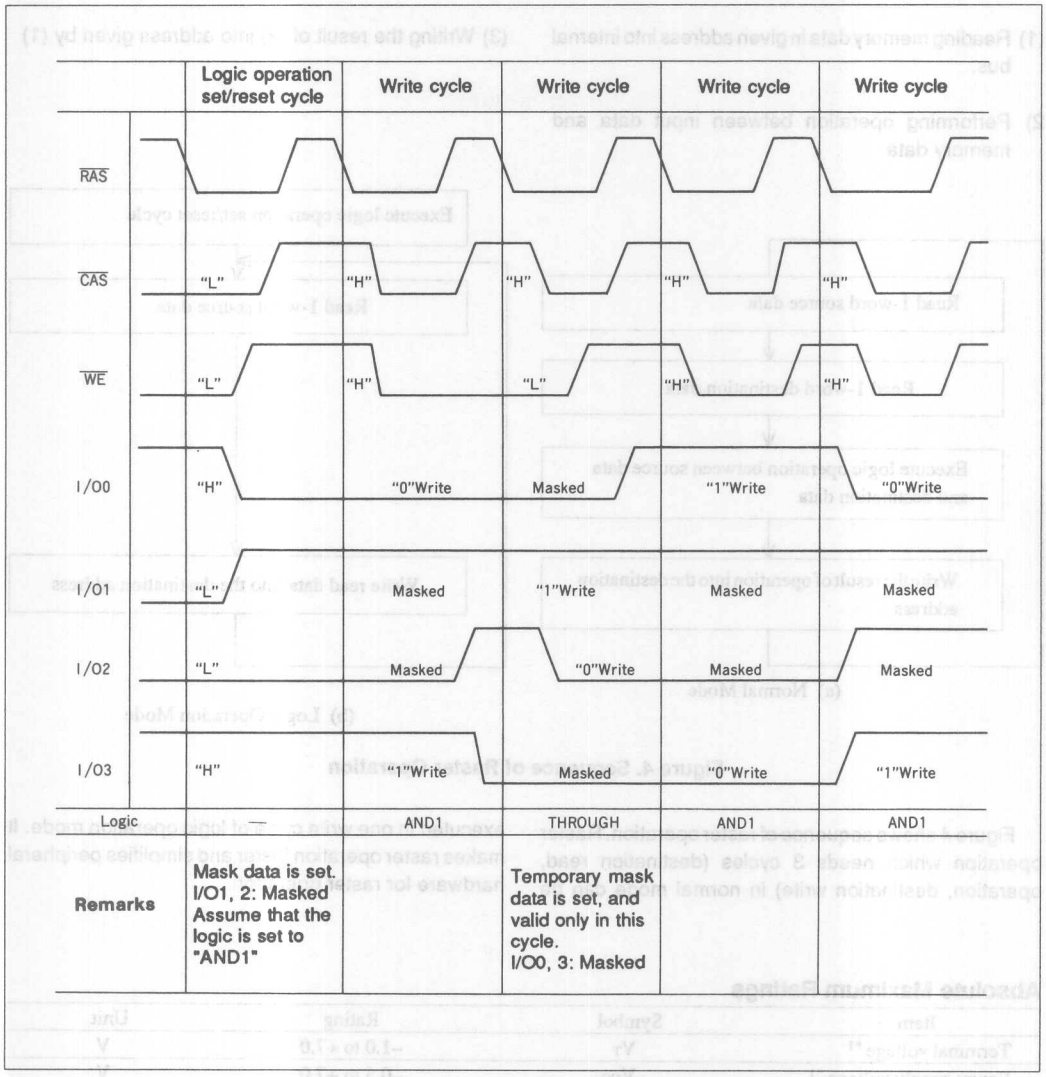


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is devided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

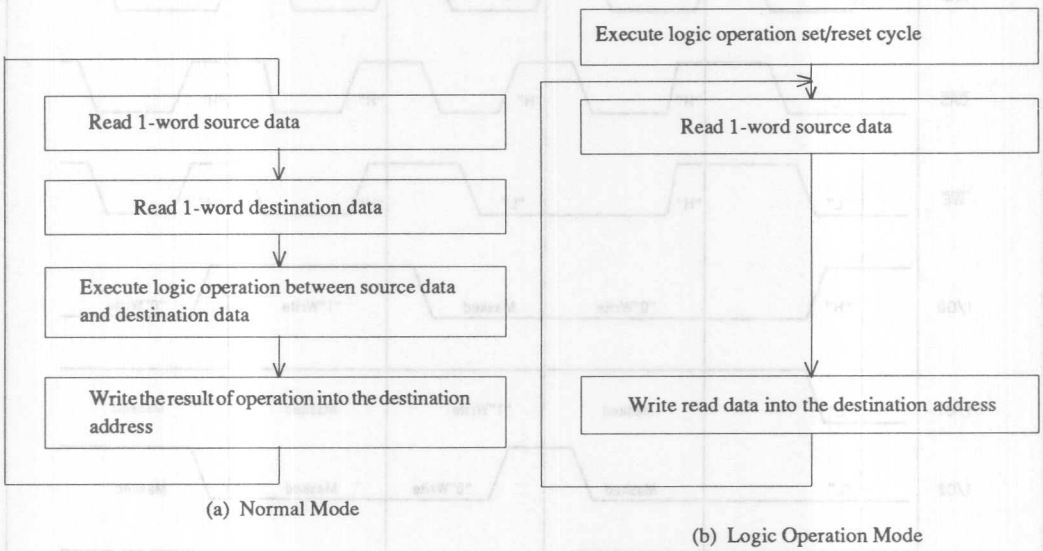
Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed Internally.

(1) Reading memory data in given address into internal bus.

2) Performing operation between input data and memory data

(3) Writing the result of (2) into address given by (1)



(a) Normal Mode

(b) Logic Operation Mode

Figure 4. Sequence of Raster Operation

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	–1.0 to +7.0	V
Power supply voltage *1	V_{CC}	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: *1. Relative to Vss.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	—	6.5	V
Input low voltage *1	V_{IL}	–0.5*2	—	0.8	V

Notes: *1. All voltages referenced to Vss.
*2. –3.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	Test Conditions		HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		RAM Port	SAM Port	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	SC = V_{IL}, $\overline{SE}$ = V_{IH}	—	70	—	70	—	60	—	55	mA	1, 2
	I_{CC7}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	120	—	120	—	100	—	85	mA	
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	—	7	—	7	—	7	—	7	mA	1
	I_{CC8}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	65	—	55	—	55	—	40	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	SC = V_{IL}, $\overline{SE}$ = V_{IH}	—	70	—	70	—	60	—	55	mA	2
	I_{CC9}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	120	—	120	—	100	—	85	mA	
Page Mode Current	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min.	SC = V_{IL}, $\overline{SE}$ = V_{IH}	—	80	—	80	—	70	—	60	mA	1, 3
	I_{CC10}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	130	—	130	—	110	—	90	mA	
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC5}	$\overline{RAS}$ Cycling t_{RC} = Min.	SC = V_{IL}, $\overline{SE}$ = V_{IH}	—	60	—	60	—	50	—	40	mA	
	I_{CC11}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	110	—	110	—	90	—	70	mA	
Data Transfer Current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	SC = V_{IL}, $\overline{SE}$ = V_{IH}	—	95	—	95	—	90	—	85	mA	2
	I_{CC12}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	135	—	135	—	125	—	115	mA	
Input Leakage Current	I_{LI}			-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}			-10	10	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4	—	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA		—	0.4	—	0.4	—	0.4	—	0.4	V	

NOTES: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

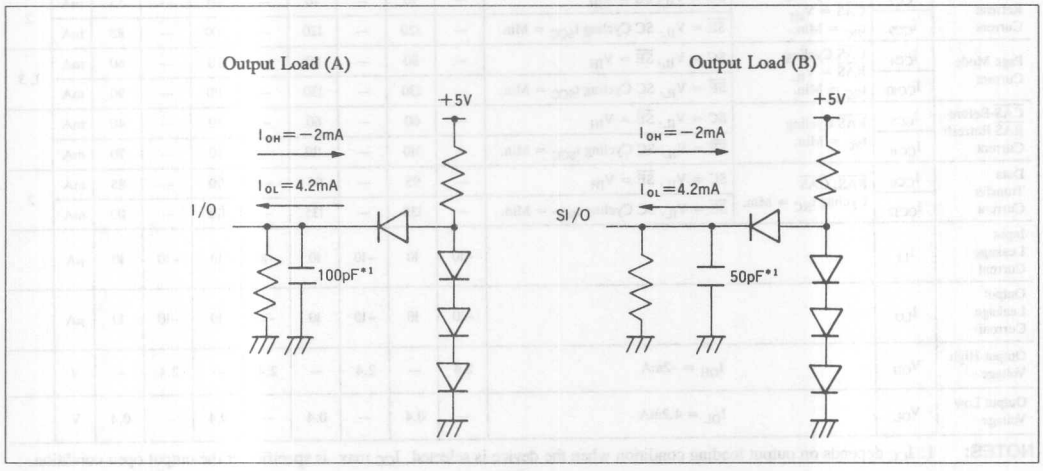
Capacitance (Ta = 25°C, Vcc = 5 V, f = 1MHz, Bias: Clock, I/O = Vcc, address = Vss)

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *11

Test Conditions

Input rise and fall time:	5 ns
Output load:	See figures
Input timing reference levels:	0.8 V, 2.4 V
Output timing reference levels:	0.4 V, 2.4 V



Note: *1. Including scope & jig.

• Common Parameter

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-In to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-In to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

• Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn Off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn Off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	

• Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-In Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	

• Read-Modify-Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Modify Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-In Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time From $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-Off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-In Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

• Refresh Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

• Transfer Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
DT Hold Time From $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
DT Hold Time From $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to DT Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to DT Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
DT to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
DT Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
DT Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-Off Delay From $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time From SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Serial Data Out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-In Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-In Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

• Serial Read Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time From SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Access Time From $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-Out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-Off Delay From $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

• Serial Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-In Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-In Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

• Logic Operation Mode

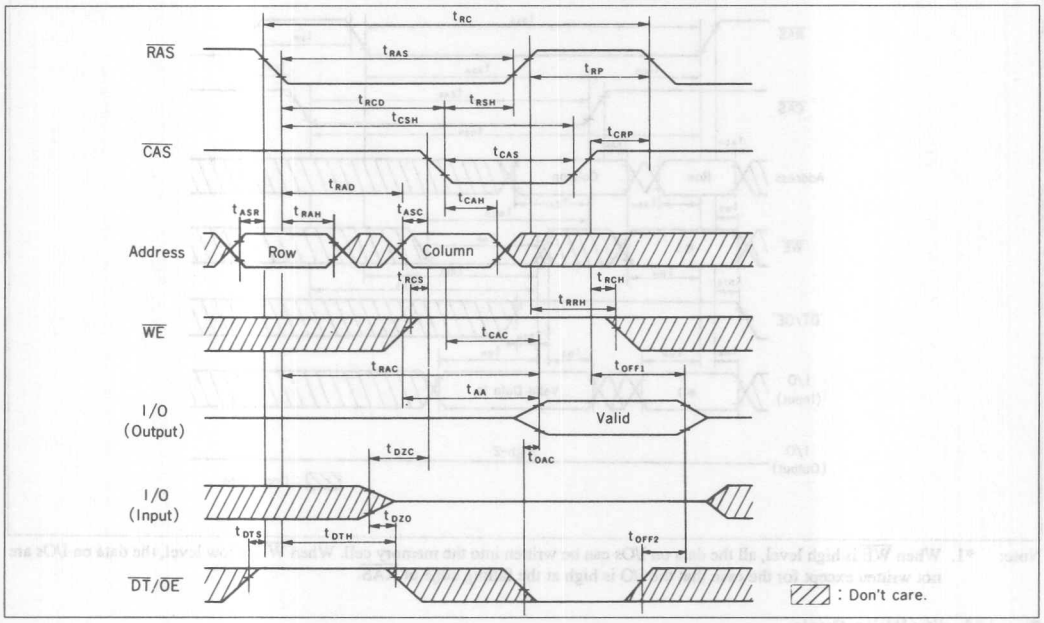
Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width in Write Cycle	t_{RFS}	140	10000	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width in Write Cycle	t_{CFS}	60	10000	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ Hold Time in Write Cycle	t_{FCSH}	140	—	140	—	165	—	200	—	ns	
$\overline{RAS}$ Hold Time in Write Cycle	t_{FRSH}	60	—	60	—	70	—	80	—	ns	
Write Cycle Time	t_{FRC}	230	—	230	—	265	—	310	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	85	—	85	—	100	—	120	—	ns	

NOTES:

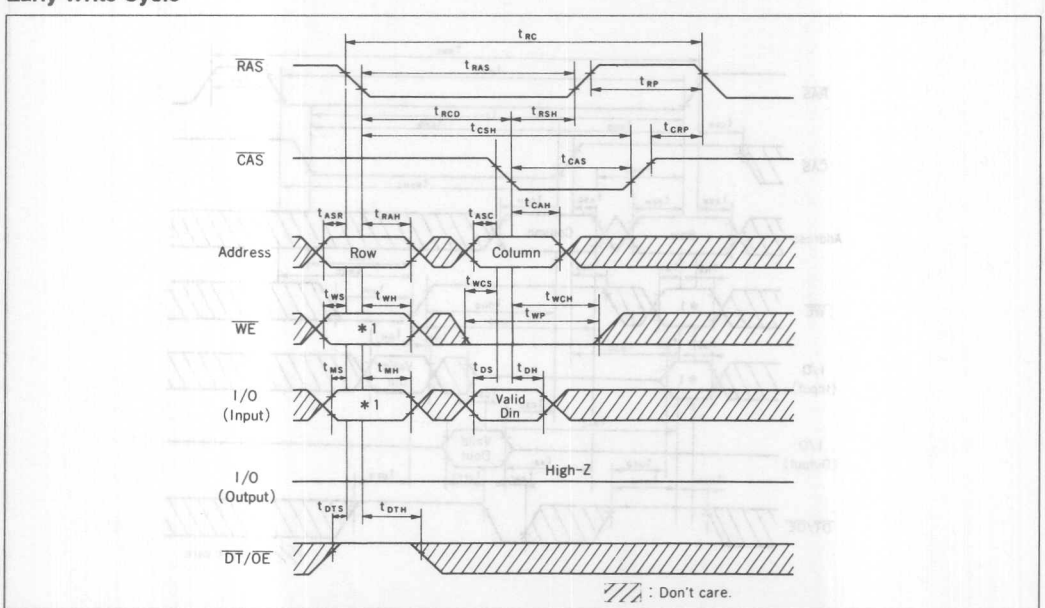
1. AC measurements assume t_T = 5ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds that value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.), access time is specified by t_{AA}.
7. t_{OFF} (max.) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200mV, V_{OL} + 200mV).
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CWD} \geq t_{CWD}$ (min.), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{SCC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).

Timing Waveforms

Read Cycle

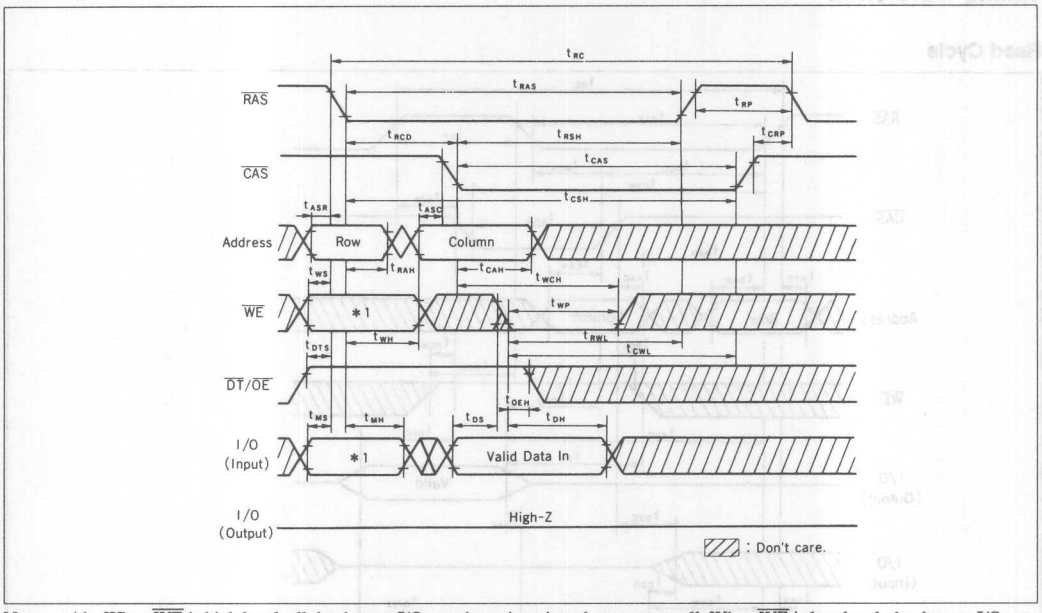


Early Write Cycle



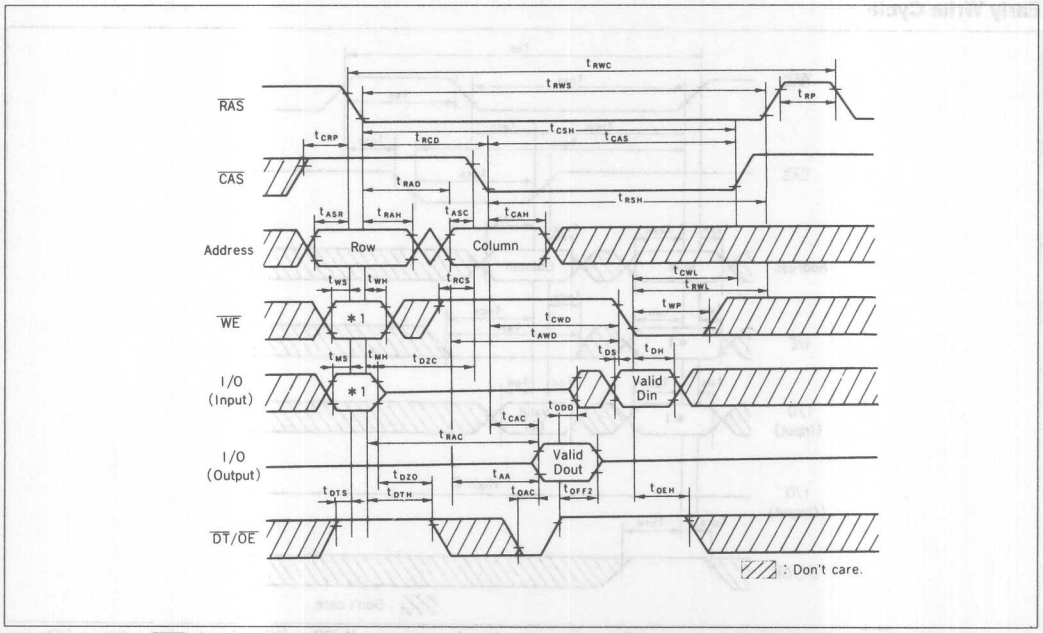
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



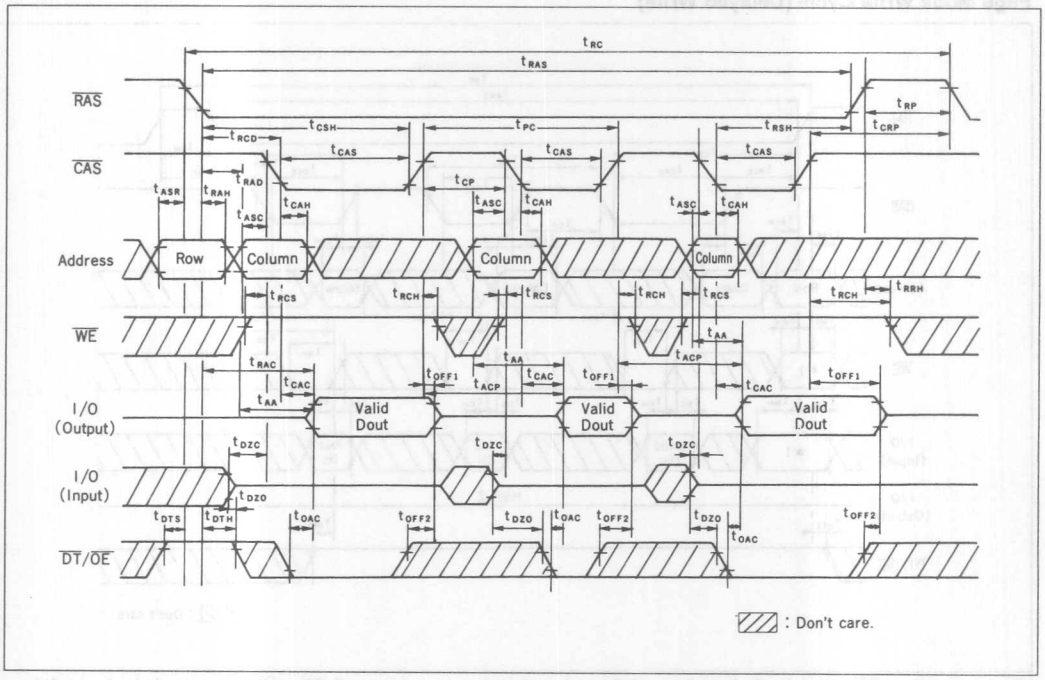
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

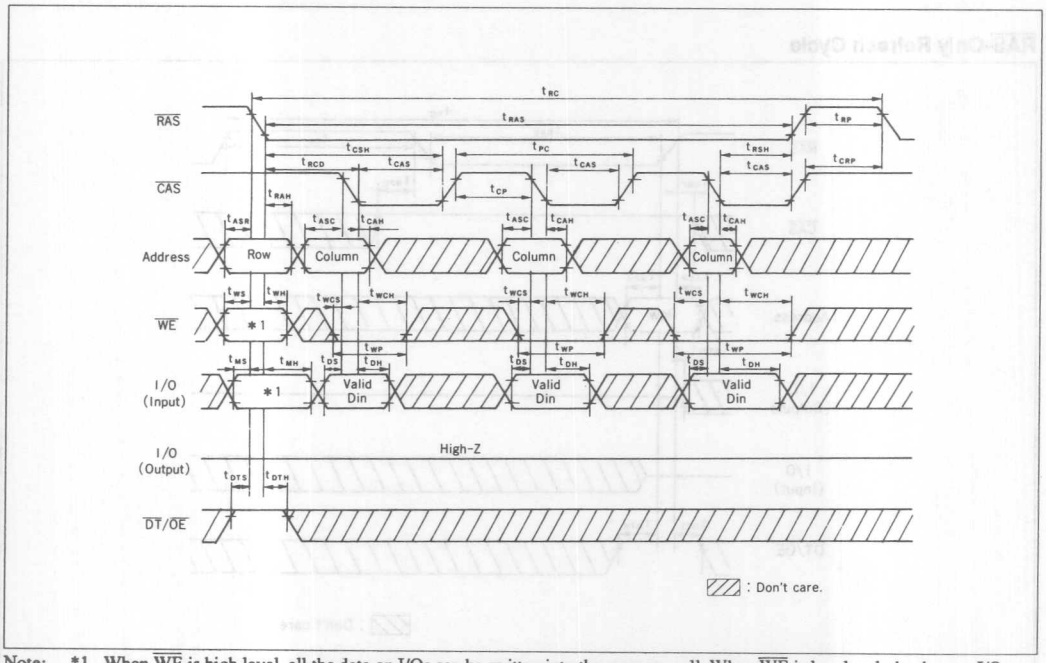


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

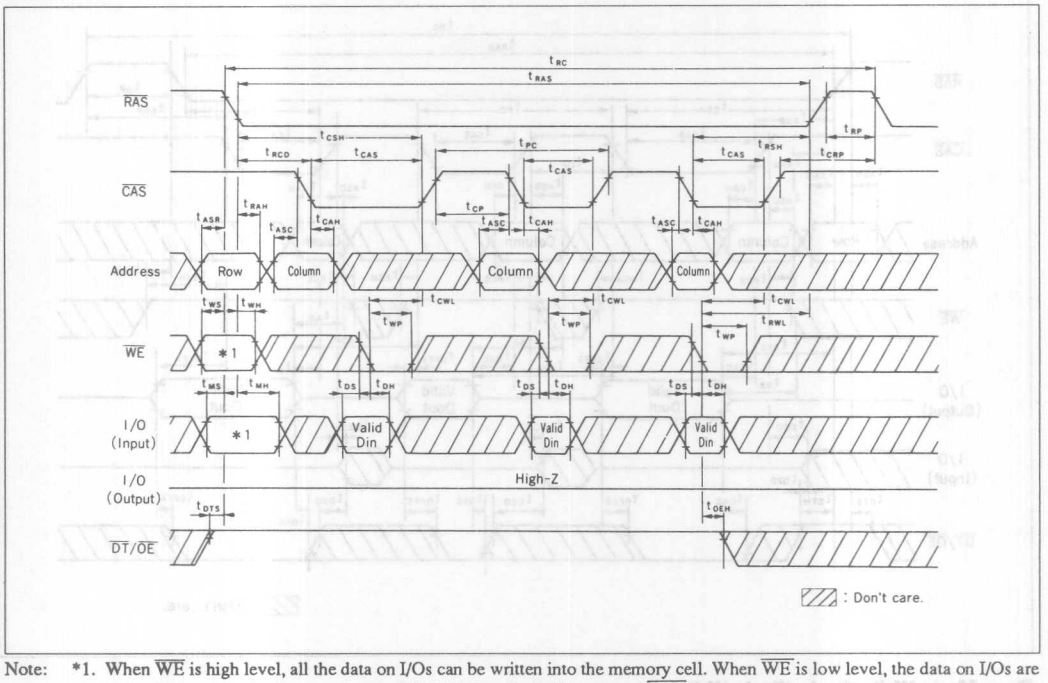


Page Mode Write Cycle (Early Write)



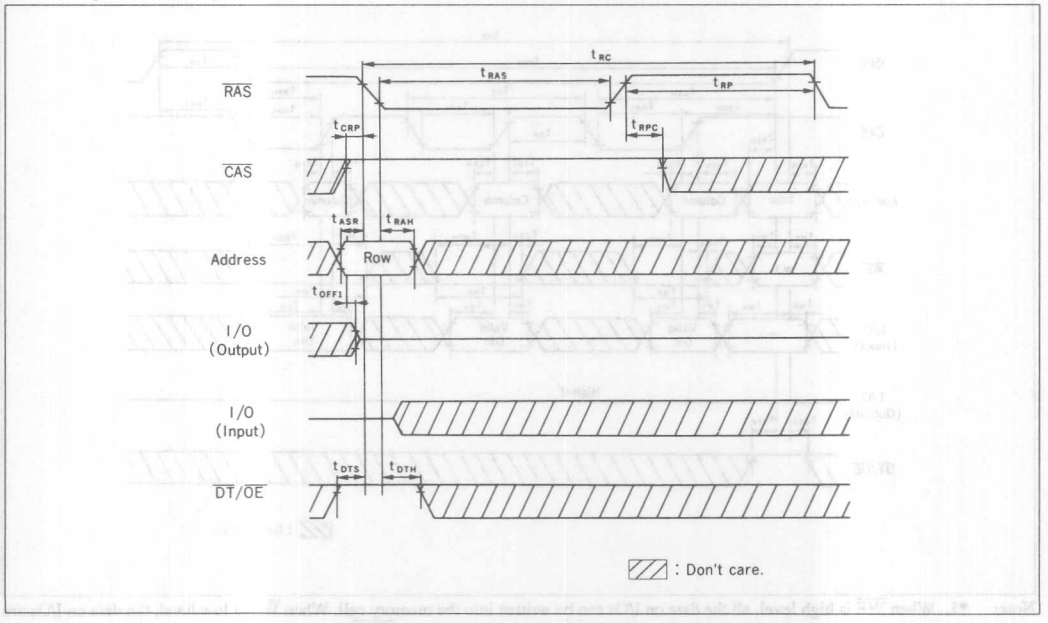
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

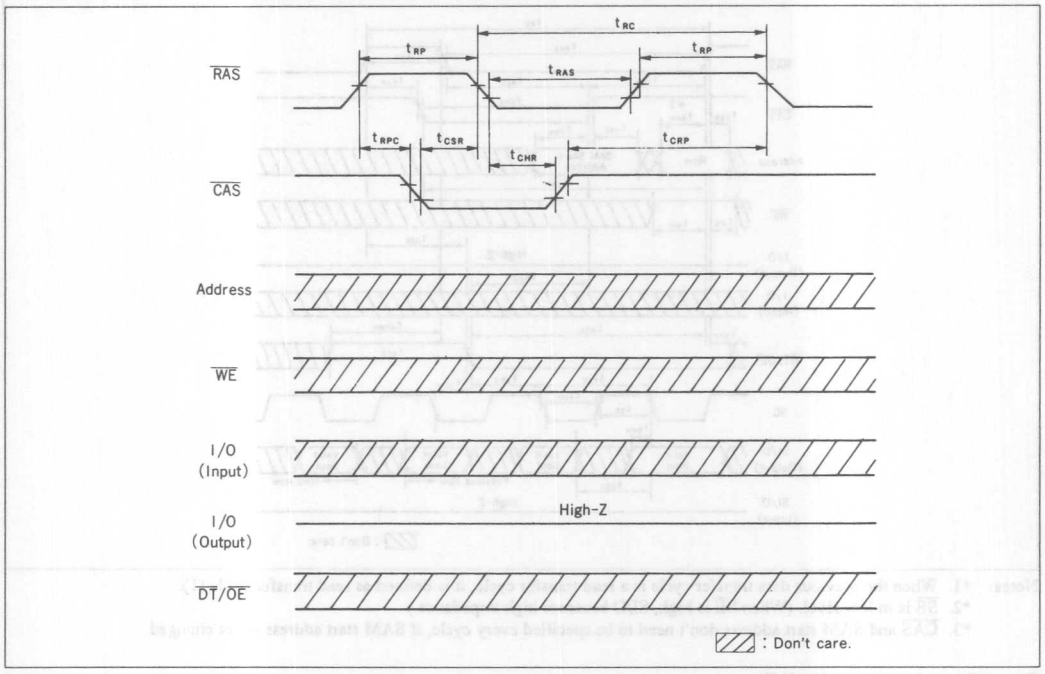


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

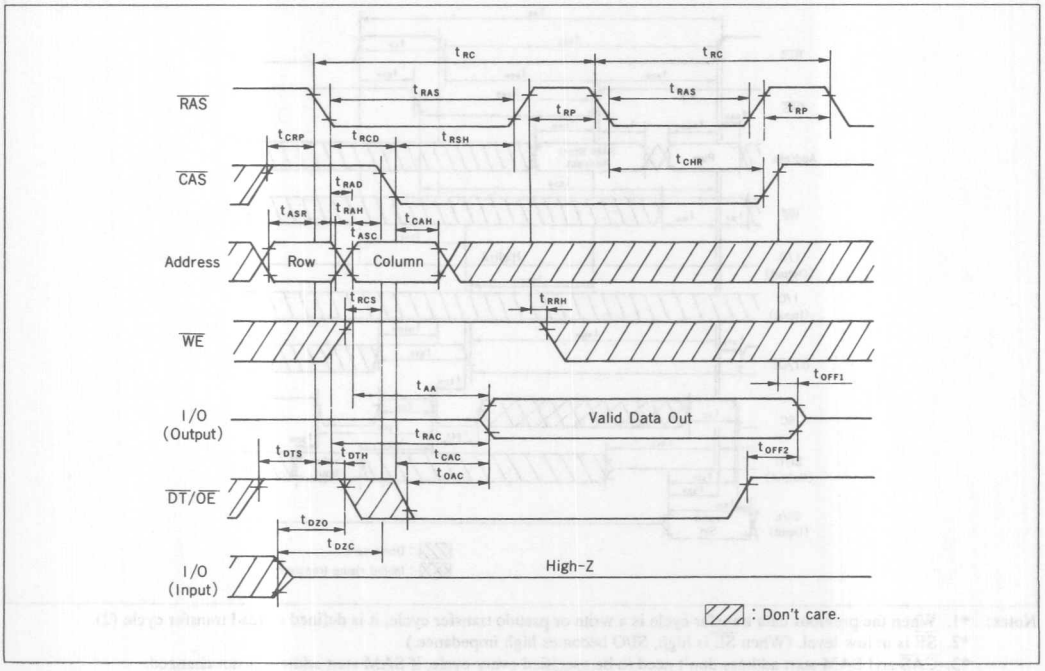
$\overline{RAS}$-Only Refresh Cycle



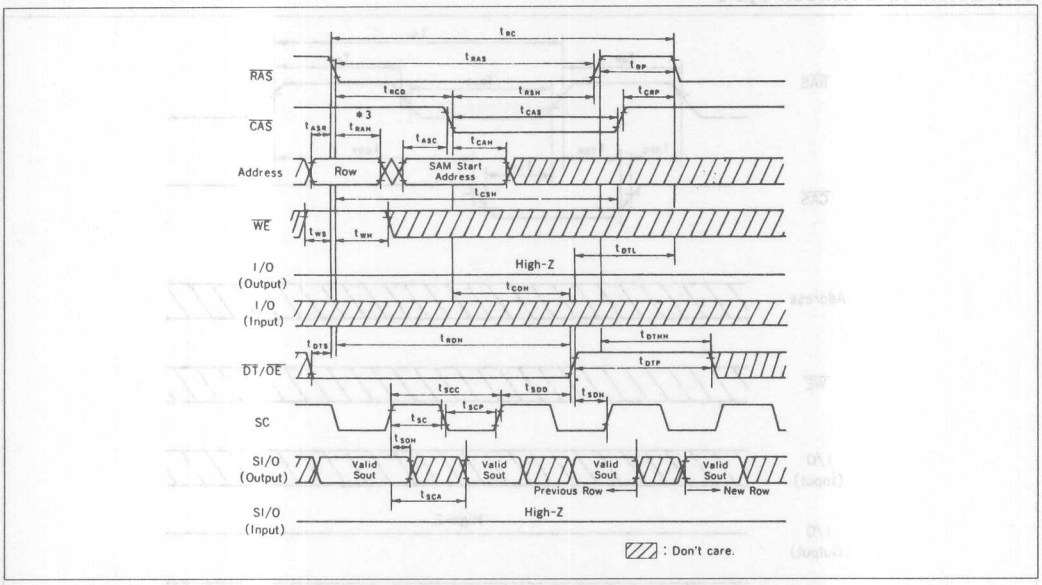
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle

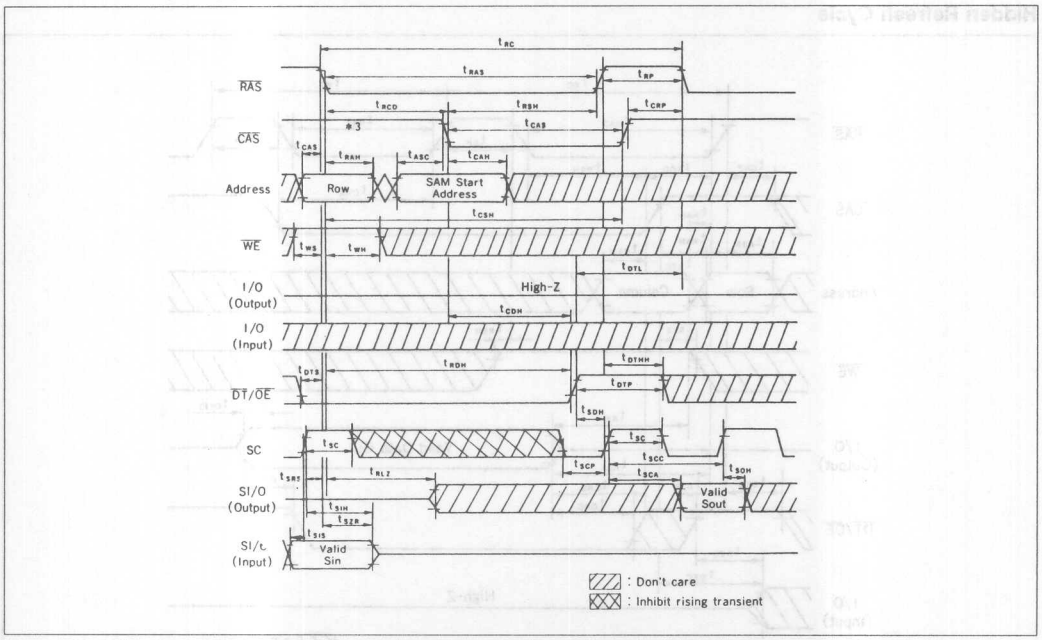


Read Transfer Cycle (1) *1,*2



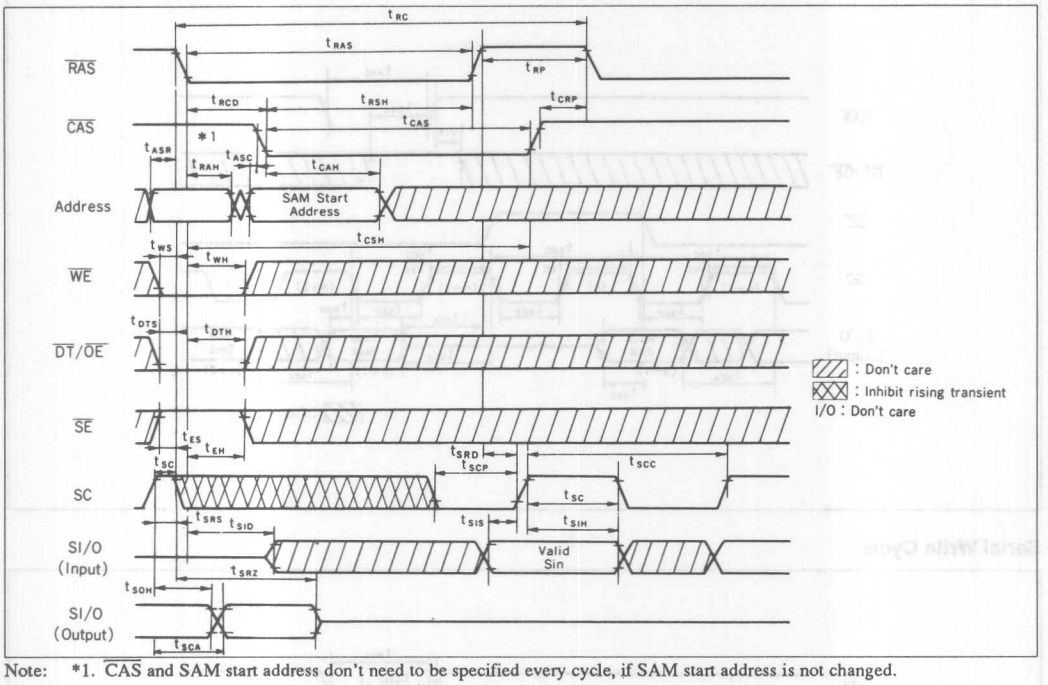
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Read Transfer Cycle (2) *1,*2



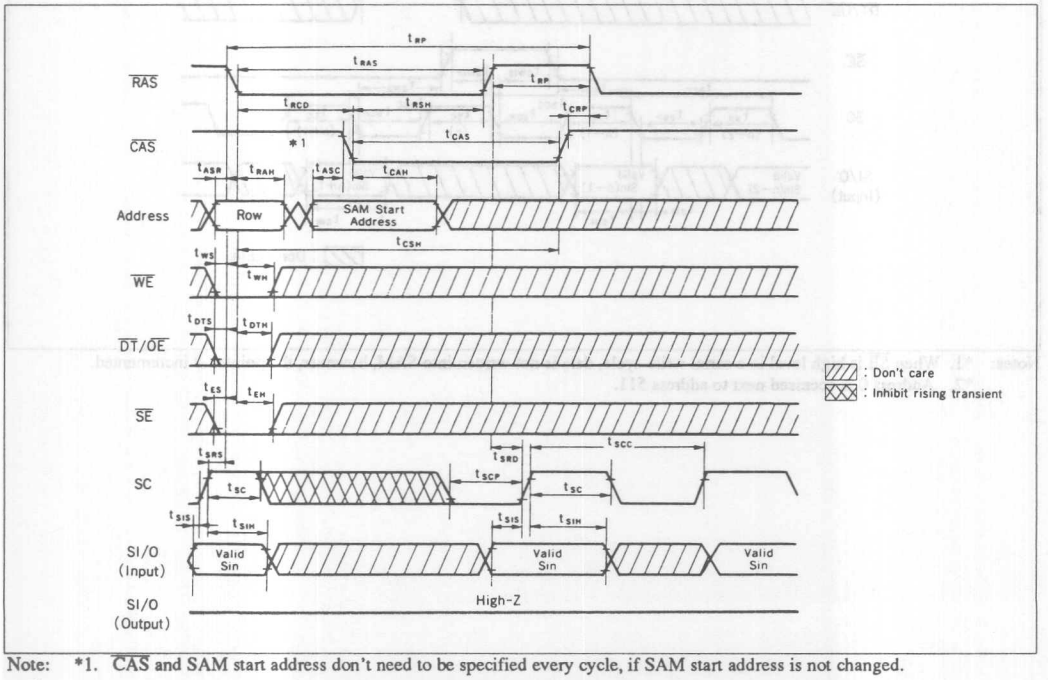
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Pseudo Transfer Cycle



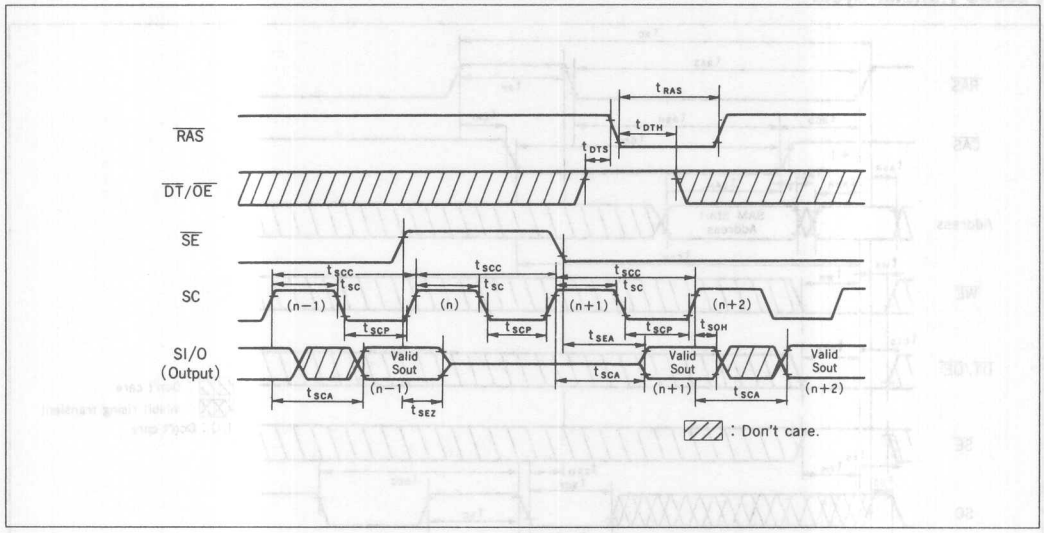
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Write Transfer Cycle

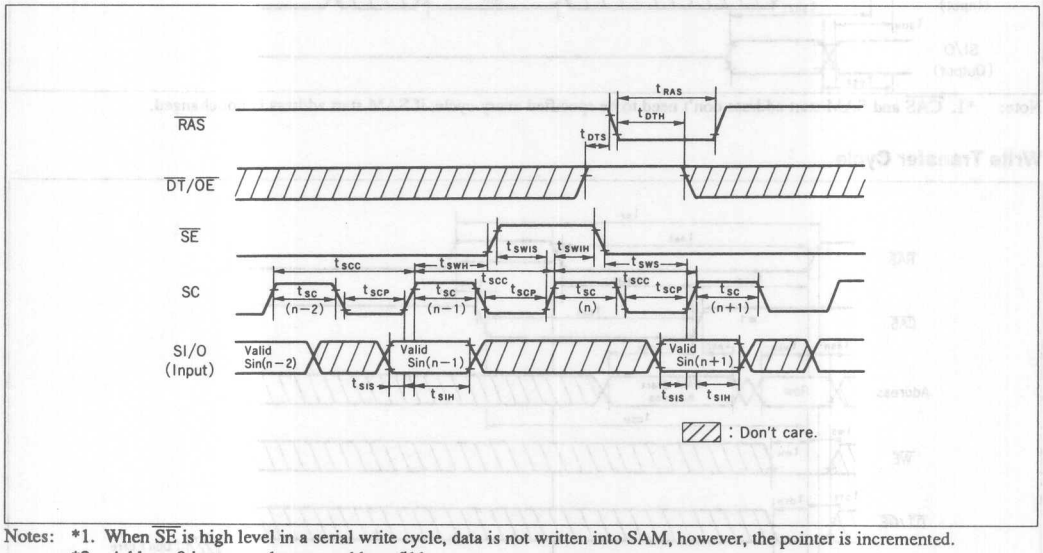


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Serial Read Cycle

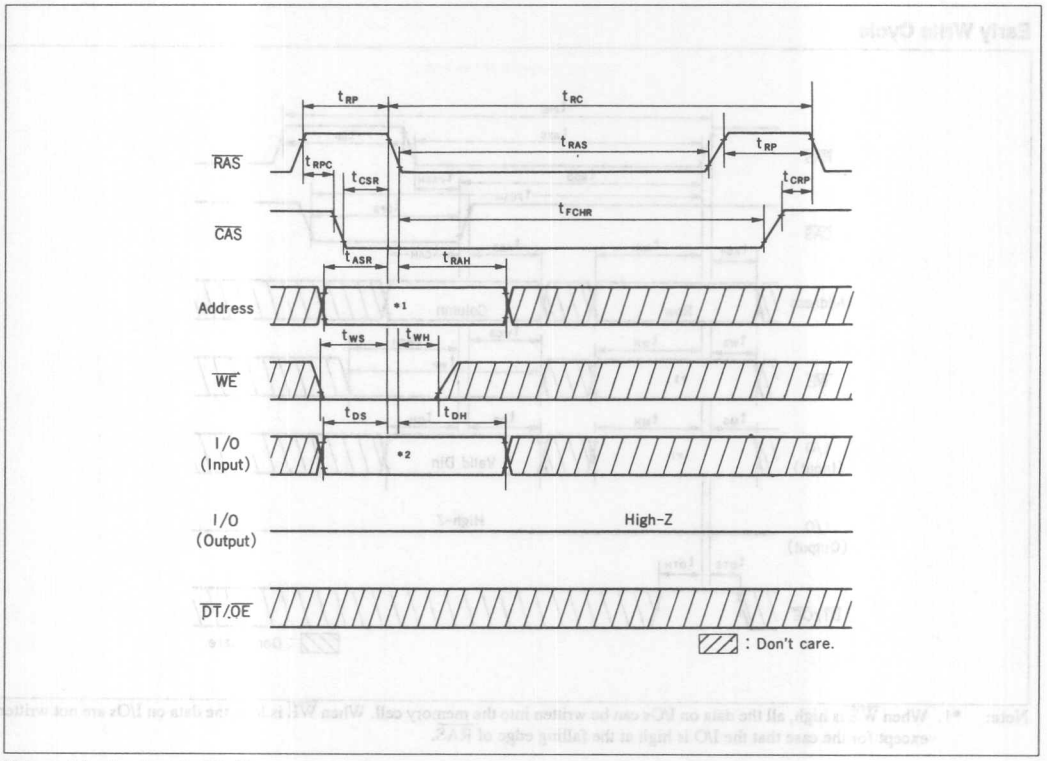


Serial Write Cycle



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

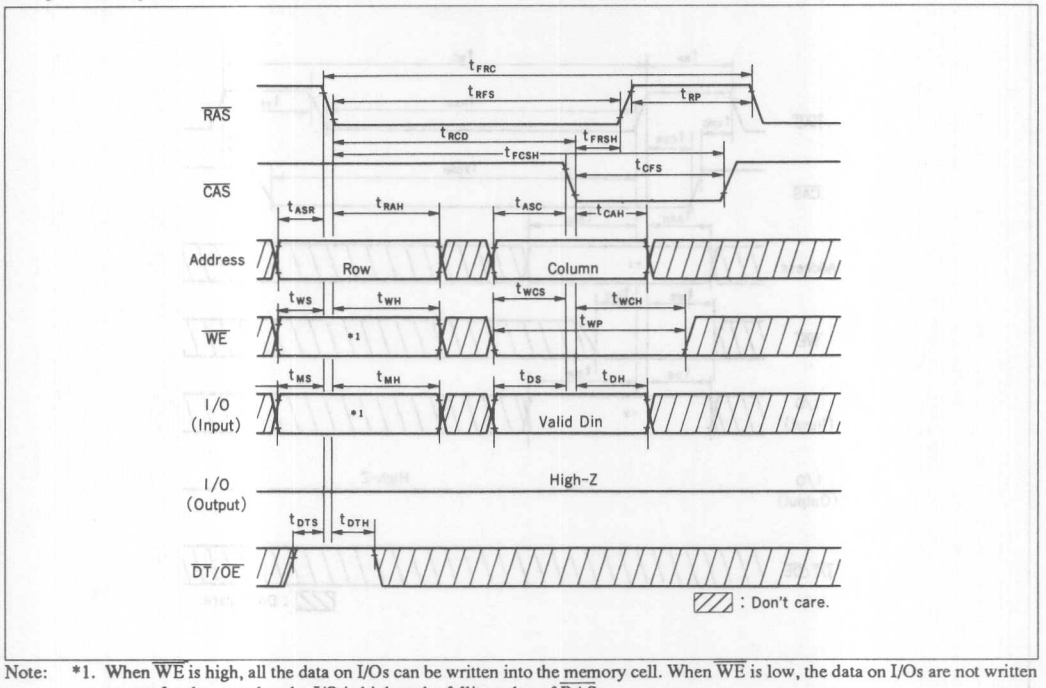
Logic Operation Set/Reset Cycle



Notes: *1. Logic code A0–A3
*2. Write mask data

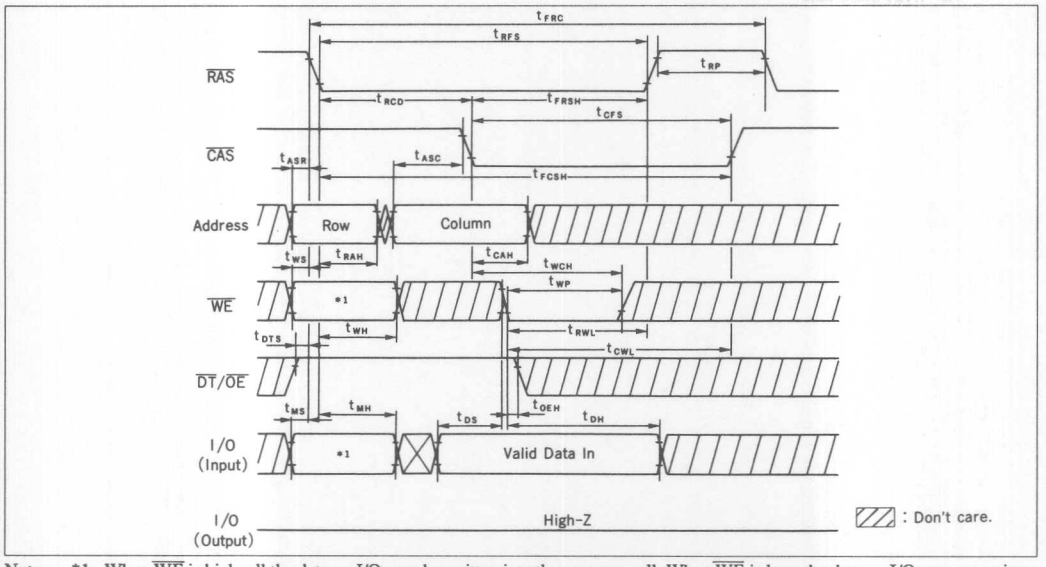
Logic Operation Mode Timing Waveforms

Early Write Cycle



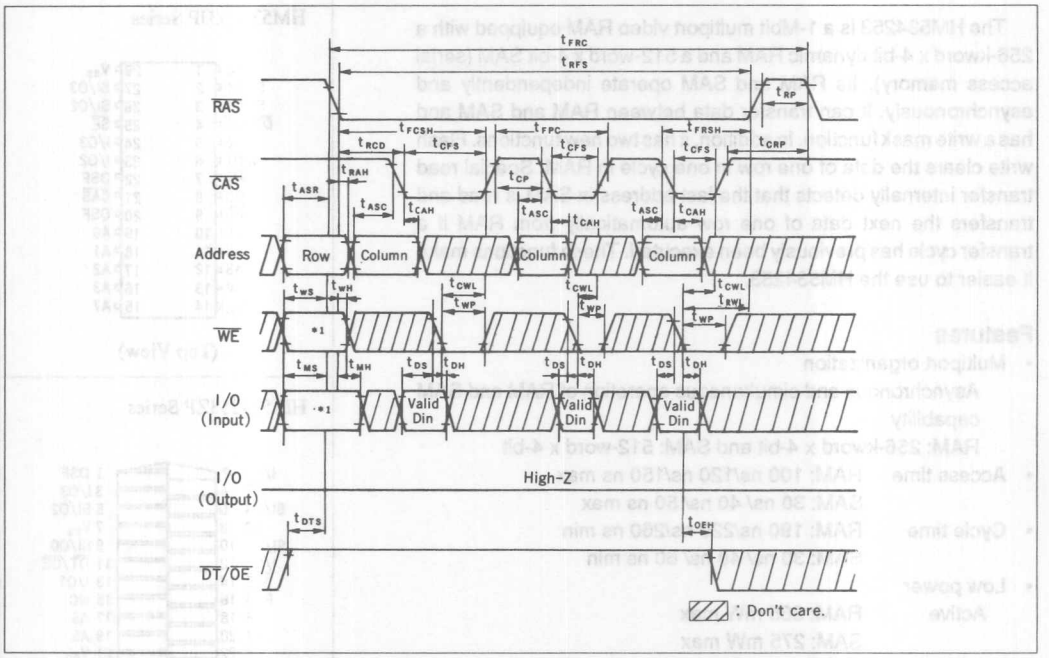
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



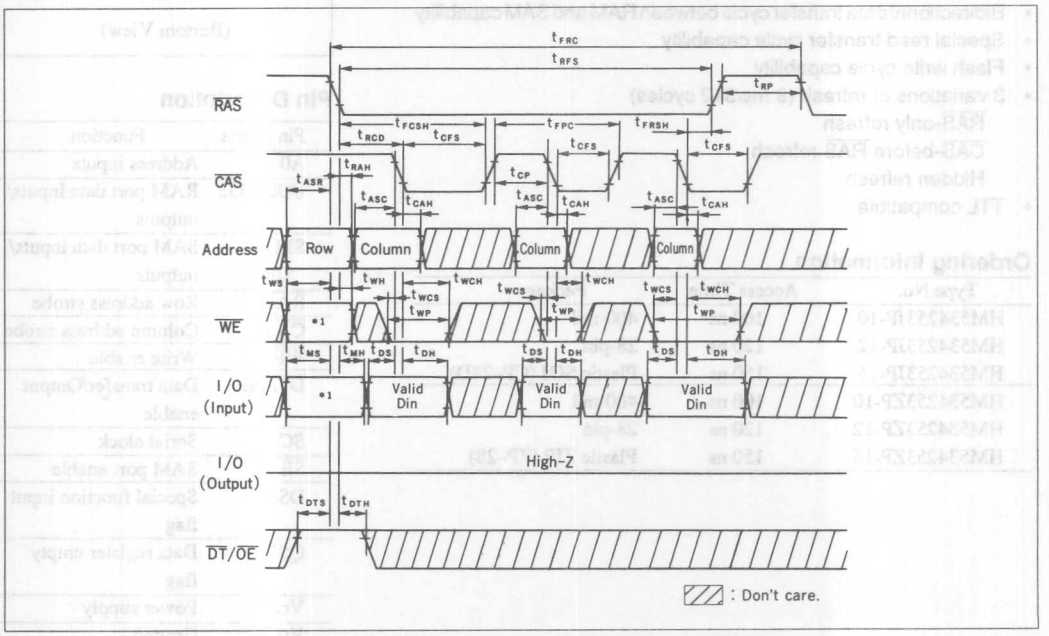
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

HM534253 Series — Preliminary

262144-Word × 4-Bit Multiport CMOS Video RAM

The HM534253 is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. In addition, it has two new functions. Flash write clears the data of one row in one cycle in RAM. Special read transfer internally detects that the last address in SAM is read and transfers the next data of one row automatically from RAM if a transfer cycle has previously been executed. These functions make it easier to use the HM534253.

Features

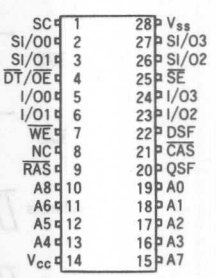
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 256-kword x 4-bit and SAM: 512-word x 4-bit
- Access time — RAM: 100 ns/120 ns/150 ns max; SAM: 30 ns/ 40 ns/ 50 ns max
- Cycle time — RAM: 190 ns/220 ns/260 ns min; SAM: 30 ns/ 40 ns/ 60 ns min
- Low power
  - Active — RAM: 385 mW max; SAM: 275 mW max
  - Standby — 40 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Special read transfer cycle capability
- Flash write cycle capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM534253JP-10	100 ns	400-mil
HM534253JP-12	120 ns	28-pin
HM534253JP-15	150 ns	Plastic SOJ (CP–28D)
HM534253ZP-10	100 ns	400-mil
HM534253ZP-12	120 ns	28-pin
HM534253ZP-15	150 ns	Plastic ZIP (ZP–28)

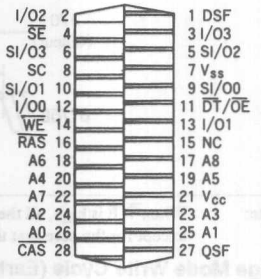
Pin Arrangement

HM534253JP Series



(Top View)

HM534253ZP Series



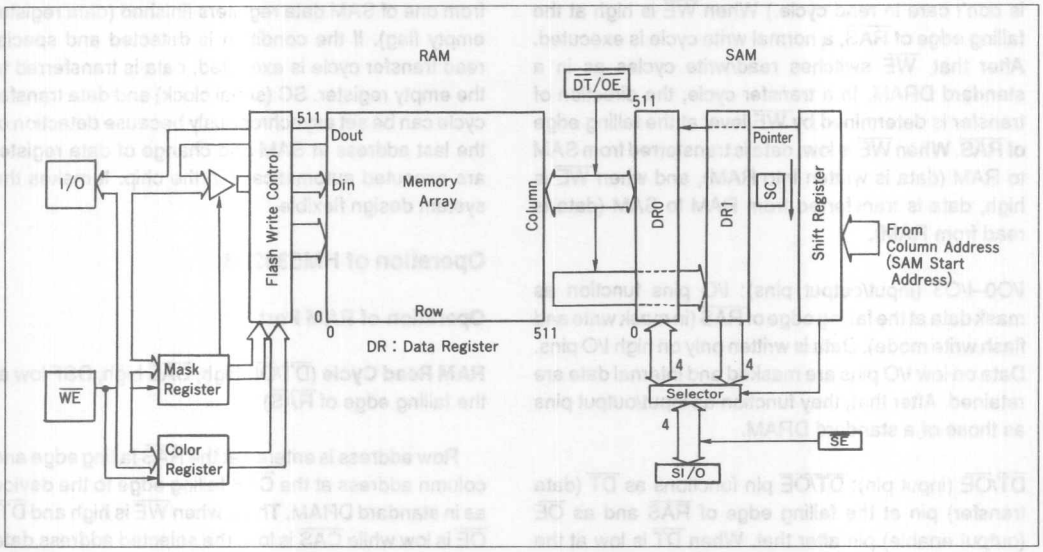
(Bottom View)

Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O3	RAM port data inputs/ outputs
SI/O0–SI/O3	SAM port data inputs/ outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF	Special function input flag
QSF	Data register empty flag
Vcc	Power supply
Vss	Ground
NC	No connection

This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Block Diagram



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM534253.

Table 1. Operation Cycles of the HM534253

Input level at the falling edge of $\overline{RAS}$					Operation Cycle
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	DSF	
H	H	H	×	L	RAM read/write
H	H	H	×	H	Color register set
H	H	L	×	L	Mask write
H	H	L	×	H	Flash write
H	L	H	×	L	Special read initialization
H	L	H	×	H	Special read transfer
H	L	L	H	×	Pseudo transfer
H	L	L	L	×	Write transfer
L	×	×	×	×	CBR Refresh

Note: ×: Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0-A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0–A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534253 turns to mask write mode. According to the I/O level at the time, write on each I/O

can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write and flash write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a special read transfer cycle or special read initialization cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special data input flag pin. It is set to high when new functions such as color register set, special read transfer, and flash write, are used.

QSF (output pin): The HM534253 has a double buffer organization which includes two SAM data registers to relax the restriction on timings of $\overline{DT}/\overline{OE}$ and SC in real time transfer cycle. QSF flag turns high when output from one of SAM data registers finished (data register empty flag). If the condition is detected and special read transfer cycle is executed, data is transferred to the empty register. SC (serial clock) and data transfer cycle can be set asynchronously because detection of the last address in SAM and change of data register are executed automatically in the chip. It makes the system design flexible.

Operation of HM534253

Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle
(Early Write, Delayed Write, Read Modify Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read modify write cycle and enables read/write to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80 %. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 µs).

Flash Write Function (See figure 1)

- Color Register Set Cycle ($\overline{CAS}$·$\overline{DT}/\overline{OE}$·$\overline{WE}$ high, DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle. 4 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it preserves the data until reset. The data set is just as same as in the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and early write and delayed write cycle can be executed. In this cycle, memory array access is not executed, so it is unnecessary to give row and column addresses.

- Flash Write Cycle ($\overline{CAS}$·$\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512 x 4 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also possible to mask I/O in this cycle. When $\overline{CAS}$·$\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is preserved. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time.

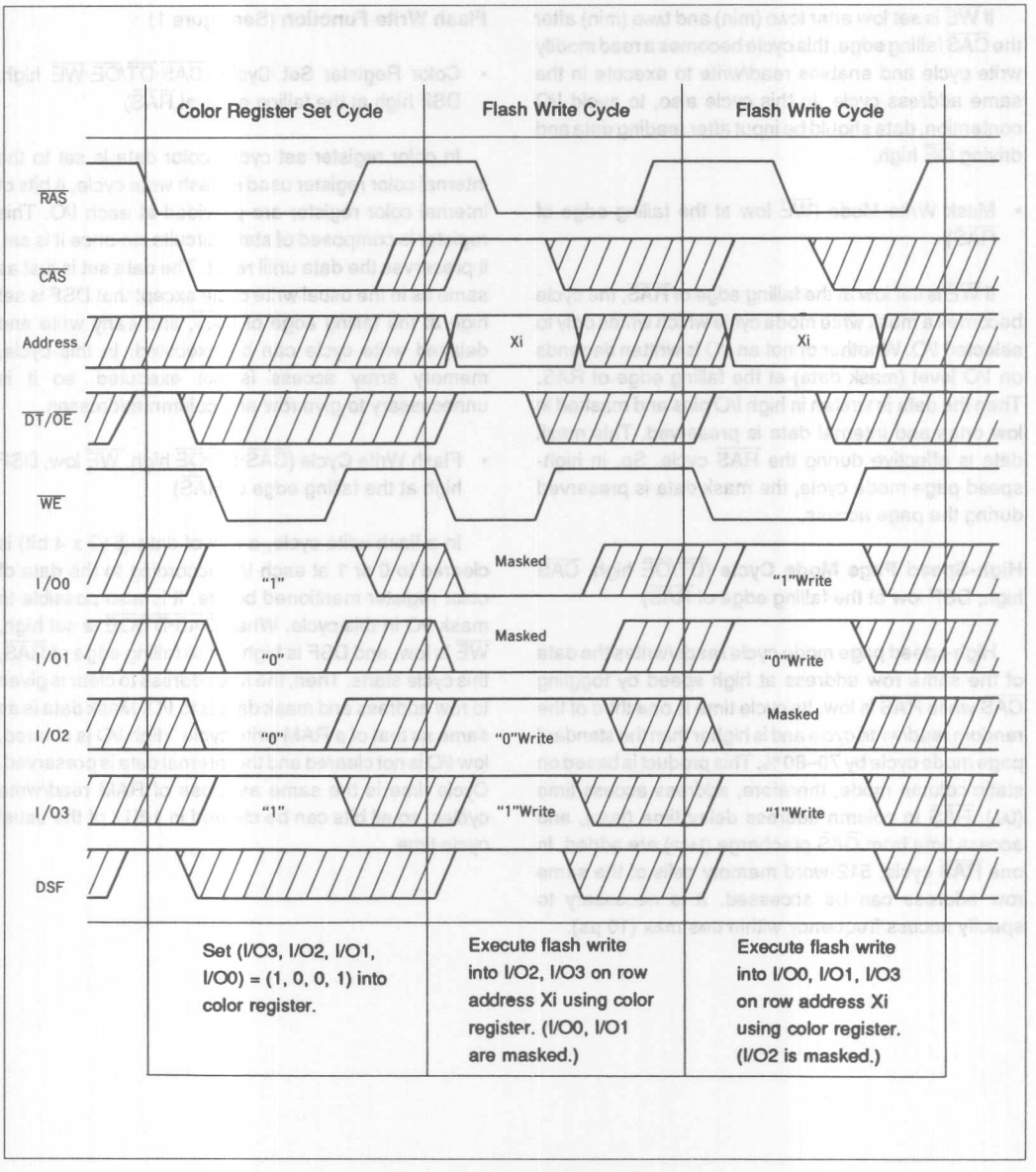


Figure 1. Use of Flash Write

Transfer Operation

The HM534253 provides the special read initialization cycle, special read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
(2) Determine direction of data transfer
  (a) Special read initialization cycle, Special read transfer cycle: RAM → SAM
  (b) Write transfer cycle: RAM ← SAM
(3) Determine input or output of SAM I/O pin (SI/O)
  Special read initialization cycle: SI/O output
  Pseudo transfer cycle, write transfer cycle: SI/O input
(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Special Read Initialization Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high, DSF low at the falling edge of $\overline{RAS}$)

If $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ high, and DSF low at the falling edge of $\overline{RAS}$, this cycle becomes a special read initialization cycle. Special read initialization is used (1) to start special read transfer operation and (2) to switch SAM input/output pin (SI/O), set in input state by pseudo transfer cycle or write transfer cycle, to output state.

If the clock is set as mentioned before, address of SAM transfer word line is set to row address and first SAM address to access (SAM start address) to column address, it becomes possible to execute SAM read after t_{SRD} (min) after $\overline{RAS}$ is high. In this cycle, SI/O outputs uncertain data after the $\overline{RAS}$ falling edge. So when SAM is in input state before executing this cycle, it is necessary to stop input before the $\overline{RAS}$ falling edge.

SAM access is inhibited while $\overline{RAS}$ is low in this cycle. SC should not be raised during $\overline{RAS}$ low.

Special Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high, DSF high at the falling edge of $\overline{RAS}$)

Ordinary multiport video RAM has some problems; (1) severe limitation on timings between processor clock $\overline{DT/OE}$ and CRT clock SC, (2) complicated external control circuit to detect SAM last address externally and to insert transfer cycle synchronously. Special read transfer cycle makes it possible to relax the timing limitations and to set serial clock (SC) and transfer cycle perfectly synchronously.

Figure 2 shows the block diagram for a special read transfer. SAM double buffers are composed of two data registers (DR). When data is read out from DR0 serially, special read transfer cycle transfers a row of RAM data, which will be read from SAM next, to DR1.

The end of data read from DR0 is detected internally and data register switching circuit automatically switches to DR1 output. So data can be output continuously.

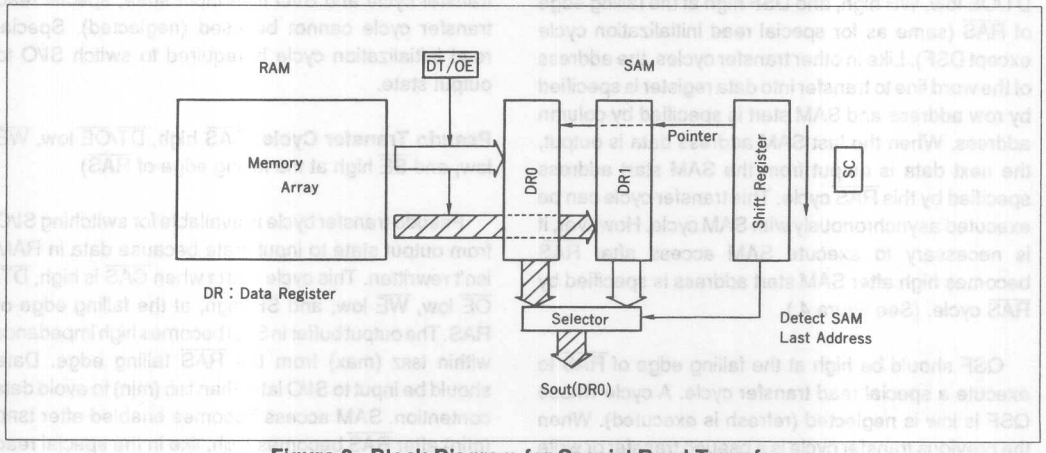


Figure 2. Block Diagram for Special Read Transfer

Figure 3 shows special read transfer operation sequence. QSF flag indicates that reading out from data resister has finished (data register empty flag), and special read transfer can be executed while QSF is high. At first, special read operation starts by executing an special read initialization cycle. So QSF becomes high, the processor gives row address and SAM start address, which is needed next, to the memory, and inserts a special read transfer cycle. Data register becomes full after a special read transfer cycle, so QSF becomes low during the cycle. When the last SAM address is accessed, QSF becomes high and the data register, which outputs from the next SAM address, changes, and serial access can be executed.

By executing these handshakes, serial clock and transfer cycle can be executed perfectly asynchronously, and flexibility of the system design is improved.

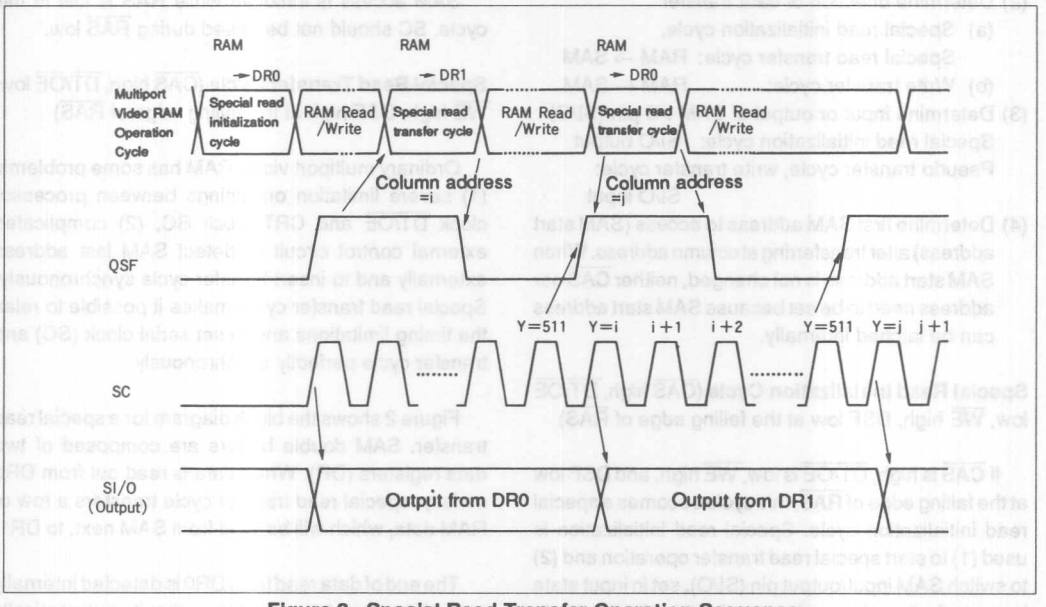


Figure 3. Special Read Transfer Operation Sequence

Special read transfer cycle is set by making $\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high, and DSF high at the falling edge of $\overline{RAS}$ (same as for special read initialization cycle except DSF). Like in other transfer cycles, the address of the word line to transfer into data register is specified by row address and SAM start is specified by column address. When the last SAM address data is output, the next data is output from the SAM start address specified by this $\overline{RAS}$ cycle. This transfer cycle can be executed asynchronously with SAM cycle. However, it is necessary to execute SAM access after $\overline{RAS}$ becomes high after SAM start address is specified by $\overline{RAS}$ cycle. (See figure 4.)

QSF should be high at the falling edge of $\overline{RAS}$ to execute a special read transfer cycle. A cycle whose QSF is low is neglected (refresh is executed). When the previous transfer cycle is a pseudo transfer or write transfer cycle and SI/O is in input state, special read transfer cycle cannot be used (neglected). Special read initialization cycle is required to switch SI/O to output state.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of RAS. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high, like in the special read

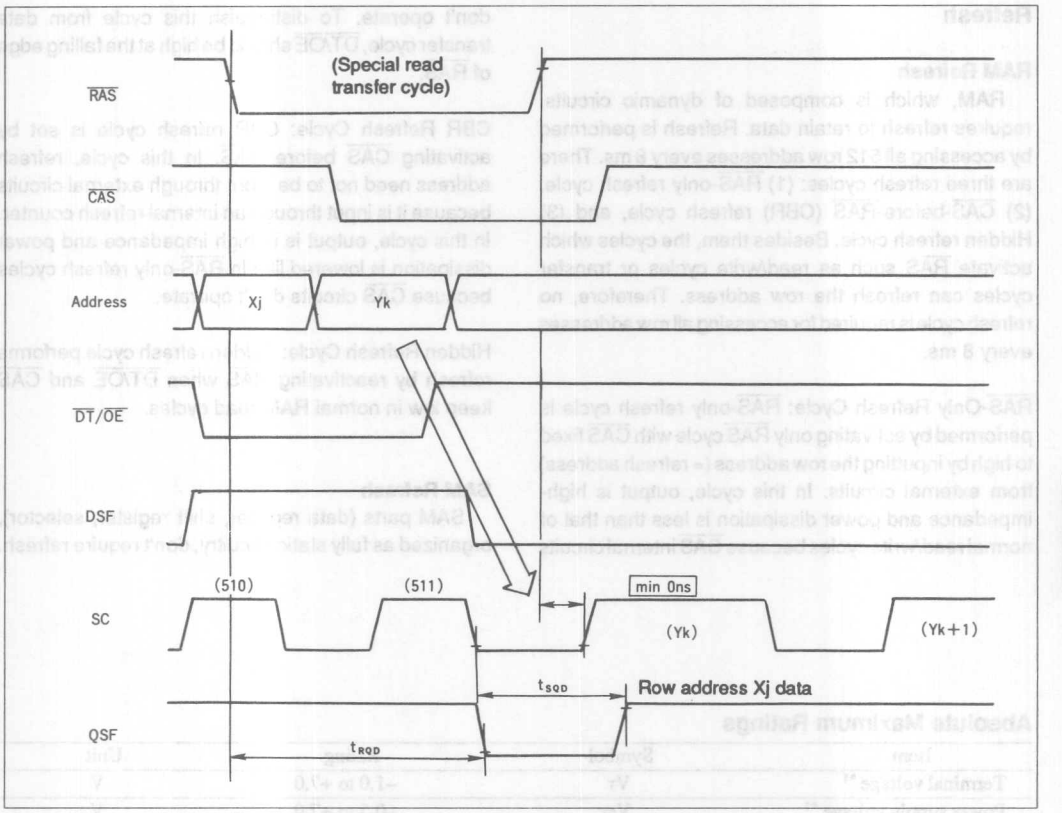


Figure 4. The Restriction of Special Read Transfer

initialization cycle. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is special read initialization cycle or special read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When the last address is accessed at the state of QSF low (data register is full), it is signaled to external circuits that special read transfer is enabled by making QSF high. Next, after SAM access, output data register is switched, then the row address data given by previous special read transfer cycle is output from the SAM start address. If special read transfer isn't performed (QSF high), the column address 0 of the same row address is accessed after the last address is accessed.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can be used to mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT/OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$-only refresh cycles because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT/OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	–1.0 to +7.0	V
Power supply voltage *1	V_{CC}	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: *1. Relative to Vss.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	—	6.5	V
Input low voltage *1	V_{IL}	–0.5*2	—	0.8	V

Notes: *1. All voltages referenced to Vss.
*2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	HM534253-10 Min	HM534253-10 Max	HM534253-12 Min	HM534253-12 Max	HM534253-15 Min	HM534253-15 Max	Unit	Test Conditions RAM port	Test Conditions SAM port
Operating current	I_{CC1}	—	70	–	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	120	–	100	—	80	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc=Min
Standby current	I_{CC2}	—	7	–	7	—	7	mA	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	–	40	—	30	mA		$\overline{SE}$ = V_{IL}, SC cycling tscc = Min
$\overline{RAS}$-only refresh current	I_{CC3}	—	60	–	50	—	40	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	110	–	90	—	70	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min
Page mode current	I_{CC4}	—	65	–	55	—	45	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL}	SC, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	115	–	95	—	75	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	60	–	50	—	40	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	110	–	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling tscc = Min
Data transfer current	I_{CC6}	—	90	–	90	—	90	mA	$\overline{RAS}$,$\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	125	–	125	—	125	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

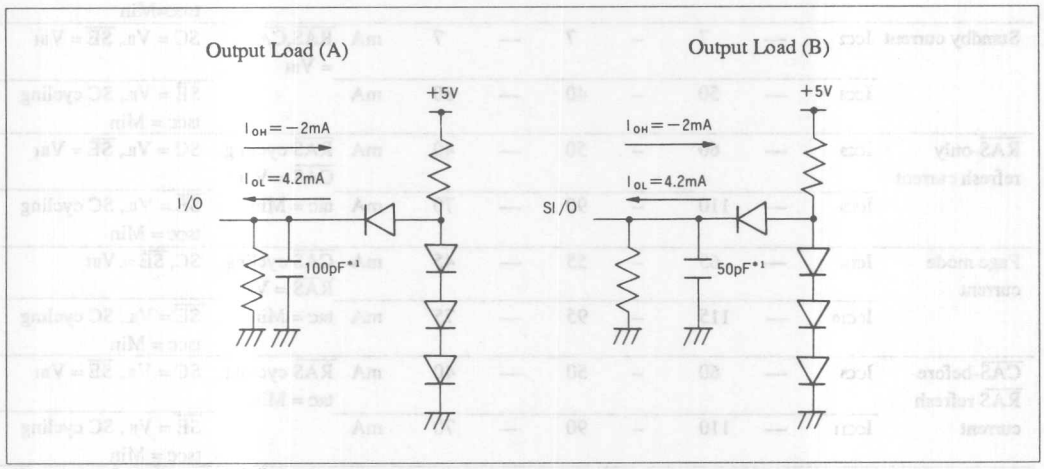
Capacitance (Ta = 25°C, Vcc = 5 V, f =1 MHz, Bias: Clock, I/O = Vcc, address = Vss)

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V) *1, *11

Test Conditions

Input rise and fall time:	5 ns
Output load:	See figures
Input timing reference levels:	0.8 V, 2.4 V
Output timing reference levels:	0.4 V, 2.4 V



Note: *1. Including scope & jig.

Common Parameter

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	30	10000	35	10000	40	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	70	25	85	30	110	ns	*5,*6
$\overline{RAS}$ hold time	t_{RSH}	30	—	35	—	40	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	*8
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	15	—	15	—	20	—	ns	
DSF to $\overline{RAS}$ setup time	t_{SFS}	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ hold time	t_{SFH}	25	—	25	—	30	—	ns	
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	
Data–in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	55	—	70	ns	*3, *6
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	*7
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	*7
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	*12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	*12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	65	25	80	ns	*5, *6
Page mode cycle time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	*9
Write command hold time	t_{WCH}	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	75	—	90	—	ns	*9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	95	—	120	—	ns	*9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	55	—	70	ns	*3,*6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	65	25	80	ns	*5,*6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Transfer Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	100	—	120	—	150	ns	*4
$\overline{RAS}$ to QSF (high) delay time	t_{RQH}	—	TBD	—	TBD	—	TBD	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	—	10	—	10	—	10	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	*7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	40	—	50	ns	*4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	

Serial Read Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	40	—	50	ns	*4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	40	ns	*4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	0	25	0	25	0	30	ns	*7
Last SC to QSF delay time	t_{SQD}	—	TBD	—	TBD	—	TBD	ns	*4

Serial Write Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	30	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	50	—	ns	

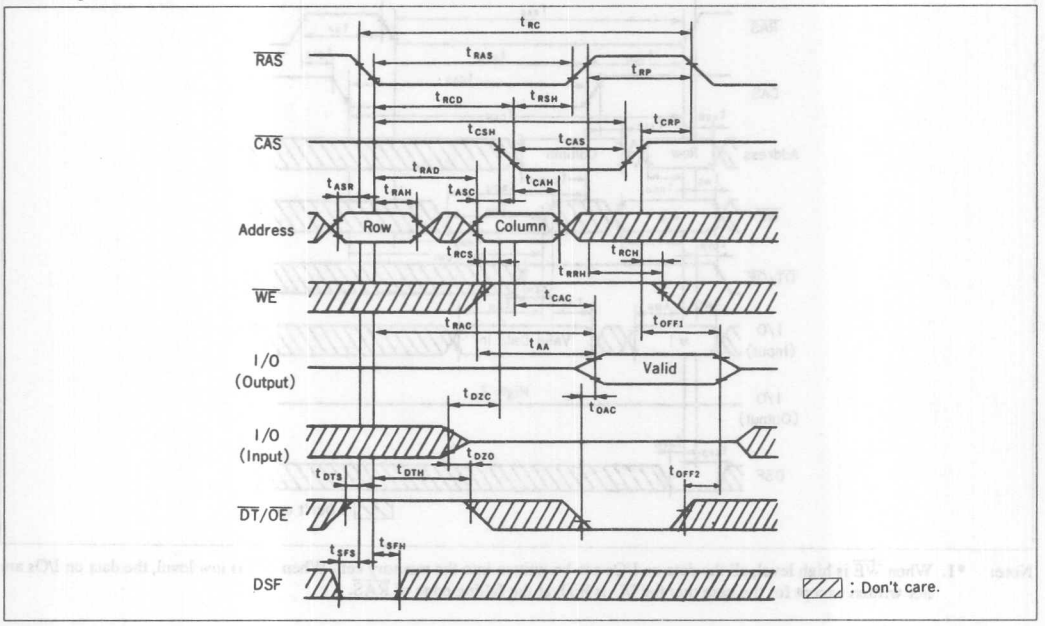
Flash Write Cycle

Item	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Flash write cycle time	t_{RCFW}	230	—	265	—	310	—	ns	
$\overline{RAS}$ pulse width	t_{RCSFW}	140	—	165	—	200	—	ns	
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{CAS}$ high level hold time referenced to $\overline{RAS}$	t_{CHHR}	20	—	25	—	30	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	

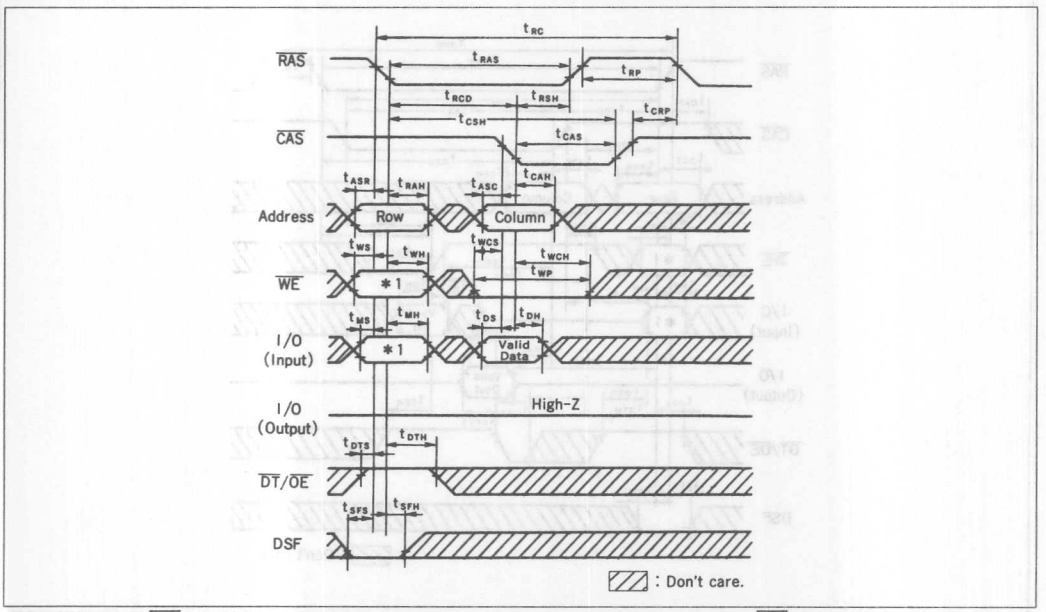
Notes:
*1. AC measurements assume $t_T = 5$ ns.
*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
*6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH}–200 mV, V_{OL}+200 mV).
*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data out pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
*11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

Timing Waveforms

Read Cycle

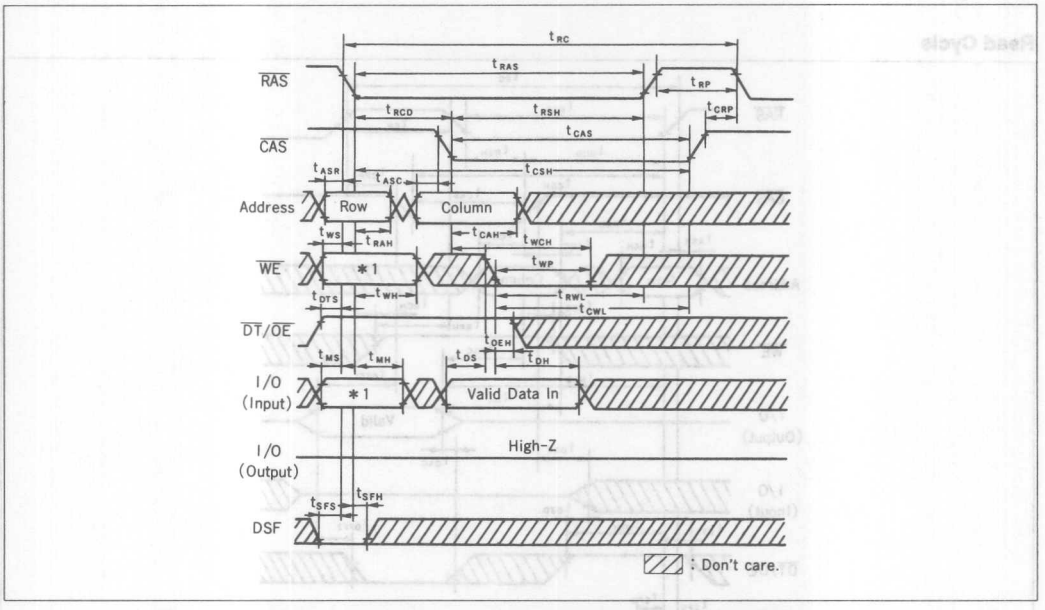


Early Write Cycle



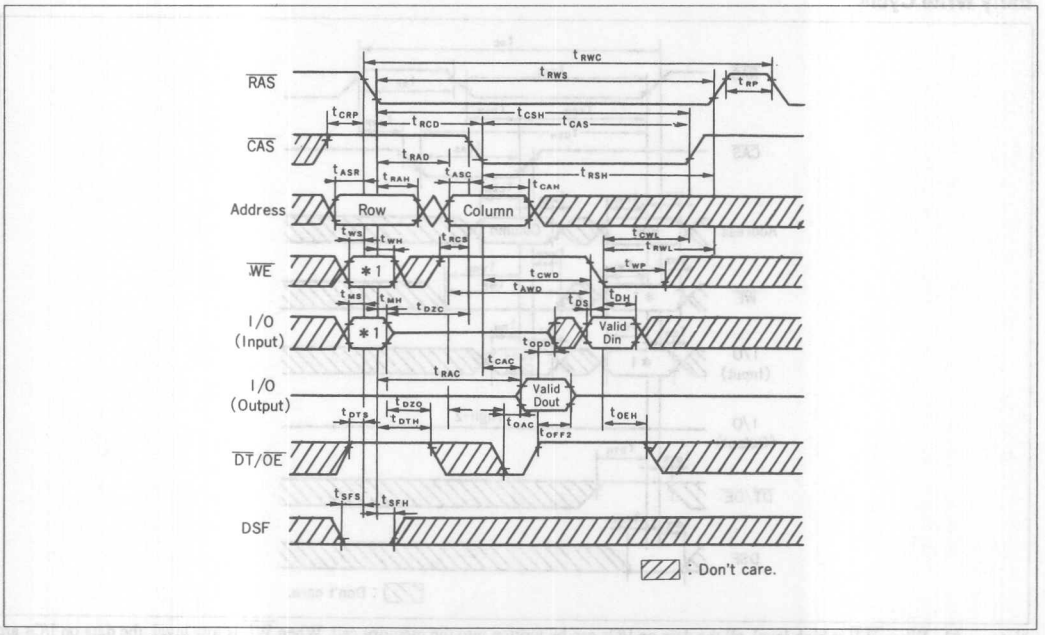
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



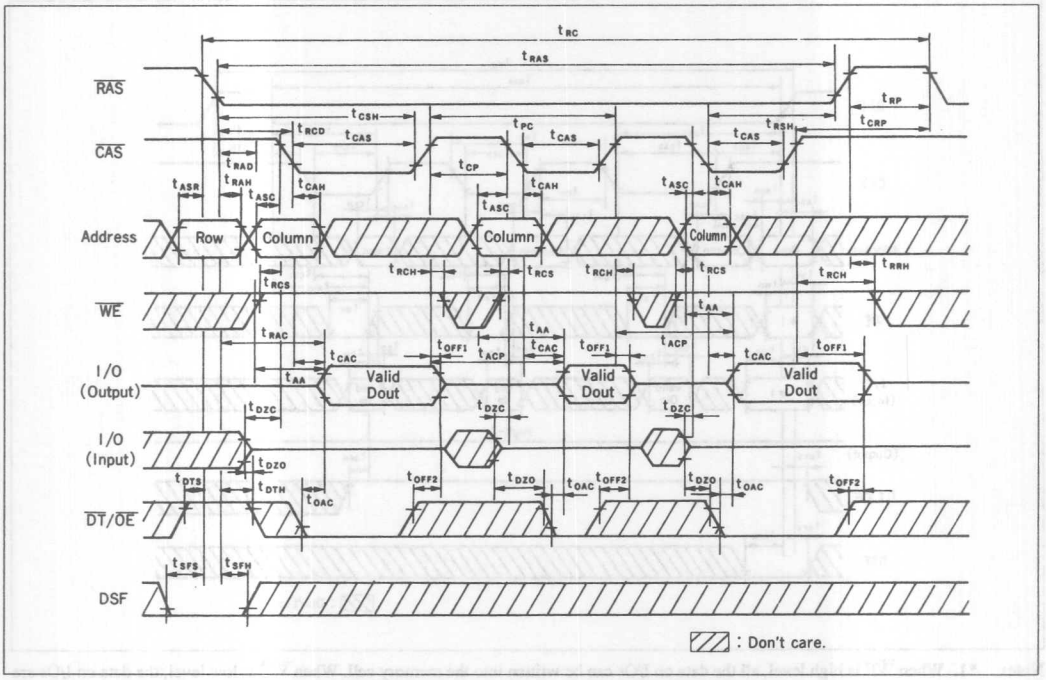
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

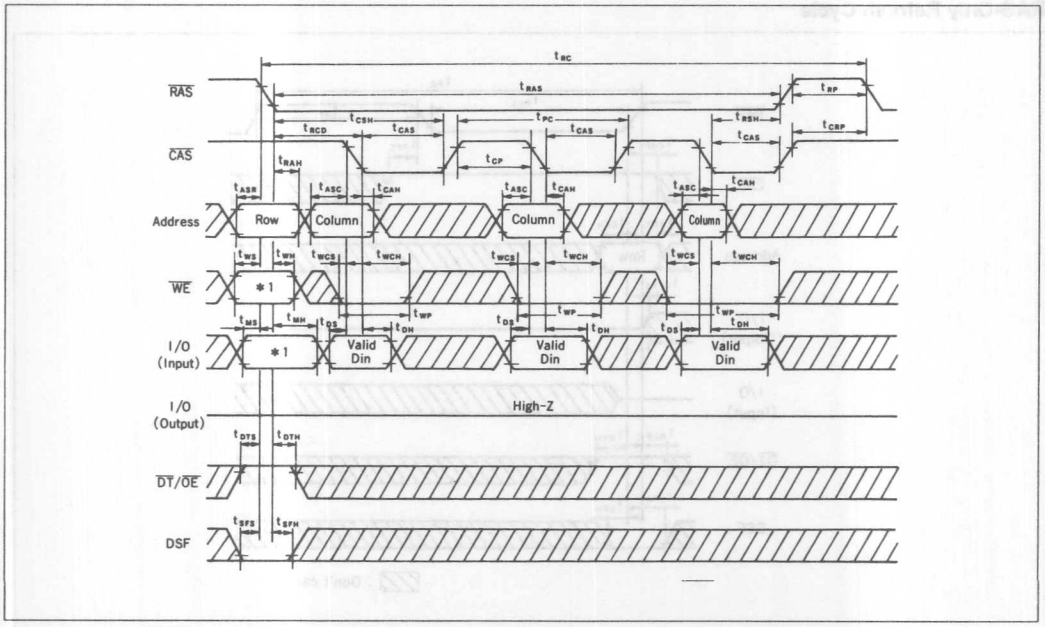


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

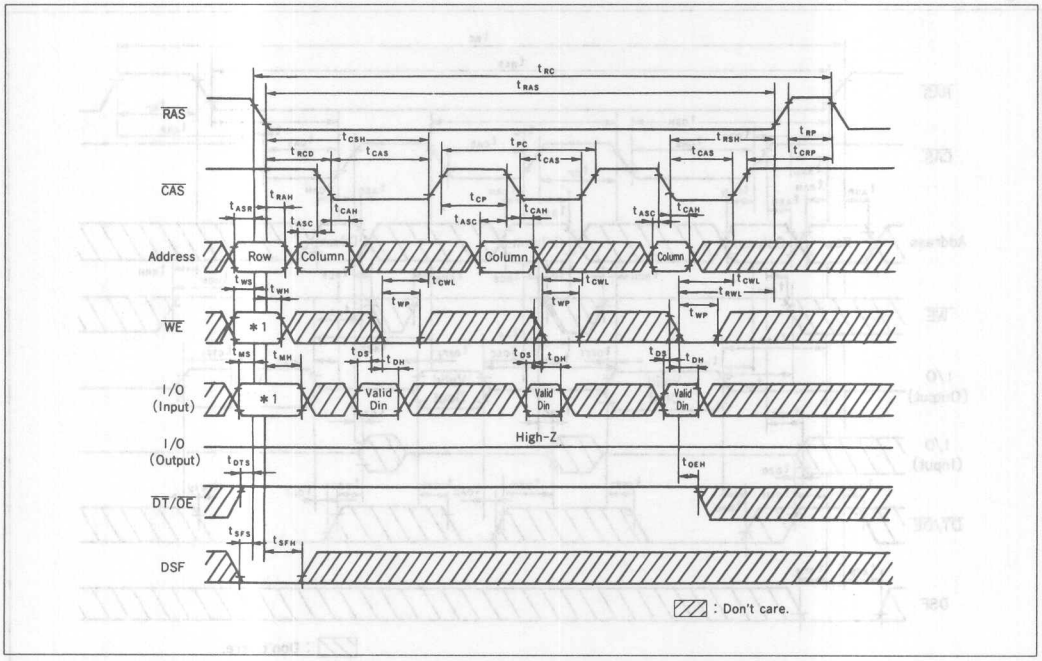


Page Mode Write Cycle (Early Write)



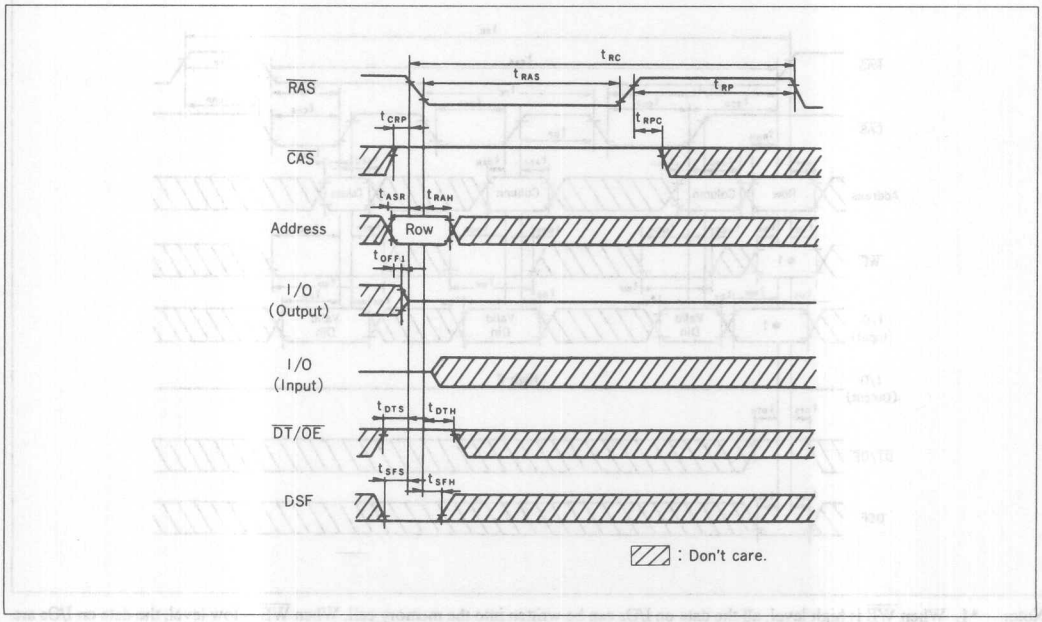
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)



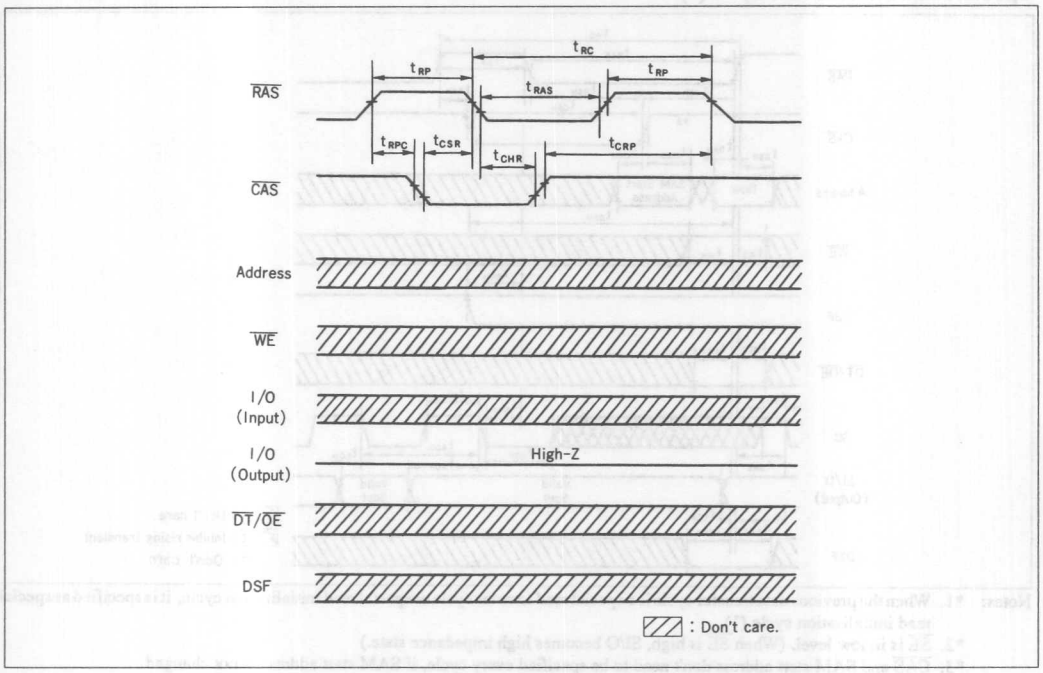
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

$\overline{RAS}$-Only Refresh Cycle

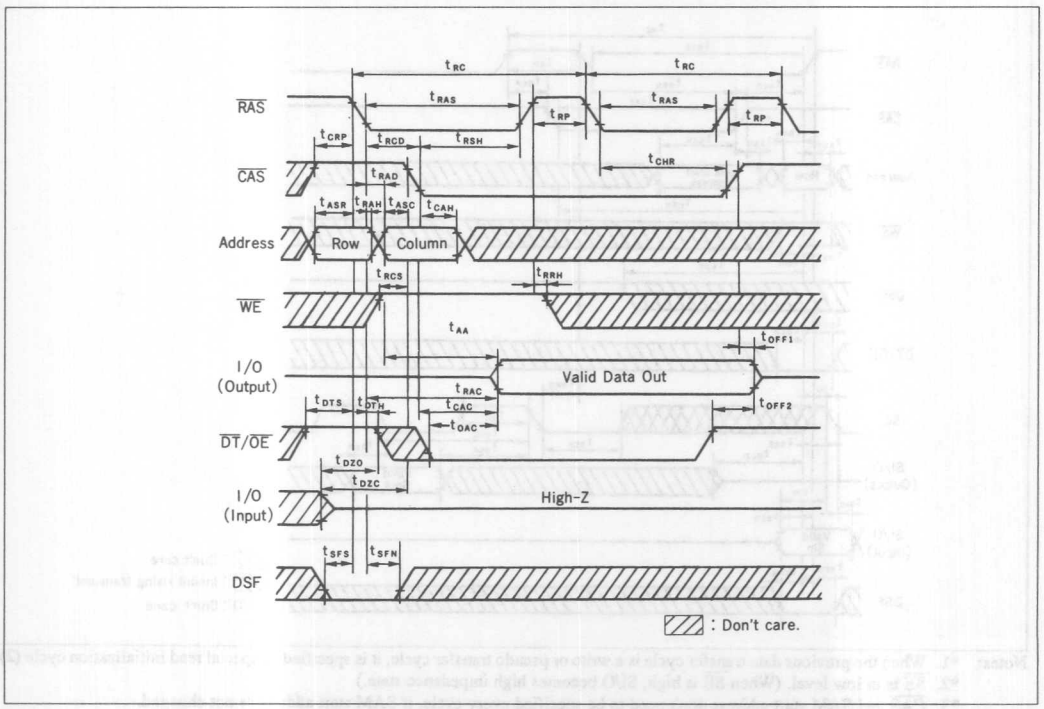


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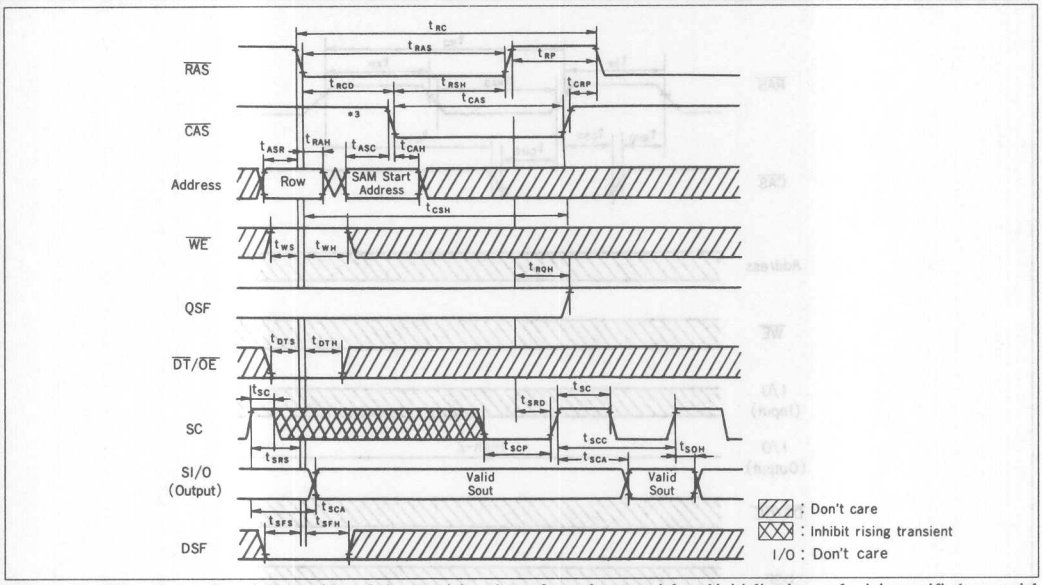
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle

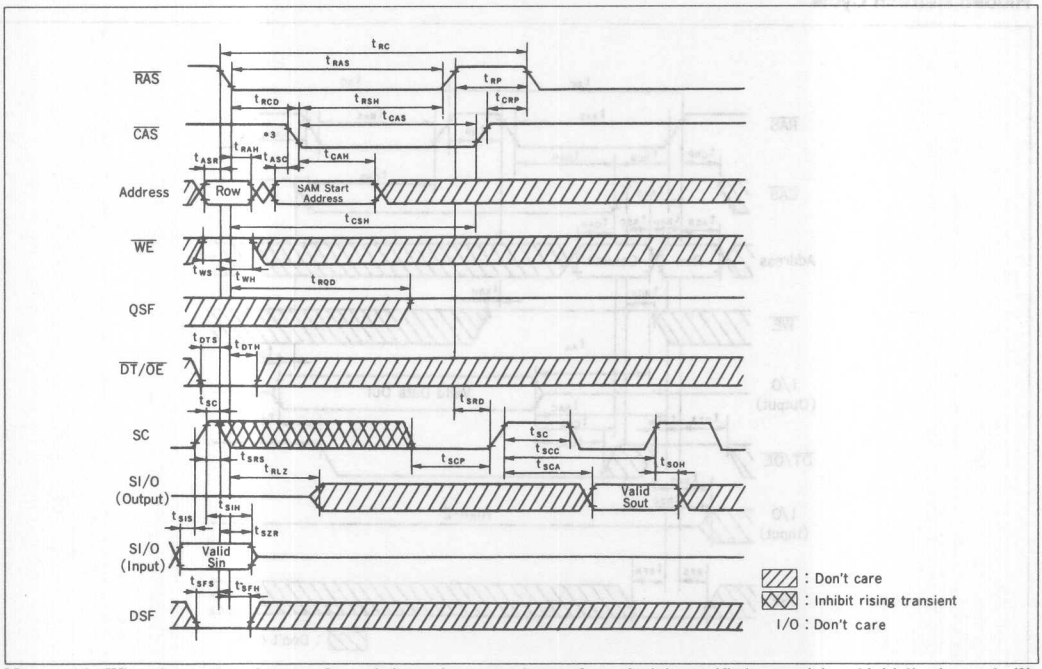


Special Read Initialization Cycle (1) *1, *2



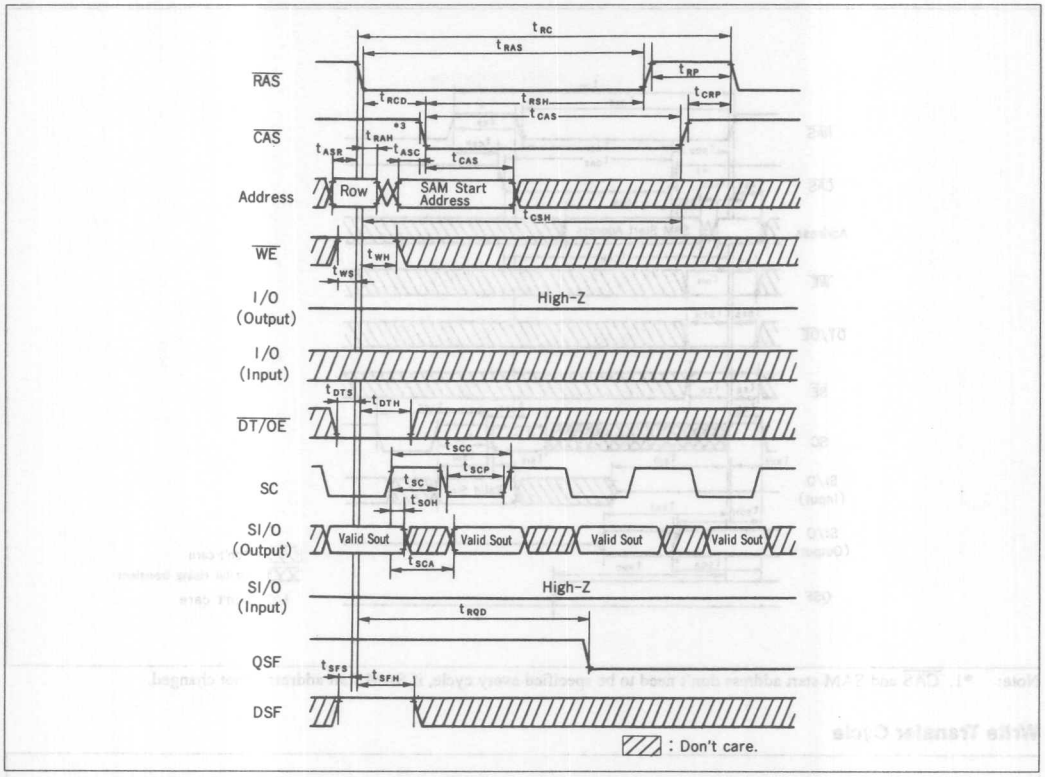
Notes: *1. When the previous data transfer cycle is a special read transfer cycle or special read initialization cycle, it is specified as special read initialization cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Special Read Initialization Cycle (2) *1, *2



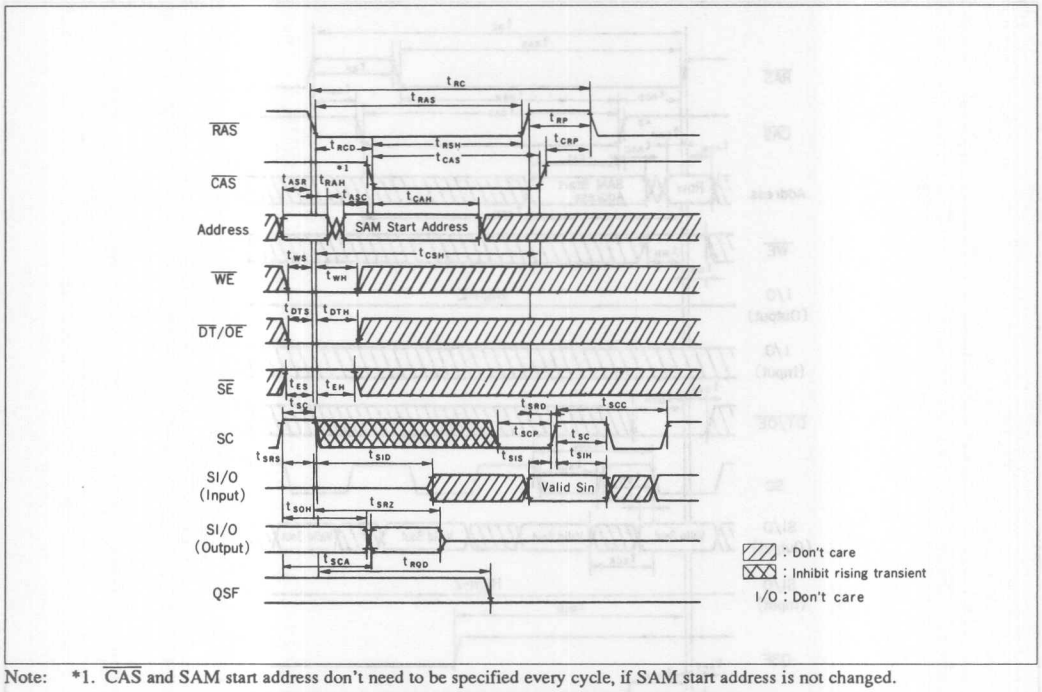
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is specified as special read initialization cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Special Read Transfer Cycle *1, *2



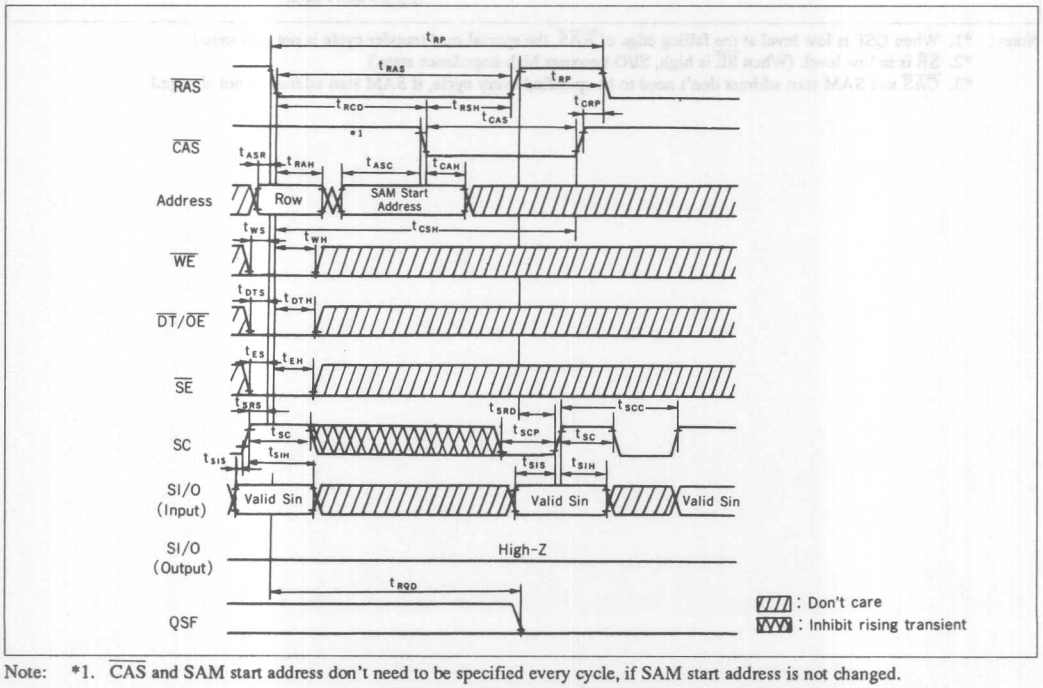
Notes: *1. When QSF is low level at the falling edge of $\overline{RAS}$, the special read transfer cycle is not performed.
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Pseudo Transfer Cycle



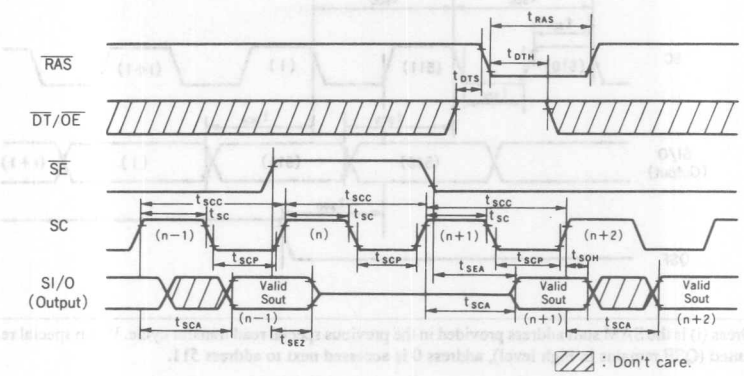
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Write Transfer Cycle

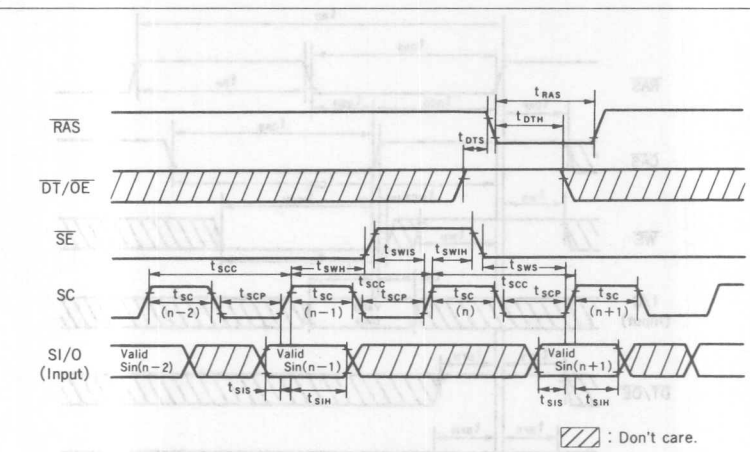


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

Serial Read Cycle

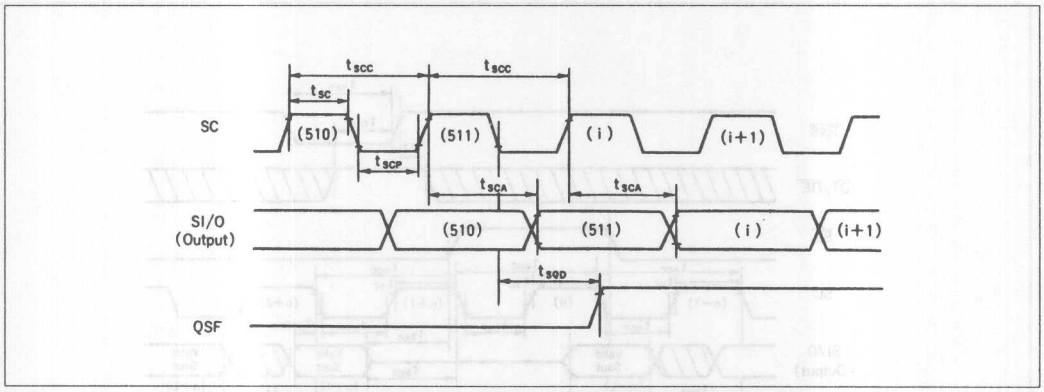


Serial Write Cycle



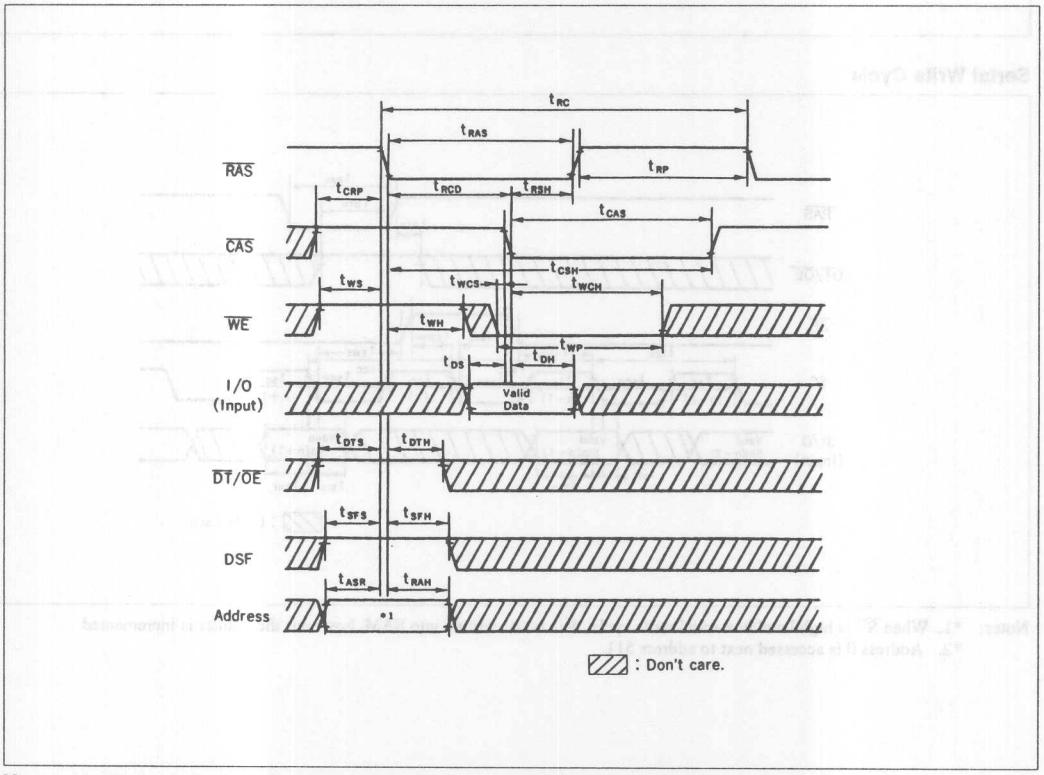
Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

Serial Read Cycle (Around Address 511 in SAM)



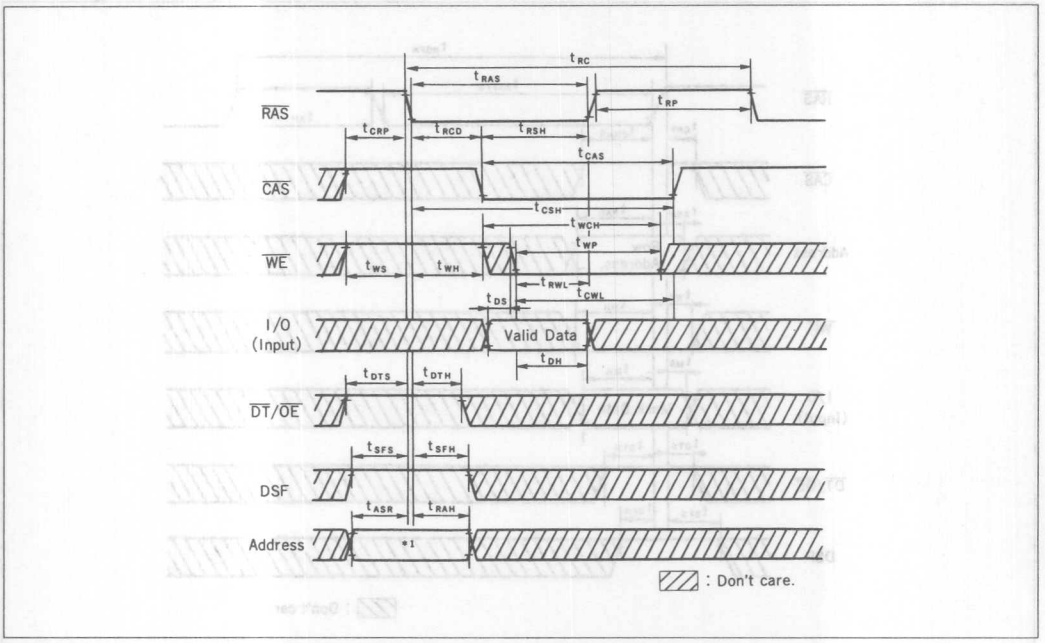
Note *1. Address (i) is the SAM start address provided in the previous special read transfer cycle. When special read transfer cycle isn't executed (QSF remains in high level), address 0 is accessed next to address 511.

Color Register Set Cycle (Early Write)



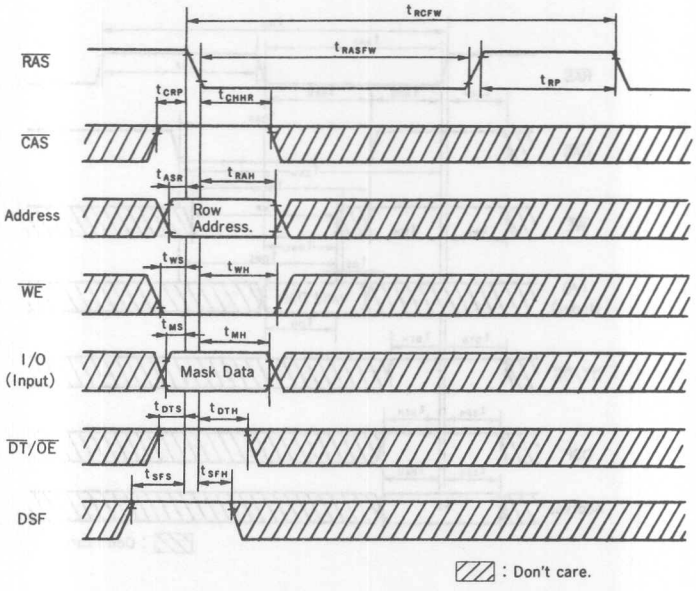
Note: *1. The level of address pin is don't care, but cannot be changed in this period.

Color Register Set Cycle (Delayed Write)



Note: *1. The level of address pin is don't care, but cannot be changed in this period.

Flash Write Cycle



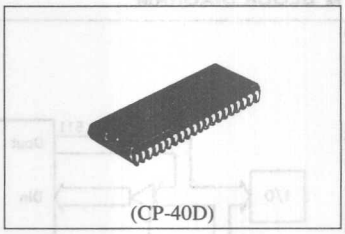
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HM538121JP/ZP-10/12/15 — Preliminary

131,072 × 8-Bit Multiport CMOS Video Random Access Memory

■ DESCRIPTION

The HM538121 is a 1-Mbit multiport video RAM equipped with a 128-kword × 8-bit dynamic RAM and a 256-word × 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory.



(CP-40D)

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM . . . . . .128-kword × 8-Bit
  - SAM . . . . . .256-word × 8-Bit
- Access Time . . . . . .RAM: 100/120/150ns (max.)
  - SAM: 30/40/50ns (max.)
- Cycle Time . . . . . .RAM: 190/220/260ns (min.)
  - SAM: 30/40/60ns (min.)
- Low Power
  - Active . . . . . .RAM: 385mW (max.)
  - SAM: 275mW (max.)
  - Standby . . . . . 40mW (max.)
- High Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle Between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8ms/512 Cycles)
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access	Package
HM538121JP-10	100ns	400-mil 40-pin Plastic SOJ (CP-40D)
HM538121JP-12	120ns	
HM538121JP-15	150ns	

■ PIN ARRANGEMENT

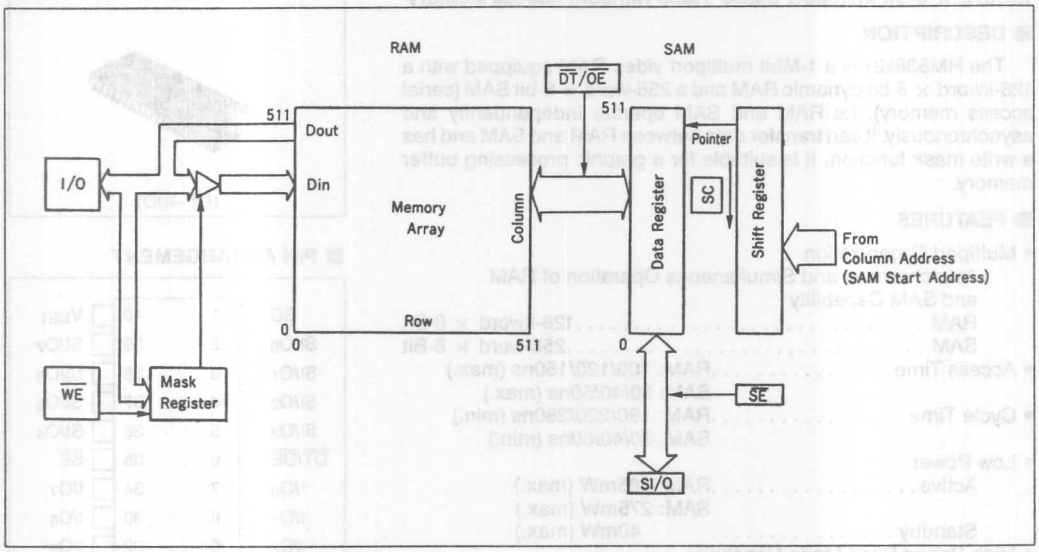


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/ Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	Non Connection

■ BLOCK DIAGRAM



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538121.

Table 1. Operation Cycles of the HM538121

Input Level at the Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	X	X	CBR Refresh

NOTE: X = Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of RAS and after. When WE is low at the falling edge of $\overline{RAS}$, the HM538121 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

OPERATION OF HM538121

Operation of RAM Port

RAM Read cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (tAA) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min.) and t_{AWD} (min.) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of RAS)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max. (10 μs).

- **Transfer Operation**

HM538121 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
  (a) Read transfer cycle: RAM → SAM
  (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
  Read transfer cycle: SI/O output
  Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of RAS)

This cycle becomes read transfer cycle by setting $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (256 × 8 bit) determined by this cycle is transferred synchronously at the rising of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address decided by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min.) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min.) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

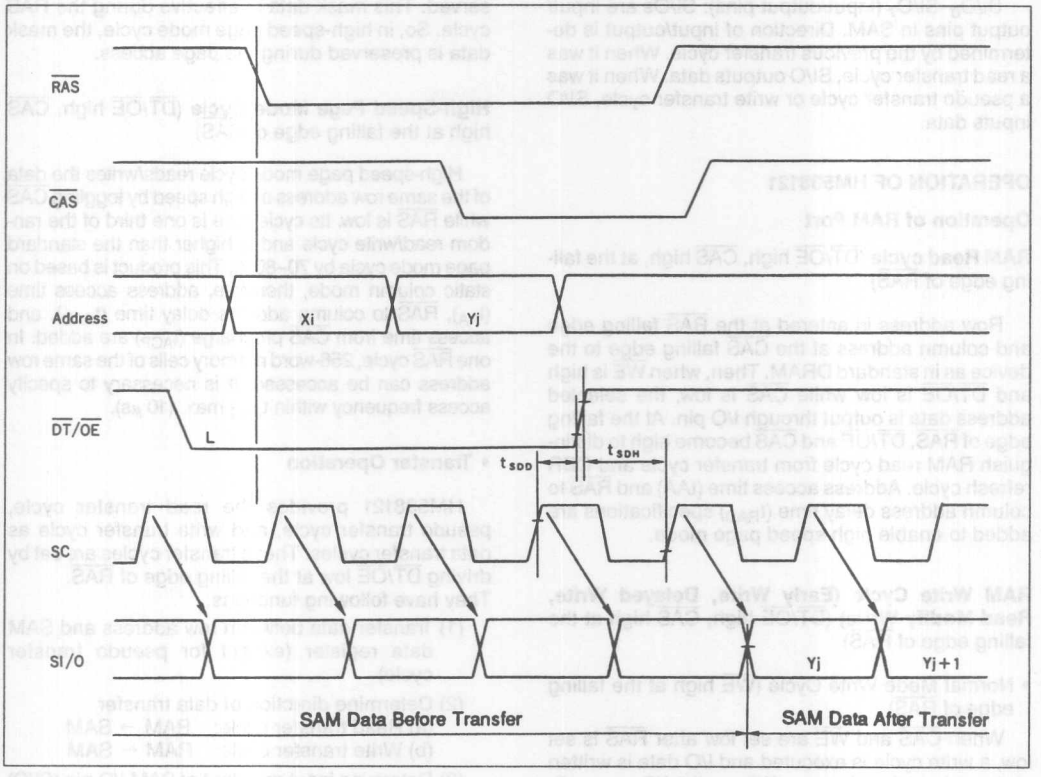


Figure 1. Real Time Read Transfer

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If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data is output after t_{RLZ} (min.) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max.) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min.) to avoid data contention. SAM access becomes enabled after t_{SRD} (min.) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min.) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

■ SAM PORT OPERATION

• Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

• Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

■ REFRESH

• RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$-only refresh cycles because $\overline{CAS}$ circuits don't operate..

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

• SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	−1.0 to +7.0	V
Power Supply Voltage(1)	V_{CC}	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: 1. Relative to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage(1)	V_{IH}	2.4	—	6.5	V
Input Low Voltage(1)	V_{IL}	−0.5(2)	—	0.8	V

NOTES: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	Test Conditions		HM538121-10		HM538121-12		HM538121-15		Unit
		RAM Port	SAM Port	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	SC, $\overline{SE}$ = V_{IH}	—	70	—	60	—	50	mA
	I_{CC7}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	120	—	100	—	80	mA
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC, $\overline{SE}$ = V_{IH}	—	7	—	7	—	7	mA
	I_{CC8}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	50	—	40	—	30	mA
$\overline{RAS}$-Only Refresh Current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	SC, $\overline{SE}$ = V_{IH}	—	60	—	50	—	40	mA
	I_{CC9}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	110	—	90	—	70	mA
Page Mode Current	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min.	SC, $\overline{SE}$ = V_{IH}	—	65	—	55	—	45	mA
	I_{CC10}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	115	—	95	—	75	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC5}	$\overline{RAS}$ Cycling t_{RC} = Min.	SC, $\overline{SE}$ = V_{IH}	—	60	—	50	—	40	mA
	I_{CC11}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	110	—	90	—	70	mA
Data Transfer Current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	SC, $\overline{SE}$ = V_{IH}	—	90	—	90	—	90	mA
	I_{CC12}		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min.	—	125	—	125	—	125	mA
Input Leakage Current	I_{LI}			−10	10	−10	10	−10	10	μA
Output Leakage Current	I_{LO}			−10	10	−10	10	−10	10	μA
Output High Voltage	V_{OH}	I_{OH} = −2mA		2.4	—	2.4	—	2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA		—	0.4	—	0.4	—	0.4	V

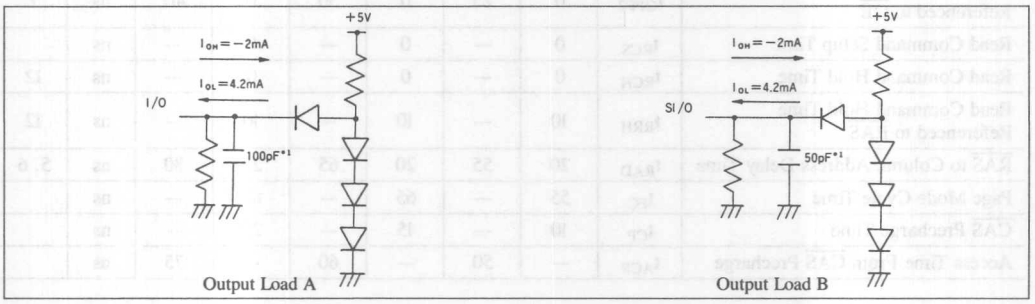
■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V, f = 1MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Address	C_{I1}	—	—	5	pF
Clocks	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (I), (II)

• Test Conditions

- Input Rise and Fall Time: 5ns
- Output Load: See Figures
- Input Timing Reference Levels: 0.8V, 2.4V
- Output Timing Reference Levels: 0.4V, 2.4V



*Including scope and jig.

• Common Parameter

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
DT to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
Data-In to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
Data-In to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	

• Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn Off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	7
Output Buffer Turn Off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	60	—	75	ns	

• Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-In Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	

• Read-Modify-Write Cycle

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Modify Write Cycle Time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-In Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-Off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-In Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

• Refresh Cycle

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Transfer Cycle

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{DT}$ Hold Time from $\overline{RAS}$	t_{RDH}	TBD	—	TBD	—	TBD	—	ns	
$\overline{DT}$ Hold Time from $\overline{CAS}$	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	TBD	—	TBD	—	TBD	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	ns	
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	30	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	30	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-Off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Serial Data Out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-In Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-In Hold Time	t_{SIH}	15	—	20	—	25	—	ns	

• Serial Read Cycle

Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	40	ns	4
Serial Data-Out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-Off Delay from $\overline{SE}$	t_{SEZ}	0	25	0	25	0	30	ns	7

• Serial Write Cycle

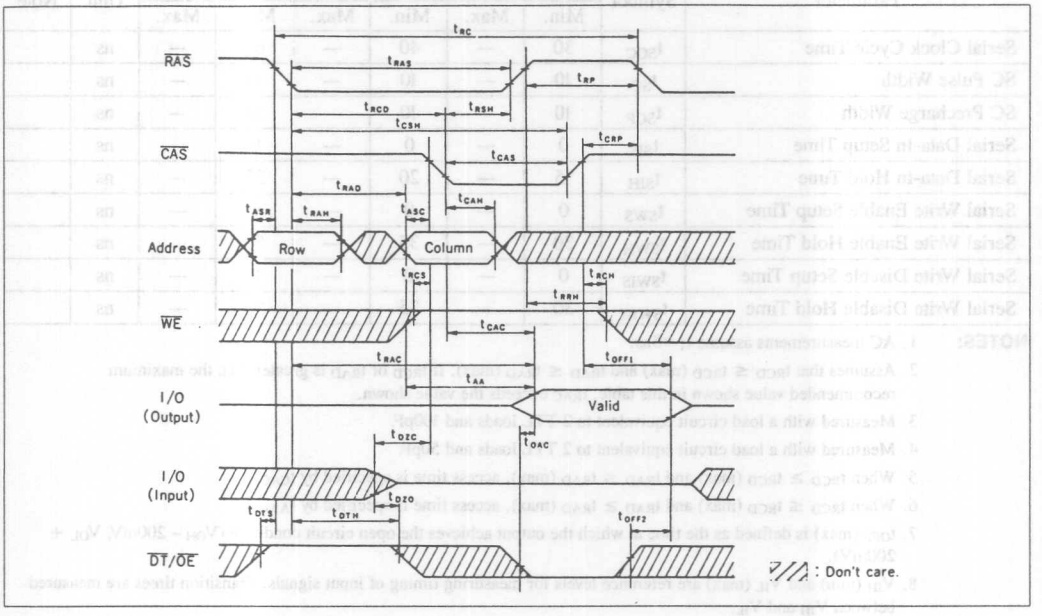
Parameter	Symbol	HM538121-10		HM538121-12		HM538121-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-In Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-In Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	50	—	ns	

NOTES:

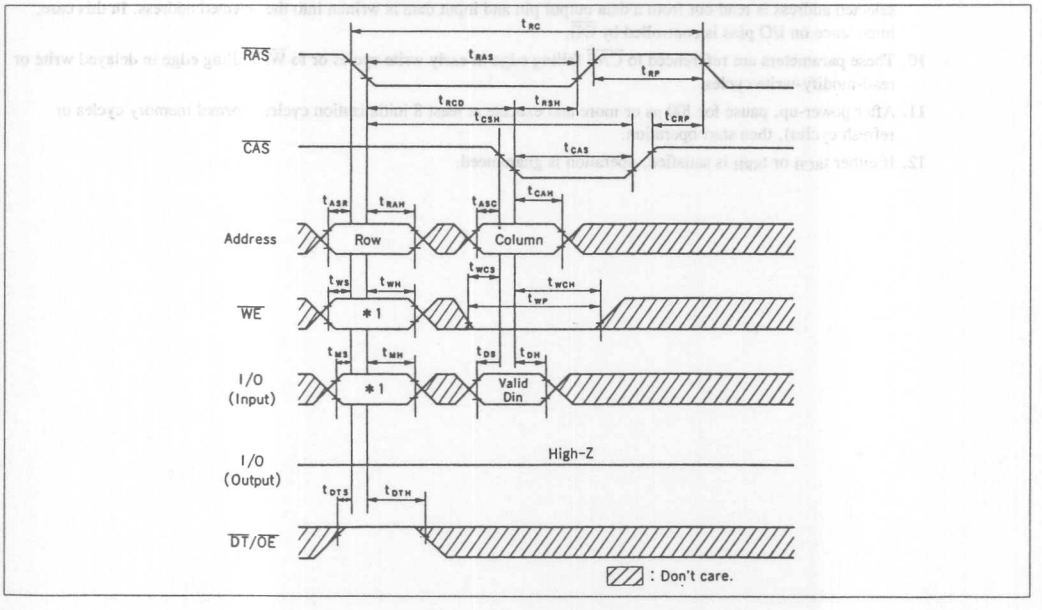
1. AC measurements assume $t_T = 5$ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200mV, V_{OL} + 200mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

■ TIMING WAVEFORMS

• Read Cycle

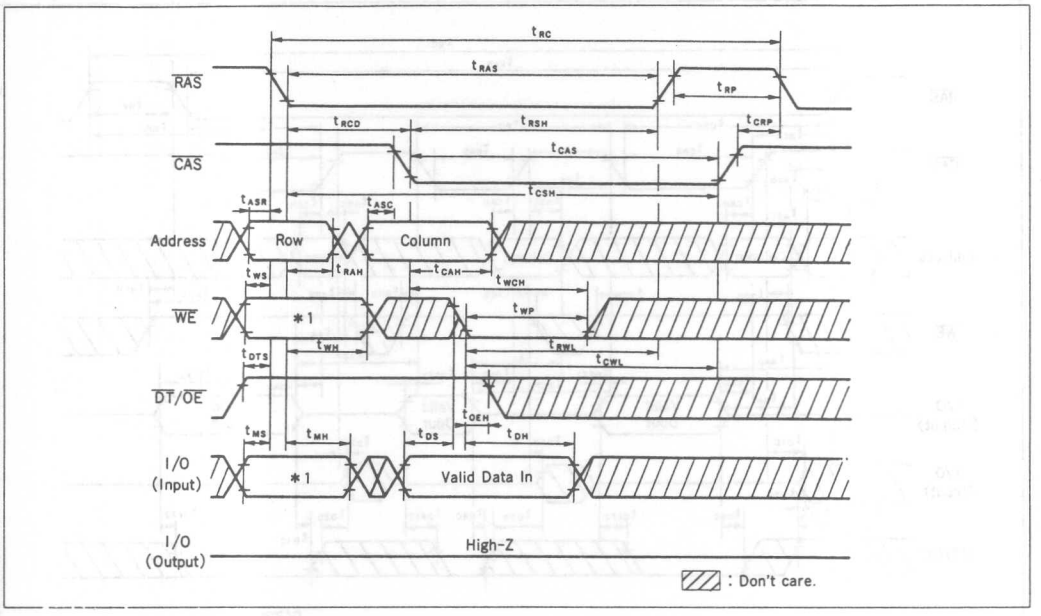


• Early Write Cycle



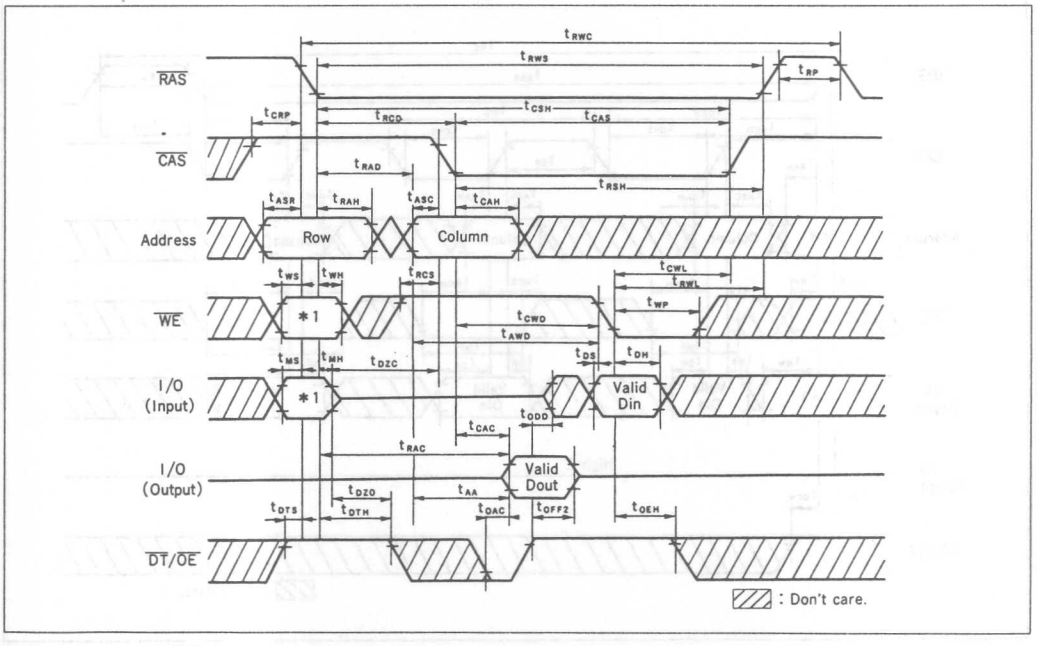
NOTE: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



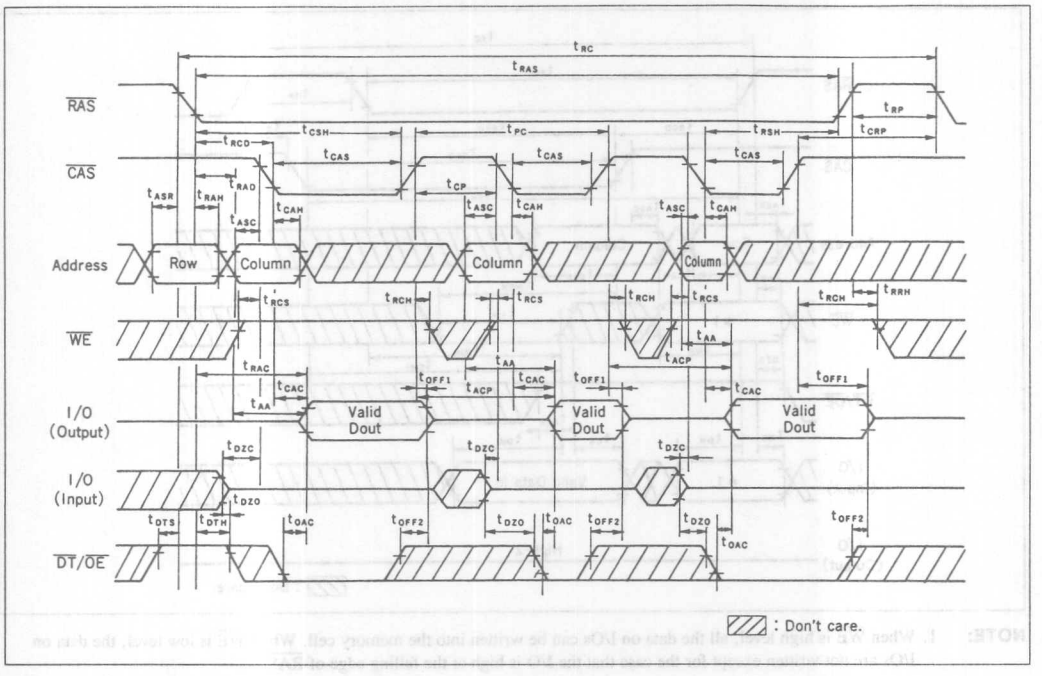
NOTE: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

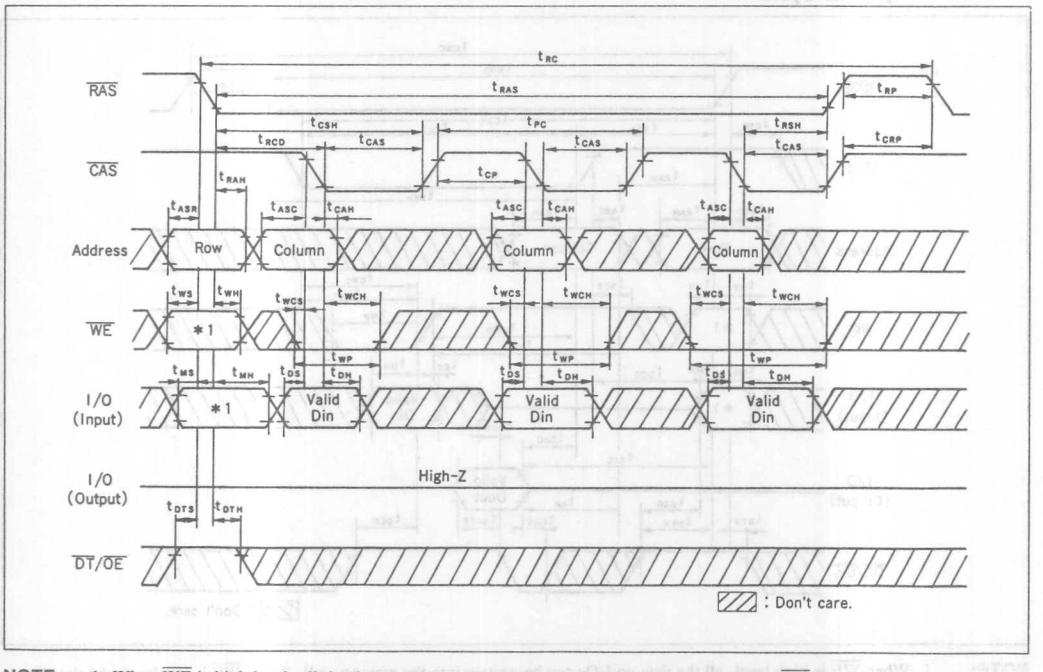


NOTE: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Read Cycle



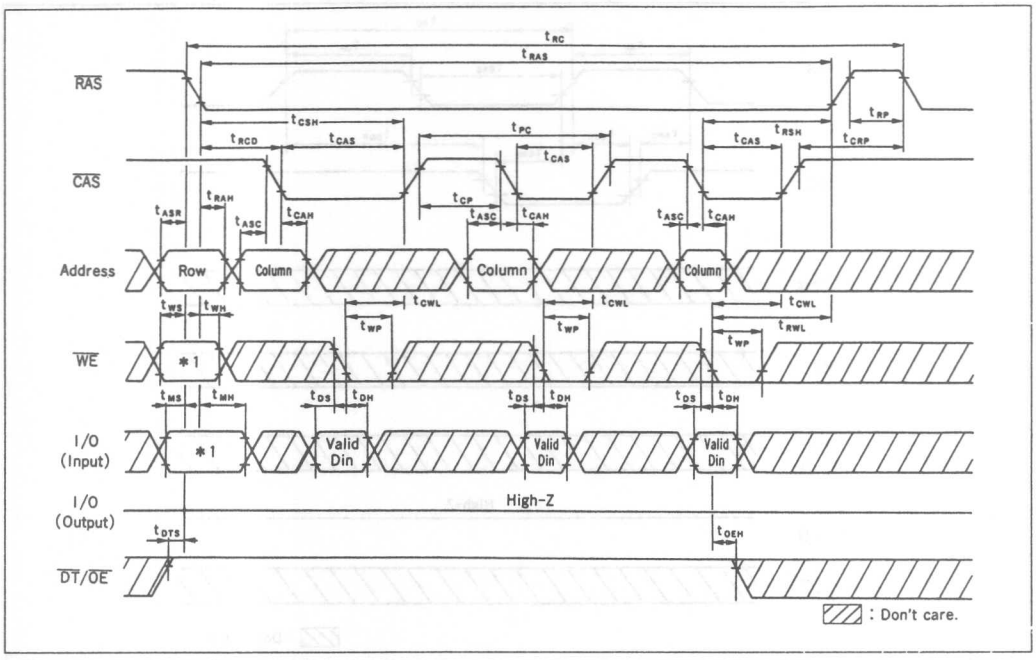
• Page Mode Write Cycle (Early Write)



NOTE: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

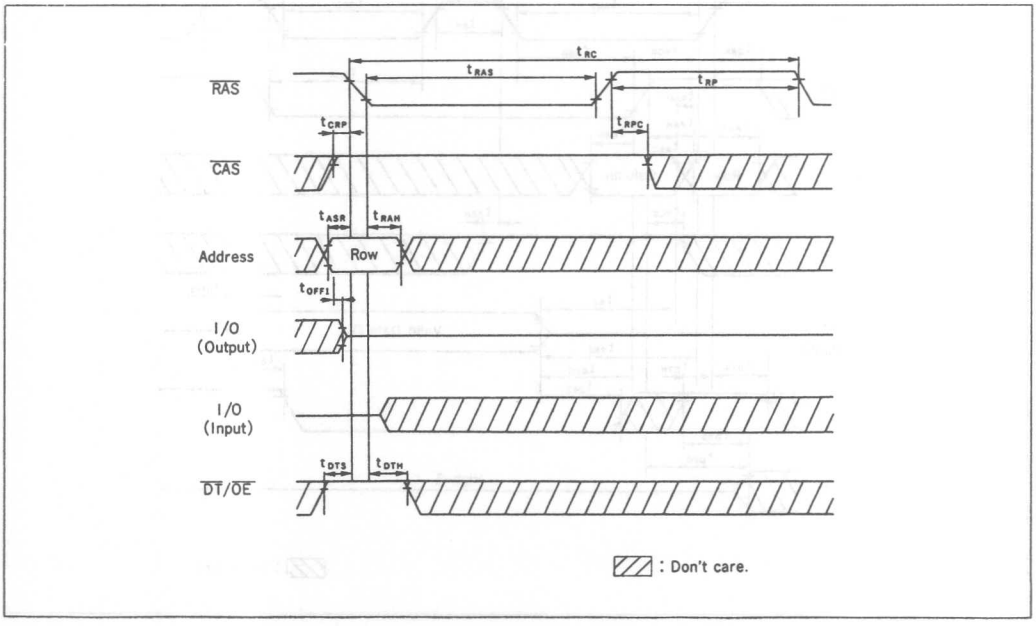
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• Page Mode Write Cycle (Delayed Write)

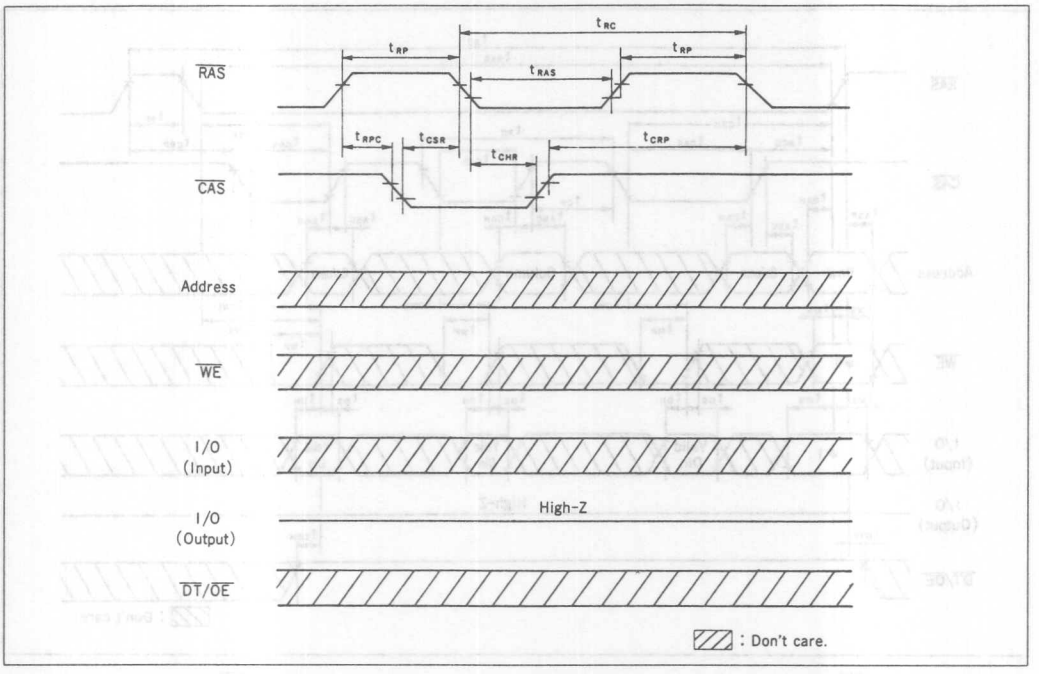


NOTE: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

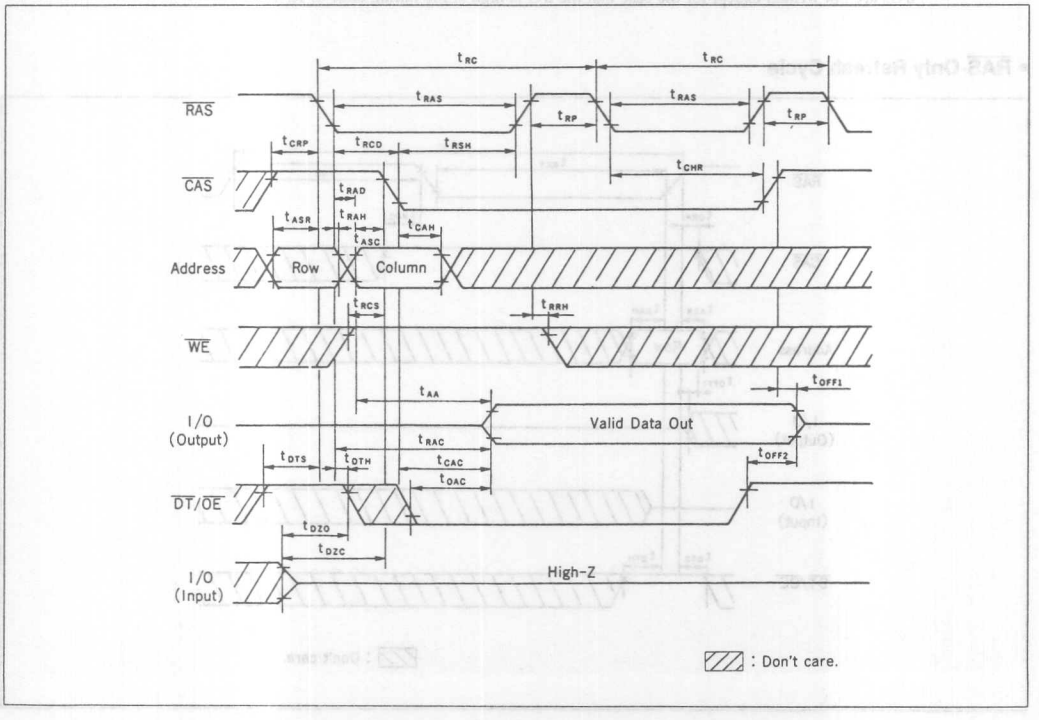
• $\overline{RAS}$-Only Refresh Cycle



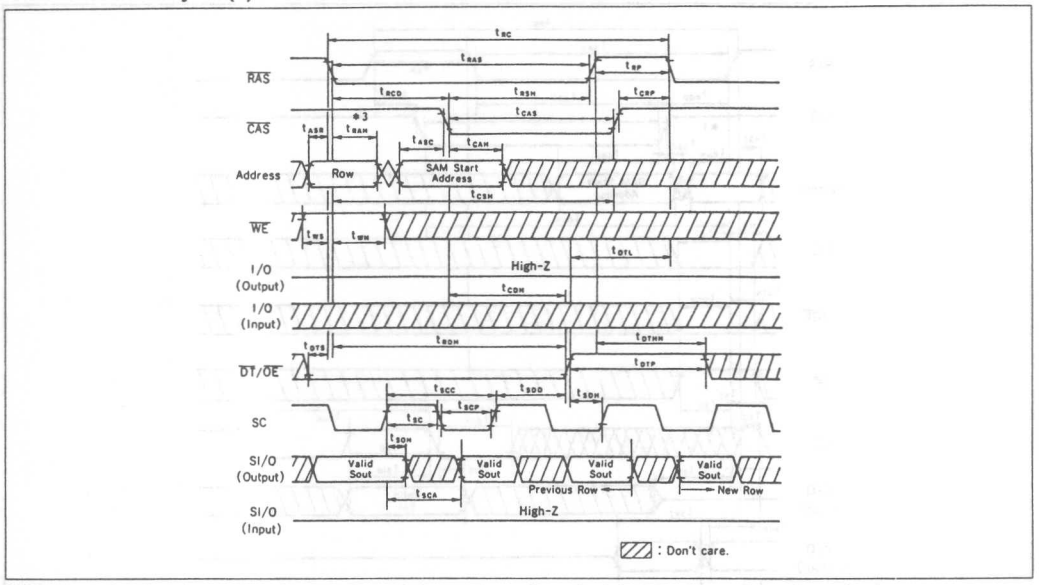
• **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle**



• **Hidden Refresh Cycle**

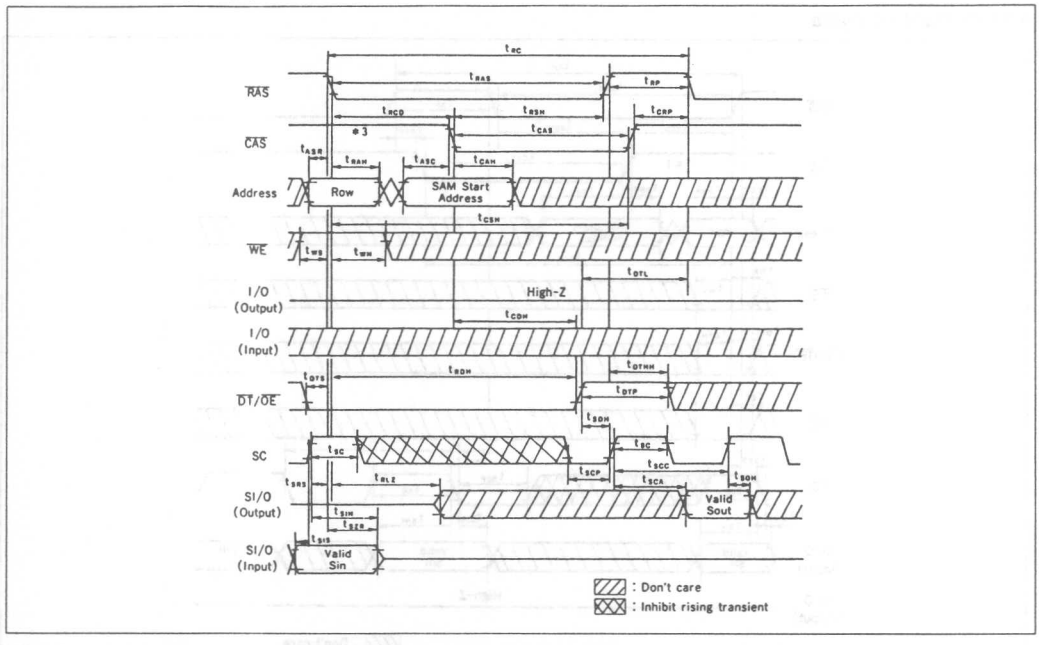


• Read Transfer Cycle (1) (1), (2)



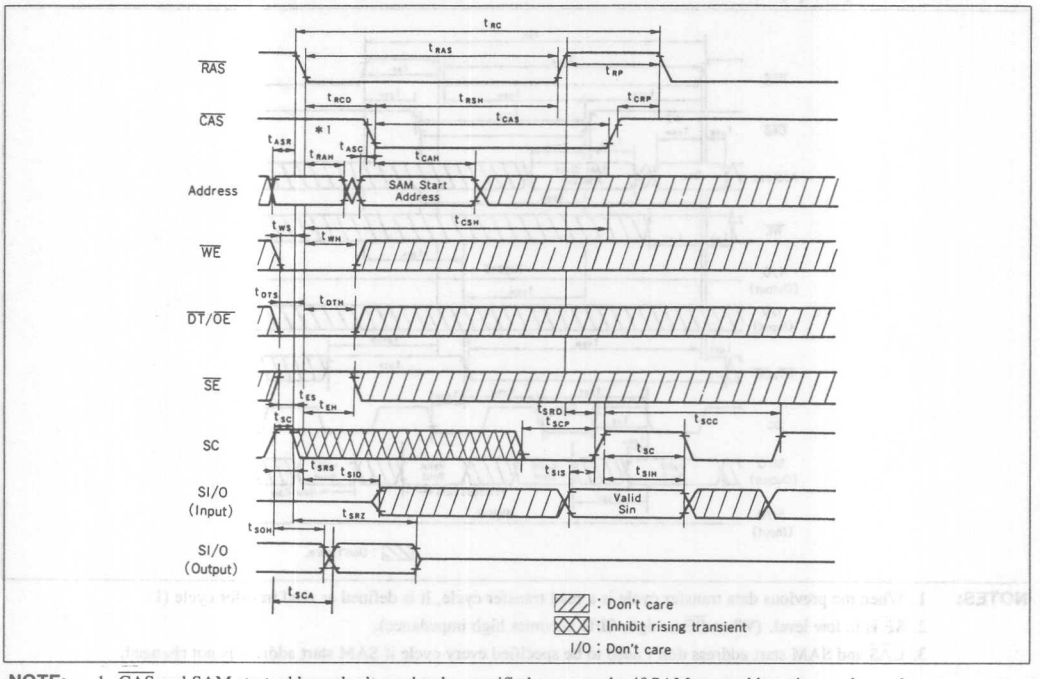
NOTES:
1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance).
3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle if SAM start address is not changed.

• Read Transfer Cycle (2) (1), (2)



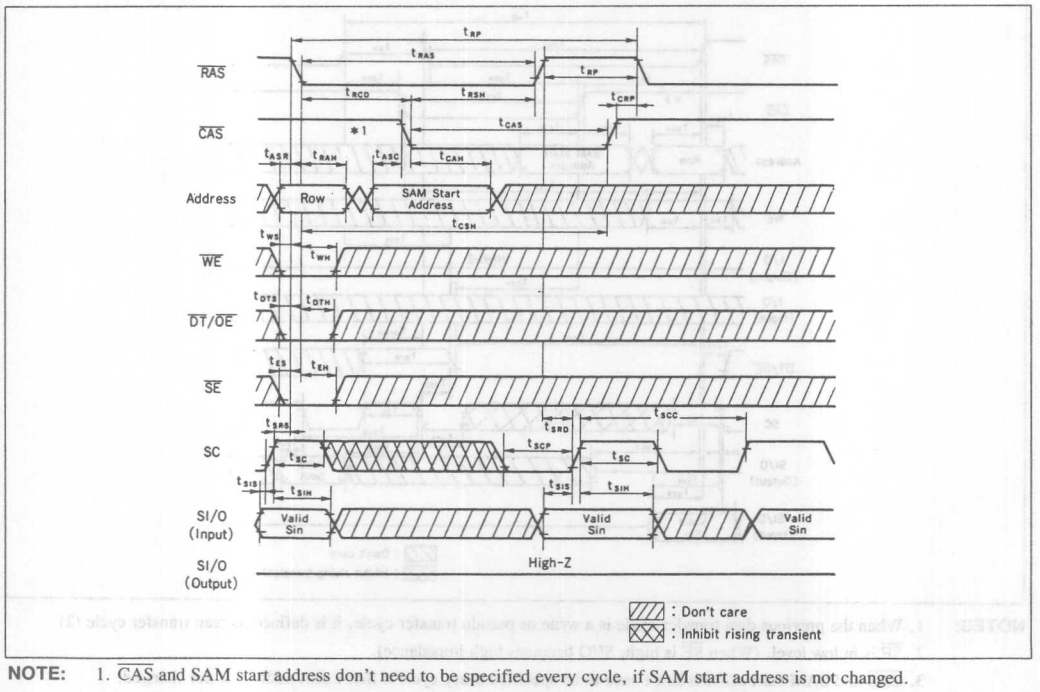
NOTES:
1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance).
3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle if SAM start address is not changed.

• **Pseudo Transfer Cycle**



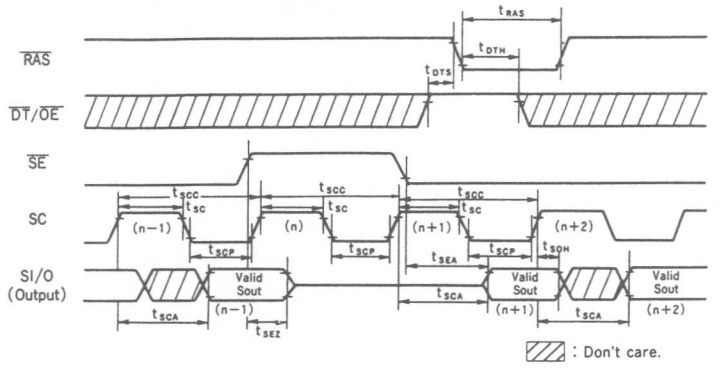
NOTE: 1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Write Transfer Cycle**

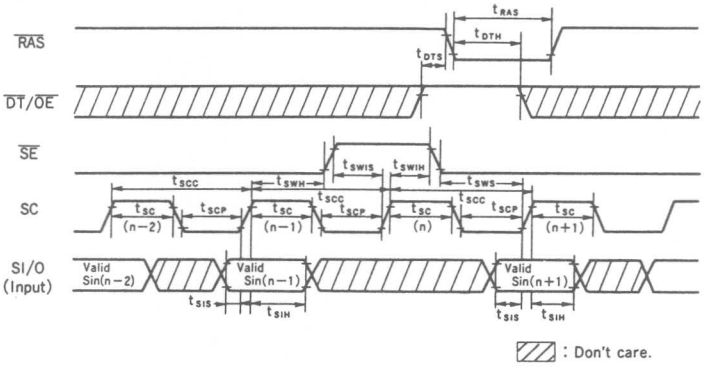


NOTE: 1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Serial Read Cycle**



• **Serial Write Cycle**



NOTES: 1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
2. Address 0 is accessed next to address 255.

Section 5
MOS Dynamic RAM

5

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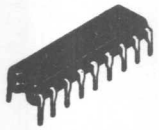
HM50464 Series

65536-word x 4-bit Dynamic Random Access Memory

■ FEATURES

- Page mode capability
- Single 5V (±10%)
- On chip substrate bias generator
- Low power: 350 mW active, 20 mW standby
- High speed: Access Time 120ns/150ns/200ns
- Output data controlled by $\overline{CAS}$ or $\overline{OE}$
- TTL compatible
- 256 refresh cycles . . . . . 4 ms
- 3 variations of refresh . . . . . $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

HM50464P Series



(DP-18B)

HM50464CP Series

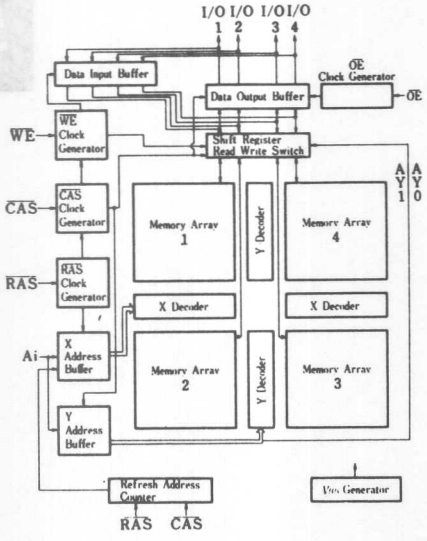


(CP-18)

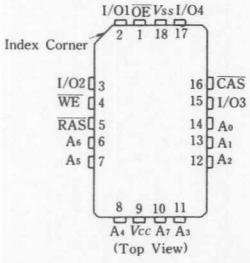
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM50464P-12	120ns	300 mil 18 pin Plastic DIP
HM50464P-15	150ns	
HM50464P-20	200ns	
HM50464CP-12	120ns	18 pin PLCC
HM50464CP-15	150ns	
HM50464CP-20	200ns	

■ BLOCK DIAGRAM



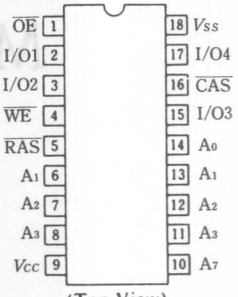
● HM50464CP Series



(Top View)

■ PIN ARRANGEMENT

● HM50464P Series



(Top View)

$A_0 - A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1 – I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_7$ (Row)	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature (Ambient)	*Topr*	0 to +70	°C
Storage Temperature (Ambient)	*Tstg*	−55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	*Iout*	50	mA

■ RECOMMENDED DC OPERATING CONDITION (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	–	6.5	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, Vss = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current (t_{RC} = min.)	I_{CC1}	–	83	–	70	–	55	mA	1
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Disable)	I_{CC2}	–	4.5	–	4.5	–	4.5	mA	
Refresh Current ($\overline{RAS}$ only refresh, t_{RC} = min.)	I_{CC3}	–	62	–	53	–	42	mA	
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Enable)	I_{CC5}	–	10	–	10	–	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min.)	I_{CC6}	–	69	–	58	–	45	mA	1
Operating Current (Page mode, t_{PC} = min.)	I_{CC7}	–	57	–	48	–	37	mA	1
Input Leakage Current (0 < *Vin* < 7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage Current (0 < *Vout* < 7V, Dout = Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output High Voltage (*Iout* = −5 mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage (*Iout* = 4.2 mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	*CI1*	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	*CI2*	–	10	pF	1
Output Capacitance	Data In/Data Out	*CI/O*	–	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Vcc = 5V ± 10%, Vss = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	30	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	–	260	–	330	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	

(to be continued)

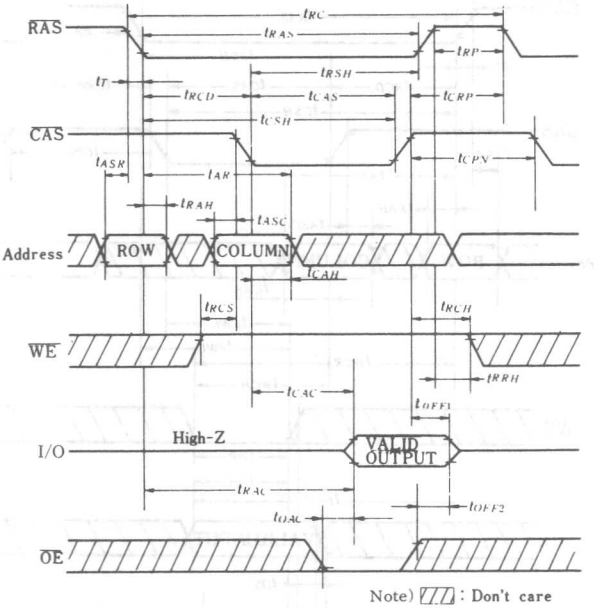
Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	–	100	–	130	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	40	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	40	–	45	–	55	–	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
Read-Write Cycle Time	t_{RWC}	305	–	360	–	450	–	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	100	–	125	–	160	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	160	–	200	–	260	–	ns	8
$\overline{CAS}$ Precharge Time	t_{CPN}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	120	–	150	–	200	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	45	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	30	–	40	–	50	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	30	–	40	–	50	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	25	–	30	–	40	–	ns	
Page Mode Cycle Time	t_{PC}	120	–	145	–	190	–	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Read-modify-write Cycle Time (Page-mode)	t_{PCM}	205	–	245	–	310	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assume that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
11. Minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh is required before using internal refresh counter.
12. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

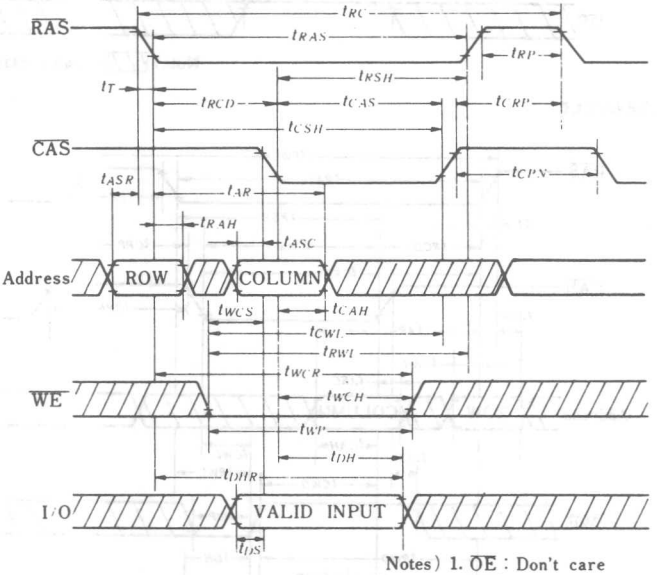
■ TIMING WAVEFORMS

• READ CYCLE



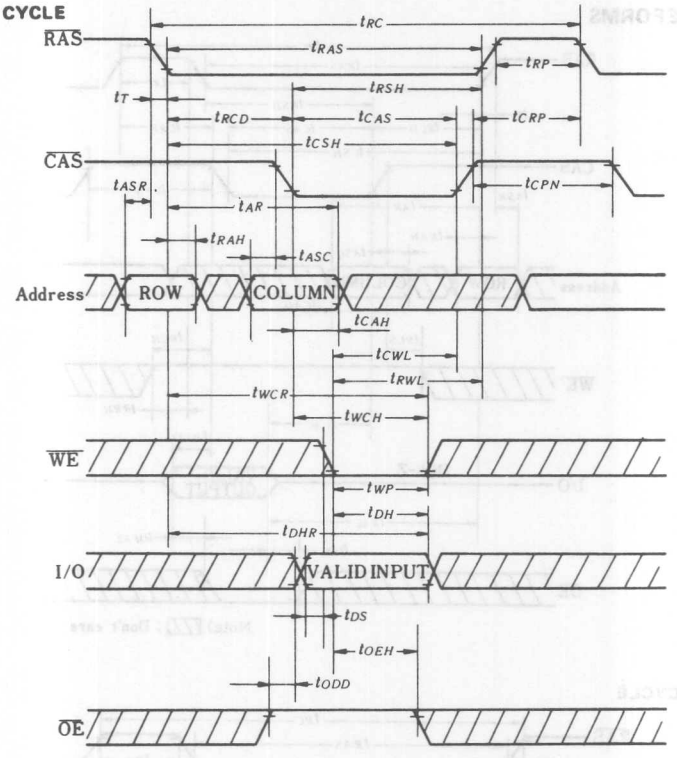
Note) ▨ : Don't care

• EARLY WRITE CYCLE



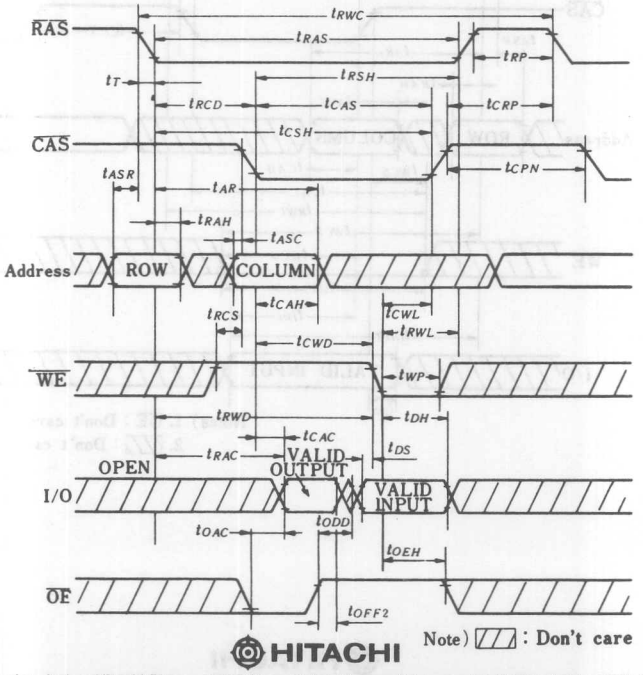
Notes) 1. $\overline{OE}$: Don't care
2. ▨ : Don't care

- **DELAYED WRITE CYCLE**



Note) ▨ : Don't care

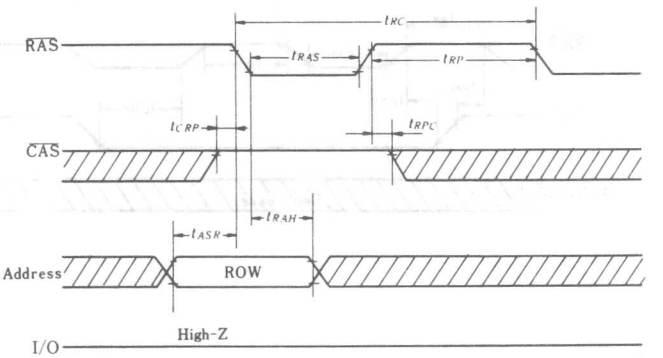
- **READ MODIFY WRITE CYCLE**



Note) ▨ : Don't care

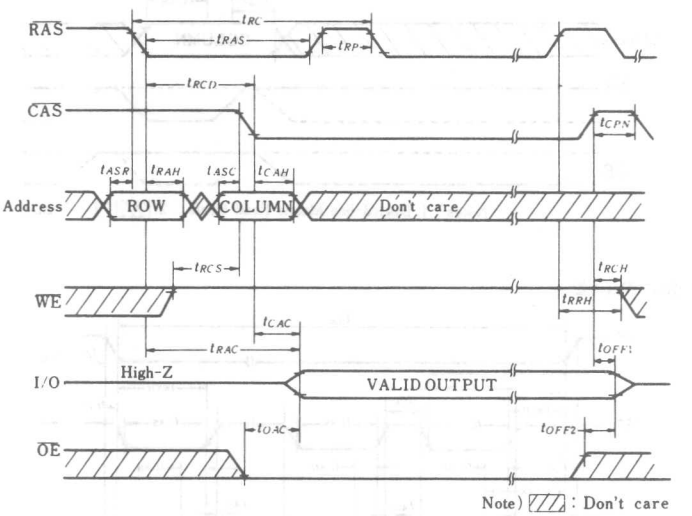
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- **$\overline{RAS}$ ONLY REFRESH CYCLE**



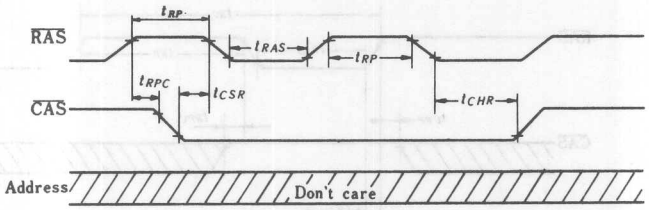
Notes) 1. $\overline{OE}$, $\overline{WE}$: Don't care
2. ▨ : Don't care

- **HIDDEN REFRESH CYCLE**

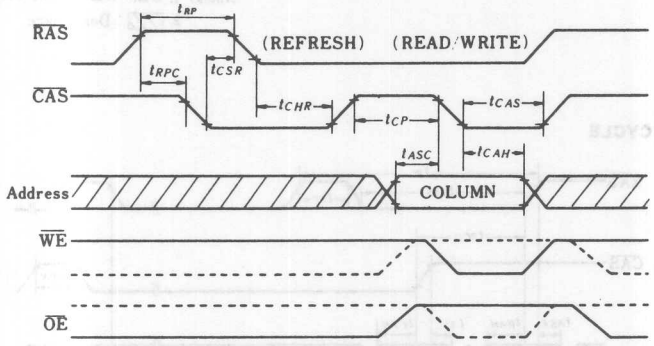


Note) ▨ : Don't care

- **$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE**

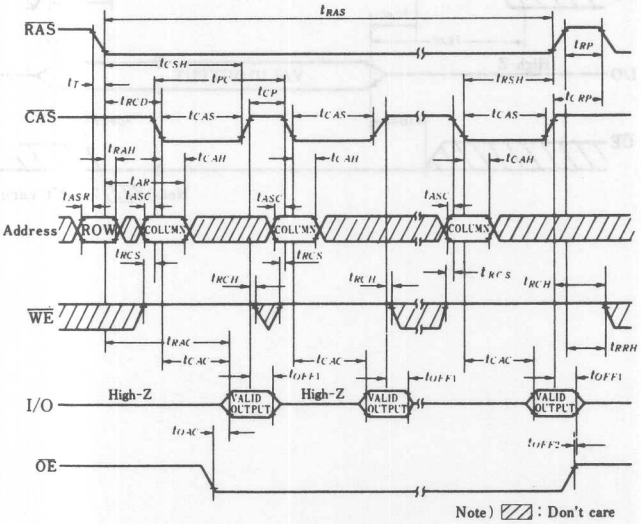


- **COUNTER TEST**



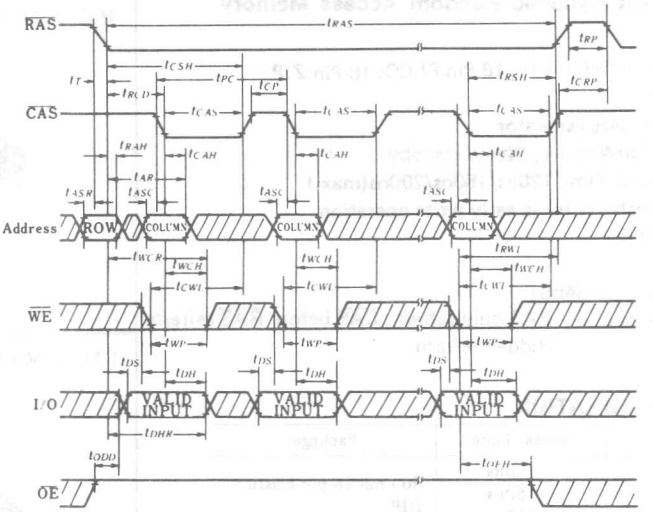
Notes) 1. Dotted-line Means Read Cycle. 2. ▨ : Don't care

- **PAGE MODE READ CYCLE**



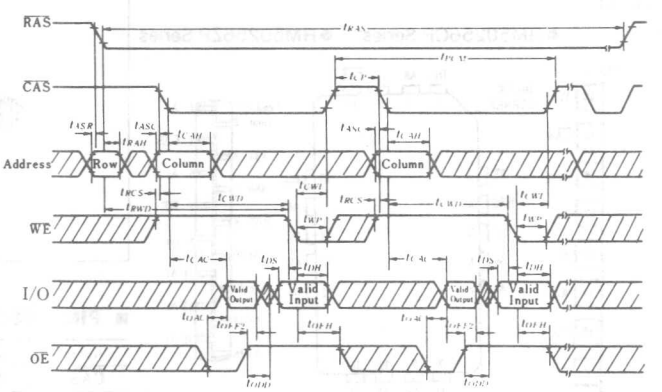
Note) ▨ : Don't care

- **PAGE MODE WRITE CYCLE**



Note) ▨ : Don't care

- **PAGE MODE READ MODIFY WRITE CYCLE**



Note) ▨ : Don't care

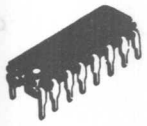
HM50256 Series

262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

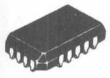
- Industry Standard 16-Pin DIP, 18-Pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles · · · (4ms)
- 3 variations of refresh · · · $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

HM50256P Series



(DP-16B)

HM50256CP Series



(CP-18)

HM50256ZP Series



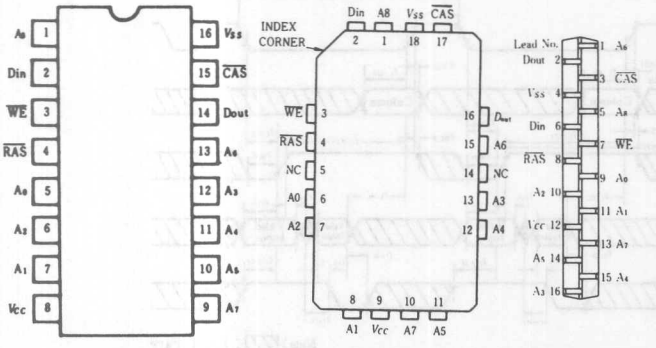
(ZP-16)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM50256P-12 HM50256P-15 HM50256P-20	120ns 150ns 200ns	300 mil 16 pin Plastic DIP
HM50256ZP-12 HM50256ZP-15 HM50256ZP-20	120ns 150ns 200ns	16 pin Plastic ZIP
HM50256CP-12 HM50256CP-15 HM50256CP-20	120ns 150ns 200ns	18 pin PLCC

■ PIN ARRANGEMENT

● HM50256P Series ● HM50256CP Series ● HM50256ZP Series

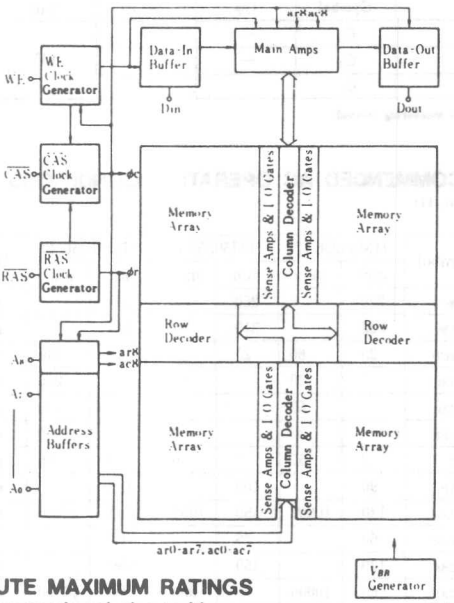


(Top View) (Top View) (Bottom View)

■ PIN DESCRIPTION

A_0~A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0~A_7	Refresh Address Inputs

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . −55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$, $\overline{CAS}$ =Cycling : t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current($\overline{RAS}$=V_{IH}, Dout =Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Page Mode Supply Current($\overline{RAS}$=V_{IL}, $\overline{CAS}$ =Cycling, t_{PC}=min)	I_{CC7}	—	57	—	48	—	37	mA	
Input leakage(0<V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage(0<V_{out}<7V, Dout=Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7		1, 2
Output Capacitance	Data-out	C_O		7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1], [10], [11]

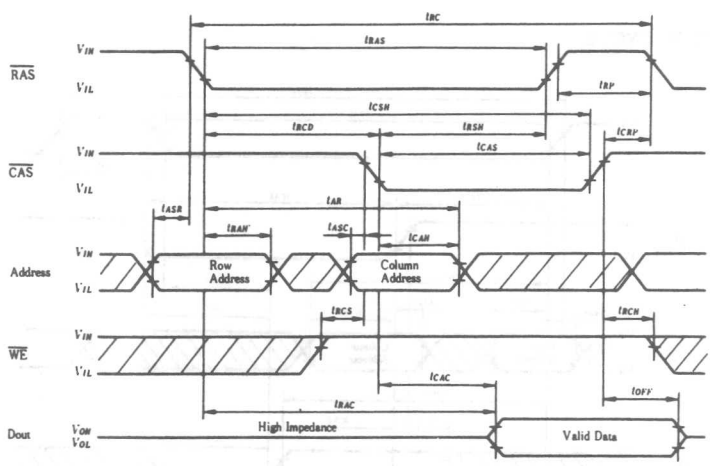
Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	220		260		330		ns	
Read-Write Cycle Time	t_{RWC}	265		310		390		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
Access Time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}		30		40		50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		120		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120		150		200		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	
Row Address Set-up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		20		ns	
Column Address Set-up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	20		25		30		ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read Command Set-up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Write Command Set-up Time	t_{WCS}	0		0		0		ns	8
Write Command Hold Time	t_{WCH}	40		45		55		ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100		120		155		ns	
Write Command Pulse Width	t_{WP}	40		45		55		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40		45		55		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40		45		55		ns	
Data-in Set-up Time	t_{DS}	0		0		0		ns	9
Data-in Hold Time	t_{DH}	40		45		55		ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100		120		155		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120		150		200		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60		75		100		ns	8
Page Mode Read or Write Cycle	t_{PC}	120		145		190		ns	
Page Mode Read Modify Write Cycle	t_{PCM}	165		195		250		ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50		60		80		ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	
Refresh Period	t_{REF}		4		4		4	ms	
$\overline{CAS}$ Set-up Time	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120		150		200		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		ns	

Notes

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refesh cycles are required before using internal refresh counter.

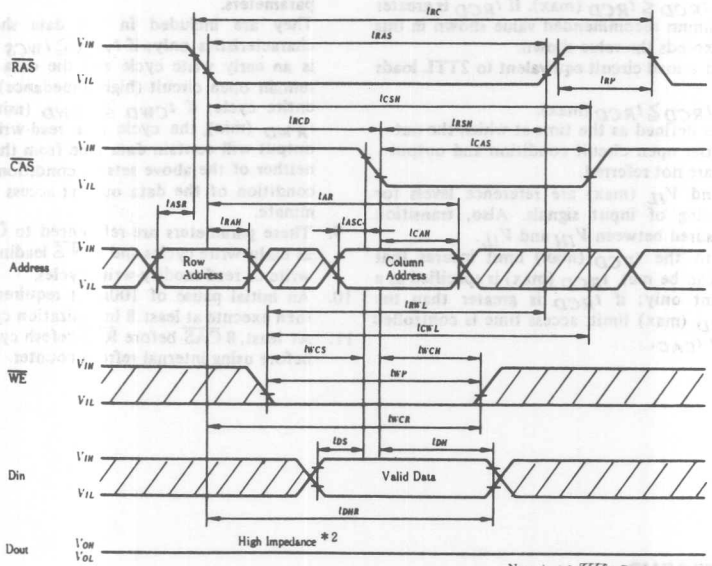
■ TIMING WAVEFORMS

● READ CYCLE



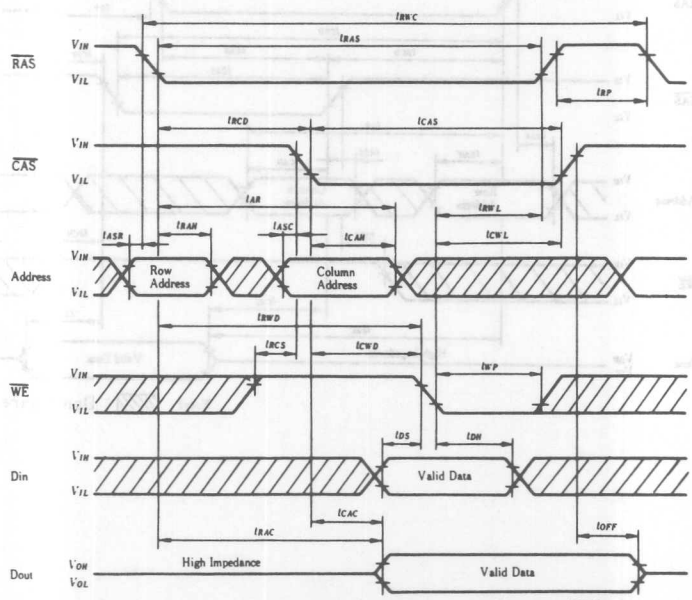
Note) ▨ : Don't care

● WRITE CYCLE



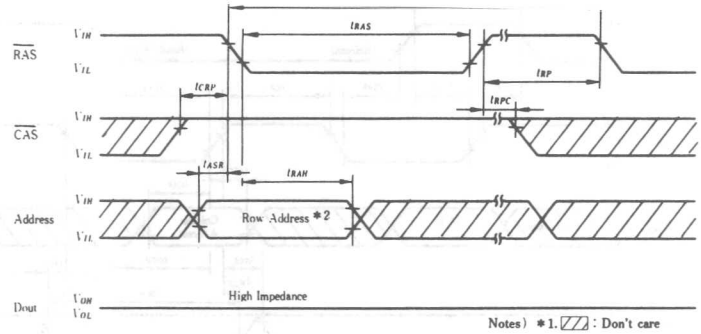
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$(min)

● READ MODIFY WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}$(min)
$t_{CWD} \geq t_{CWD}$(min)

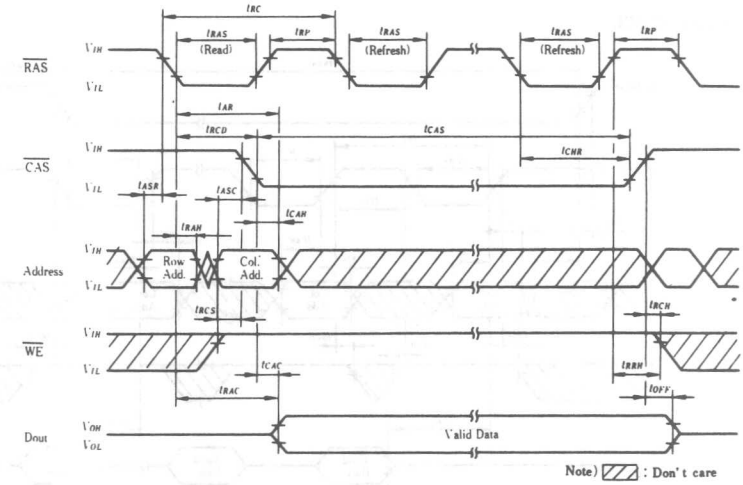
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Notes) *1. ▨ : Don't care

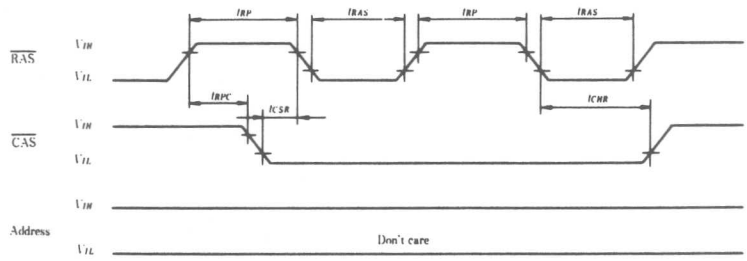
*2. Refresh Address A0-A7(AX0-AX7)

●HIDDEN REFRESH CYCLE

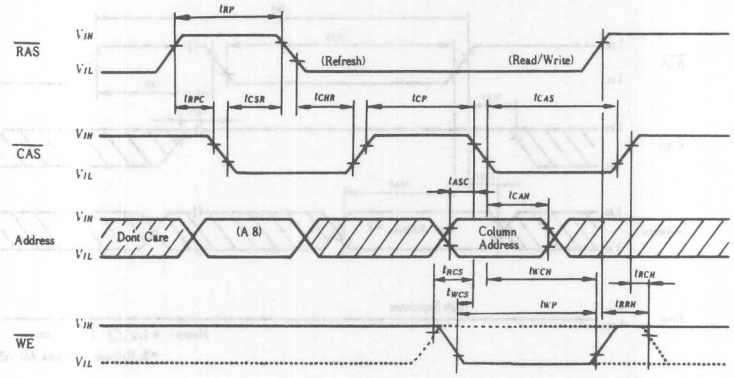


Note) ▨ : Don't care

●$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

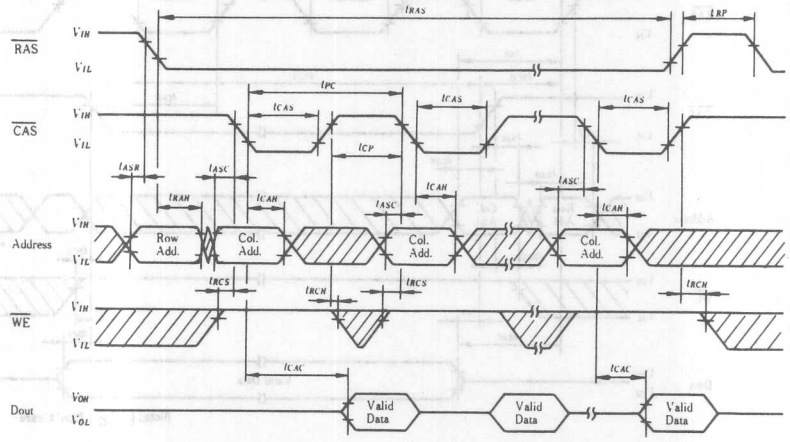


● COUNTER TEST



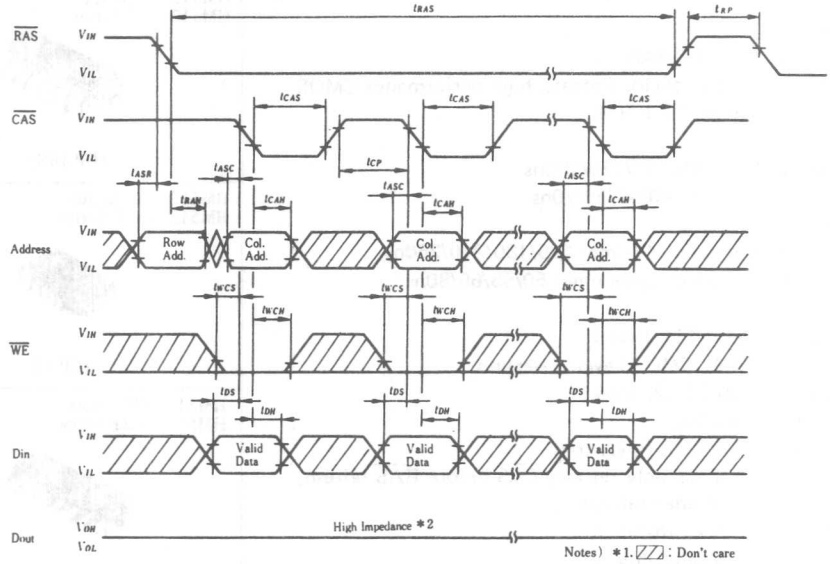
Notes) *1. ▨ : Don't care
*2. Dotted Line Means Read Cycle.

● PAGE MODE READ CYCLE



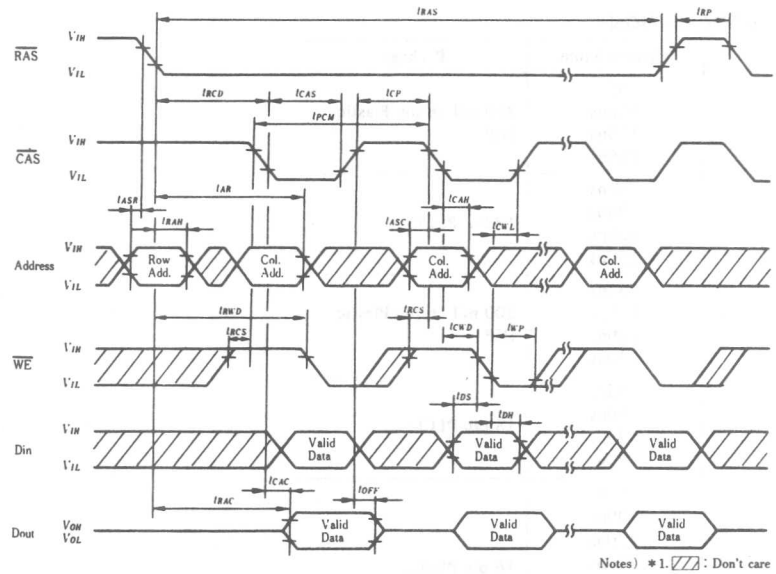
Note) ▨ : Don't care

● PAGE MODE WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$(min)

● PAGE MODE READ MODIFY WRITE CYCLE

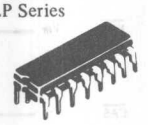


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)

HM51256 Series

262144-word × 1-bit CMOS Dynamic Random Access Memory

HM51256P Series
HM51256LP Series



(DP-16B)

HM51256CP Series
HM51256LCP Series



(CP-18)

HM51256ZP Series
HM51256LZP Series



(ZP-16)

■FEATURE

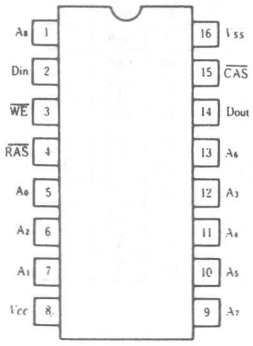
- 262, 144 word x 1 bit DRAM
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
  - Row access time: 85/100/120/150ns
  - Address access time: 40/45/55/70ns
- Cycle time
  - Random read/write cycle time: 155/180/210/250ns
  - High speed page mode cycle time: 50/55/65/80ns
- Lower power
  - Standby: 11mW (TTL Level)
    1.1mW (CMOS Level: L-version)
  - Active: 385/330/275/220mW
- Refresh: 256 cycles/4ms
  256 cycles/32ms (L-version)
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast $\overline{CAS}$ output control

■ ORDERING INFORMATION

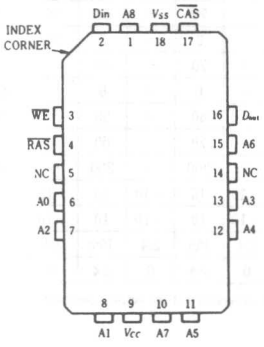
Type No.	Access Time	Package
HM51256P-8	85ns	300 mil 16 pin Plastic DIP
HM51256P-10	100ns	
HM51256P-12	120ns	
HM51256P-15	150ns	
HM51256CP-8	85ns	18 Pin PLCC
HM51256CP-10	100ns	
HM51256CP-12	120ns	
HM51256CP-15	150ns	
HM51256LP-8	85ns	300 mil 16 pin Plastic DIP
HM51256LP-10	100ns	
HM51256LP-12	120ns	
HM51256LP-15	150ns	
HM51256LCP-8	85ns	18 pin PLCC
HM51256LCP-10	100ns	
HM51256LCP-12	120ns	
HM51256LCP-15	150ns	
HM51256ZP-8	85ns	16 pin Plastic ZIP
HM51256ZP-10	100ns	
HM51256ZP-12	120ns	
HM51256ZP-15	150ns	
HM51256LZP-8	85ns	
HM51256LZP-10	100ns	
HM51256LZP-12	120ns	
HM51256LZP-15	150ns	

PIN ARRANGEMENT

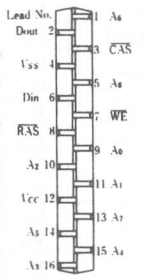
- HM51256P Series
  HM51256LP Series
- HM51256CP Series
  HM51256LCP Series
- HM51256ZP Series
  HM51256LZP Series



(Top View)



(Top View)



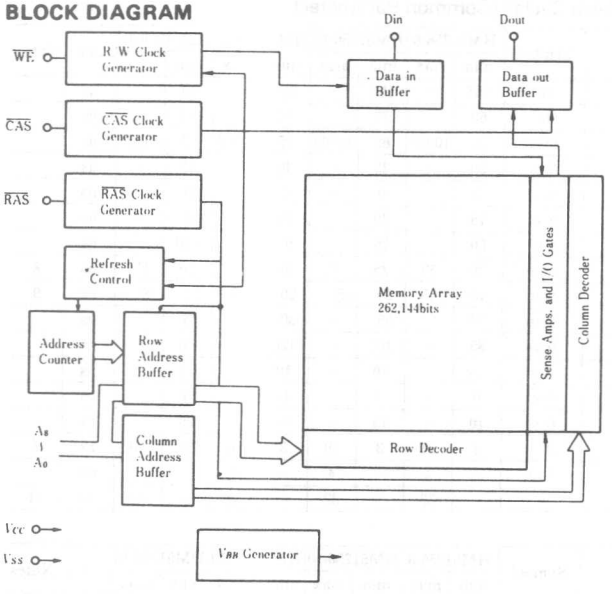
(Bottom View)

A_0-A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0-A_7	Refresh Address Inputs

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	–	70	–	60	–	50	–	40	mA	1
Standby Current ($\overline{RAS}$= V_{IH}, Dout=High Impedance)	I_{CC2}	–	2	–	2	–	2	–	2	mA	
Refresh Current ($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	–	70	–	60	–	50	–	40	mA	
Standby Current ($\overline{RAS}$= V_{IH}, Dout Enable)	I_{CC4}	–	6	–	6	–	6	–	6	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC5}	–	60	–	55	–	45	–	35	mA	
High Speed Page Mode Supply Current ($\overline{RAS}$= V_{IL}, $\overline{CAS}$ Cycling, t_{PC}=min.)	I_{CC6}	–	70	–	60	–	50	–	40	mA	1
Standby Current ($\overline{RAS}$, $\overline{CAS}$= V_{CC}−0.2V)	I_{CC7}	–	200	–	200	–	200	–	200	μA	2
Input leakage (0< V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage (0< V_{out}<7V, Dout=Disable)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA	
Output levels High (I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. This specification is guaranteed only for L-version.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1
Output Capacitance	Data-out	C_O	–	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	–	25	–	30	–	35	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	–	75	–	90	–	110	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	
		–	32	–	32	–	32	–	32	ms	21

● Read Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6

● Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

● Read-Modify-Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10

● Refresh Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Prechange to $\overline{CAS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

● High Speed Page Mode Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	50	–	55	–	65	–	80	–	ns	18, 20
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	55	75000	65	75000	75	75000	95	75000	ns	19
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	20	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	
Access Time from Column Precharge Time	t_{CAP}	–	45	–	50	–	60	–	75	ns	20

● High Speed Page Mode Read-Modify-Write Cycle

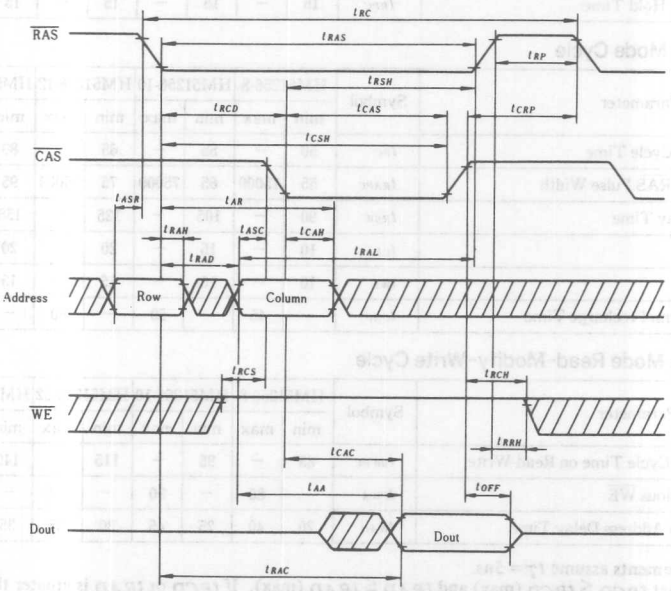
Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time on Read-Write	t_{RWPC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15

Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a Reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWPC} (min) = t_{AWD} (min) + t_{WAD} (max) + t_T.
13. Assumes that $t_{WAD} \leqq t_{WAD}$ (max). If t_{WAD} is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$ (max).
15. Operation with the t_{WAD} (max) limit insures that t_{PWA} (max) can be met, t_{WAD} (max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. An intial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
17. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.
18. Assumes that $t_{ASC} = t_{CP} - 5$ ns.
19. t_{RAPC} is determined by $\overline{RAS}$ pulse width in High Speed Page mode cycle.
20. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
21. This specification is guaranteed only for L-version.

■TIMING WAVEFORMS

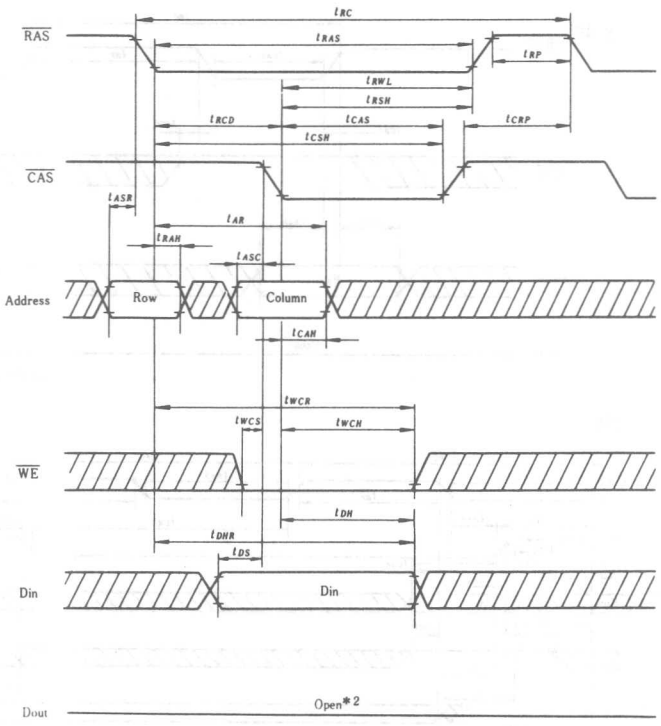
●Read Cycle



Note) ▨ : Don't care

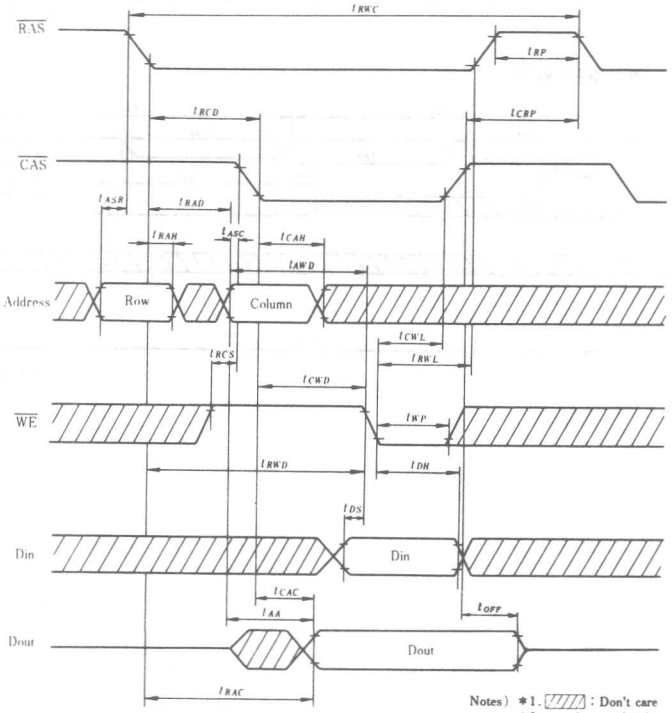
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● Write Cycle



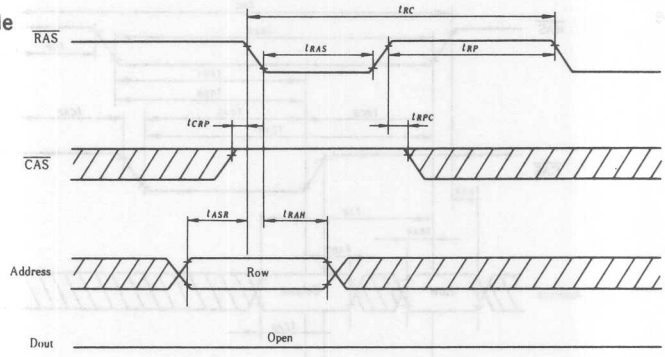
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$ (min)

● Read Modify Write Cycle



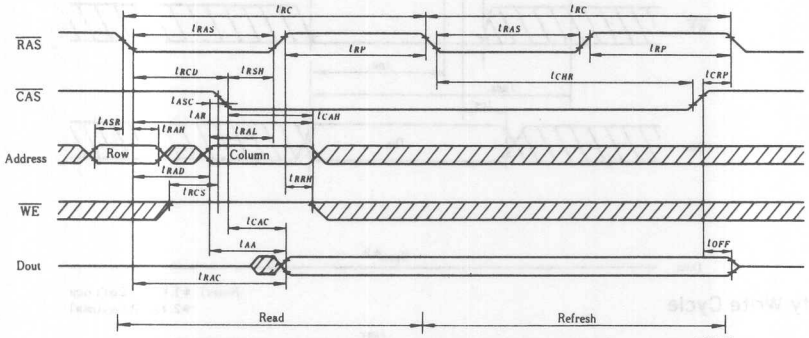
Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$ (min)
$t_{CWD} \geqq t_{CWD}$ (min)
$t_{AWD} \geqq t_{AWD}$ (min)

● $\overline{RAS}$ Only Refresh Cycle



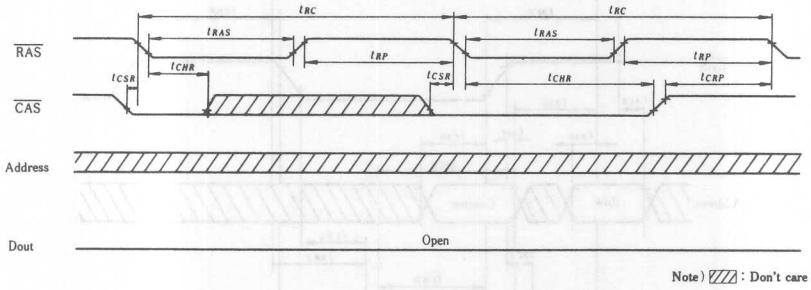
Note) ▨ : Don't care

● Hidden Refresh Cycle



Note) ▨ : Don't care

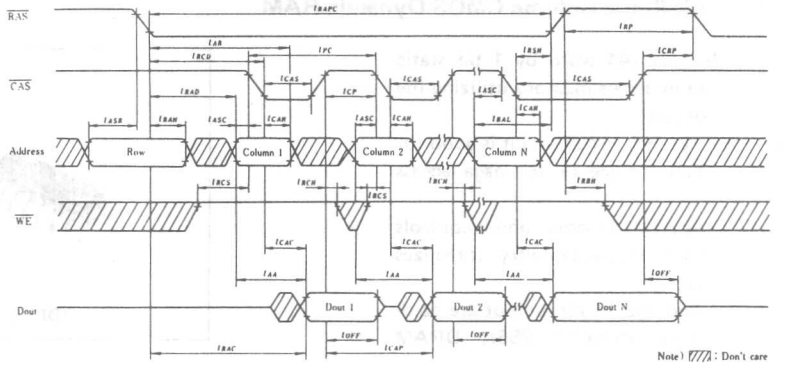
● $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note) ▨ : Don't care

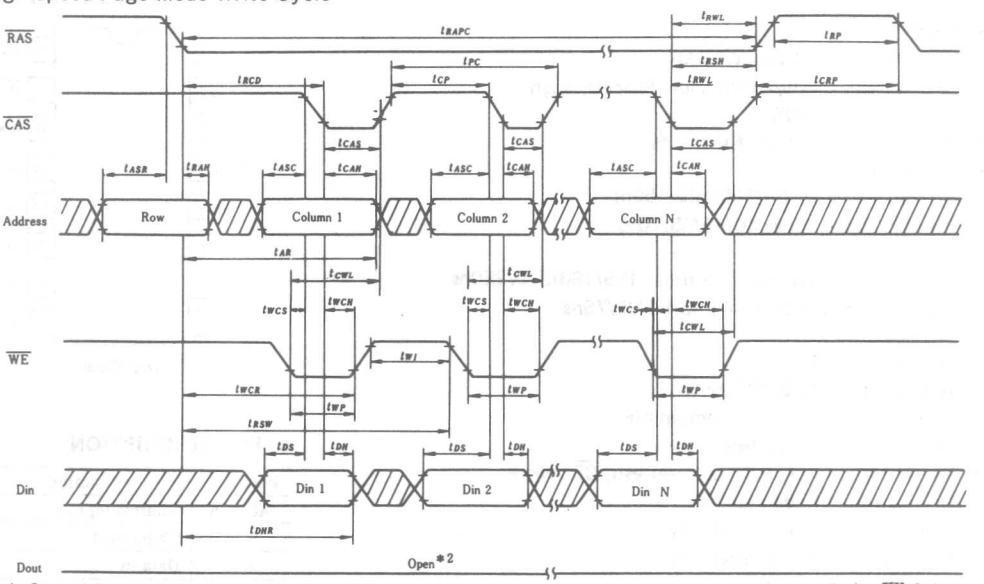
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● High Speed Page Mode Read Cycle



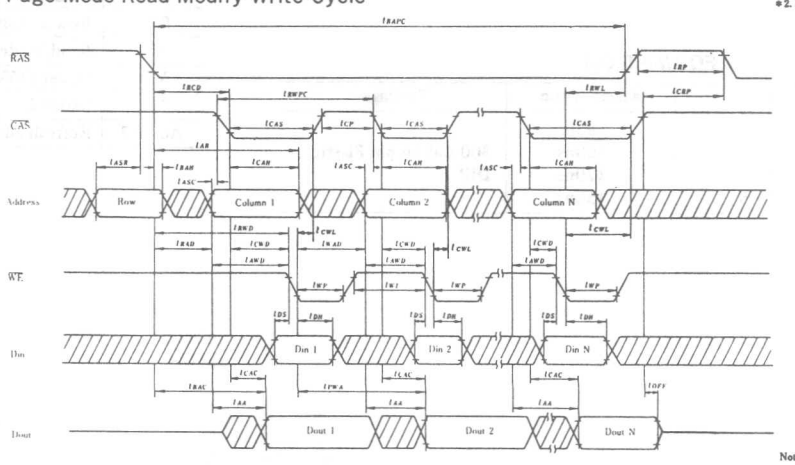
Note) ▨ : Don't care

● High Speed Page Mode Write Cycle



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

● High Speed Page Mode Read Modify Write Cycle

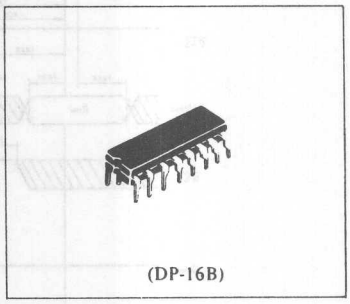


Note) ▨ : Don't care

HM51258 Series

262144-word x 1-bit Static Column CMOS Dynamic RAM

The HM51258 is the 262,144 word by 1 bit static column dynamic random access memory utilizing the Hitachi 2μm CMOS process.
This device has static column circuit and it is good for high performance main storage or for page access applications.
While the row circuitry is still dynamic, and it controls the power consumed in the static circuitry. It realizes very low power dissipation.
Multiplexed address and the 16 pin pinout are compatible with the fully dynamic 256K DRAM HM50256.



(DP-16B)

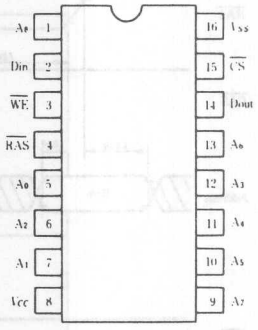
■ FEATURES

- 262,144 word x 1 bit SCRAM
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage 5V ± 10%
- Access time
  Row access time: 85/100/120/150ns
  Address access time: 40/45/55/70ns
- Cycle time
  Random Read&Write cycle time: 155/180/210/250ns
  Static Column cycle time: 45/50/60/75ns
- Lower power
  Standby: 11mW
  Active: 385/330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh
- Static column mode capability
- Edge triggered write capability
- Fast $\overline{CS}$ output control

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM51258P-8	85ns	300 mil 16 pin Plastic DIP
HM51258P-10	100ns	
HM51258P-12	120ns	
HM51258P-15	150ns	

■PIN ARRANGEMENT

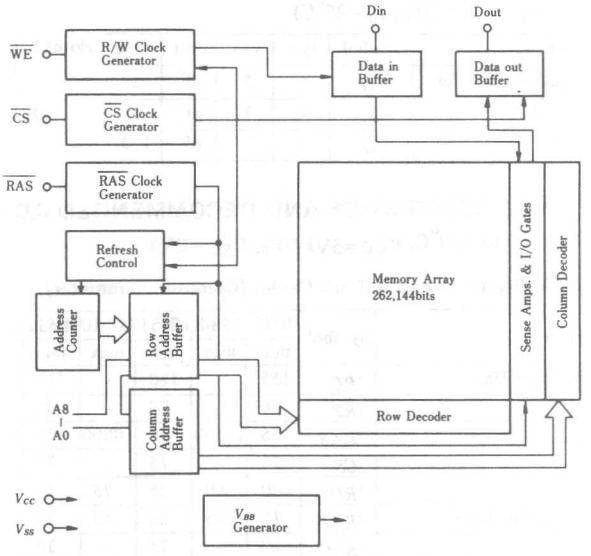


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A8	Address inputs
$\overline{CS}$	Chip select
Din	Data in
Dout	Data out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/Write input
Vcc	Power (+5V)
Vss	Ground
A0–A7	Refresh address inputs

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=0 to +70°C)

Parameter	Sybmol	Test conditions	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Note
			min	max	min	max	min	max	min	max		
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ Cycling; t_{RC}=min.	–	70	–	60	–	50	–	40	mA	1
Standby current	I_{CC2}	$\overline{RAS}$=V_{IH}, Dout=High Impedance	–	2	–	2	–	2	–	2	mA	
Refresh current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC}=min	–	70	–	60	–	50	–	40	mA	
Standby current	I_{CC4}	$\overline{RAS}$=V_{IH}, Dout Enable	–	6	–	6	–	6	–	6	mA	1
Refresh current	I_{CC5}	$\overline{CS}$ before $\overline{RAS}$ Refresh, t_{RC}=min		60	–	55	–	45	–	35	mA	
Operating current	I_{CC6}	Static Column Mode, t_{RSC}, t_{WSC}=min		70	–	60	–	50	–	40	mA	1
Input leakage	I_{LI}	V_{in}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage	I_{LO}	V_{out}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{out}=−5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{out}=4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.

■ CAPACITANCE (V_{CC}=5V±10%, T_a=25°C)

Parameter		Symbol	typ	max	Unit	Note
Input capacitance	Address, Data-In	C_{I1}	–	5	pF	1
	Clock	C_{I2}	–	7	pF	1
Output capacitance	Data-Out	C_O	–	7	pF	1, 2

Note) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS} = 0V)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CS}$ Pulse Width	t_{CS}	25	–	25	–	30	–	35	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-Up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	
● Read Cycle											
Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	85	–	100	–	120	–	150	–	ns	
Read Command Set-Up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
$\overline{RAS}$ to Column Address Hold Time	t_{AH}	10	–	15	–	15	–	20	–	ns	16
Output Hold Time from Address	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6
● Write Cycle											
Column Address Set-Up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$ on Write	t_{AWR}	60	–	75	–	90	–	110	–	ns	
Write Command Set-Up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

(to be continued)

• Read-Modify-Write Cycle

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10
Output Hold Time from $\overline{WE}$	t_{OHW}	25	–	25	–	25	–	25	–	ns	

• Refresh Cycle

$\overline{CS}$ Set-up Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

• SC Mode Cycle

SC Mode Cycle Time on Read	t_{RSC}	45	–	50	–	60	–	75	–	ns	
SC Mode Cycle Time on Write	t_{WSC}	45	–	50	–	60	–	75	–	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
SC Mode $\overline{RAS}$ Pulse Width	t_{RASC}	55	75000	65	75000	75	75000	95	75000	ns	
$\overline{CS}$ Precharge Time	t_{CP}	10	–	10	–	15	–	15	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	

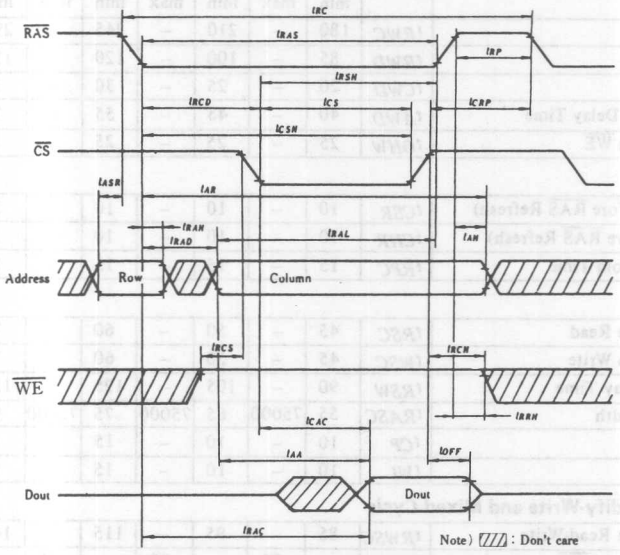
• SC Mode Read-Modify-Write and Mixed Cycle

SC Mode Cycle Time on Read-Write	t_{RWSC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15
Column Address Hold Time to Previous $\overline{WE}$	t_{PWH}	80	–	90	–	110	–	140	–	ns	

Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $tRAD \leqq tRAD$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \geqq t_{RAD}$(max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$(min), $t_{CWD} \geqq t_{CWD}$(min) and $t_{AWD} \geqq t_{AWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWSC}(min) = t_{AWD}(min) + t_{WAD}(max) + t_T
13. Assumes that $tWAD \leqq tWAD$(max). If $tWAD$ is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$(max).
15. Operation with the t_{WAD}(max) limit insures that t_{PWA}(max) can be met, t_{WAD}(max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD}(max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is defined as the time at which the column address hold.
17. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
18. At least, 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

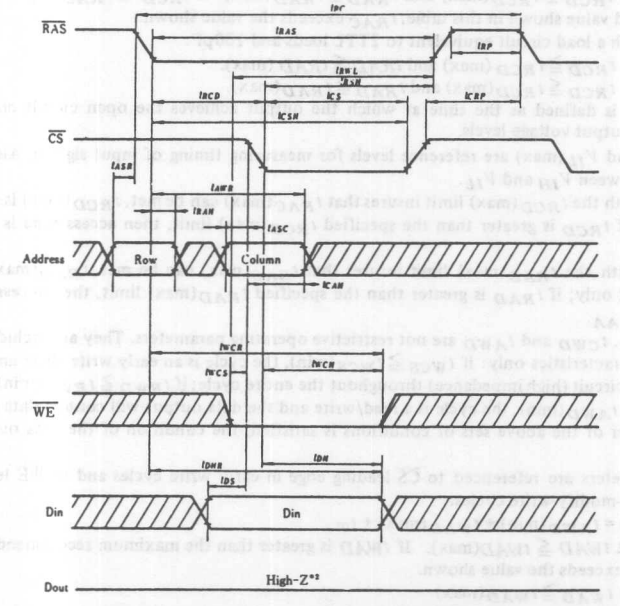
■ TIMING WAVEFORMS

● Read Cycle



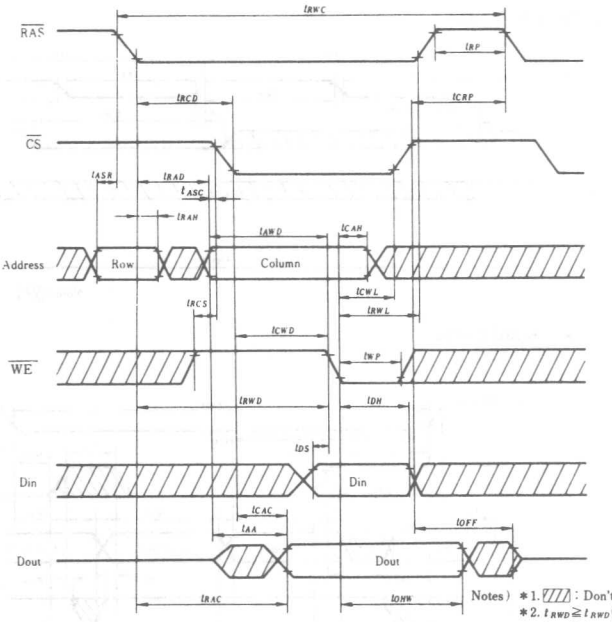
Note) ▨ : Don't care

● Write Cycle



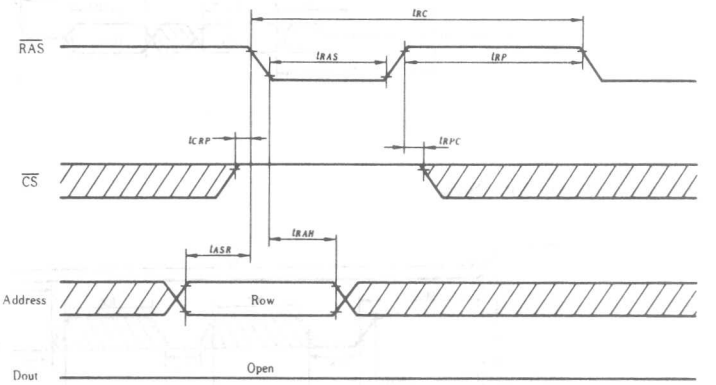
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

• Read-Modify-Write Cycle



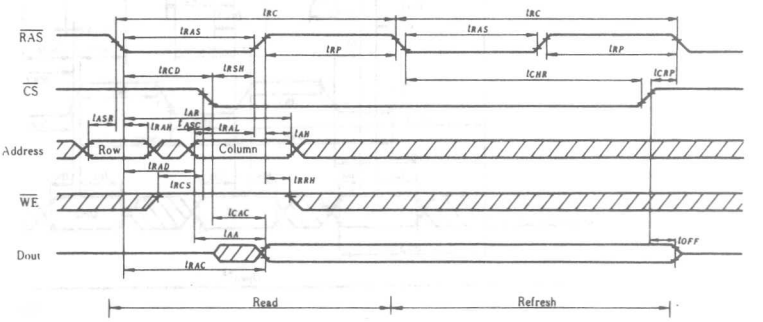
Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)
$t_{AWD} \geqq t_{AWD}$(min)

• RAS Only Refresh Cycle



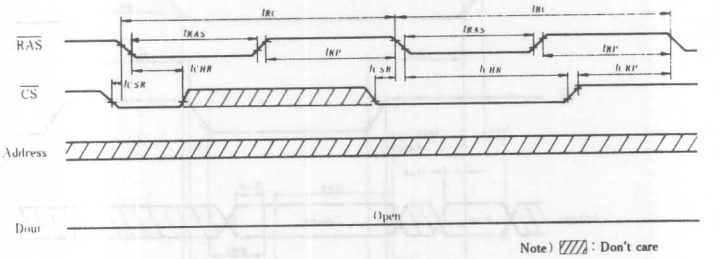
Note) ▨ : Don't care

• Hidden Refresh Cycle



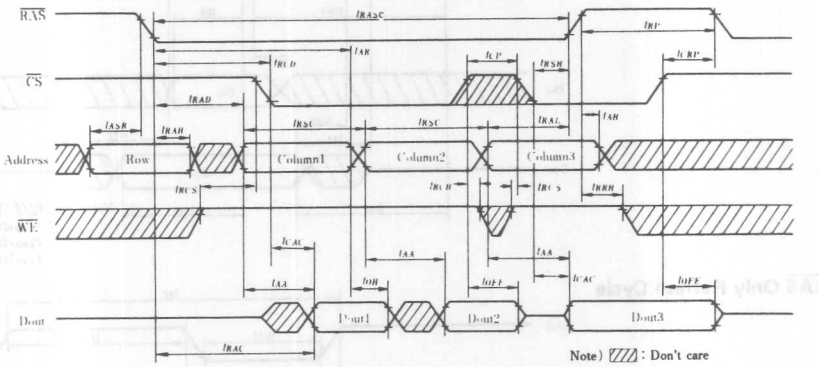
Note) ▨ : Don't care

• $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle



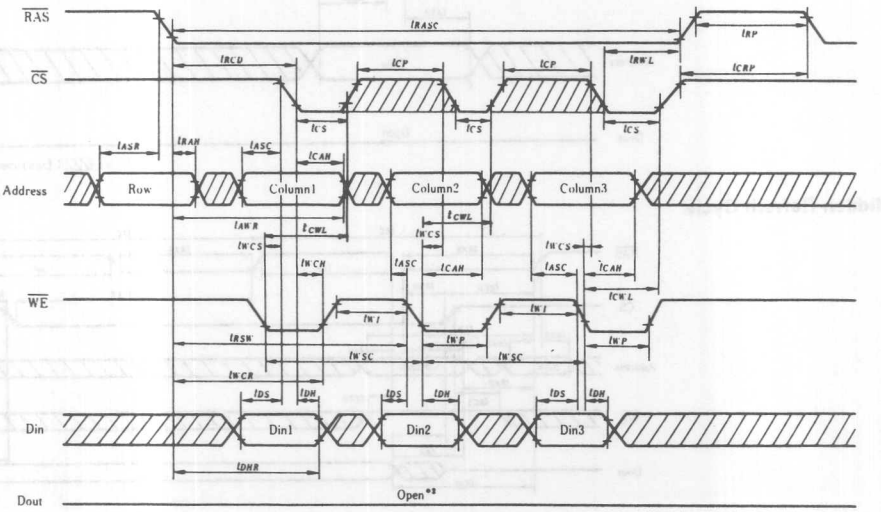
Note) ▨ : Don't care

• Static Column Mode Read Cycle



Note) ▨ : Don't care

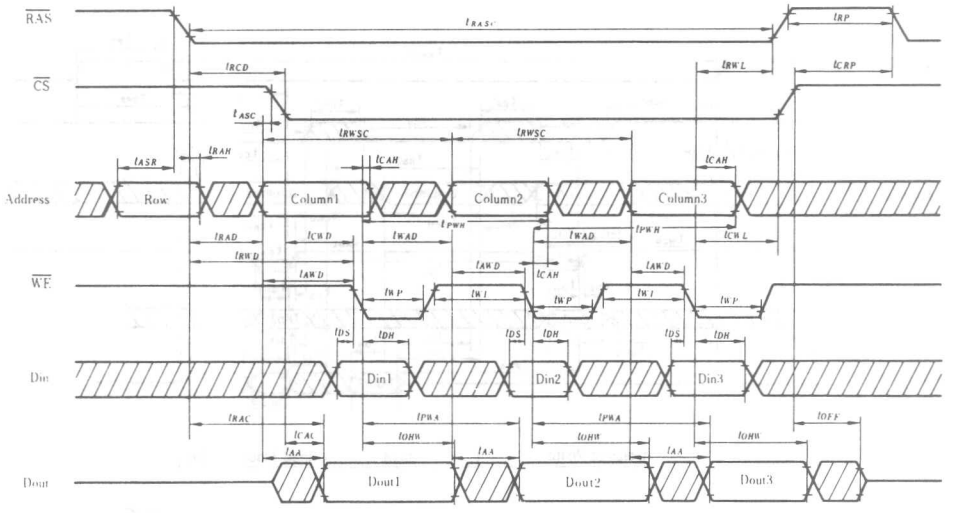
• Static Column Mode Write Cycle



Notes) *1. ▨: Don't care
*2. $t_{WCS} \geqq t_{WCS}$ (min)

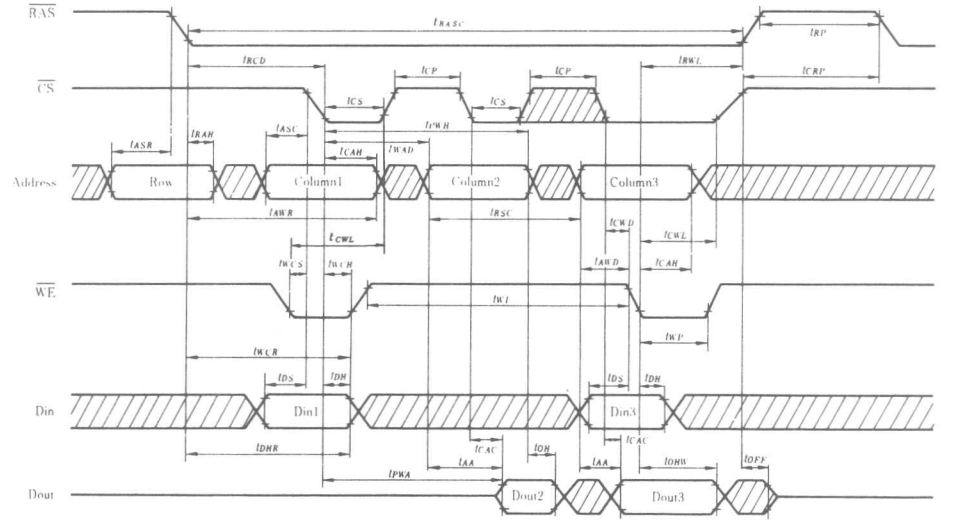
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- **Static Column Mode Read-Modify-Write Cycle**

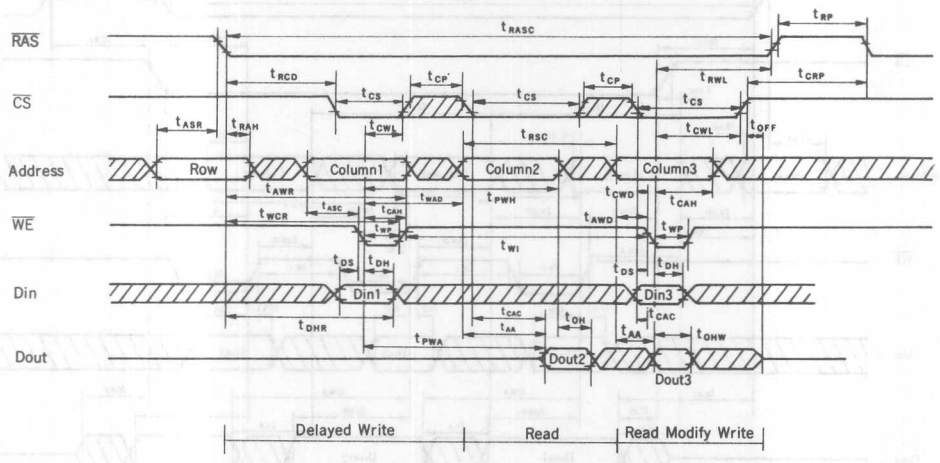


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}$(min)
$t_{CWD} \geq t_{CWD}$(min)
$t_{AWD} \geq t_{AWD}$(min)

- **Static Column Mode Mixed Cycle-1**



• Static Column Mode Mixed Cycle-2



Note) ▨ : Don't care.

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HM514256 Series

262144-word x 4-bit CMOS Dynamic RAM

The Hitachi HM514256 Series is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256 has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM514256 offers Page Mode as a high speed access mode.

Multiplexed address input permits the HM514256 to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

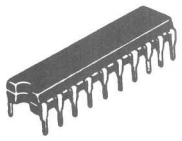
Features

- High Speed . . . . . Access Time 80/100/120ns (max)
- Lower Power . . . . Active 363/302.5/258.5 mW (max)
  Standby 11 mW (max)
- Single 5V (±10%)
- Page Mode
- 512 refresh cycle . . . . . 8 ms
- 2 variations of refresh . . . . . $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

Ordering Information

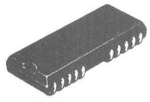
Type No.	Access Time	Package
HM514256P-8	80ns	300 mil 20-pin Plastic DIP
HM514256P-10	100ns	
HM514256P-12	120ns	
HM514256JP-8	80ns	300 mil 20-pin Plastic SOJ
HM514256JP-10	100ns	
HM514256JP-12	120ns	
HM514256ZP-8	80ns	400 mil 20-pin Plastic ZIP
HM514256ZP-10	100ns	
HM514256ZP-12	120ns	

HM514256P Series



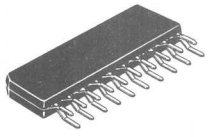
(DP-20NA)

HM514256JP Series



(CP-20D)

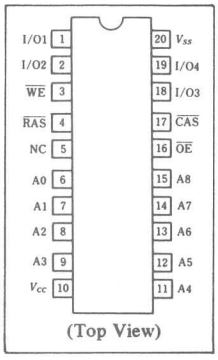
HM514256ZP Series



(ZP-20)

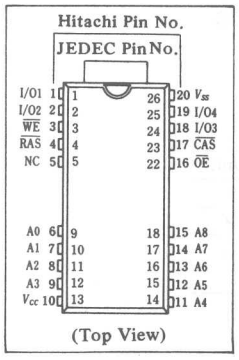
Pin Arrangement

HM514256P Series



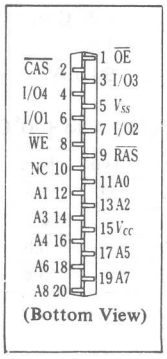
(Top View)

HM514256JP Series



(Top View)

HM514256ZP Series

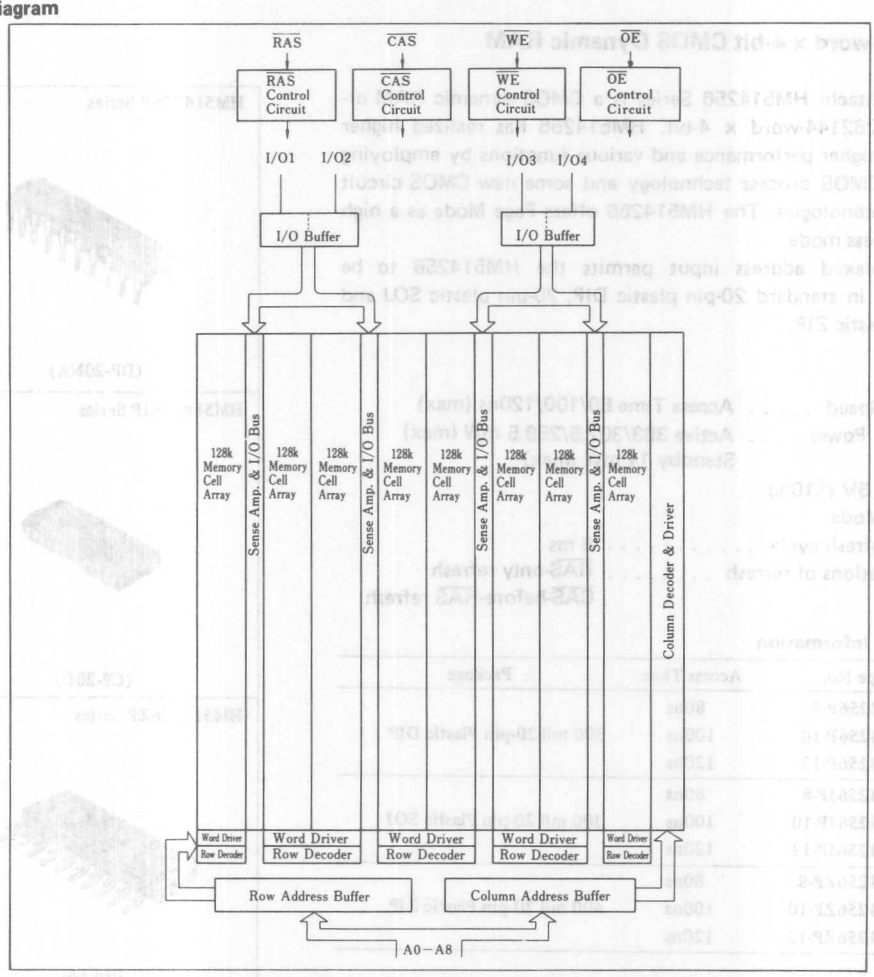


(Bottom View)

Pin Description

A0–A8	Address Input
A0–A8	Refresh Address Input
I/O1–I/O4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . -55°C to +125°C
Power dissipation . . . . . 1 W
Short circuit output current . . . . . 50 mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.5	5.0	5.5	V
Input High voltage		V_{IH}	2.4	–	6.5	V
Input Low voltage	I/O Pin	V_{IL}	−1.0	–	0.8	V
	Others	V_{IL}	−2.0	–	0.8	

Note: All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, T_a = 0 to +70°C)

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Test conditions		Notes
		Min	Max	Min	Max	Min	Max				
Operating current	I_{CC1}	–	66	–	55	–	47	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.		1,2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$=V_{IH} Dout=High-Z	TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$,$\overline{CAS}$≧V_{CC}–0.2V Dout=High-Z	CMOS interface	
Refresh current	I_{CC3}	–	66	–	55	–	47	mA	$\overline{RAS}$-only refresh, t_{RC}=Min.		2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$ =V_{IL}, Dout enable		1
Refresh current	I_{CC6}	–	66	–	55	–	47	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min.		
Operating current	I_{CC7}	–	66	–	55	–	47	mA	Page mode, $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min		1, 3
Input leakage	I_{LI}	–10	10	–10	10	–10	10	µA	V_{in} = 0 to +7V		
Output leakage	I_{LO}	–10	10	–10	10	–10	10	µA	V_{out} = 0 to +7V, Dout = disable		
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = –5mA		
	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{OL} = 4.2mA		

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Type	Max	Unit	Notes
Input capacitance	Address	C_{I1}	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	–	7	pF	1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	–	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, T_a = to +70°C)*1,*10,*11

Test Conditions

- Input rise and fall times: 5ns
  Input timing reference levels: 0.8V, 2.4V
  Output load: 2TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10000	50	10000	60	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	40	25	50	25	60	ns	
$\overline{RAS}$ hold time	t_{RSH}	40	–	50	–	60	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
Refresh period	t_{REF}	–	8	–	8	–	8	ns	
$\overline{OE}$ to data-in delay time	t_{ODD}	20	–	25	–	30	–	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	–	25	–	30	–	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	25	–	25	–	30	–	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	–	0	–	0	–	ns	

Read Cycle

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	2,3
Access time from $\overline{CAS}$	t_{CAC}	–	40	–	50	–	60	ns	3,4
Access time from $\overline{OE}$	t_{OAC}	–	25	–	25	–	30	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Output buffer turn-off delay time	t_{OFF1}	–	20	–	25	–	30	ns	5
Output buffer turn-off delay time referenced to $\overline{OE}$	t_{OFF2}	–	20	–	25	–	30	ns	5

Write Cycle

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	8
Write command hold time	t_{WCH}	20	–	20	–	25	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	–	35	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	–	35	–	40	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in hold time	t_{DH}	20	–	20	–	25	–	ns	9

Read-Modify-Write Cycle

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-Write cycle time	t_{RWC}	225	–	265	–	305	–	ns	
Read-Write cycle $\overline{RAS}$ pulse width	t_{RWS}	145	–	175	–	205	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	–	135	–	160	–	ns	8
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	70	–	85	–	100	–	ns	8

Refresh Cycle

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	10	–	ns	

Page Mode Cycle

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Page mode read or write cycle	t_{PC}	60	–	70	–	85	–	ns	
Page mode $\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	15	–	ns	

Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514256-8		HM514256-10		HM514256-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Page mode read modify write cycle time	t_{PCM}	125	–	145	–	170	–	ns	
Page mode read modify write $\overline{CAS}$ pulse width	t_{CRW}	105	–	125	–	145	–	ns	

Notes) *1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).

*5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*6. Transition times are measured between V_{IH} and V_{IL}.

*7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min) and $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

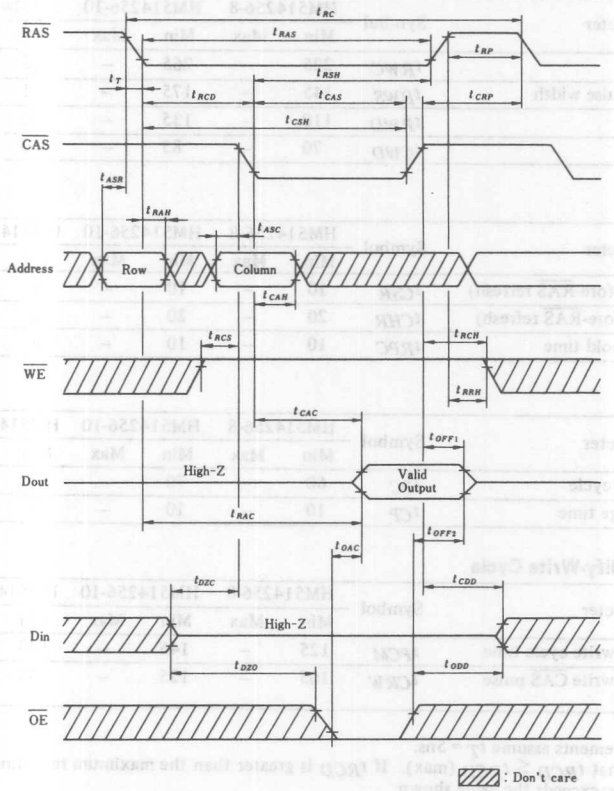
*9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

*10. An initial pause of 100μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

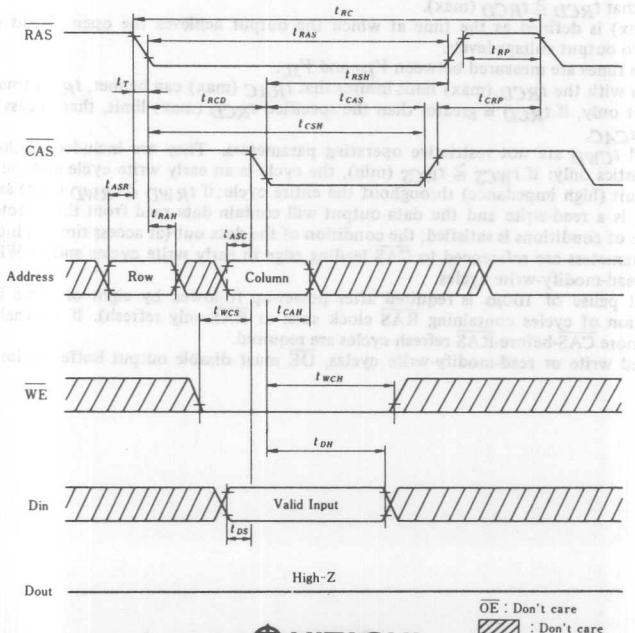
*11. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

Timing Waveforms

Read Cycle

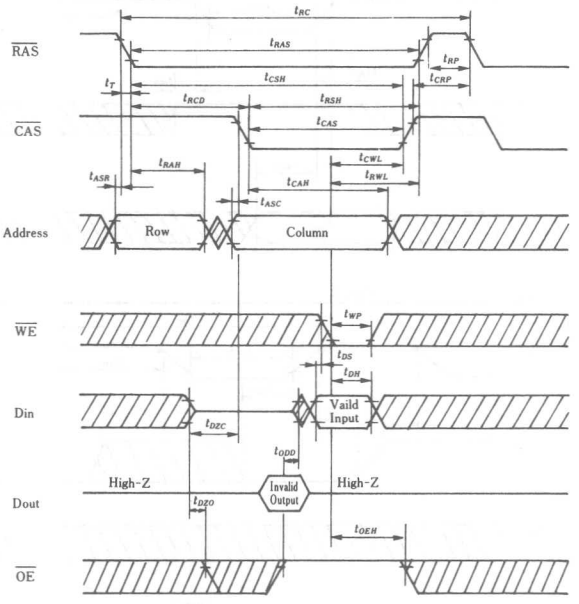


Early Write Cycle

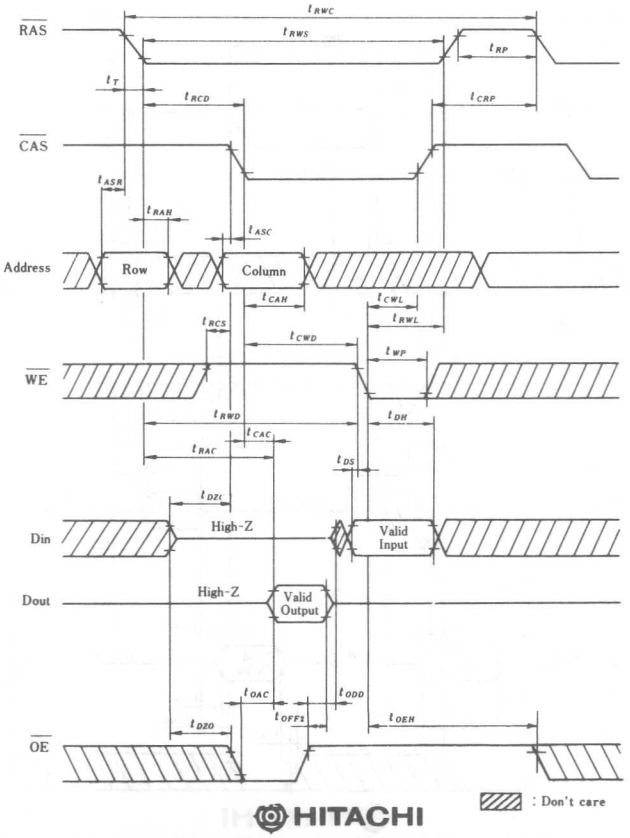


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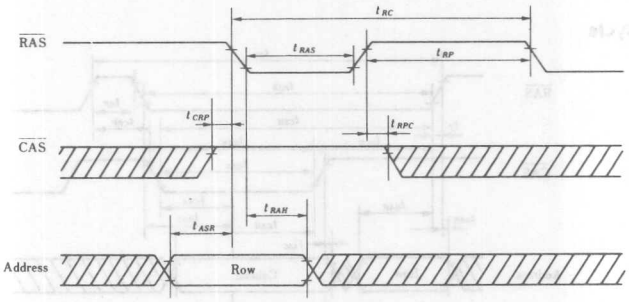
Delayed Write Cycle



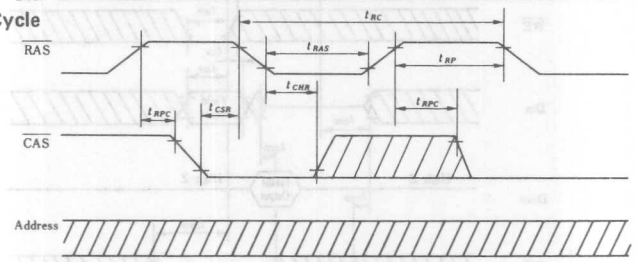
Read-Modify-Write Cycle



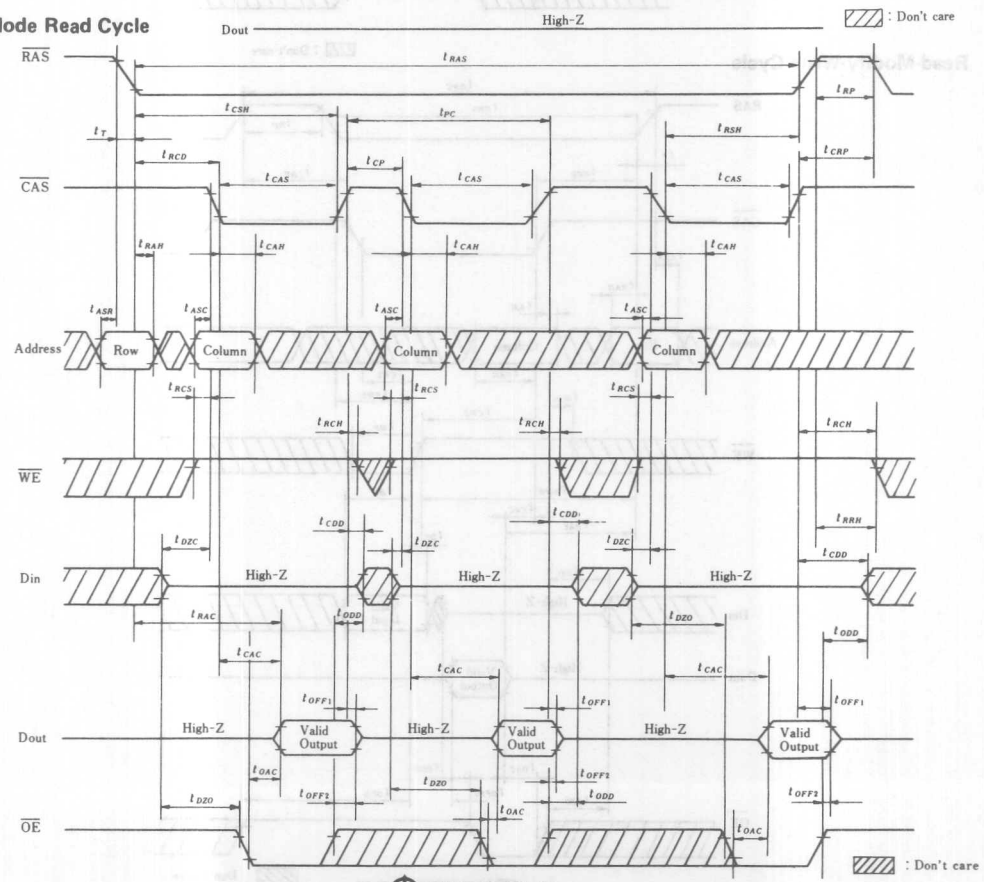
RAS-Only Refresh Cycle



CAS-before-RAS Refresh Cycle

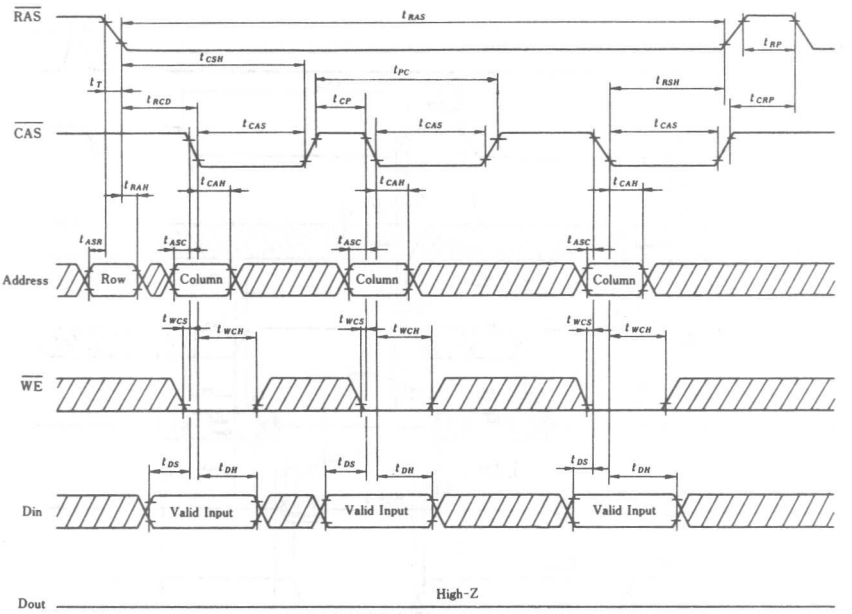


Page Mode Read Cycle

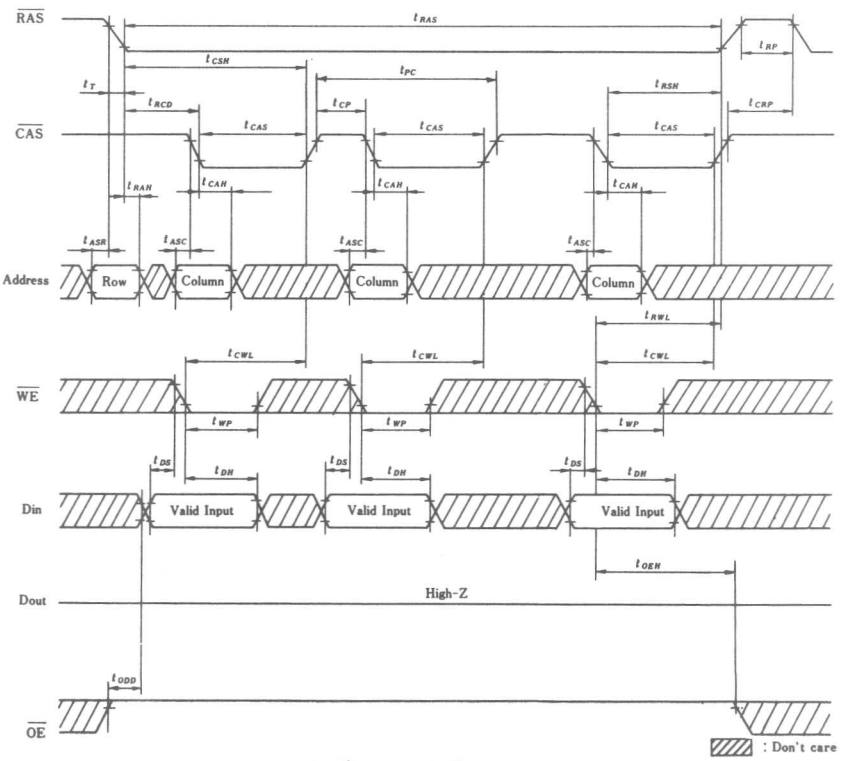


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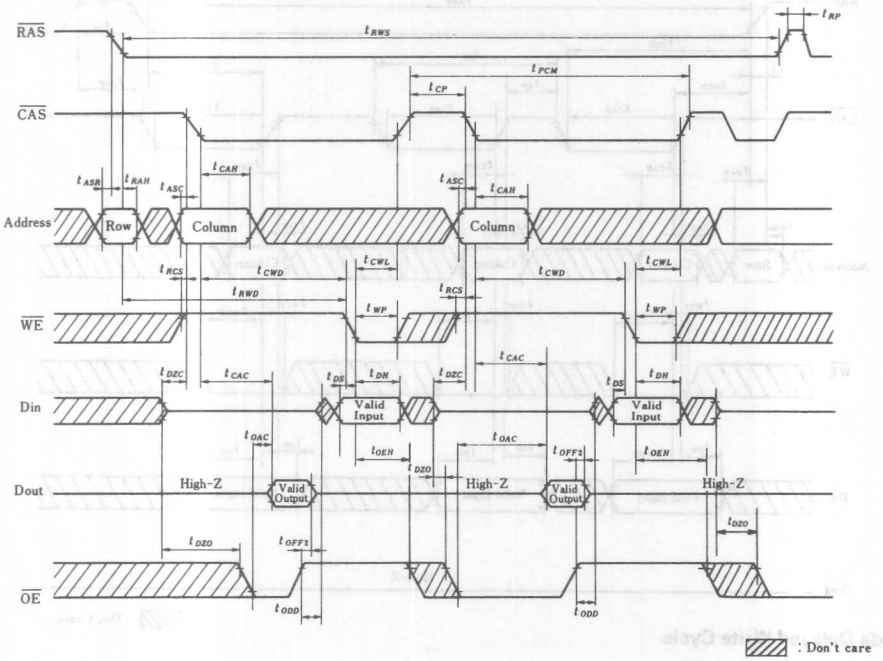
Page Mode Early Write Cycle



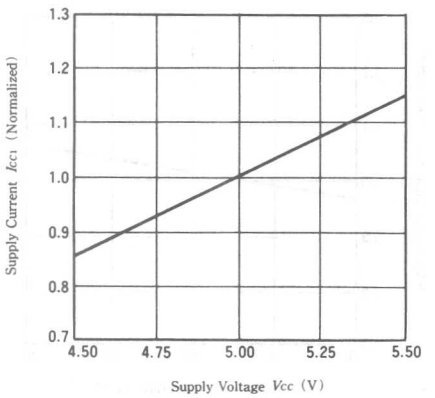
Page Mode Delayed Write Cycle



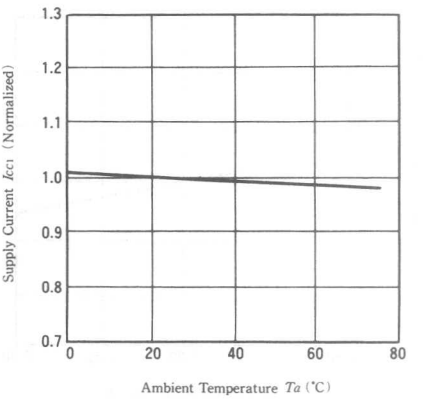
Page Mode Read-Modify-Write Cycle



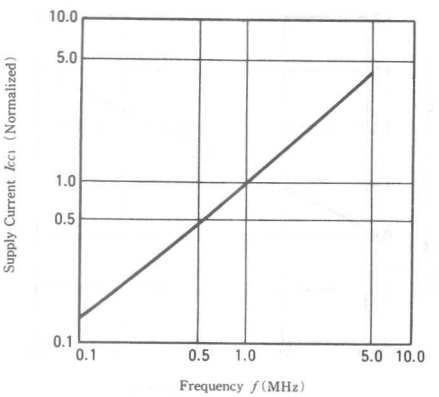
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



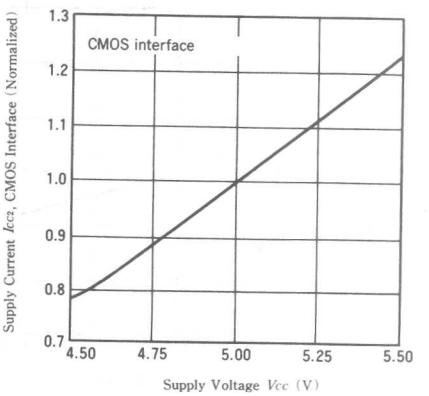
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



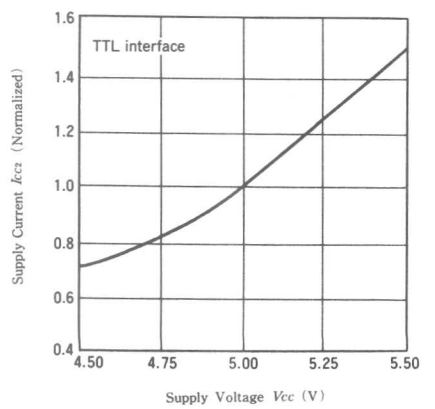
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



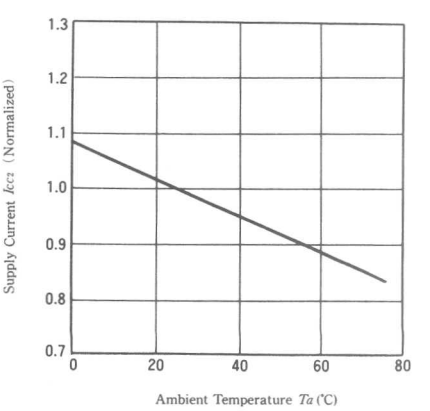
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



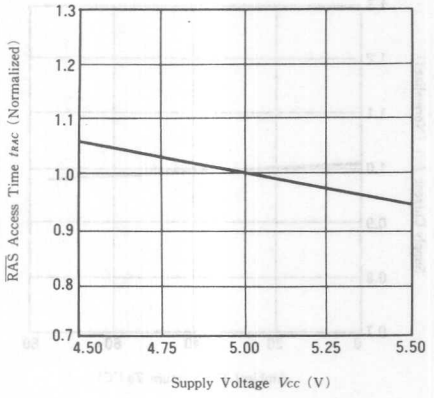
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



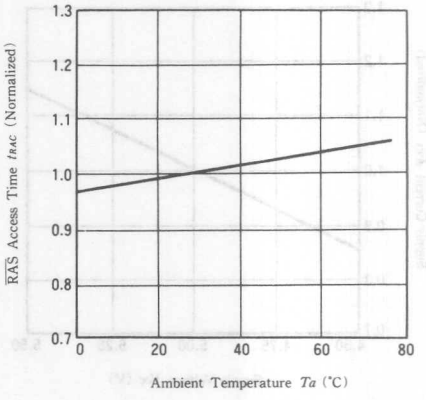
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



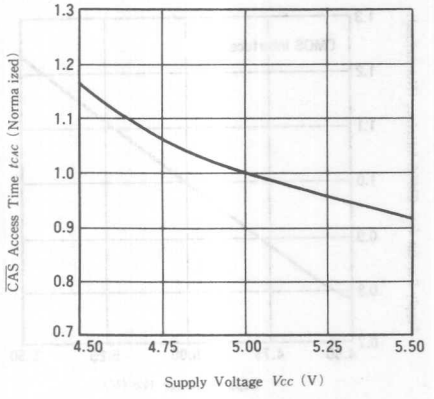
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



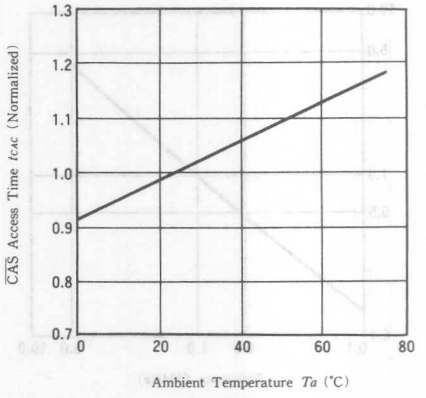
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATUR



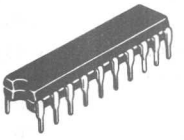
HM514256S Series
HM514256A Series

262144-Word × 4-Bit CMOS Dynamic RAM

The Hitachi HM514256S/A is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256S/A has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514256S/A offers Fast Page Mode as a high speed access mode.

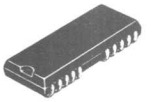
Multiplexed address input permits the HM514256S/A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514256SP Series
HM514256AP Series



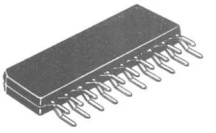
(DP-20NA)

HM514256SJP Series
HM514256AJP Series



(CP-20D)

HM514256SZP Series
HM514256AZP Series



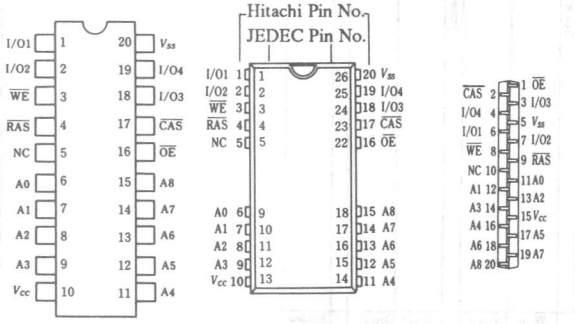
(ZP-20)

Features

- Single 5 V (±10%)
- High speed: Access Time 80 ns/100 ns/120 ns (max)
- Low power: Standby 11 mW (max)
  Active 363 mW/302.5 mW/258.5 mW (max)
- Fast page mode capability
- 512 refresh cycles: (8 ms)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

Pin Arrangement

- HM514256SP Series
- HM514256AP Series
- HM514256SJP Series
- HM514256AJP Series
- HM514256SZP Series
- HM514256AZP Series



Pin Description

Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

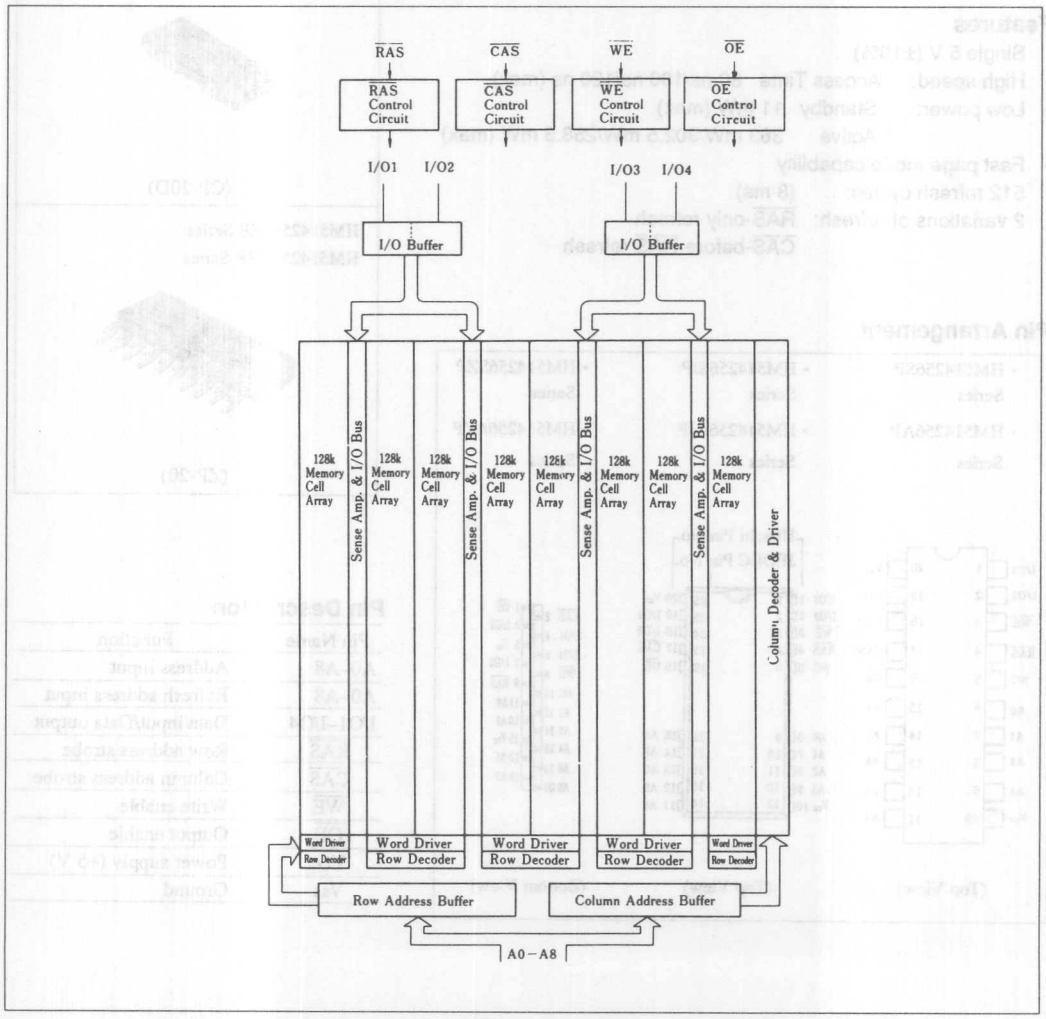
Ordering Information

Type No.	Access Time	Package
HM514256P-8S	80 ns	300-mil 20-pin
HM514256P-10S	100 ns	plastic DIP
HM514256P-12S	120 ns	(DP-20NA)
HM514256JP-8S	80 ns	300-mil 20-pin
HM514256JP-10S	100 ns	plastic SOJ
HM514256JP-12S	120 ns	(CP-20D)
HM514256ZP-8S	80 ns	400-mil 20-pin
HM514256ZP-10S	100 ns	plastic ZIP
HM514256ZP-12S	120 ns	(ZP-20)

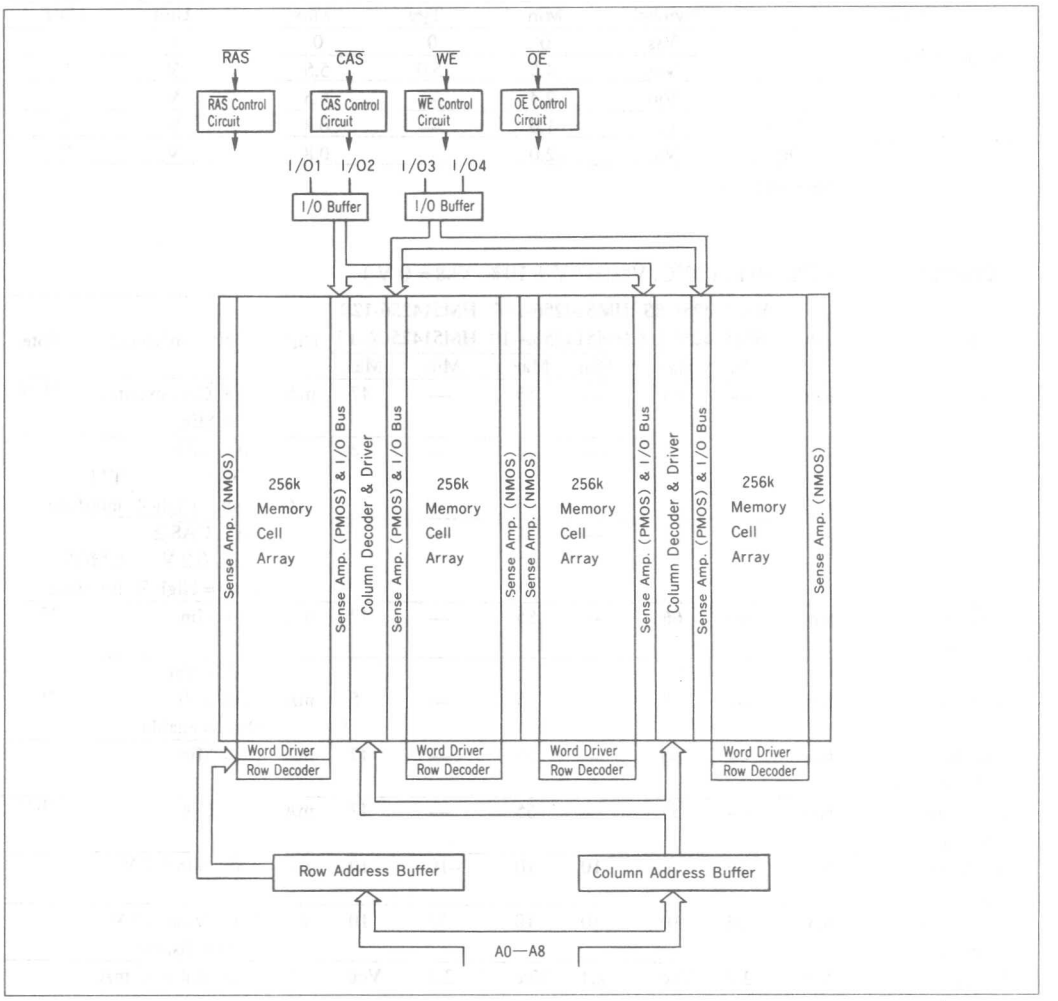
Type No.	Access Time	Package
HM514256AP-8	80 ns	300-mil 20-pin
HM514256AP-10	100 ns	plastic DIP
HM514256AP-12	120 ns	(DP-20NA)
HM514256AJP-8	80 ns	300-mil 20-pin
HM514256AJP-10	100 ns	plastic SOJ
HM514256AJP-12	120 ns	(CP-20D)
HM514256AZP-8	80 ns	400-mil 20-pin
HM514256AZP-10	100 ns	plastic ZIP
HM514256AZP-12	120 ns	(ZP-20)

Block Diagram

HM514256S Series



HM514256A Series



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−1.0 to +7.0	V
Supply voltage relative to Vss	Vcc	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	*1
Input high voltage		V_{IH}	2.4	—	6.5	V	*1
Input low voltage	I/O pin	V_{IL}	–1.0	—	0.8	V	*1
	Others	V_{IL}	–2.0	—	0.8	V	*1

Note: *1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM514256-8S HM514256A-8 Min	HM514256-8S HM514256A-8 Max	HM514256-10S HM514256A-10 Min	HM514256-10S HM514256A-10 Max	HM514256-12S HM514256A-12 Min	HM514256-12S HM514256A-12 Max	Unit	Test Conditions	Note
Operating current	I_{CC1}	—	66	—	55	—	47	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	*1, *2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z TTL interface	
		—	1	—	1	—	1		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z CMOS interface	
$\overline{RAS}$-only refresh current	I_{CC3}	—	66	—	55	—	47	mA	t_{RC} = Min	*2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	*1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	66	—	55	—	47	mA	t_{RC} = Min	
Fast page mode current	I_{CC7}	—	55	—	55	—	47	mA	t_{PC} = Min	*1, *3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Item		Symbol	Typ	Max	Unit	Note
Input capacitance	Address	C_{I1}	—	5	pF	*1
	Clock	C_{I2}	—	7	pF	*1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	—	10	pF	*1, *2

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*14

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	*1, *7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	

Read Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	*3, *4
Access time from Address	t_{AA}	—	40	—	45	—	55	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to RAS lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF1}	—	20	—	25	—	30	ns	*6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	25	—	30	ns	*6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	*10
Write command hold time	t_{WCH}	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	*11
Data-in hold time	t_{DH}	20	—	20	—	25	—	ns	*11

Read-Modify-Write Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	—	135	—	160	—	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	55	—	60	—	70	—	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	70	—	80	—	95	—	ns	*10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Item	Symbol	HM514256-8S HM514256A-8		HM514256-10S HM514256A-10		HM514256-12S HM514256A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	*12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	*13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast page mode read-write cycle time	t_{PCM}	110	—	115	—	135	—	ns	

Notes: *1. AC measurements assume $t_T = 5$ns.

*2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

*5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).

*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between V_{IH} and V_{IL}.

*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

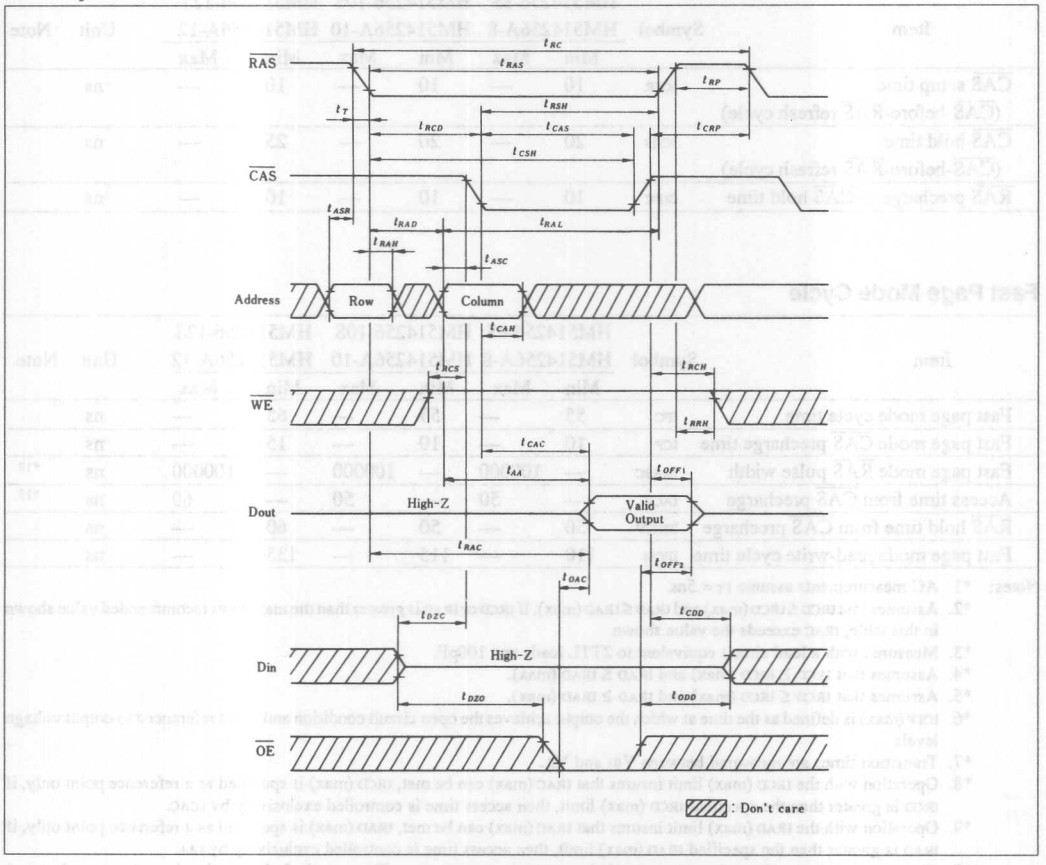
*12. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.

*13. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

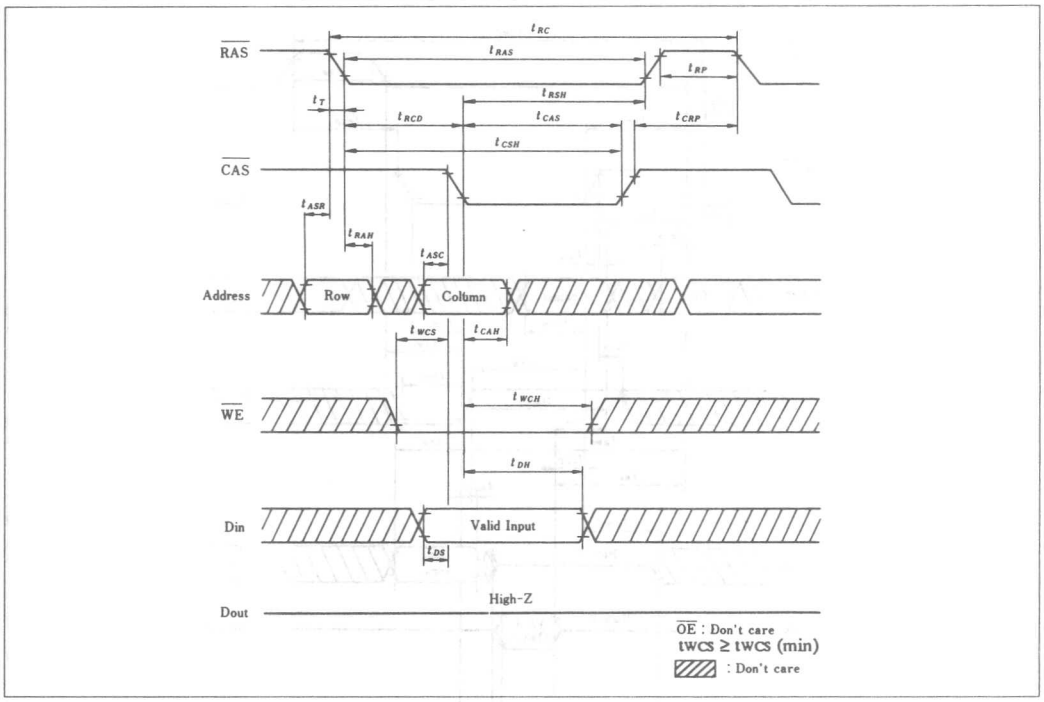
*14. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

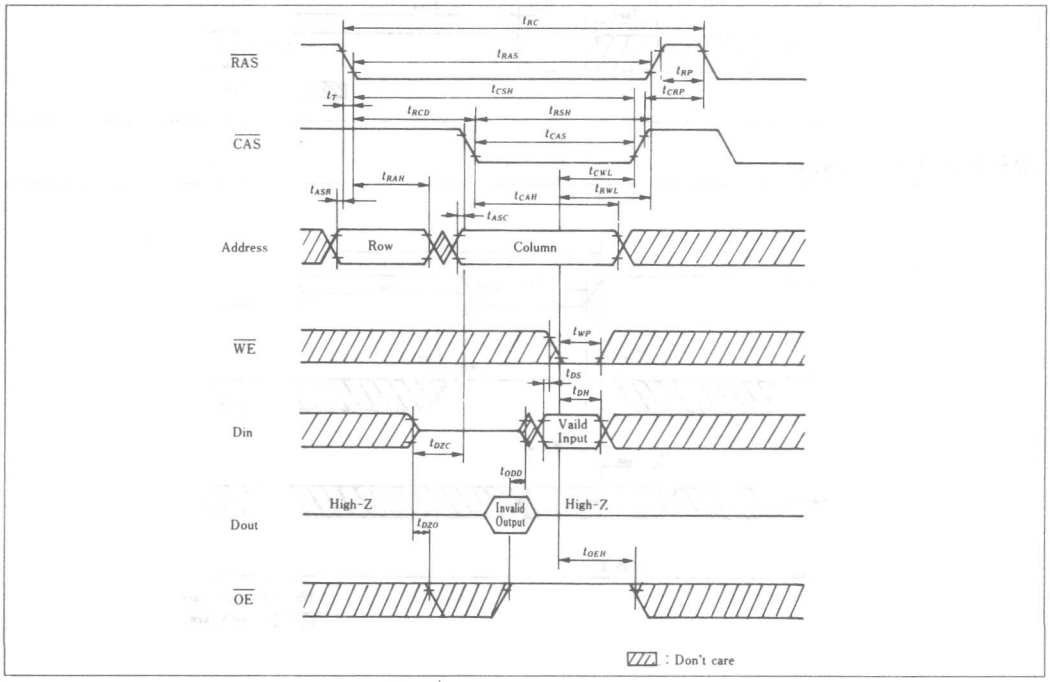
Read Cycle



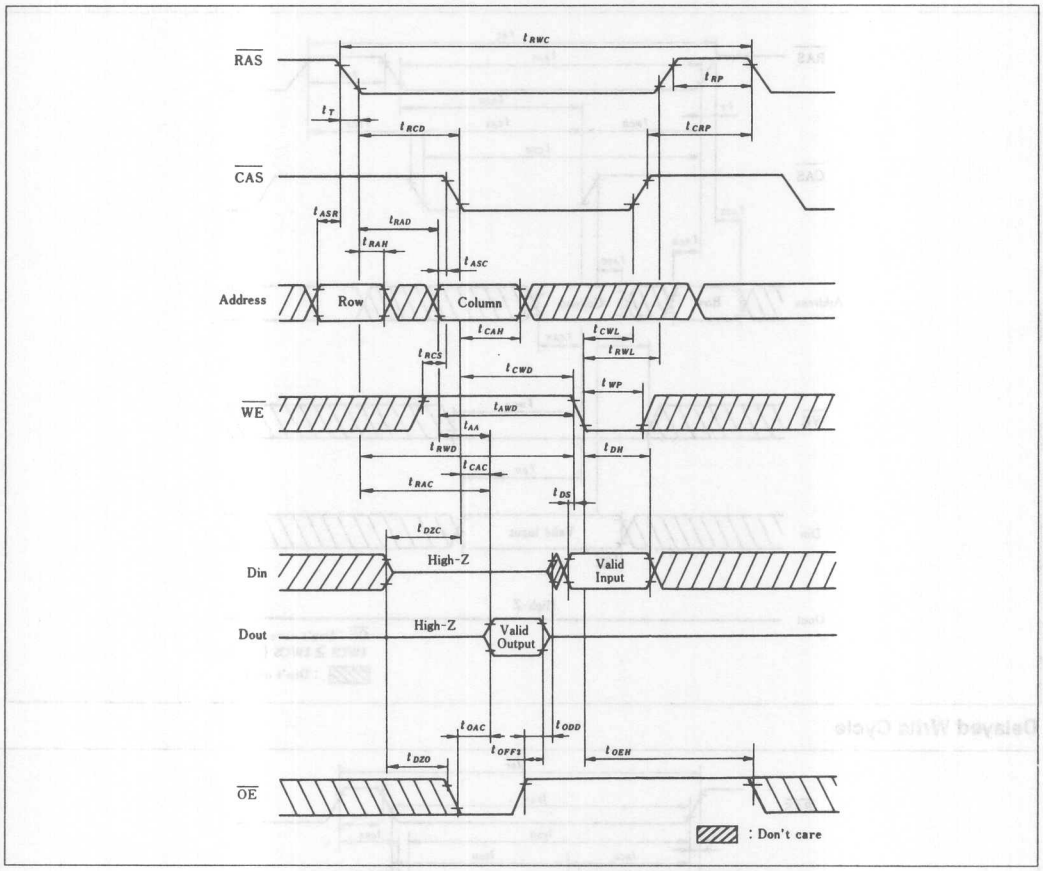
Early Write Cycle



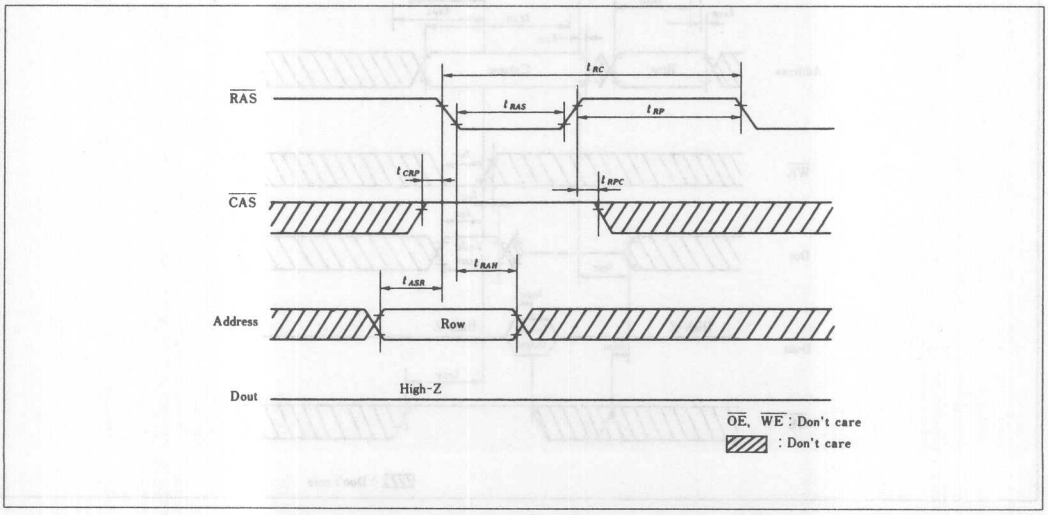
Delayed Write Cycle



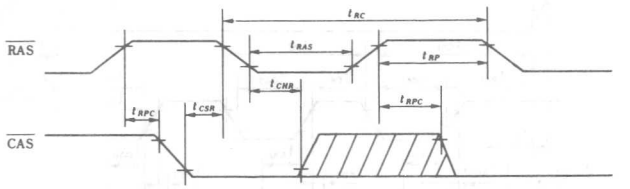
Read-Modify-Write Cycle



RAS-Only Refresh Cycle

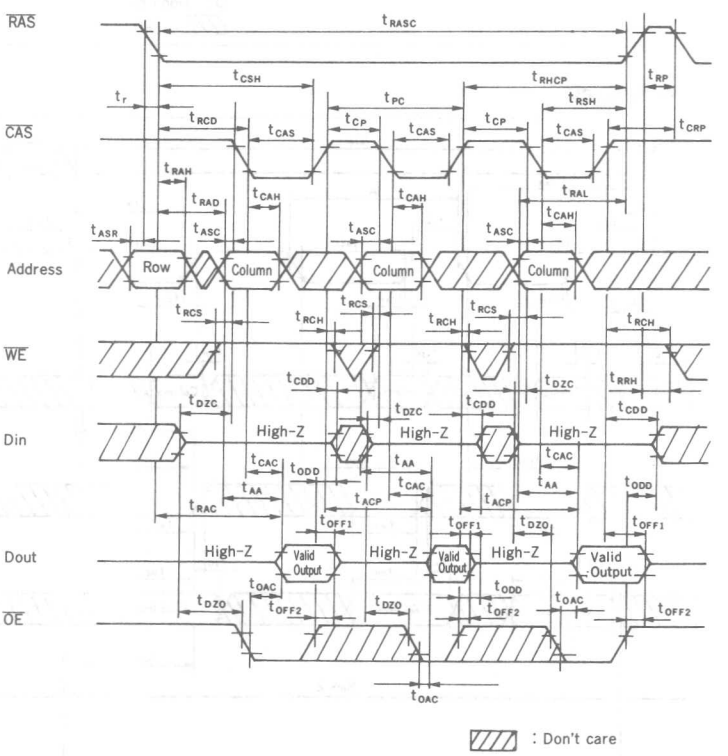


CAS-before-RAS Refresh Cycle



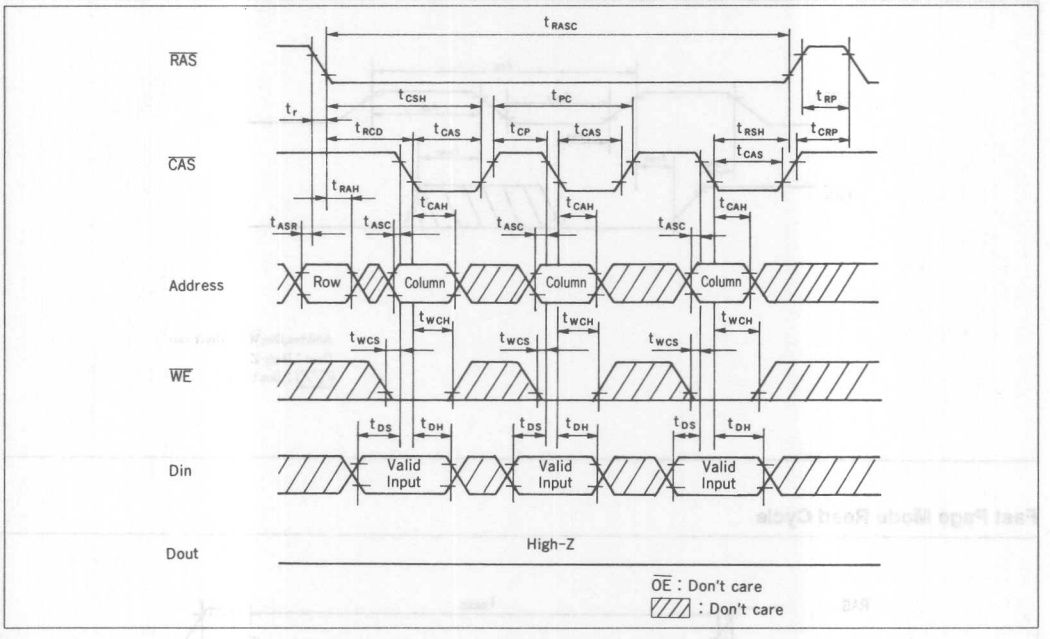
Address, Din, $\overline{WE}$: Don't care
Dout : High-Z
▨ : Don't care

Fast Page Mode Read Cycle

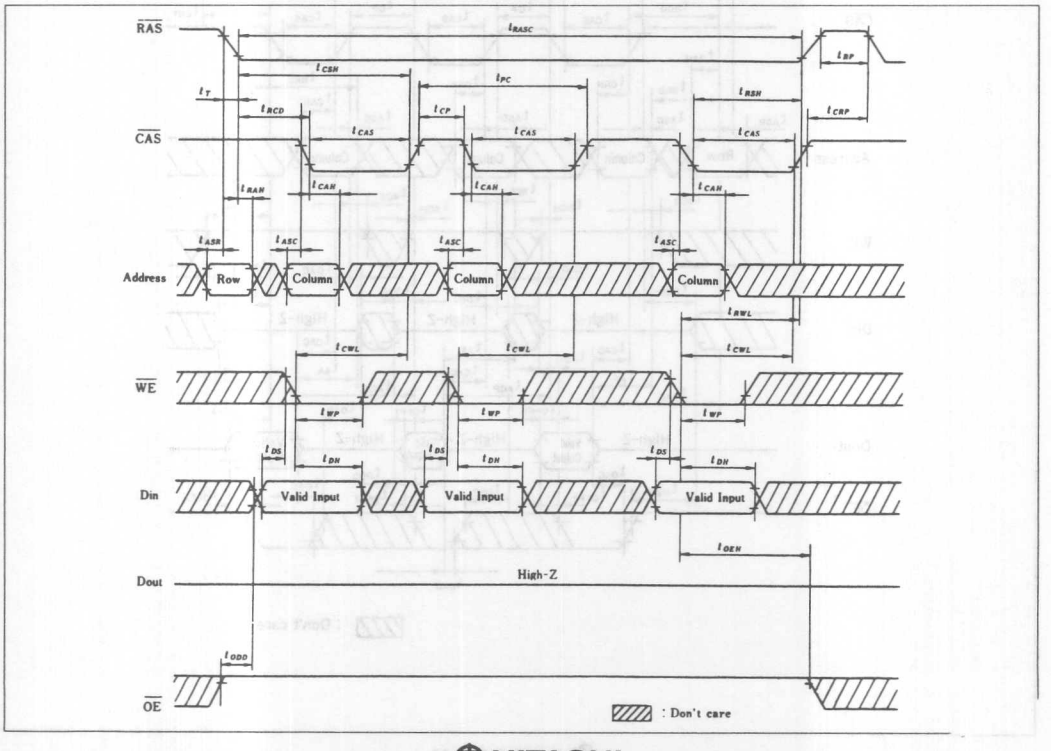


▨ : Don't care

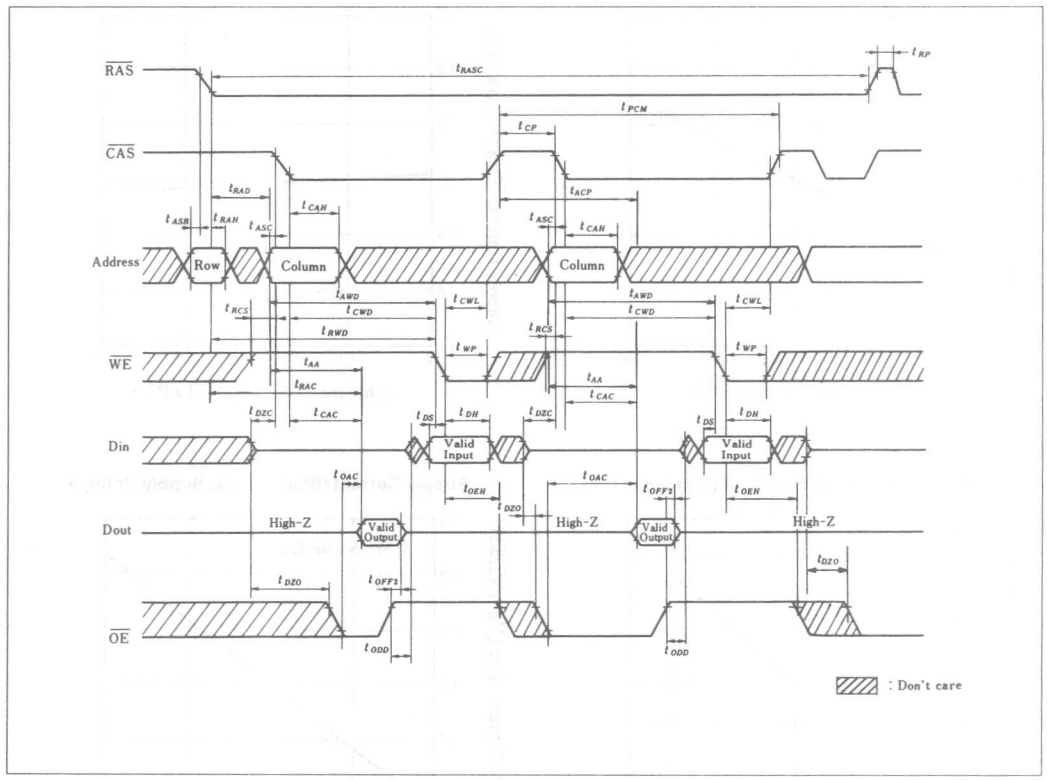
Fast Page Mode Early Write Cycle



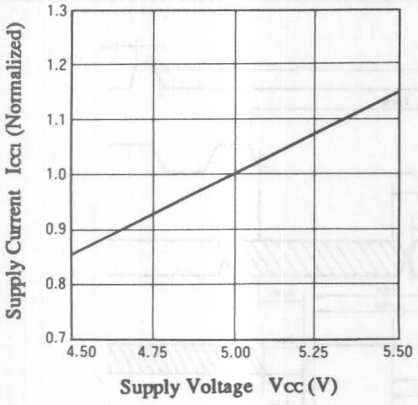
Fast Page Delayed Write Cycle



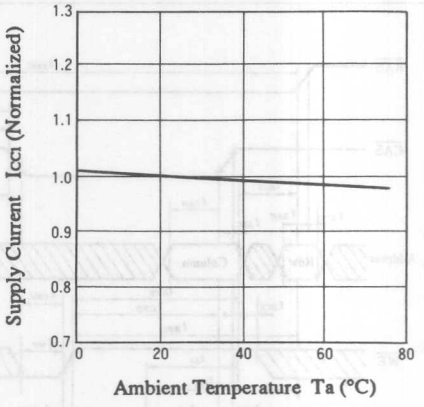
Fast Page Mode Read-Modify-Write Cycle



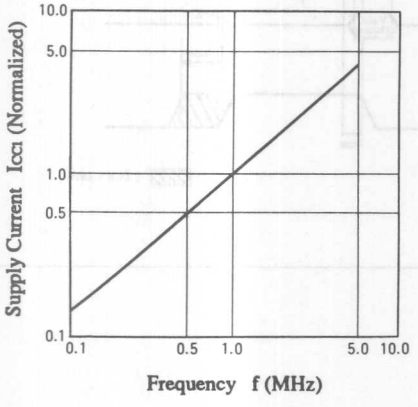
Supply Current (Active) vs. Supply Voltage



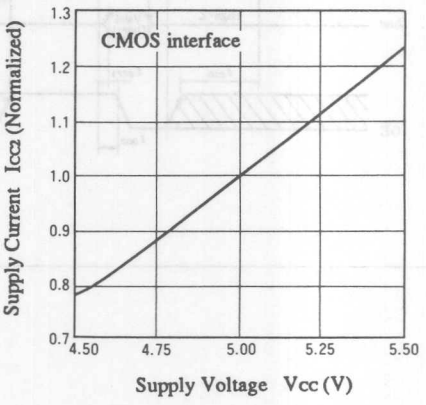
Supply Current (Active) vs. Ambient Temperature



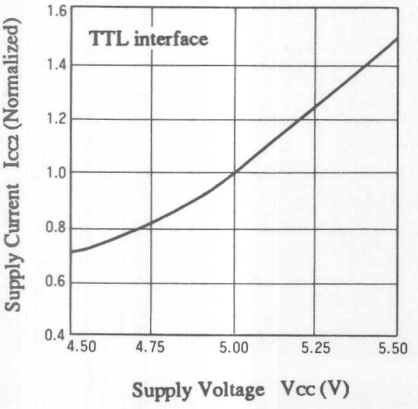
Supply Current (Active) vs. Frequency



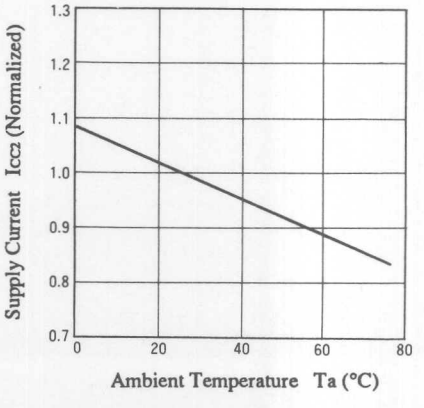
Supply Current (Standby) vs. Supply Voltage



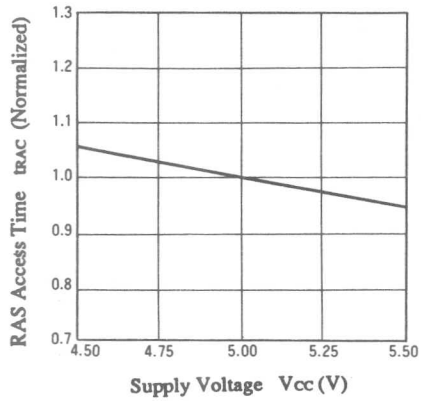
Supply Current (Standby) vs. Supply Voltage



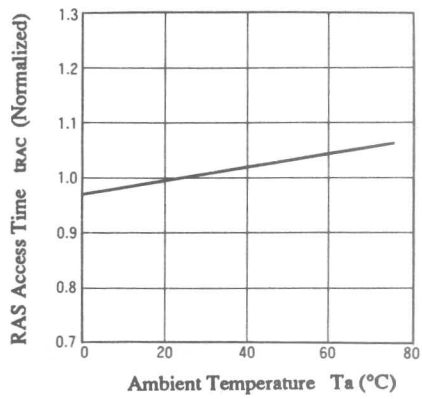
Supply Current (Standby) vs. Ambient Temperature



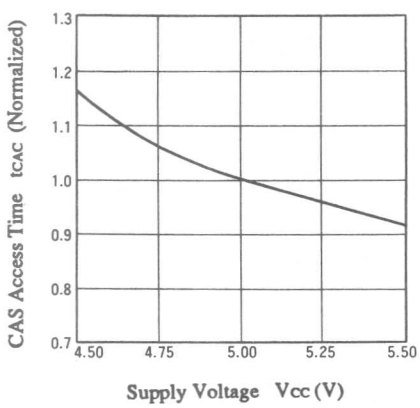
$\overline{RAS}$ Access Time vs. Supply Voltage



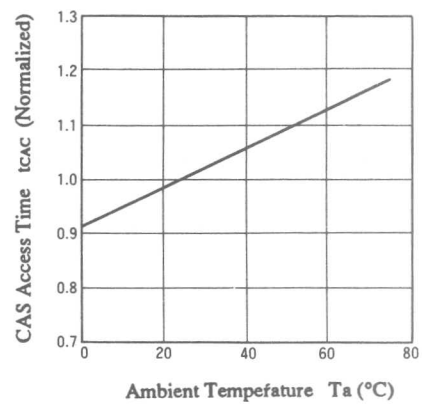
$\overline{RAS}$ Access Time vs. Ambient Temperature



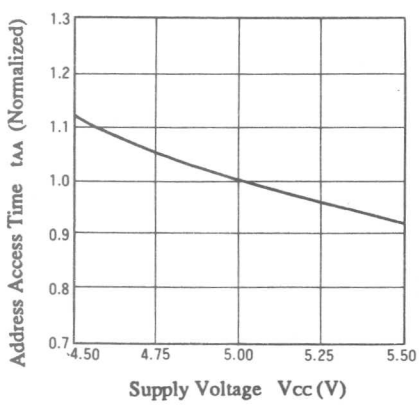
$\overline{CAS}$ Access Time vs. Supply Voltage



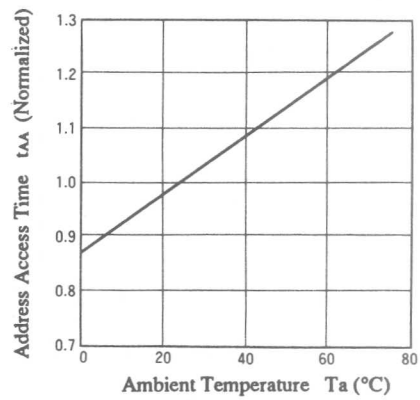
$\overline{CAS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature



HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HM514256API/AJPI/AZPI-6/7/8/10/12 — Preliminary
(Extended Temperature Range Version)

262,144-Word × 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514256A is a CMOS dynamic RAM organized 262,144-word × 4-bit. HM514256A has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM514256A offers Fast Page Mode as a high speed access mode.

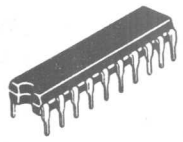
Multiplexed address input permits HM514256A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time . . . . . .60/70/80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .495/440/363/303/259mW (max.)
  - Standby Mode . . . . . .11mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycles . . . . . .(8 ms)
- 2 Variations of Refresh
  - $\overline{\text{RAS}}$-Only Refresh
  - $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

■ ORDERING INFORMATION

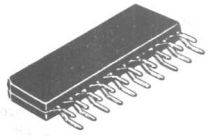
Part No.	Access	Package
HM514256API-6	60ns	300 mil 20 pin Plastic DIP (DP-20NA)
HM514256API-7	70ns	
HM514256API-8	80ns	
HM514256API-10	100ns	
HM514256API-12	120ns	
HM514256AJPI-6	60ns	300 mil 20 pin Plastic SOJ (CP-20D)
HM514256AJPI-7	70ns	
HM514256AJPI-8	80ns	
HM514256AJPI-10	100ns	
HM514256AJPI-12	120ns	
HM514256AZPI-6	60ns	400 mil 20 pin Plastic ZIP (ZP-20)
HM514256AZPI-7	70ns	
HM514256AZPI-8	80ns	
HM514256AZPI-10	100ns	
HM514256AZPI-12	120ns	



(DP-20NA)



(CP-20D)



(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
I/O_1–I/O_4	Data-In/Data-Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	Power Supply (+5.0V)
V_{SS}	Ground

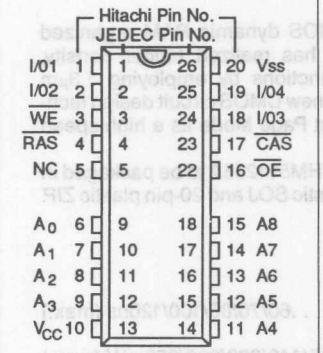
■ PIN ARRANGEMENT

• HM514256AP Series



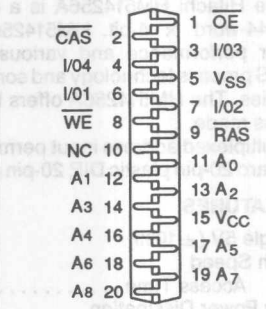
(Top View)

• HM514256AJP Series



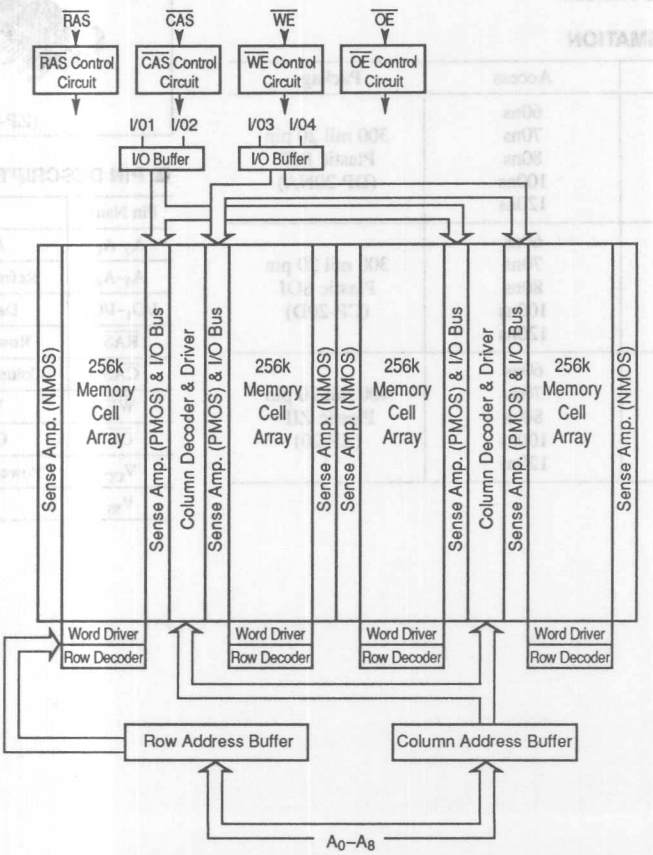
(Top View)

• HM514256AZP Series



(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = −40 to +85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC CHARACTERISTICS (T_a = −40 to +85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = min.	—	90	—	80	—	66	—	55	—	47	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	—	2	—	2	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	1	—	1	—	1	—	1	—	1	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = min.	—	90	—	80	—	66	—	55	—	47	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	5	—	5	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = min.	—	80	—	70	—	66	—	55	—	47	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = min.	—	80	—	70	—	55	—	55	—	47	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-In, Data-Out)	$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = -40°C to 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1], [14]

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Set-Up Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Set-Up Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Delay Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

• Read Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Set-Up Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	10	—	10	—	10	—	10	—	10	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	—	30	—	35	—	40	—	45	—	55	ns	
Output Buffer Turn-Off Time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-Off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

• Write Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-Up Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-In Set-Up Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

• Refresh Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-Up Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

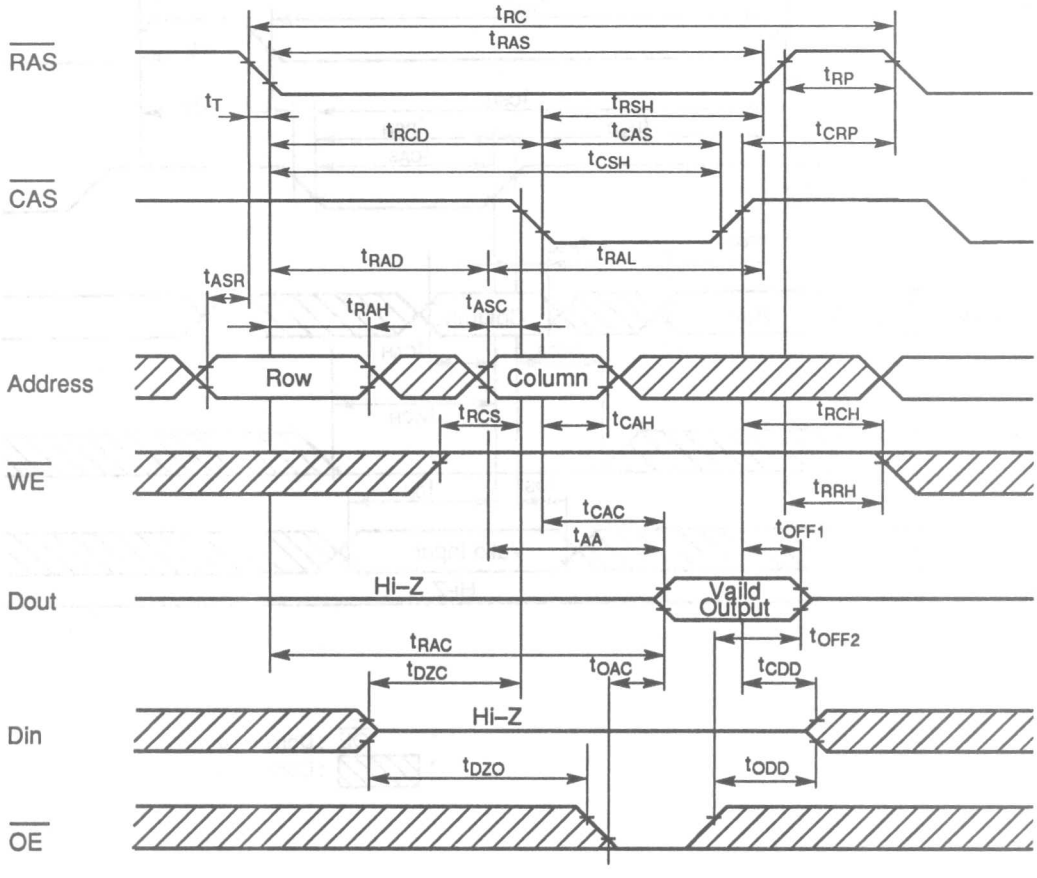
Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Prechart Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	40	—	45	—	50	—	50	—	60	—	ns	
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

NOTES:

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

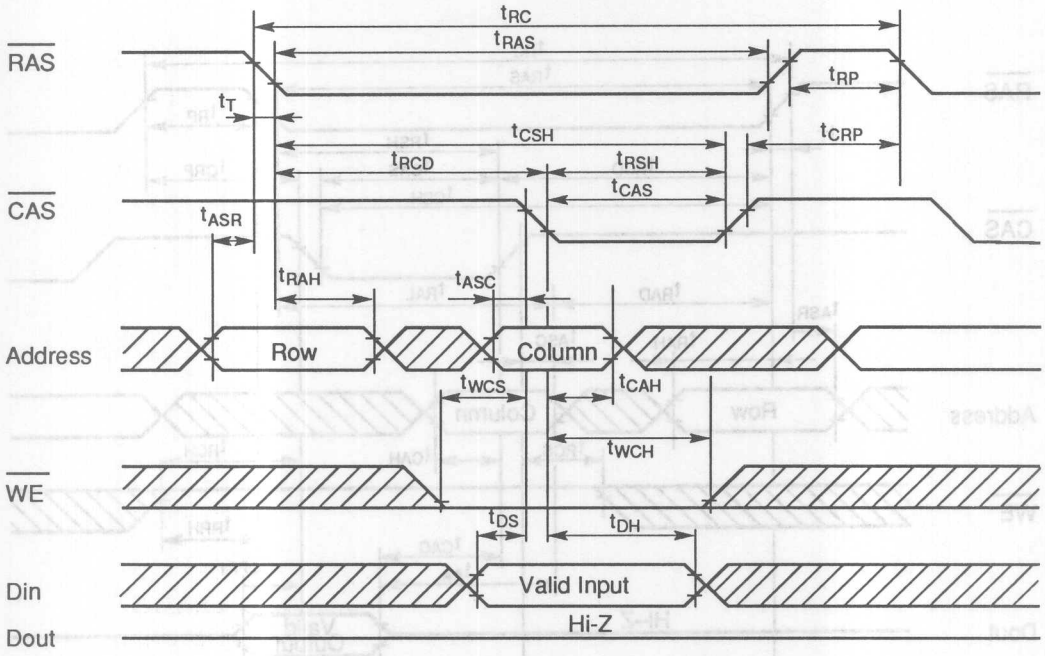
■ TIMING WAVEFORMS

• Read Cycle



* ▨ : Don't care

• **Early Write Cycle**

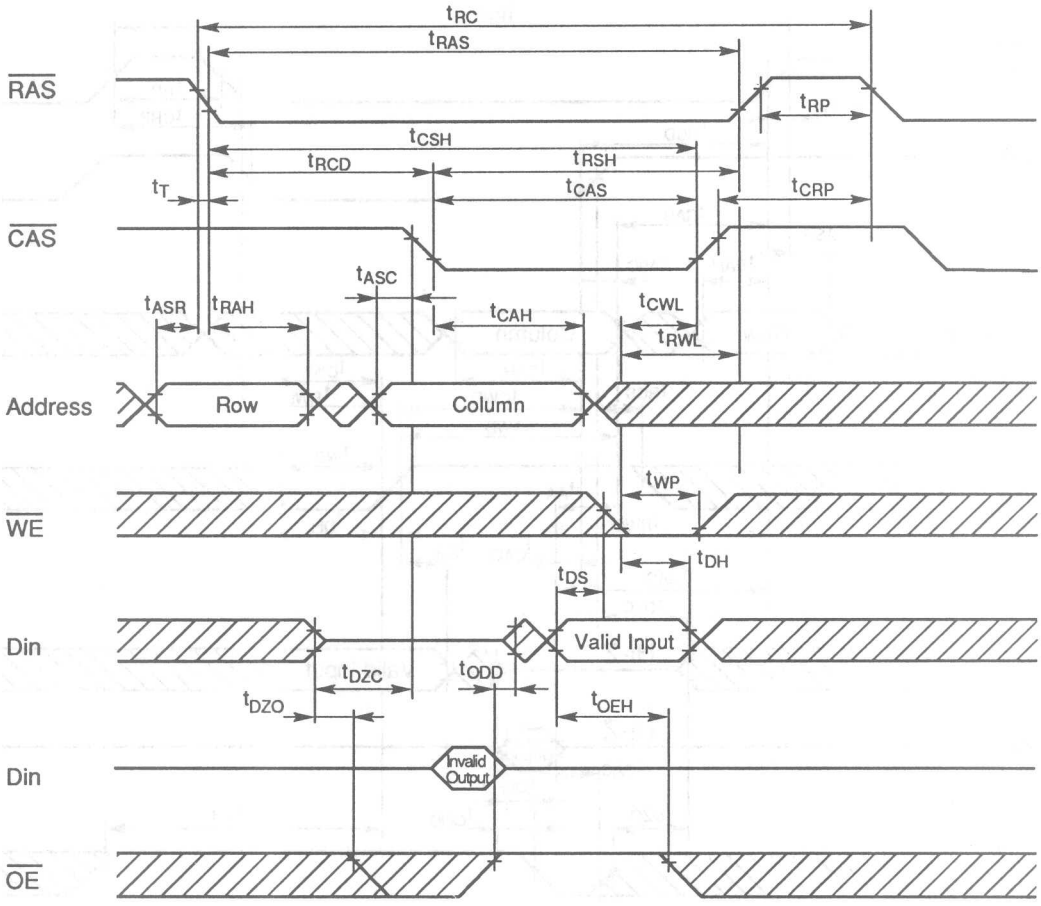


* $\overline{OE}$: Don't care

* ▨ : Don't care

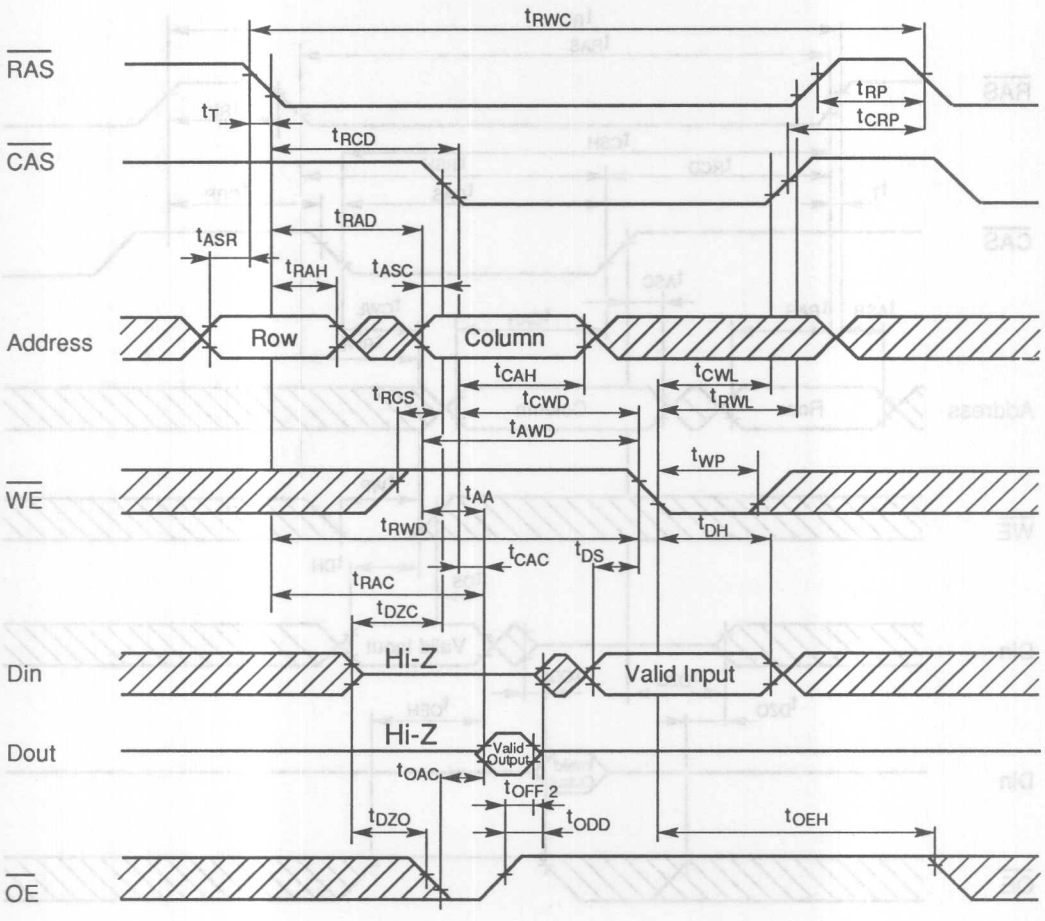
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• **Delayed Write Cycle**



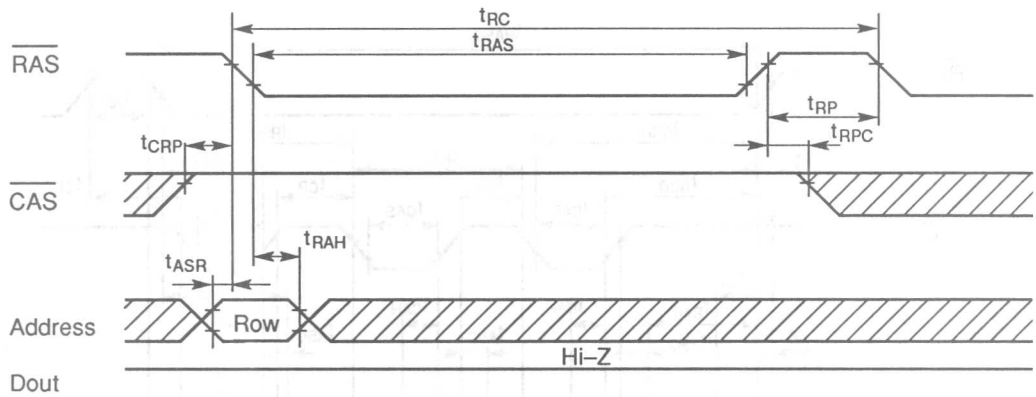
* ▨ : Don't care

• **Read-Modify-Write Cycle**



• : Don't care

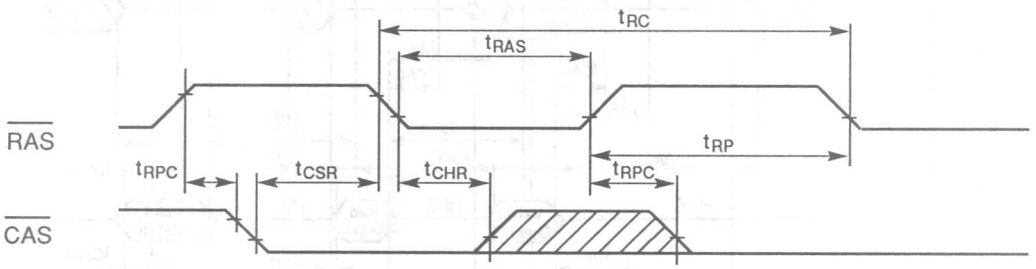
• **$\overline{RAS}$-Only Refresh Cycle**



1 $\overline{OE}$, $\overline{WE}$: Don't care

2 ▨ : Don't care

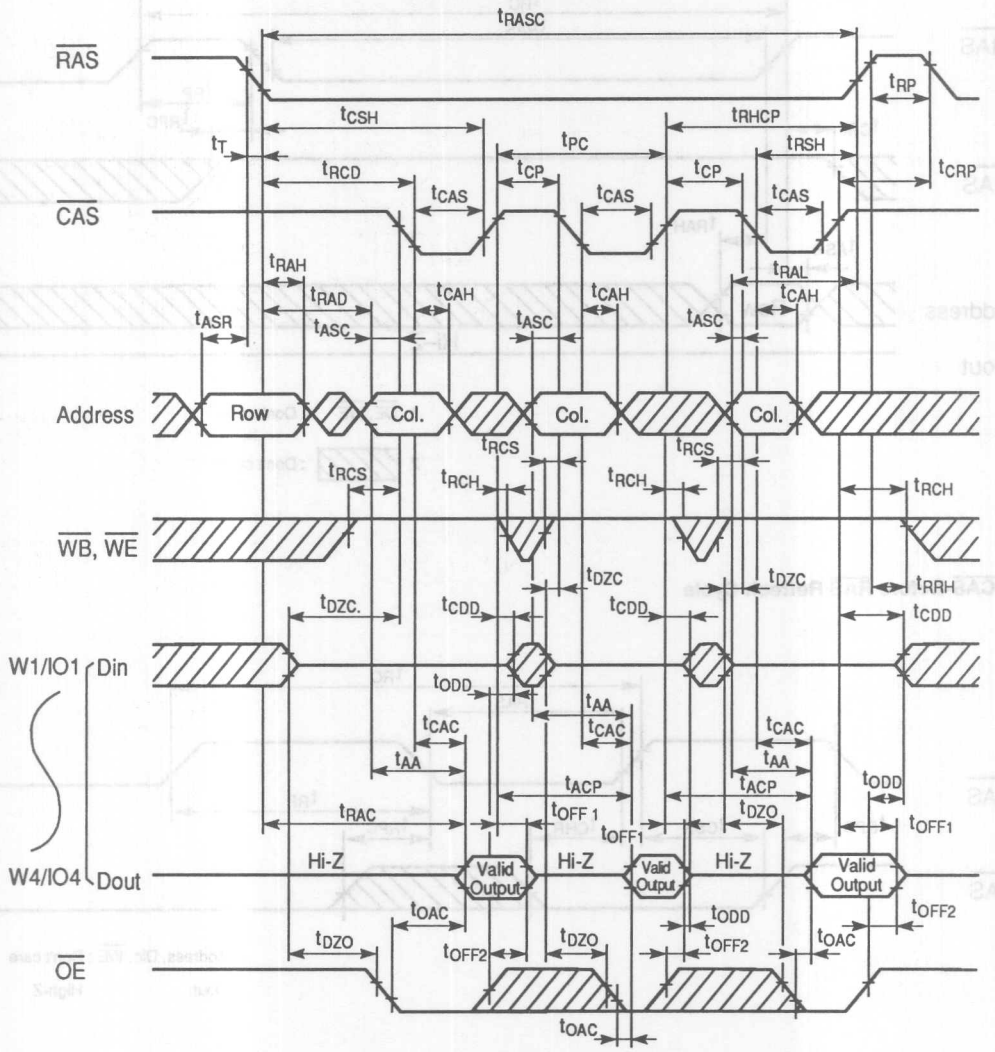
• **$\overline{CAS}$-Before $\overline{RAS}$ Refresh Cycle**



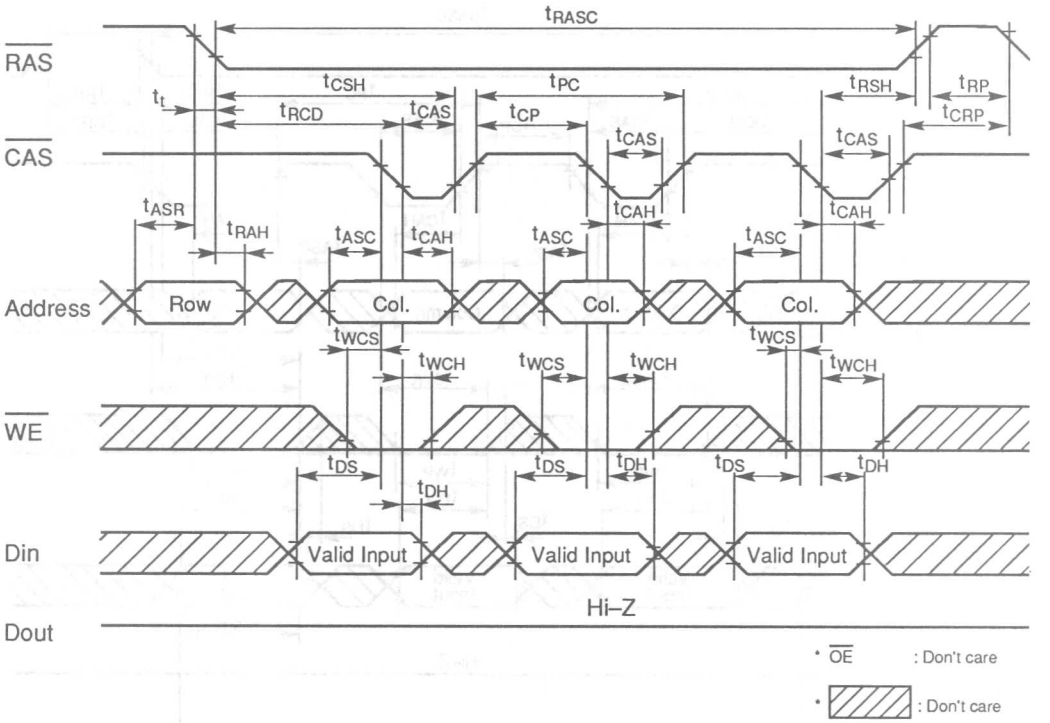
Address, Din, $\overline{WE}$: Don't care

Dout: High-Z

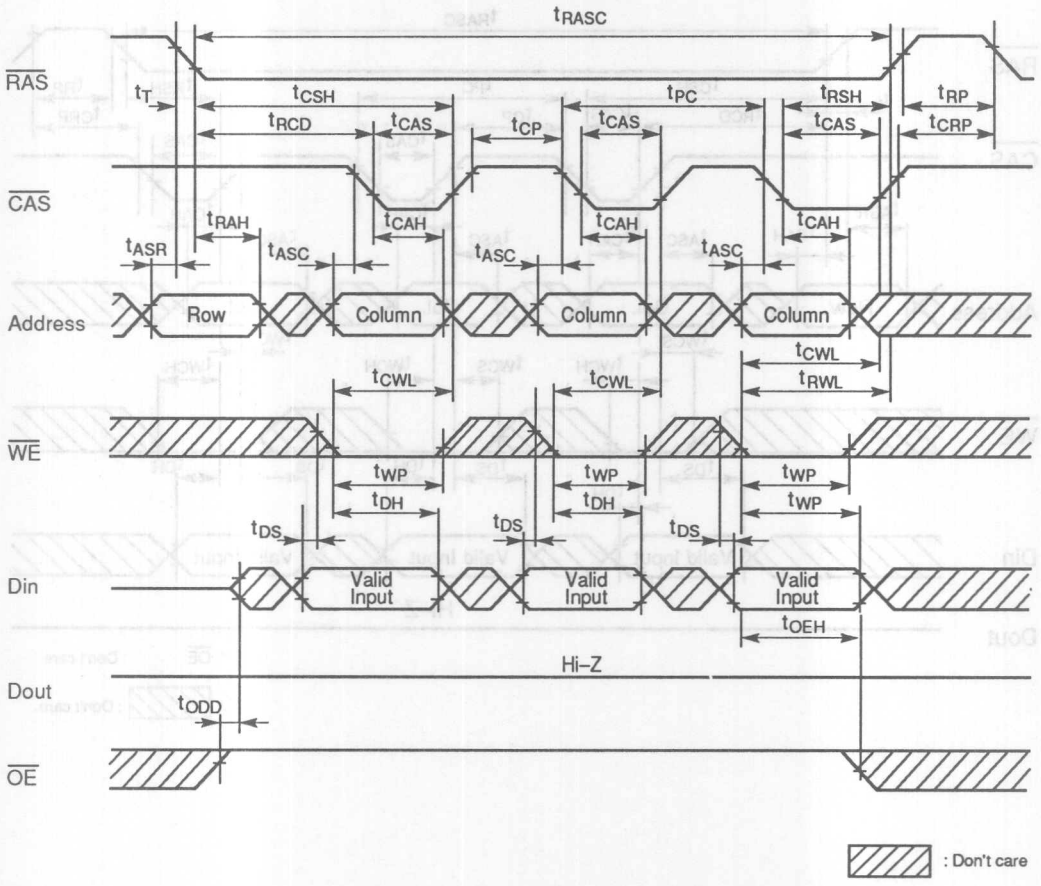
• **Fast Page Mode Read Cycle**



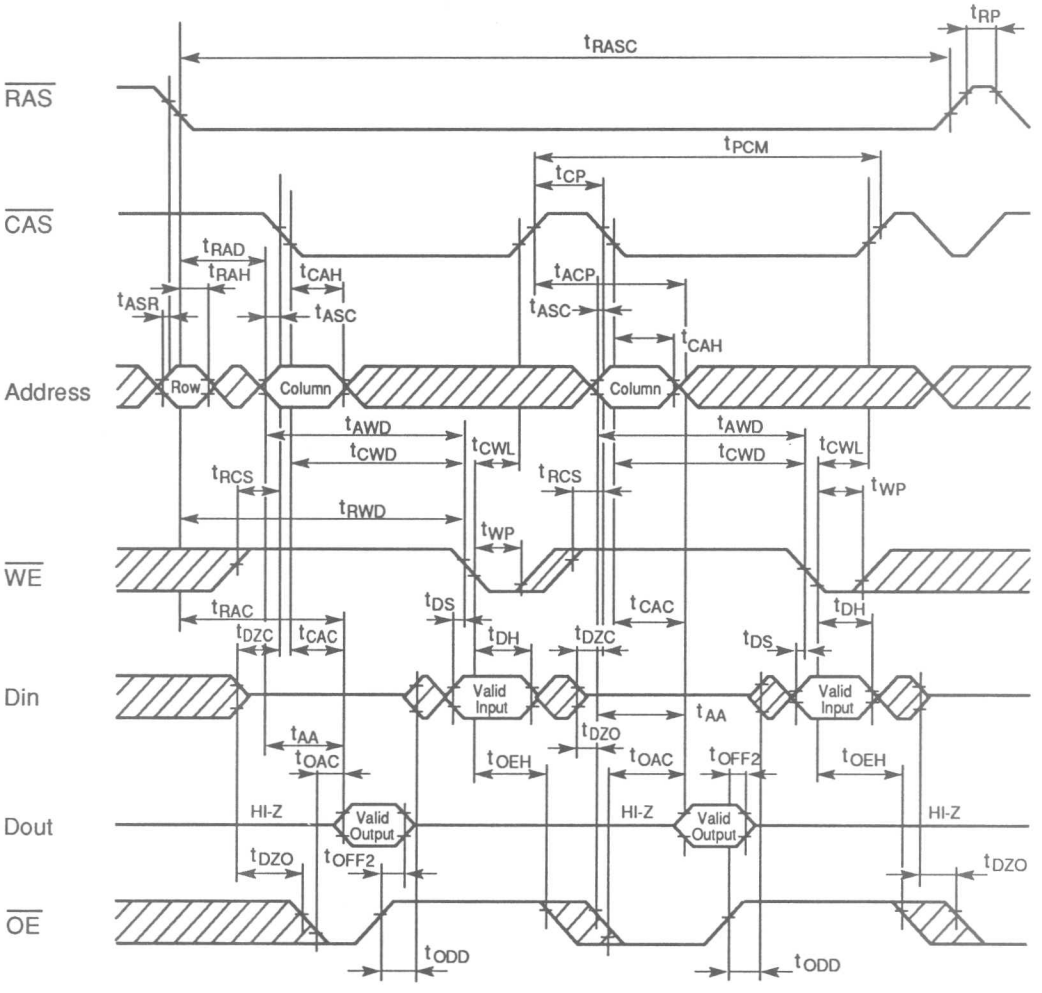
• **Fast Page Mode Early Write Cycle**



• **Fast Page Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



HM514256ALP/ALJP/ALZP-8/10/12 — Preliminary

262,144-Word × 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514256ALP/ALJP/ALZP family is a CMOS dynamic RAM organized 262,144-word × 4-bit. HM514256ALP/ALJP/ALZP has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM514256ALP/ALJP/ALZP offers Fast Page Mode as a high speed access mode.

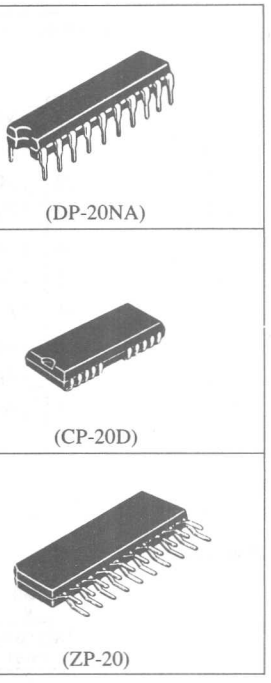
Multiplexed address input permits HM514256ALP/ALJP/ALZP to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time . . . . . .80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .363/303/259mW (max.)
  - Standby Mode . . . . . .1.7mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycles . . . . . .(64 ms)
- 2 Variations of Refresh
  - $\overline{\text{RAS}}$-Only Refresh
  - $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

■ ORDERING INFORMATION

Part No.	Access	Package
HM514256ALP-8	80ns	300 mil 20 pin Plastic DIP (DP-20NA)
HM514256ALP-10	100ns	
HM514256ALP-12	120ns	
HM514256ALJP-8	80ns	300 mil 20 pin Plastic SOJ (CP-20D)
HM514256ALJP-10	100ns	
HM514256ALJP-12	120ns	
HM514256ALZP-8	80ns	400 mil 20 pin Plastic ZIP (ZP-20)
HM514256ALZP-10	100ns	
HM514256ALZP-12	120ns	



(DP-20NA)

(CP-20D)

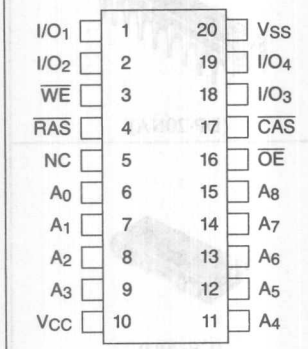
(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
I/O_1–I/O_4	Data-In/Data-Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	Power Supply (+5.0V)
V_{SS}	Ground

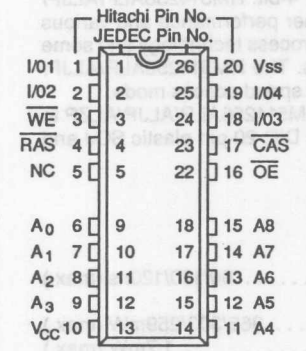
■ PIN ARRANGEMENT

• HM514256ALP Series



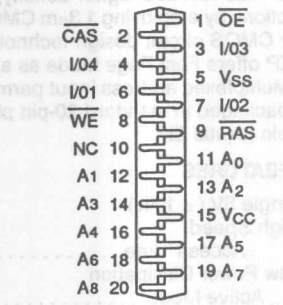
(Top View)

• HM514256ALJP Series



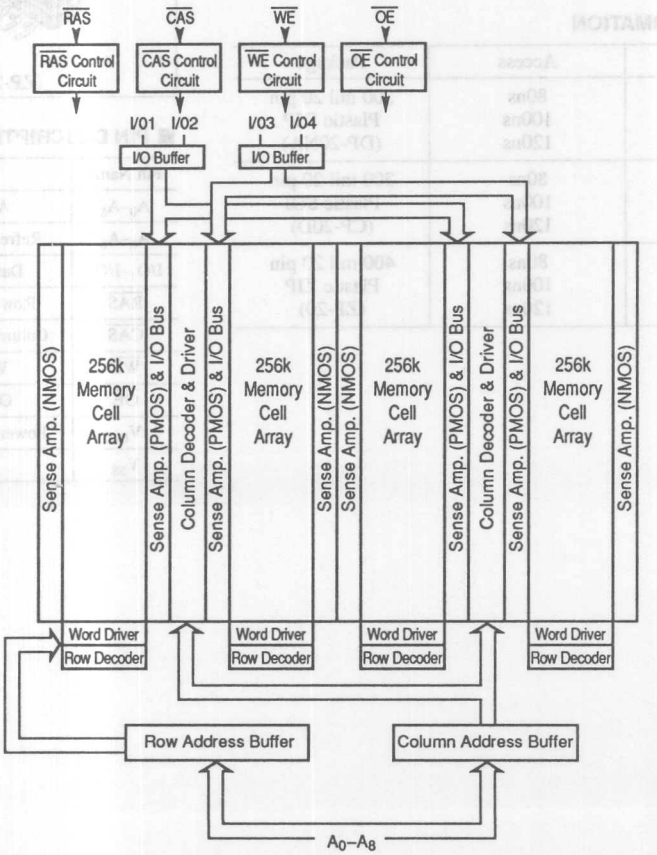
(Top View)

• HM514256ALZP Series



(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = min.	—	66	—	55	—	47	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High Z	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{OUT} = High Z	—	300	—	300	—	300	μA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = min.	—	66	—	55	—	47	mA	2
Battery Back-Up Current	I_{CC4}	t_{RC} = 125μs, $\overline{CAS}$ Before $\overline{RAS}$ Cycling	—	300	—	300	—	300	μA	4
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	66	—	55	—	47	mA	1
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	55	—	55	—	47	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} = t_{RAS} min. to 1 μs
Input voltage: I/O pin ≥ V_{CC} − 0.2V or ≤ 0.2V or open; Others ≥ V_{CC} − 0.2V or ltet 0.2V

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-In, Data-Out)	$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1], [14]

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-Up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-Up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Delay Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	64	—	64	—	64	ms	

• Read Cycle

Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF1}	—	20	—	25	—	30	ns	6
Output Buffer Turn-Off to $\overline{OE}$	t_{OFF2}	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

• Write Cycle

Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	ns	11	

• Read-Modify-Write Cycle

Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Write Cycle Time	t_{RWC}	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

• Refresh Cycle

Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

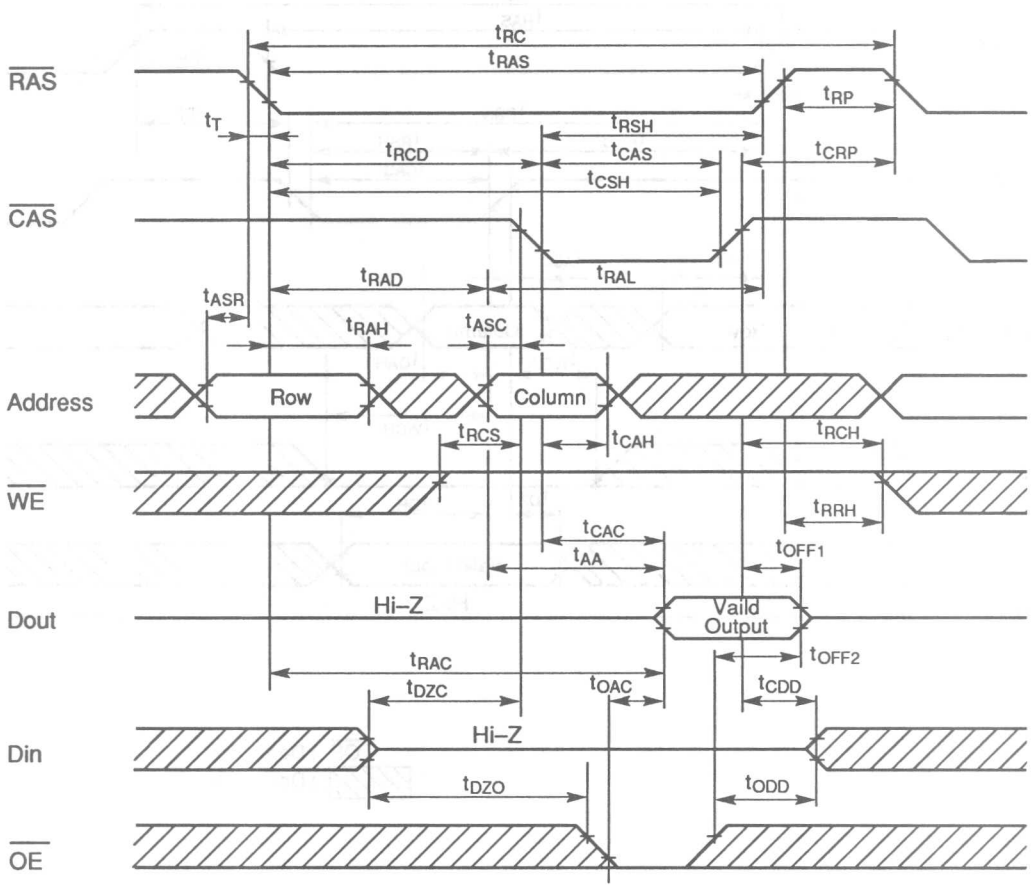
Parameter	Symbol	HM514256AL-8		HM514256AL-10		HM514256AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PCM}	110	—	115	—	135	—	ns	

NOTES:

1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

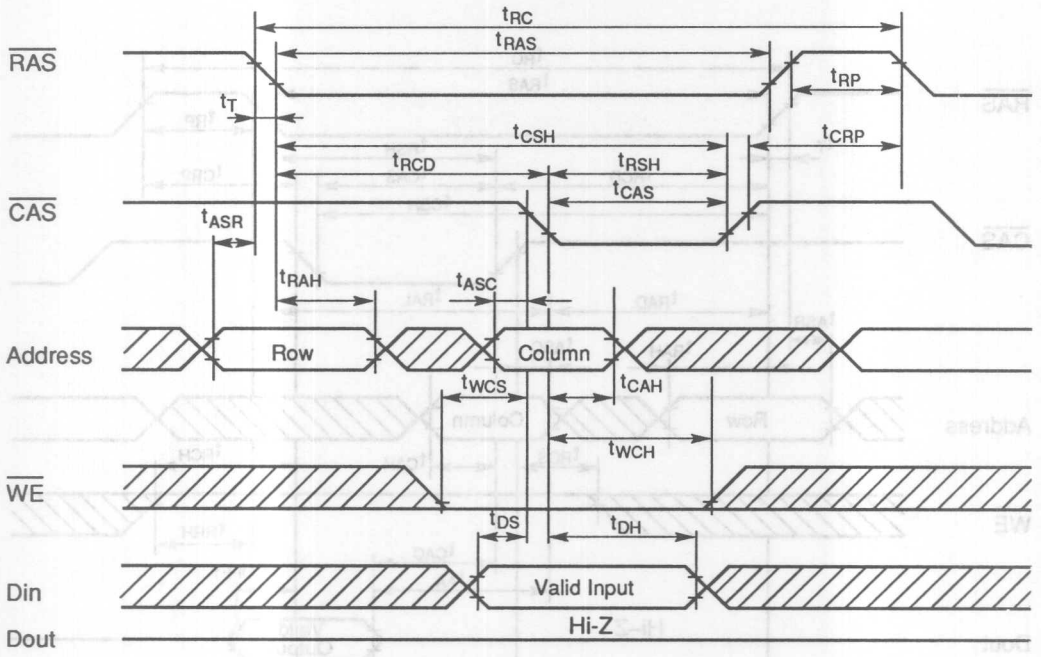
■ TIMING WAVEFORMS

• Read Cycle



* : Don't care

• **Early Write Cycle**

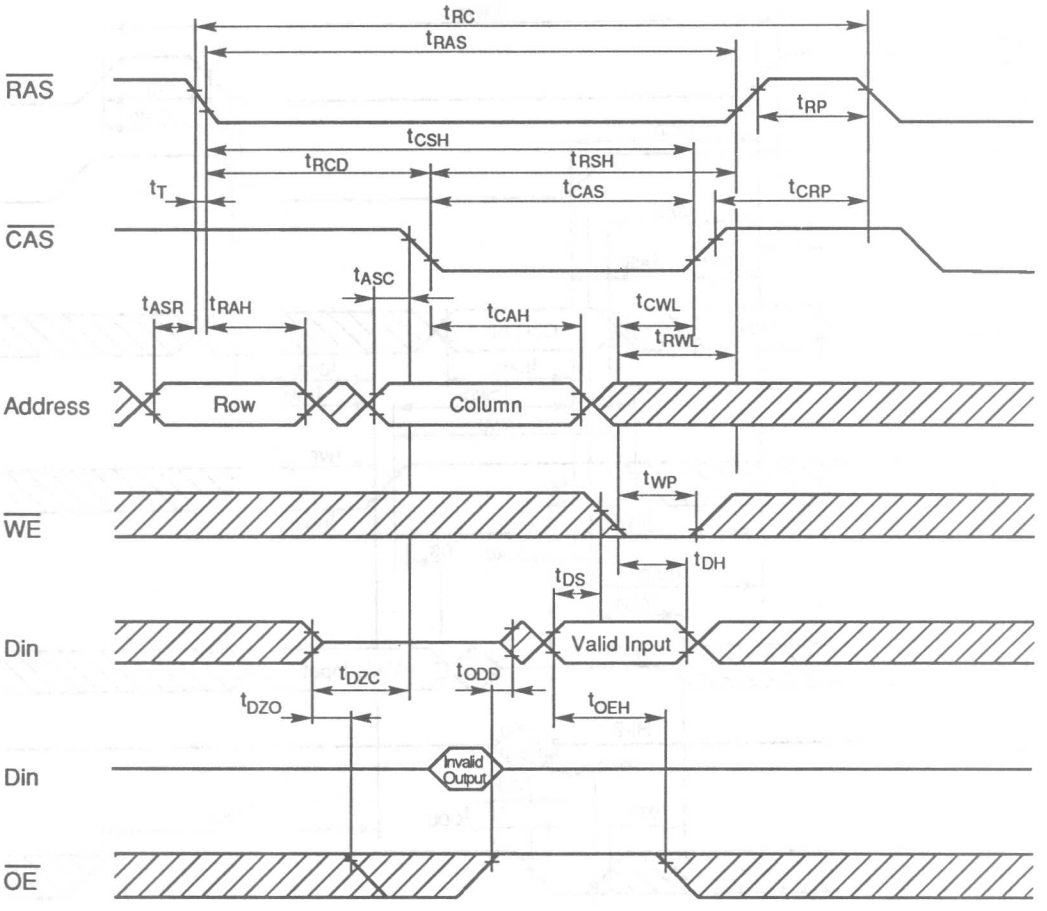


* $\overline{OE}$: Don't care

* ▨ : Don't care

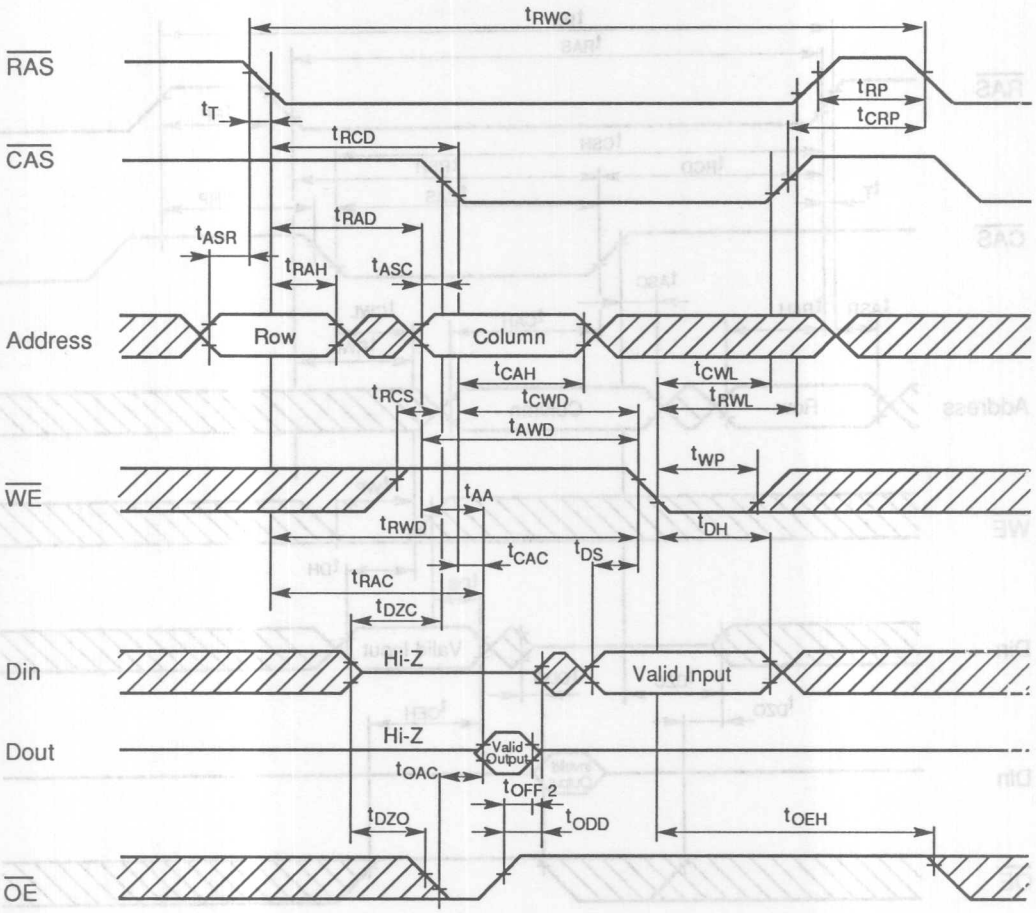
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• **Delayed Write Cycle**



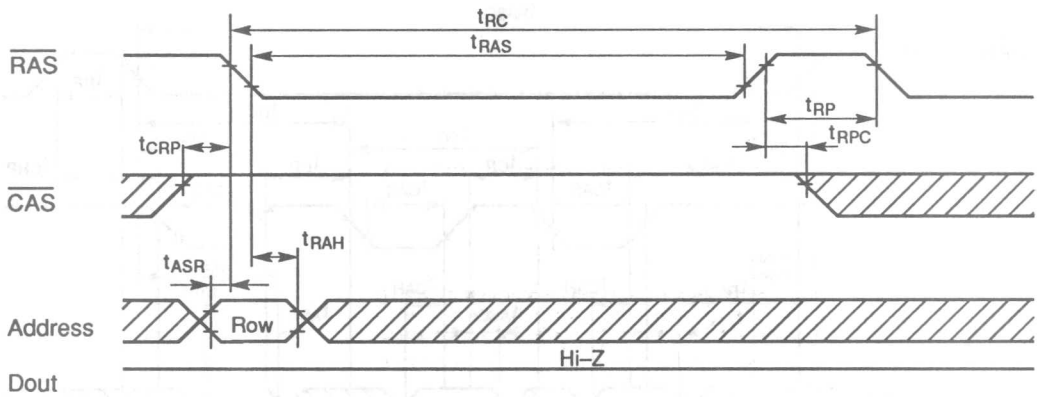
* ▨ : Don't care

• **Read-Modify-Write Cycle**



• : Don't care

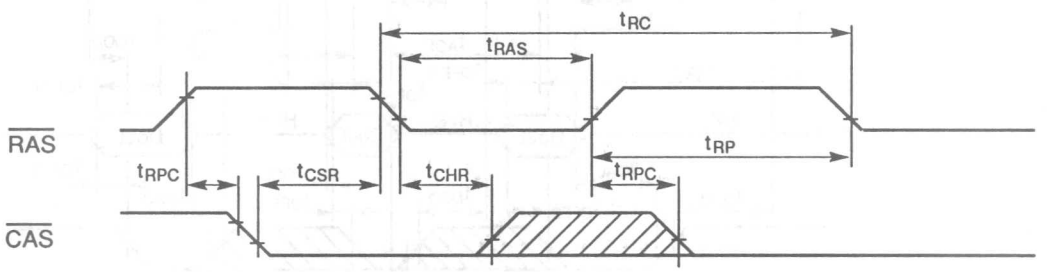
• $\overline{RAS}$-Only Refresh Cycle



1 $\overline{OE}$, $\overline{WE}$: Don't care

2 : Don't care

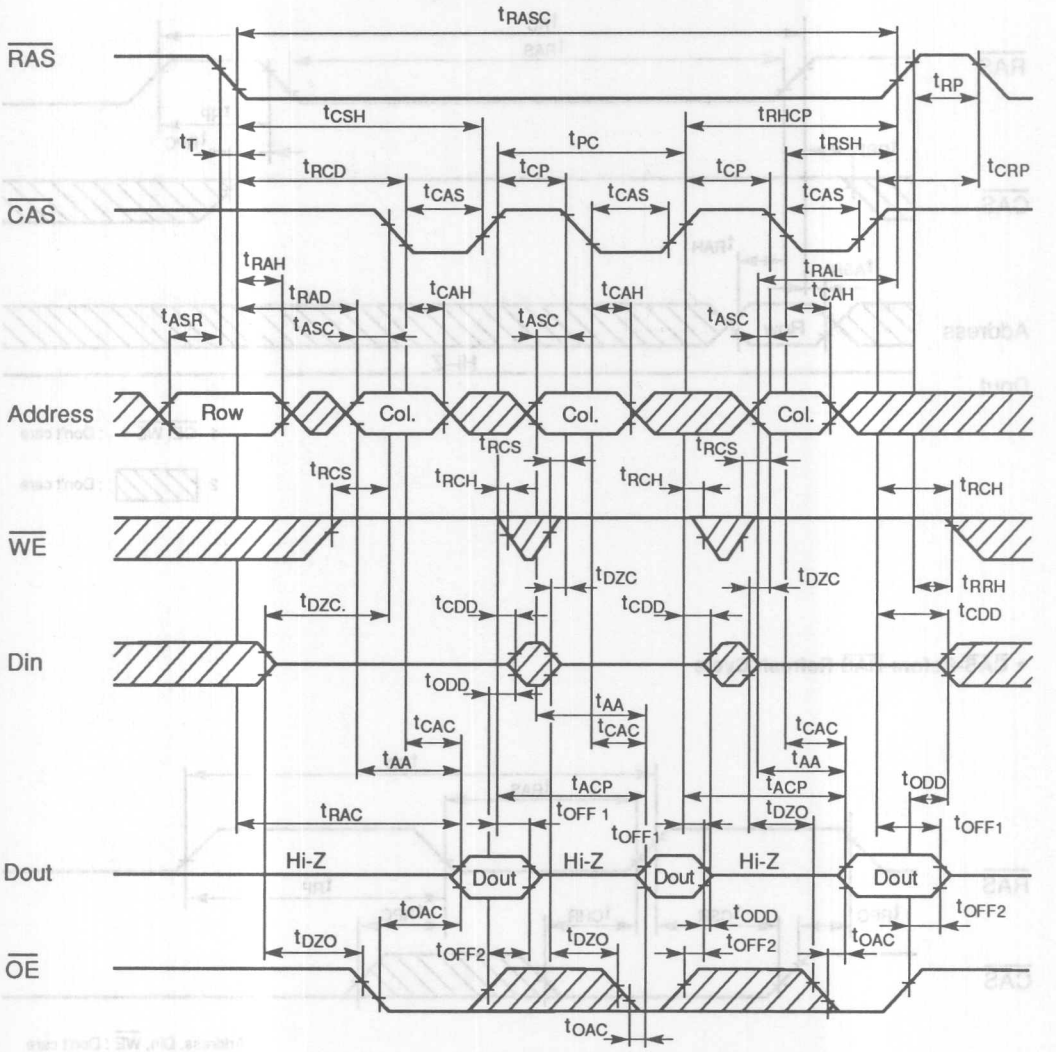
• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



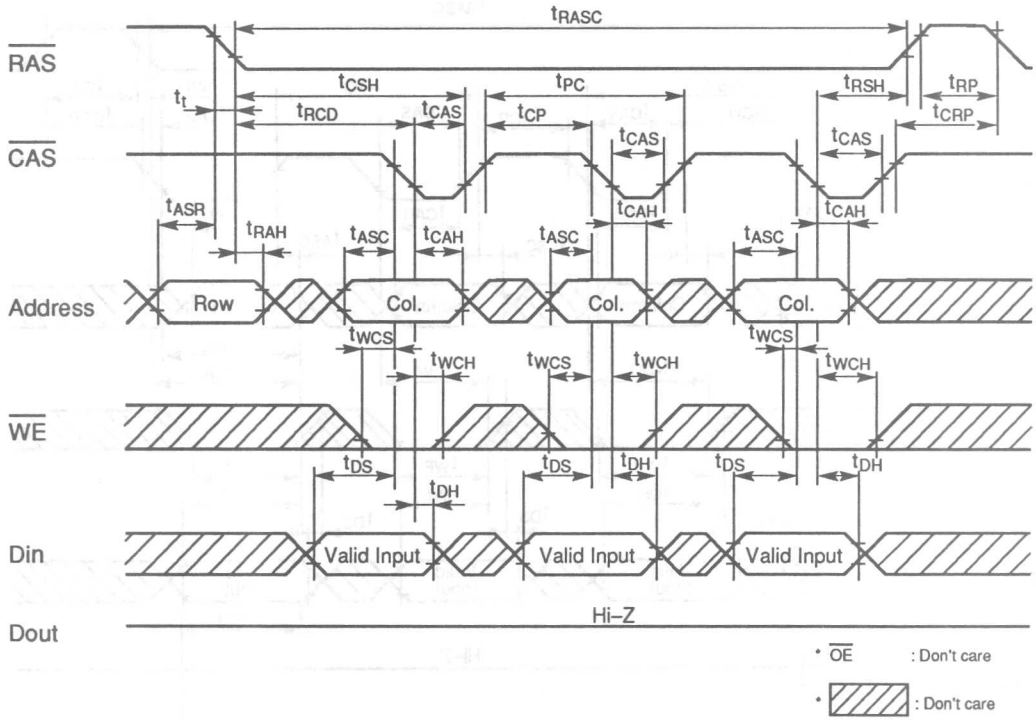
Address, Din, $\overline{WE}$: Don't care

Dout: High-Z

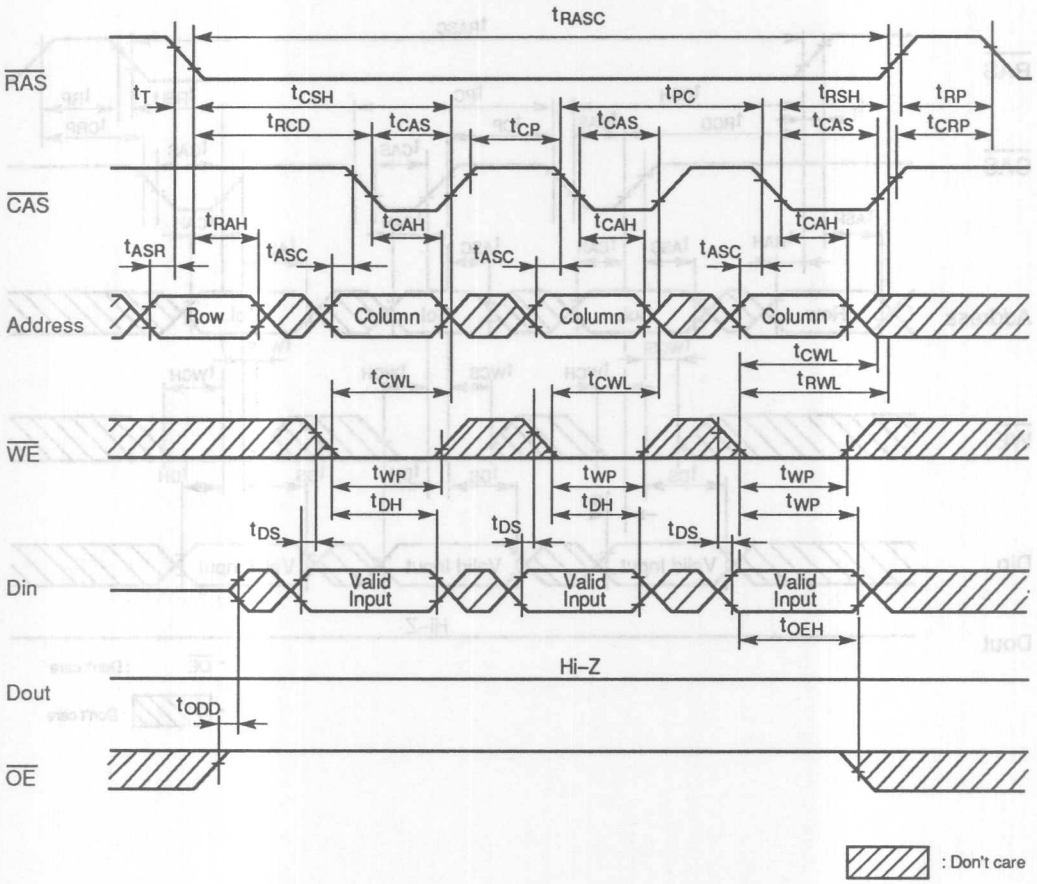
• **Fast Page Mode Read Cycle**



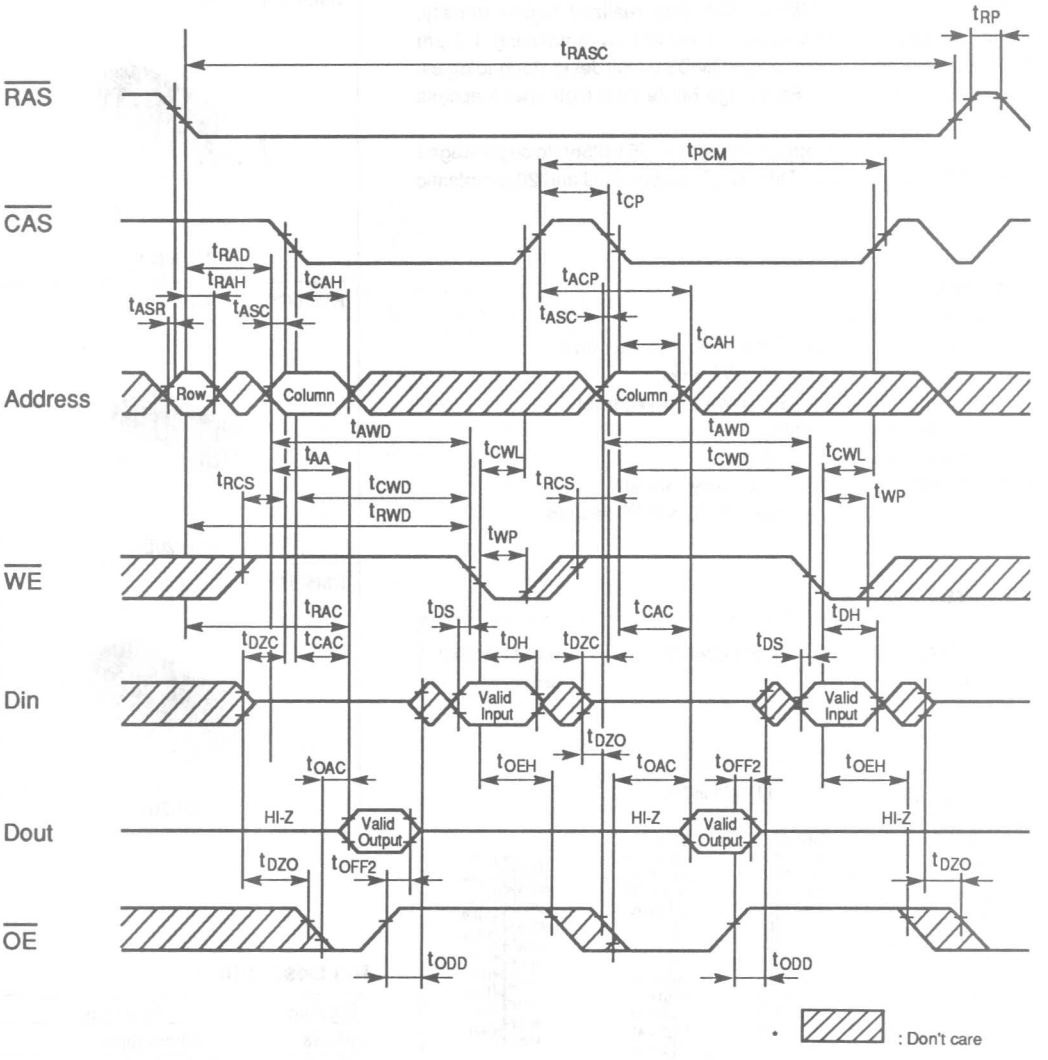
• **Fast Page Mode Early Write Cycle**



• **Fast Page Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



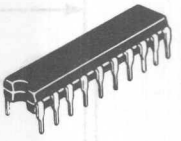
HM514256H Series

262144-Word × 4-Bit CMOS Dynamic RAM

The Hitachi HM514256H is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256H has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514256H offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514256H to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514256HP Series



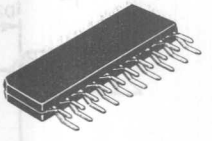
(DP-20NA)

HM514256HJP Series



(CP-20D)

HM514256HZP Series

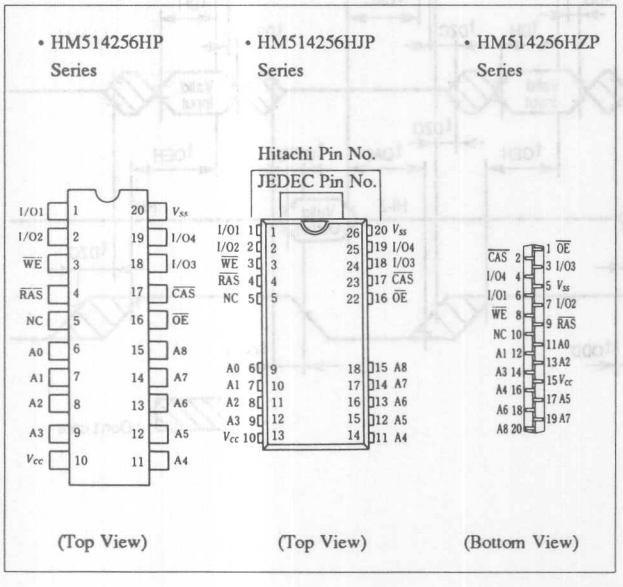


(ZP-20)

Features

- Single 5 V (±10%)
- High speed: Access Time 60 ns/70 ns (max)
- Low power: Standby 11 mW (max)
  Active 495 mW/440 mW (max)
- Fast page mode capability
- 512 refresh cycles: (8 ms)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

Pin Arrangement



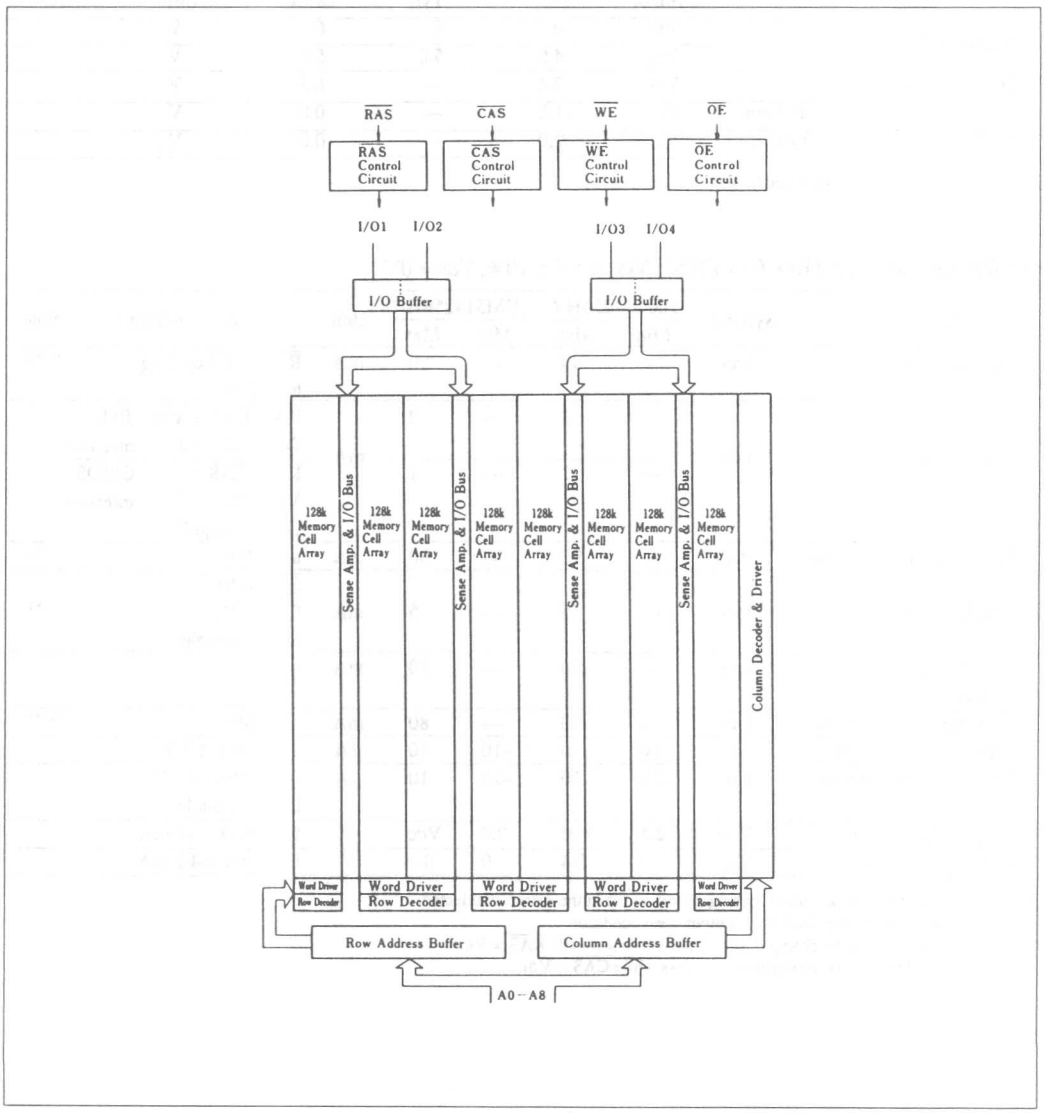
Pin Description

Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM514256HP-6	60 ns	300-mil 20-pin plastic DIP (DP-20NA)
HM514256HP-7	70 ns	
HM514256HJP-6	60 ns	300-mil 20-pin plastic SOJ (CP-20D)
HM514256HJP-7	70 ns	
HM514256HZP-6	60 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514256HZP-7	70 ns	

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–1.0 to +7.0	V
Supply voltage relative to Vss	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		Vss	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	*1
Input high voltage		V_{IH}	2.4	—	6.5	V	*1
Input low voltage	I/O pin	V_{IL}	–1.0	—	0.8	V	*1
	Others	V_{IL}	–2.0	—	0.8	V	*1

Note: *1. All voltage referenced to Vss.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, Vss = 0V)

Item	Symbol	HM514256H-6 Min	HM514256H-6 Max	HM514256H-7 Min	HM514256H-7 Max	Unit	Test Conditions	Note
Operating current	I_{CC1}	—	90	—	80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	*1, *2
Standby current	I_{CC2}	—	2	—	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} TTL interface Dout = High-Z	
		—	1	—	1		$\overline{RAS}$, $\overline{CAS}$ ≥ Vcc-0.2V CMOS interface Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	mA	t_{RC} = Min	*2
Standby current	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	*1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	mA	t_{RC} = Min	
Fast page mode current	I_{CC7}	—	90	—	80	mA	t_{PC} = Min	*1, *3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	Vcc	2.4	Vcc	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Item		Symbol	Typ	Max	Unit	Note
Input capacitance	Address	C_{I1}	—	5	pF	*1
	Clock	C_{I2}	—	7	pF	*1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	—	10	pF	*1, *2

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2 $\overline{CAS}$ = W_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*14

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514256H-6		HM514256H-7		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	125	—	140	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ to RAS precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	*1, *7
Refresh period	t_{REF}	—	8	—	8	ms	

Read Cycle

Item	Symbol	HM514256H-6		HM514256H-7		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	ns	*3, *4
Access time from address	t_{AA}	—	30	—	35	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Output buffer turn-off time	t_{OFF1}	—	20	—	20	ns	*6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	ns	*6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	20	—	ns	

Write Cycle

Item	Symbol	HM514256H-6		HM514256H-7		Unit	Note
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	*10
Write command hold time	t_{WCH}	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	*11
Data-in hold time	t_{DH}	15	—	15	—	ns	*11

Read-Modify-Write Cycle

Item	Symbol	HM514256H-6		HM514256H-7		Unit	Note
		Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	175	—	190	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	—	95	—	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	55	—	60	—	ns	*10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM514256H-6		HM514256H-7		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	15	—	15	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	

Fast Page Mode Cycle

Item	Symbol	HM514256H-6		HM514256H-7		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	45	—	50	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	ns	*12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	ns	*13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	ns	
Fast page mode read-write cycle time	t_{PCM}	90	—	100	—	ns	

Notes: *1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

*5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).

*6. t_{OFF}(max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between V_{IH} and V_{IL}.

*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusiviely by t_{AA}.

*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-wirte cycles.

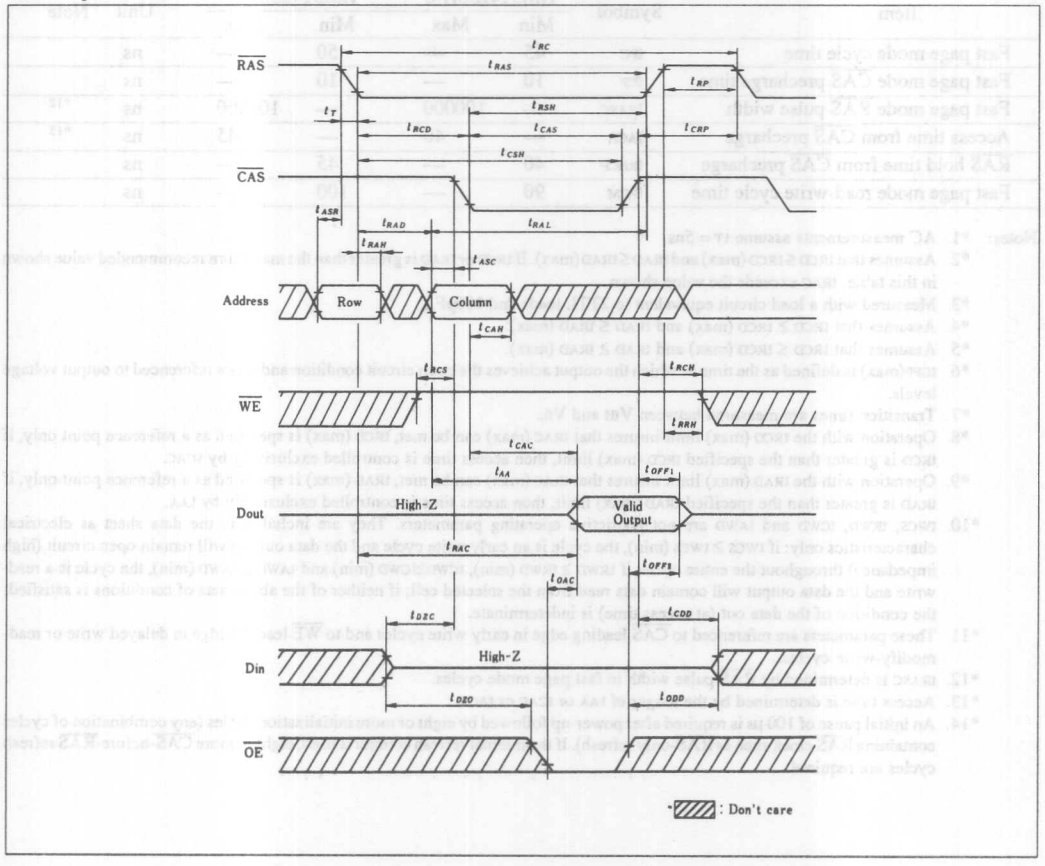
*12. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.

*13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.

*14. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

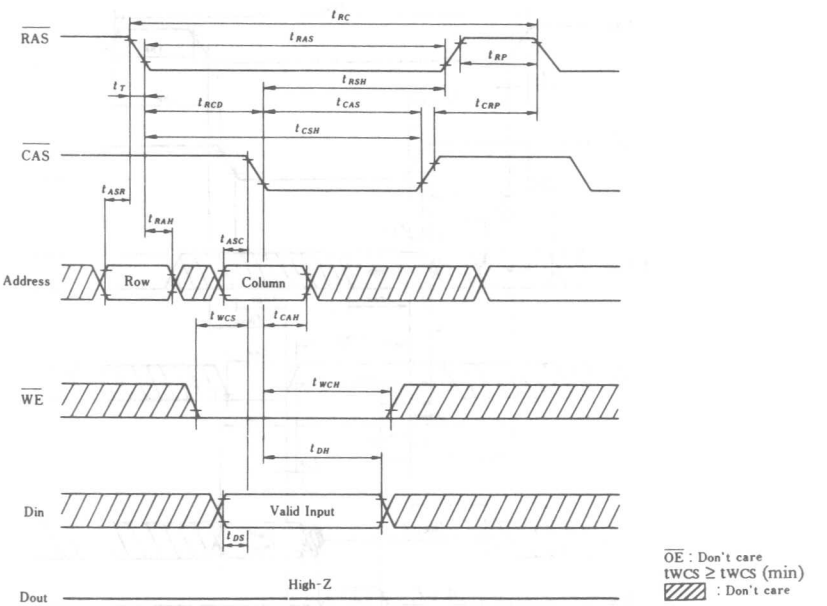
Timing Waveforms

Read Cycle

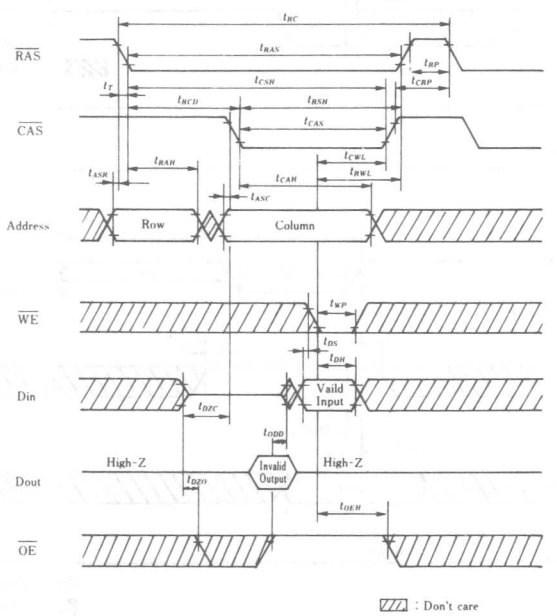


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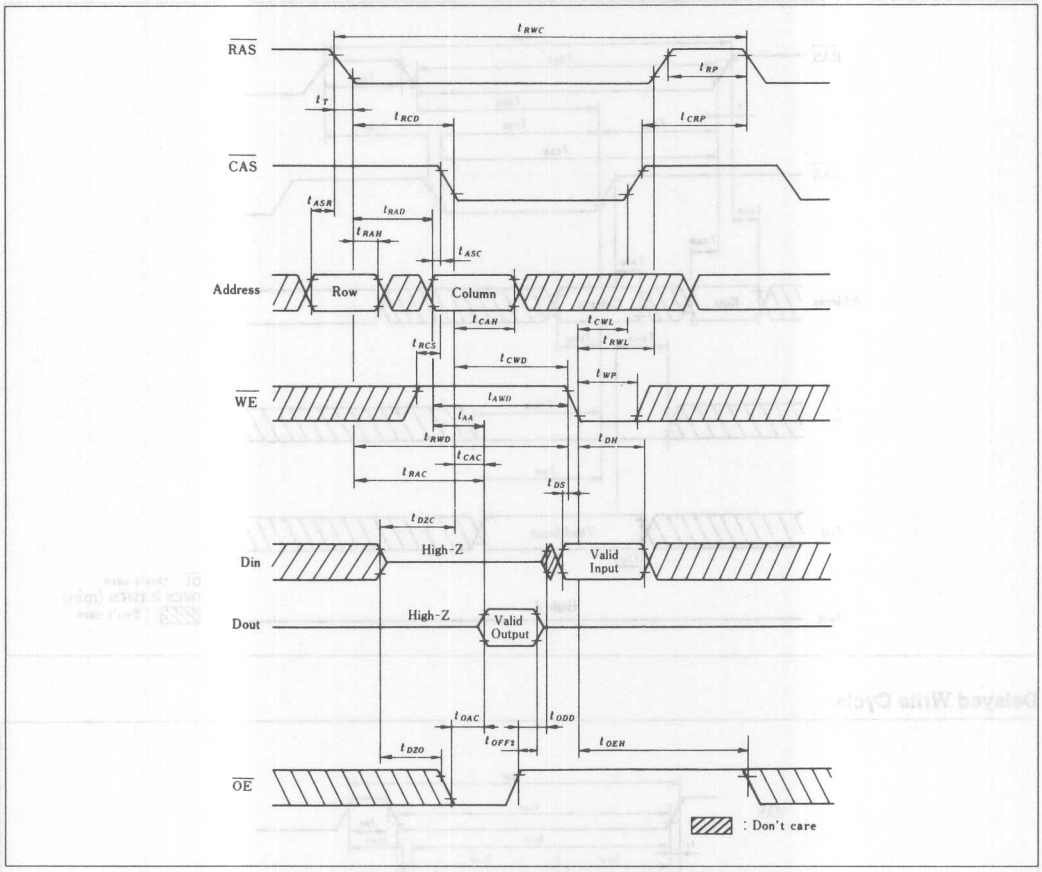
Early Write Cycle



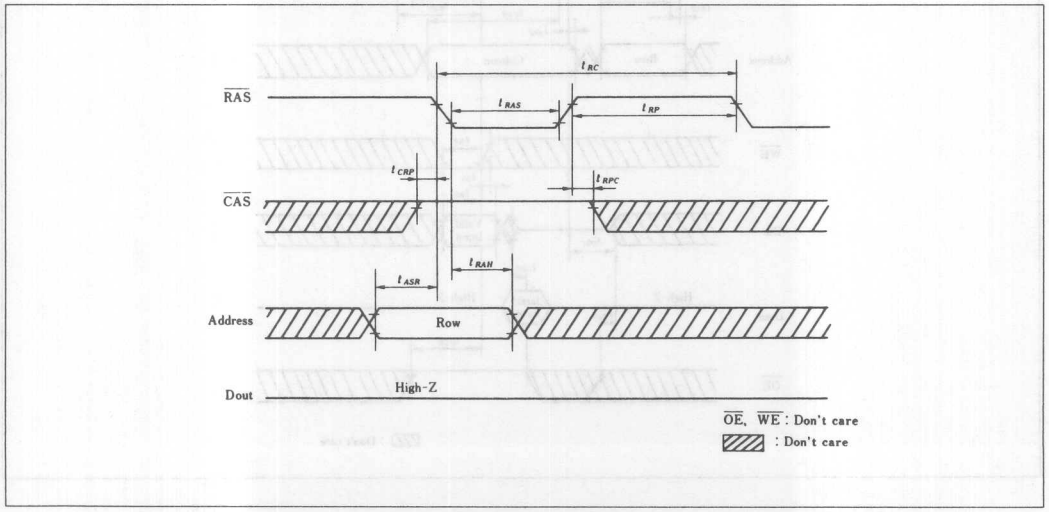
Delayed Write Cycle



Read-Modify-Write Cycle

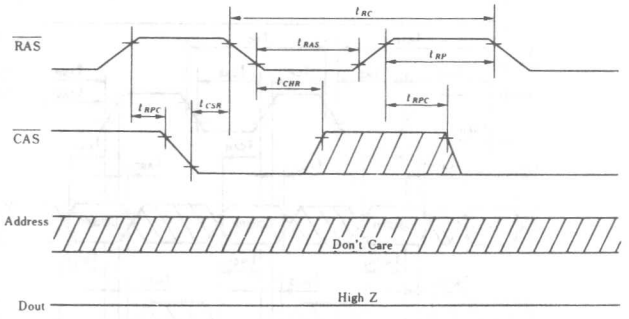


RAS-Only Refresh Cycle

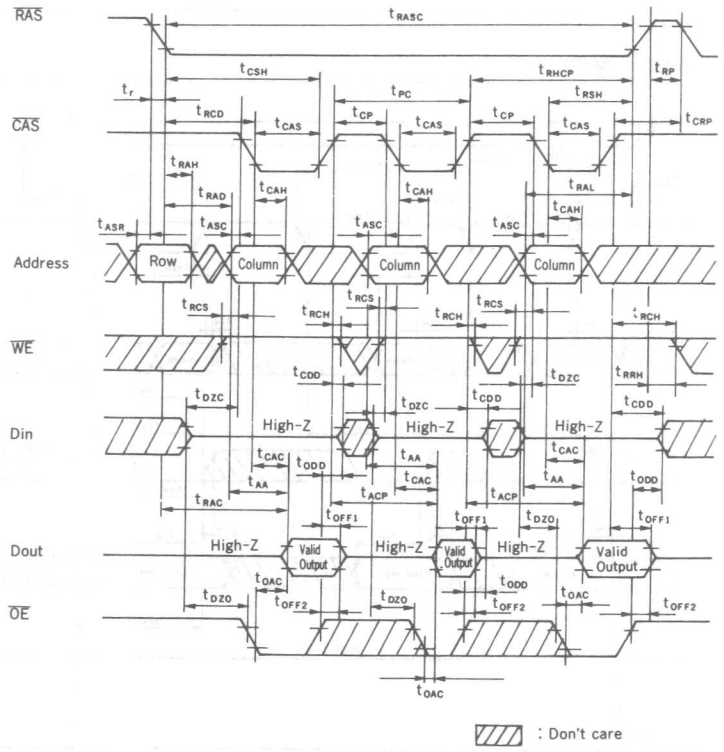


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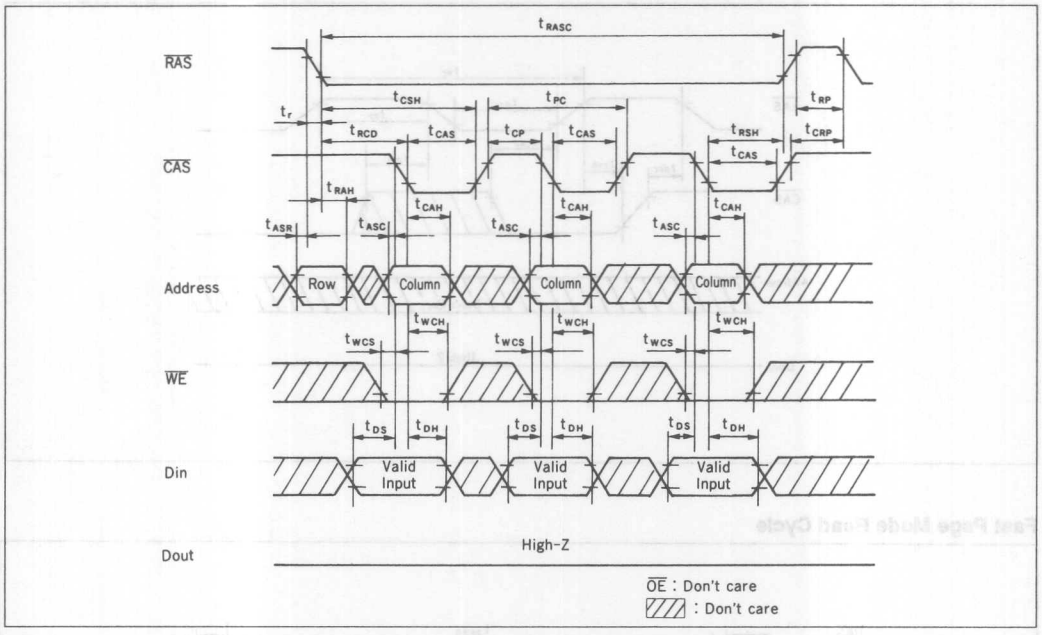
CAS-before-RAS Refresh Cycle



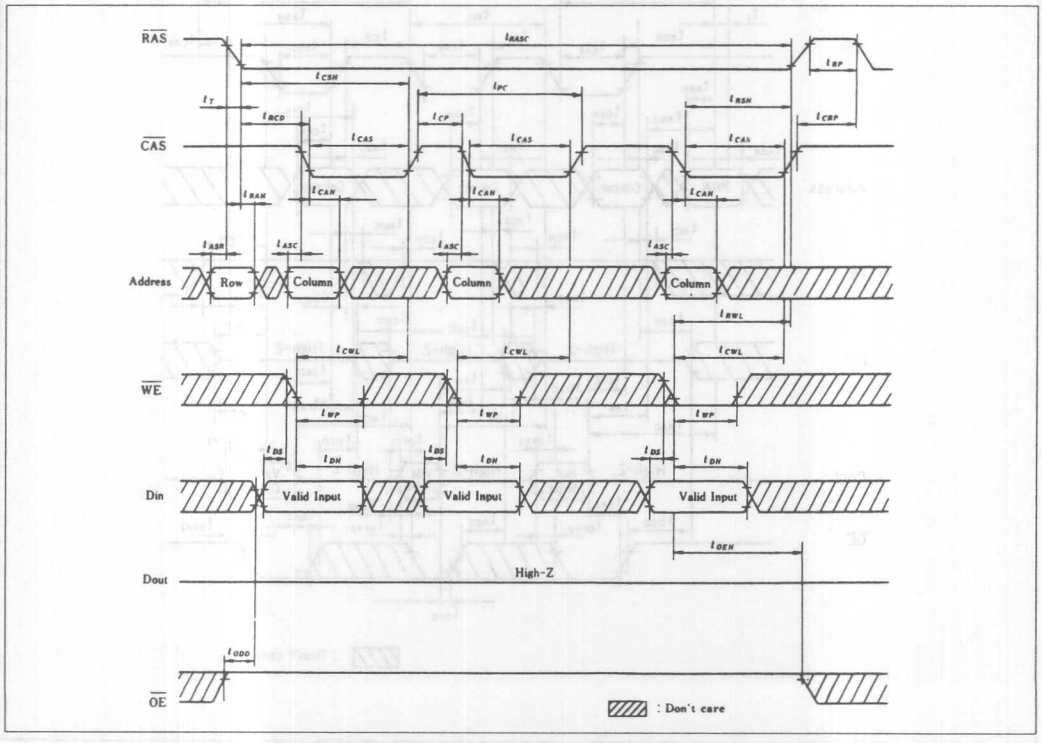
Fast Page Mode Read Cycle



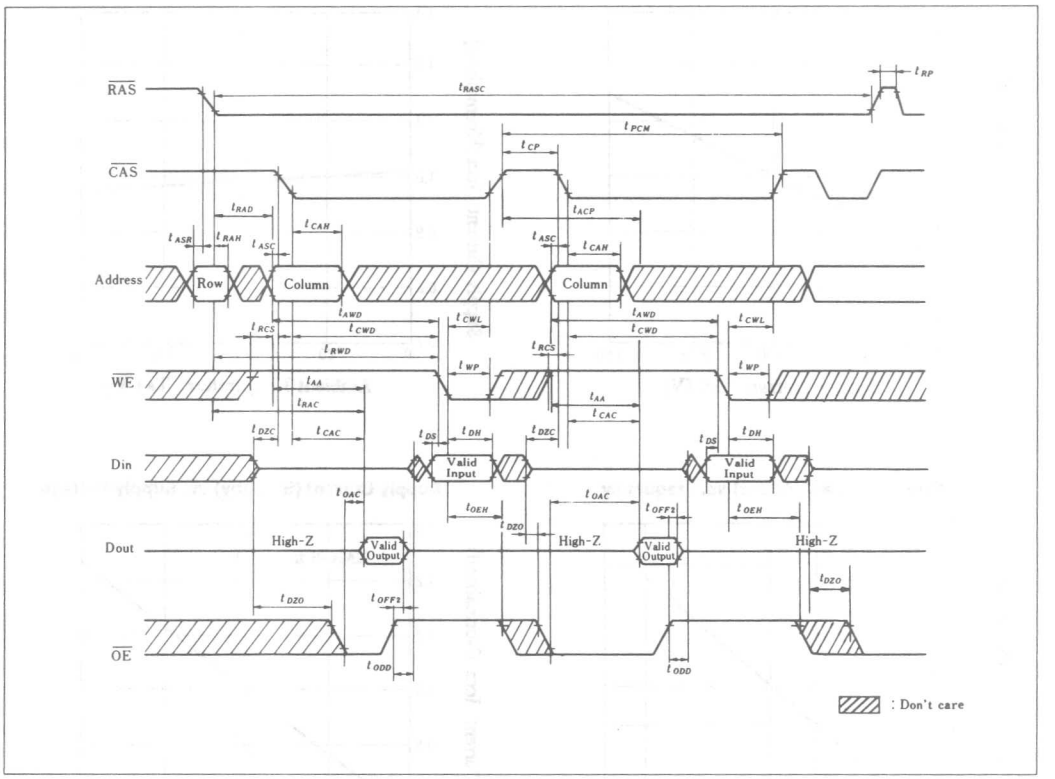
Fast Page Mode Early Write Cycle



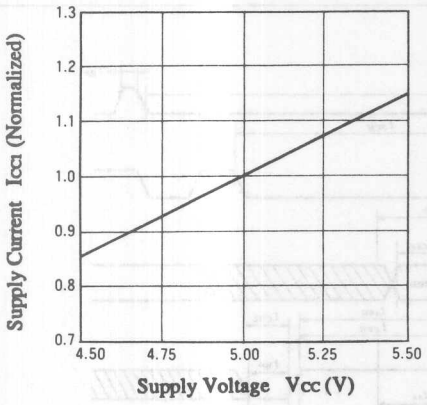
Fast Page Delayed Write Cycle



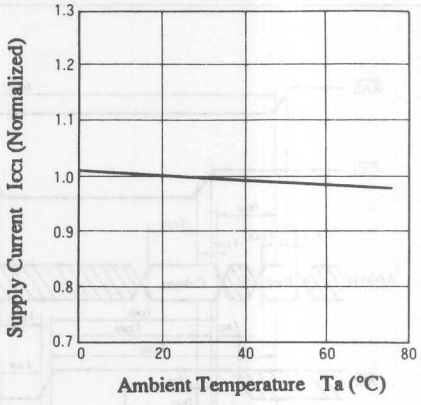
Fast Page Mode Read-Modify-Write Cycle



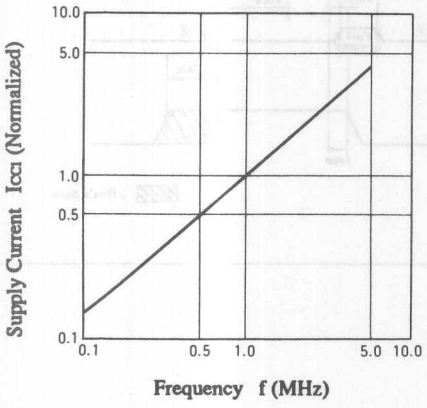
Supply Current (Active) vs. Supply Voltage



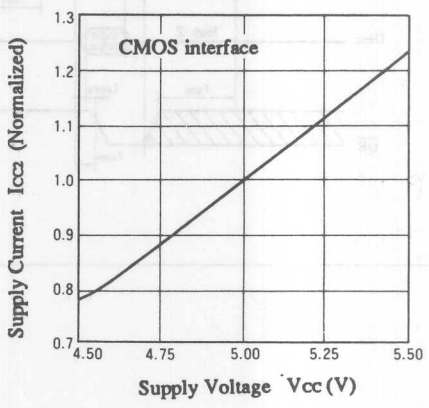
Supply Current (Active) vs. Ambient Temperature



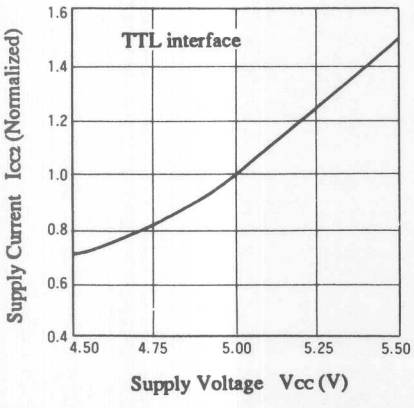
Supply Current (Active) vs. Frequency



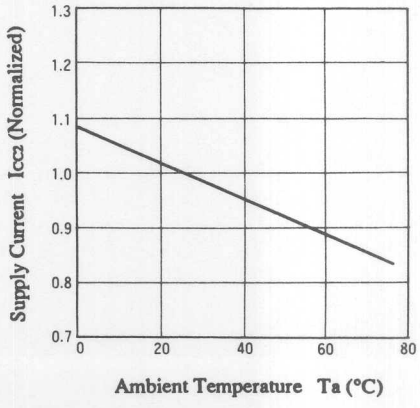
Supply Current (Standby) vs. Supply Voltage



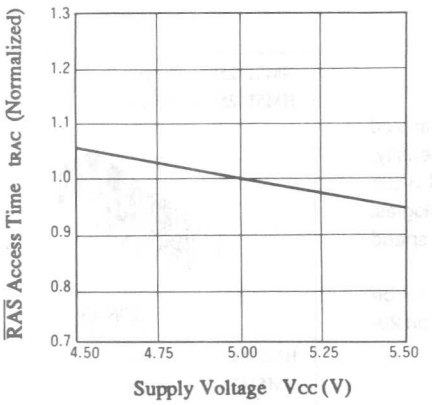
Supply Current (Standby) vs. Supply Voltage



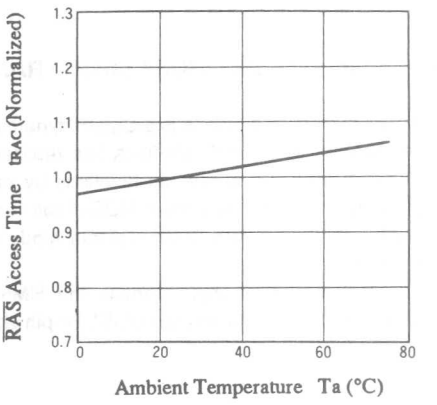
Supply Current (Standby) vs. Ambient Temperature



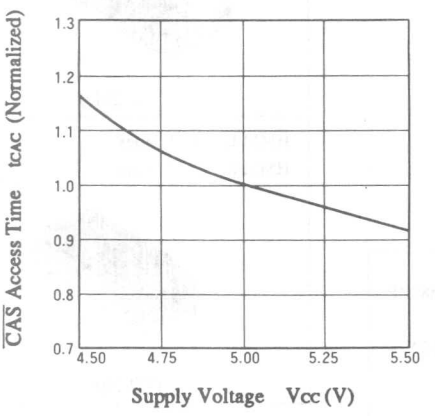
$\overline{RAS}$ Access Time vs. Supply Voltage



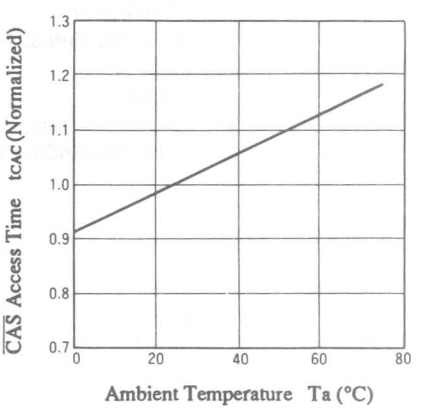
$\overline{RAS}$ Access Timve vs. Ambient Temperature



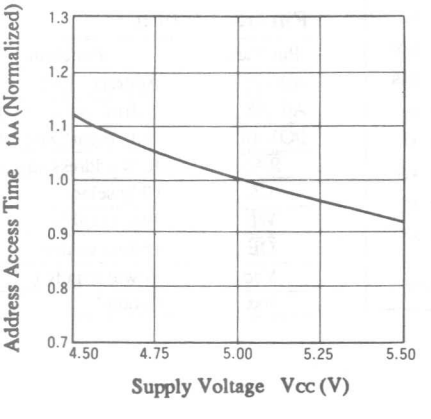
$\overline{CAS}$ Access Time vs. Supply Voltage



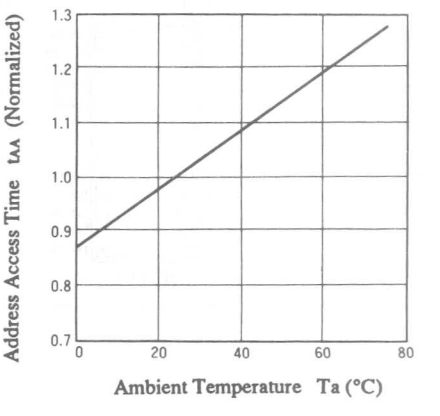
$\overline{CAS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature



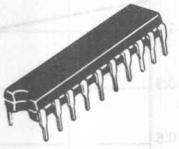
HM514258S Series
HM514258A Series

262144-Word × 4-Bit CMOS Dynamic RAM

The Hitachi HM514258S/A is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514258S/A has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514258S/A offers Static Column Mode as a high speed access mode.

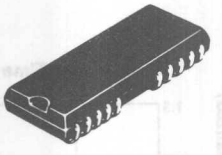
Multiplexed address input permits the HM514258S/A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514258SP Series
HM514258AP Series



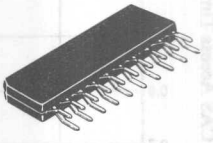
(DP-20NA)

HM514258SJP Series
HM514258AJP Series



(CP-20D)

HM514258SZP Series
HM514258AZP Series



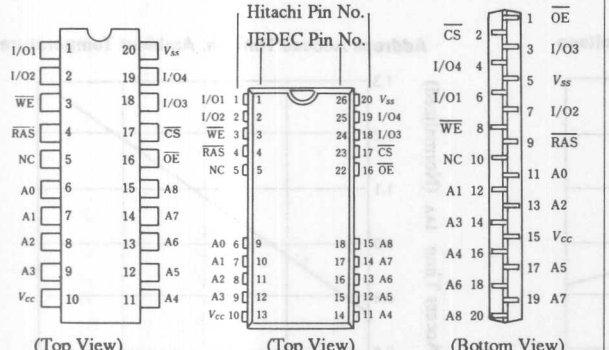
(ZP-20)

Features

- Single 5 V (±10%)
- High speed: Access Time 80 ns/100 ns/120 ns (max)
- Low power: Standby 11 mW (max)
  Active 413 mW/358 mW/303 mW (max)
- Static column mode capability
- 512 refresh cycles: (8 ms)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CS}$-before-$\overline{RAS}$ refresh

Pin Arrangement

- HM514258SP Series
- HM514258AP Series
- HM514258SJP Series
- HM514258AJP Series
- HM514258SZP Series
- HM514258AZP Series



Pin Description

Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

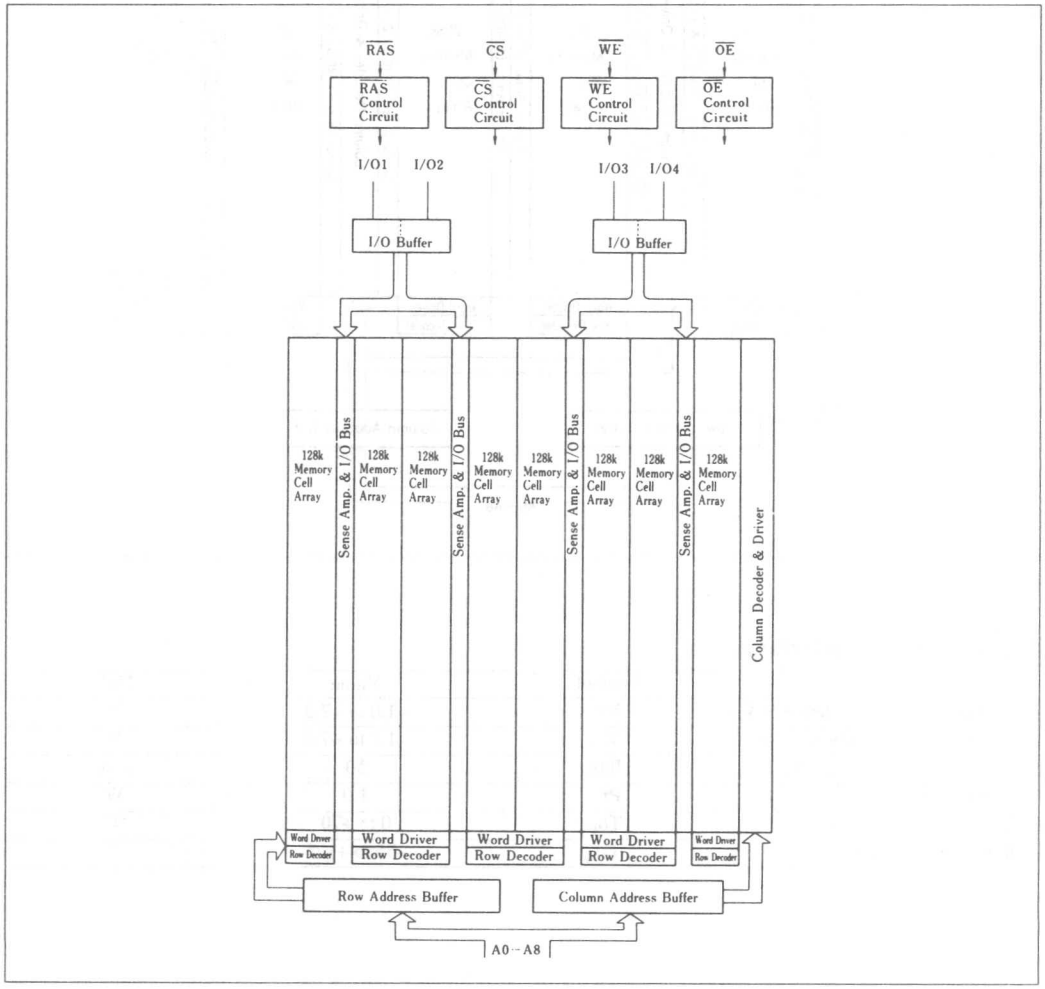
Ordering Information

Type No.	Access Time	Package
HM514258P-8S	80 ns	300-mil 20-pin
HM514258P-10S	100 ns	plastic DIP
HM514258P-12S	120 ns	(DP-20NA)
HM514258JP-8S	80 ns	300-mil 20-pin
HM514258JP-10S	100 ns	plastic SOJ
HM514258JP-12S	120 ns	(CP-20D)
HM514258ZP-8S	80 ns	400-mil 20-pin
HM514258ZP-10S	100 ns	plastic ZIP
HM514258ZP-12S	120 ns	(ZP-20)

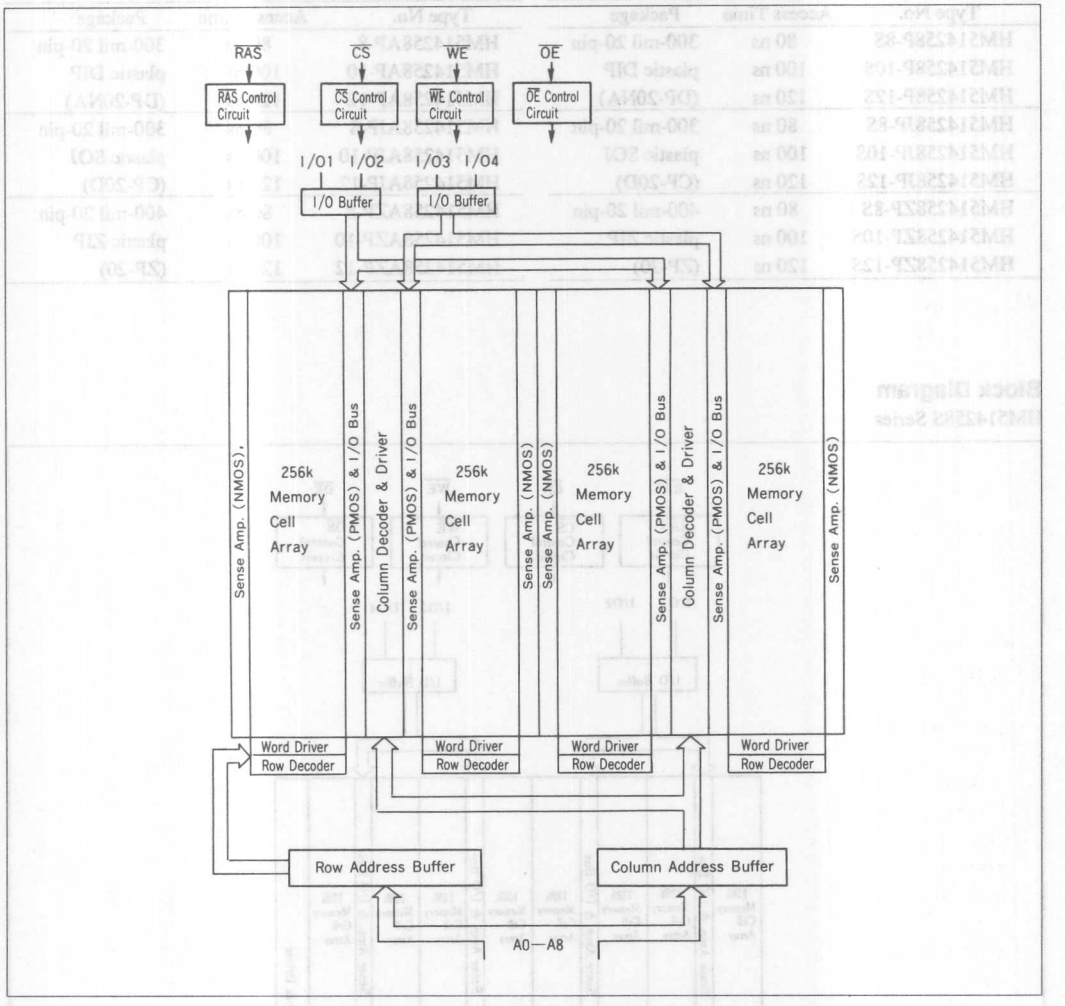
Type No.	Access Time	Package
HM514258AP-8	80 ns	300-mil 20-pin
HM514258AP-10	100 ns	plastic DIP
HM514258AP-12	120 ns	(DP-20NA)
HM514258AJP-8	80 ns	300-mil 20-pin
HM514258AJP-10	100 ns	plastic SOJ
HM514258AJP-12	120 ns	(CP-20D)
HM514258AZP-8	80 ns	400-mil 20-pin
HM514258AZP-10	100 ns	plastic ZIP
HM514258AZP-12	120 ns	(ZP-20)

Block Diagram

HM514258S Series



HM514258A Series



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–1.0 to +7.0	V
Supply voltage relative to Vss	Vcc	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	*1
Input high voltage		V_{IH}	2.4	—	6.5	V	*1
Input low voltage	I/O pin	V_{IL}	–1.0	—	0.8	V	*1
	Others	V_{IL}	–2.0	—	0.8	V	*1

Note: *1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	HM514258-8S HM514258A-8 Min	Max	HM514258-10S HM514258A-10 Min	Max	HM514258-12S HM514258A-12 Min	Max	Unit	Test Conditions	Note
Operating current	I_{CC1}	—	75	—	65	—	55	mA	$\overline{RAS}$, $\overline{CS}$ cycling t_{RC} = Min	*1, *2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	$\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	TTL interface
		—	1	—	1	—	1		RAS, CS ≥ Vcc-0.2V Dout = High-Z	CMOS interface
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	65	—	55	mA	t_{RC} = Min	*2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} Dout = enable	*1
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	65	—	55	—	45	mA	t_{RC} = Min	
Static column mode current	I_{CC9}	—	65	—	55	—	45	mA	t_{SC} = Min	*1, *3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: *1. I_{CC} depends on output load condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Item		Symbol	Typ	Max	Unit	Note
Input capacitance	Address	C_{I1}	—	5	pF	*1
	Clock	C_{I2}	—	7	pF	*1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	—	10	pF	*1, *2

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*17, *18

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ pulse width	t_{SP}	25	10000	30	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	0	—	ns	
Column address hold time	t_{AHW}	20	—	25	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	55	25	70	25	90	ns	*8
$\overline{RAS}$ hold time	t_{RSL}	25	—	30	—	30	—	ns	
$\overline{CS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	*1, *7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	

Read Cycle

Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	tRAC	—	80	—	100	—	120	ns	*2, *3
Access time from $\overline{CS}$	tACS	—	25	—	30	—	30	ns	*3, *4
Access time from address	tAA	—	40	—	50	—	55	ns	*3, *5, *14
Access time from $\overline{OE}$	tOAC	—	25	—	25	—	30	ns	
Read command setup time	tRCS	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CS}$	tRCH	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	tRRH	10	—	10	—	10	—	ns	
$\overline{RAS}$ to column address hold time	tAHR	15	—	15	—	15	—	ns	*16
$\overline{RAS}$ to column address delay time	tRAD	17	40	20	50	20	65	ns	*9
Column address to $\overline{RAS}$ lead time	tRAL	40	—	50	—	55	—	ns	
Column address hold time from $\overline{RAS}$	tAR	80	—	100	—	120	—	ns	
Ooutput buffer turn-off time	tOFF	—	20	—	25	—	30	ns	*6
Output buffer turn-off to $\overline{OE}$	tOFF2	—	20	—	25	—	30	ns	*6
Output hold time from address	tAOH	5	—	5	—	5	—	ns	
$\overline{CS}$ to Din delay time	tCDD	20	—	25	—	30	—	ns	
$\overline{CS}$ hold time from $\overline{OE}$	tOCH	25	—	25	—	30	—	ns	
$\overline{OE}$ hold time from $\overline{RAS}$	tROH	80	—	100	—	120	—	ns	
$\overline{OE}$ hold time from $\overline{CS}$	tCOH	25	—	25	—	30	—	ns	
$\overline{OE}$ pulse width	tOEP	25	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	tWCS	0	—	0	—	0	—	ns	*10
Write command hold time	tWCH	20	—	25	—	25	—	ns	
Write command hold time to $\overline{RAS}$	tWCR	75	—	95	—	115	—	ns	
Write command pulse width	tWP	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	tRWL	25	—	25	—	30	—	ns	
Write command to $\overline{CS}$ lead time	tCWL	25	—	25	—	30	—	ns	
Din setup time	tDS	0	—	0	—	0	—	ns	*11
Din hold time	tDH	20	—	25	—	25	—	ns	*11
Din hold time to $\overline{RAS}$	tDHR	75	—	95	—	115	—	ns	
Column address hold time from $\overline{RAS}$	tAWR	75	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	tRWC	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	110	—	135	—	160	—	ns	*10
$\overline{CS}$ to $\overline{WE}$ delay time	tCWD	55	—	65	—	70	—	ns	*10
Column address to $\overline{WE}$ delay time	tAWD	70	—	85	—	95	—	ns	*10

Refresh Cycle

Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{ZRH}	10	—	10	—	10	—	ns	

Static Column Mode Cycle

Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static column mode cycle time	t_{SC}	45	—	55	—	60	—	ns	
Static column mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	–	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	90	—	110	—	135	—	ns	
Static column mode $\overline{CS}$ precharge time	t_{SI}	10	—	10	—	15	—	ns	
Static column mode $\overline{WE}$ precharge time	t_{WI}	10	—	10	—	15	—	ns	

Static Column Mode Read-modify-Write Cycle and Mixed Cycle

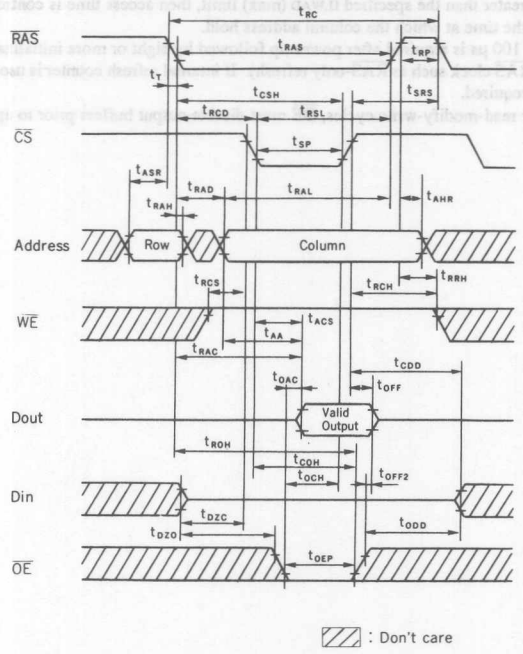
Item	Symbol	HM514258-8S HM514258A-8		HM514258-10S HM514258A-10		HM514258-12S HM514258A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static column mode cycle time on read-modify-write	t_{SRW}	120	—	140	—	160	—	ns	*12
Access time from first $\overline{WE}$	t_{ALW}	—	85	—	100	—	115	ns	*3, *13
Last $\overline{WE}$ to column address delay time	t_{LWAD}	25	45	25	50	30	60	ns	*15
Last $\overline{WE}$ to column address hold time	t_{AHLW}	85	—	100	—	115	—	ns	

Notes:
*1. AC measurements assume t_T = 5ns.
*2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
*4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
*5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
*7. Transition times are measured between V_{IH} and V_{IL}.
*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
*11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-wirte cycles.
*12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T

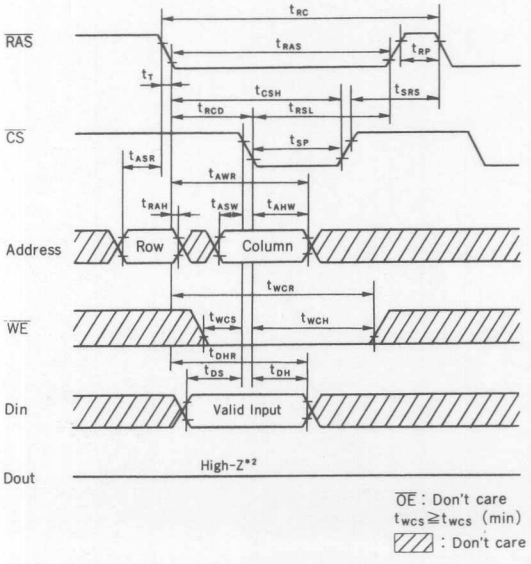
*13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recomended value shown in this table, t_{ALW} exceeds the value shown.
*14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
*15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
*16. t_{AHR} is defined as the time at which the column address hold.
*17. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CS}$-before-$\overline{RAS}$ refresh cycles are required.
*18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

Timing Waveforms

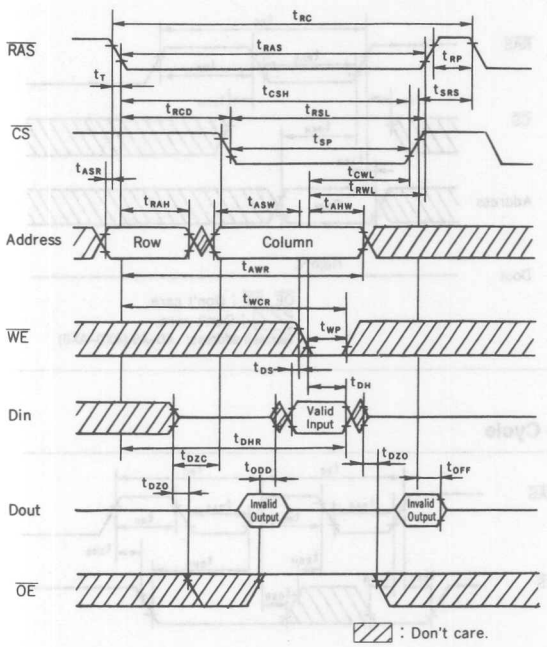
Read Cycle



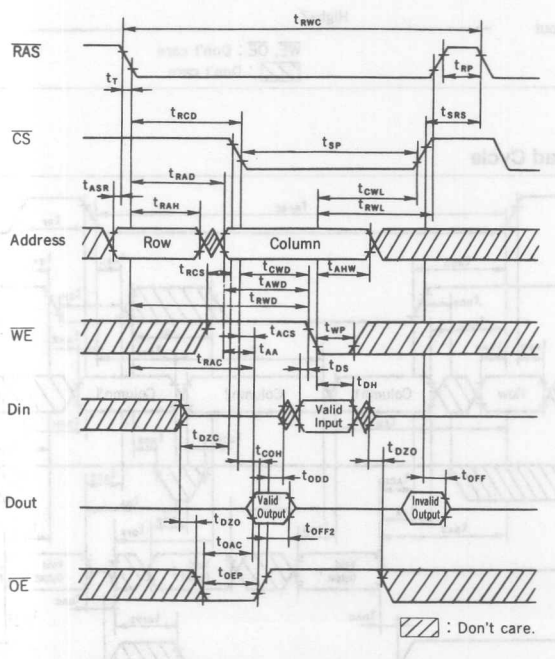
Early Write Cycle



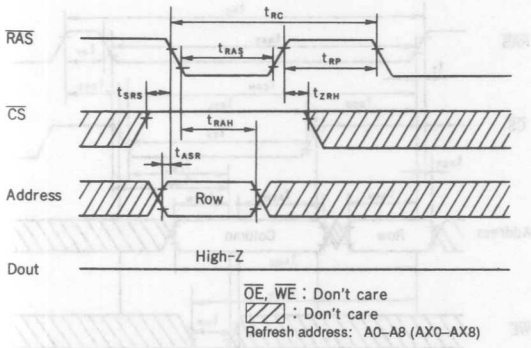
Delayed Write Cycle



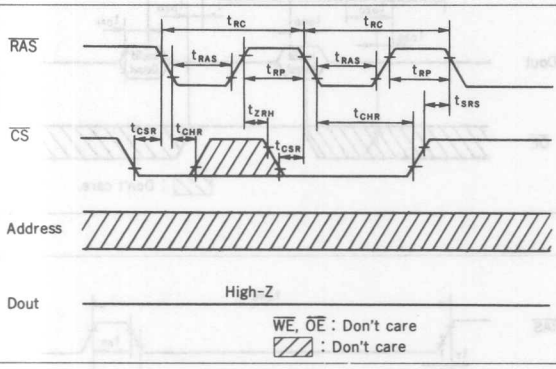
Read-Modify-Write Cycle



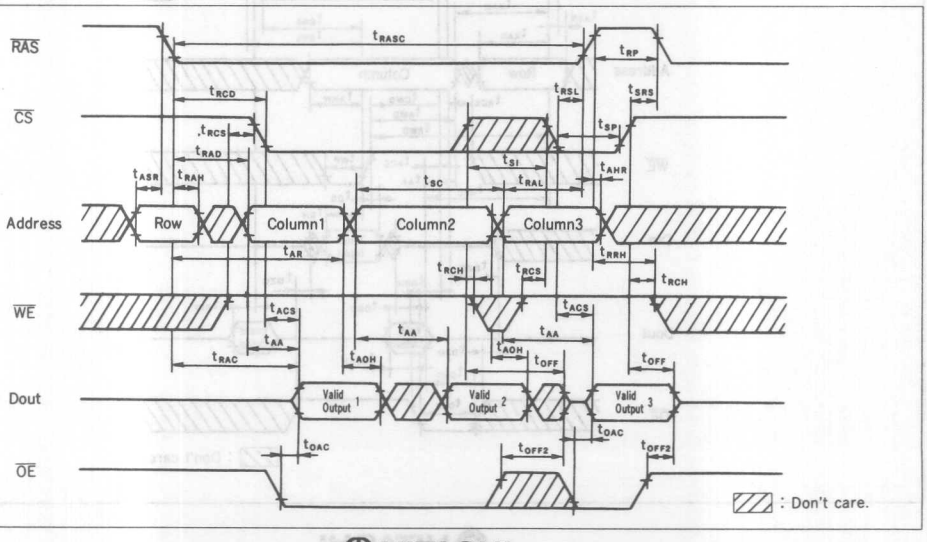
$\overline{RAS}$-Only Refresh Cycle



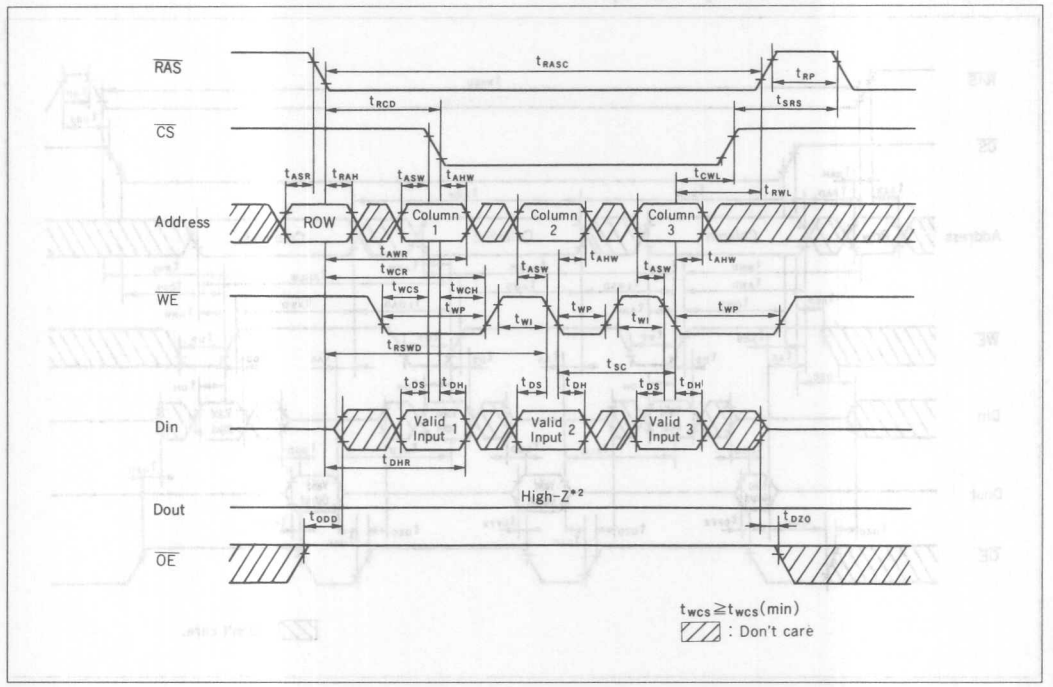
$\overline{CS}$-before-$\overline{RAS}$ Refresh Cycle



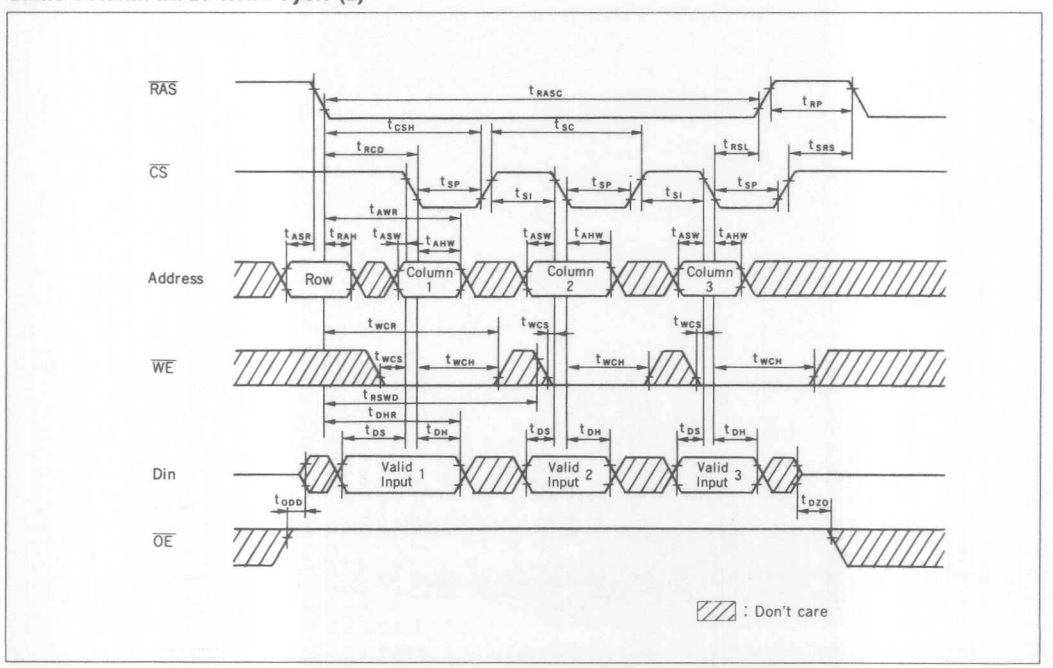
Static Column Mode Read Cycle



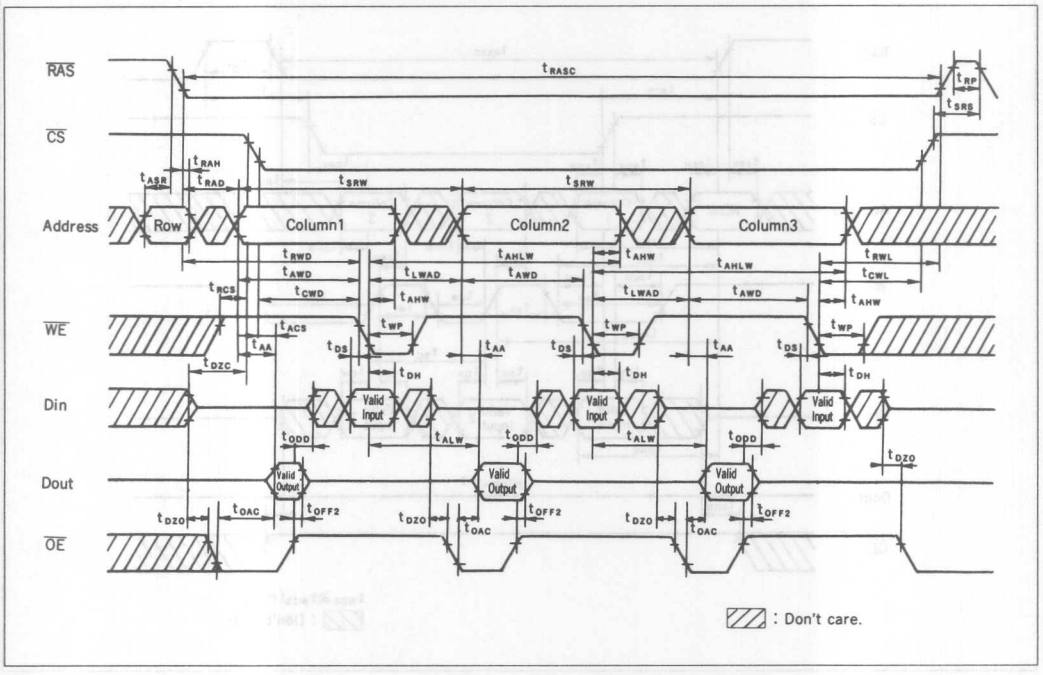
Static Column Mode Write Cycle (1)



Static Column Mode Write Cycle (2)

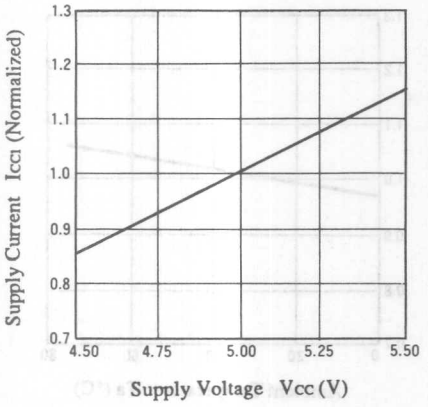


Static Column Mode Read-Modify-Write Cycle

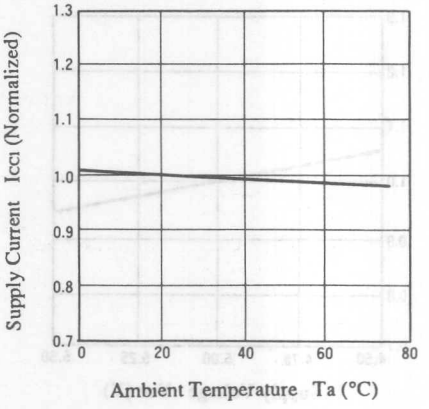


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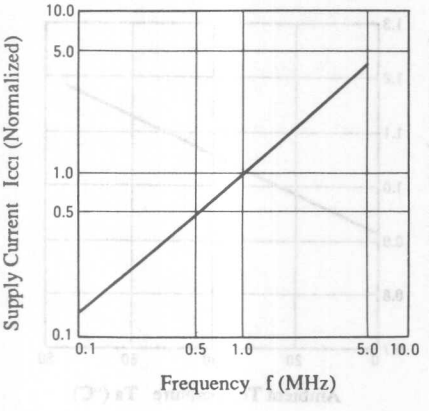
Supply Current (Active) vs. Supply Voltage



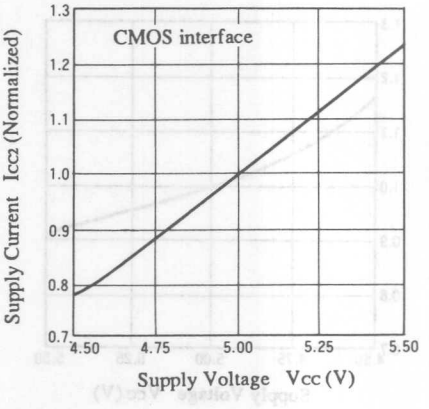
Supply Current (Active) vs. Ambient Temperature



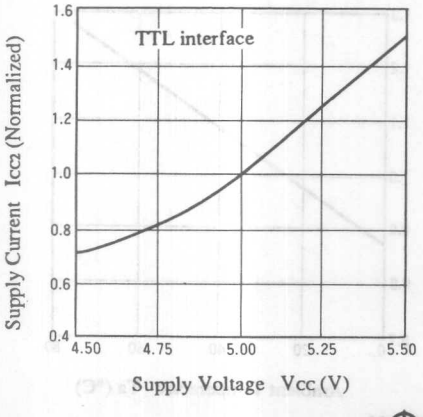
Supply Current (Active) vs. Frequency



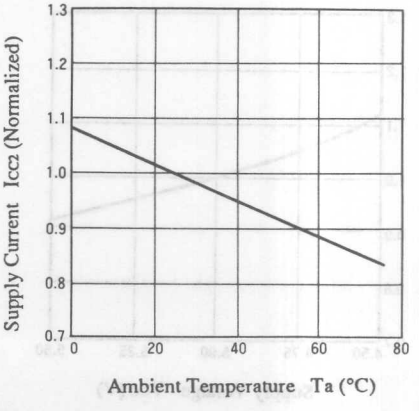
Supply Current (Standby) vs. Supply Voltage



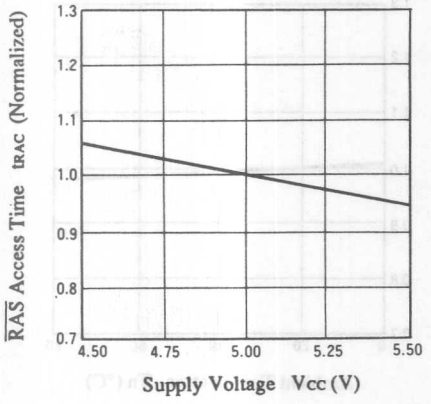
Supply Current (Standby) vs. Supply Voltage



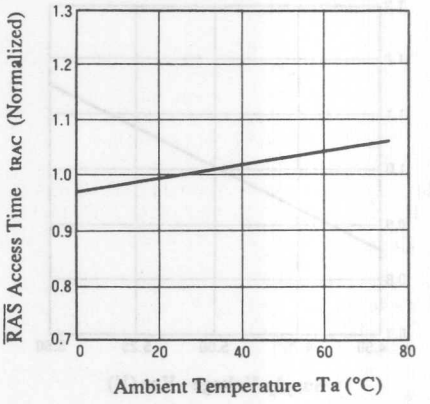
Supply Current (Standby) vs. Ambient Temperature



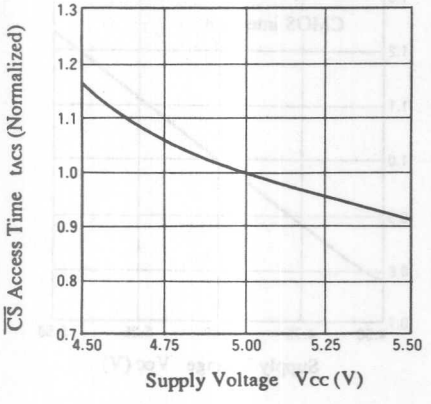
$\overline{RAS}$ Access Time vs. Supply Voltage



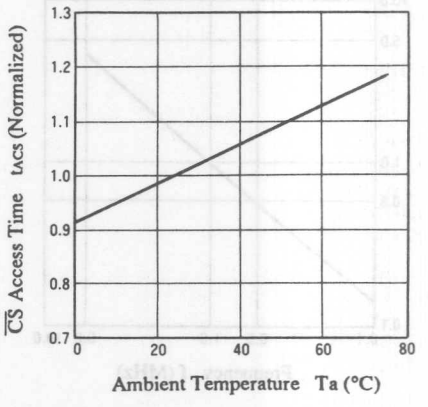
$\overline{RAS}$ Access Time vs. Ambient Temperature



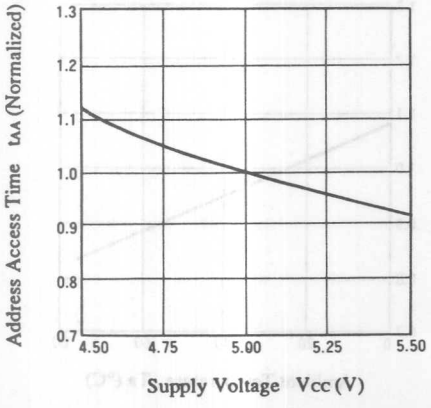
$\overline{CS}$ Access Time vs. Supply Voltage



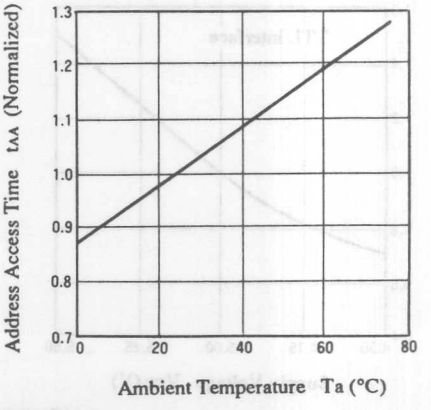
$\overline{CS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature



HM514266AP/AJP/AZP-6/7/8/10/12 — Preliminary

262,144-Word × 4-Bit Dynamic Random Access Memory

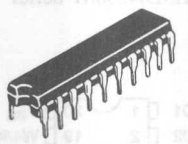
■ DESCRIPTION

The Hitachi HM514266A is a CMOS dynamic RAM organized 262,144-word × 4-bit. HM514266A has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM514266A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits HM514266A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

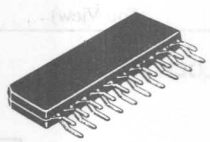
- Single 5V (±10%)
- High Speed
  - Access Time . . . . . .60/70/80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .495/440/363/303/259mW (max.)
  - Standby Mode . . . . . .11mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycles . . . . . .(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Write per bit capability



(DP-20NA)



(CP-20D)



(ZP-20)

■ ORDERING INFORMATION

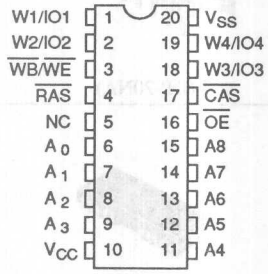
Part No.	Access	Package
HM514266AP-6	60ns	300 mil 20 pin Plastic DIP (DP-20NA)
HM514266AP-7	70ns	
HM514266AP-8	80ns	
HM514266AP-10	100ns	
HM514266AP-12	120ns	
HM514266AJP-6	60ns	300 mil 20 pin Plastic SOJ (CP-20D)
HM514266AJP-7	70ns	
HM514266AJP-8	80ns	
HM514266AJP-10	100ns	
HM514266AJP-12	120ns	
HM514266AZP-6	60ns	400 mil 20 pin Plastic ZIP (ZP-20)
HM514266AZP-7	70ns	
HM514266AZP-8	80ns	
HM514266AZP-10	100ns	
HM514266AZP-12	120ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
W_1/IO_1–W_1/IO_4	Write Select/ Data-In/Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Per Bit/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5.0V)
V_{SS}	Ground

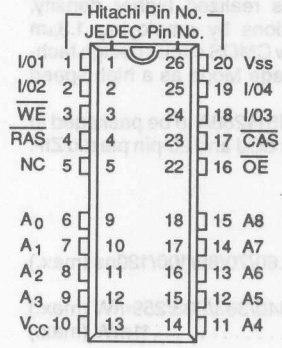
■ PIN ARRANGEMENT

• HM514266AP Series



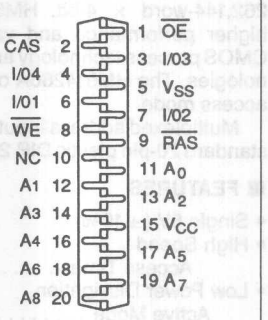
(Top View)

• HM514266AJP Series



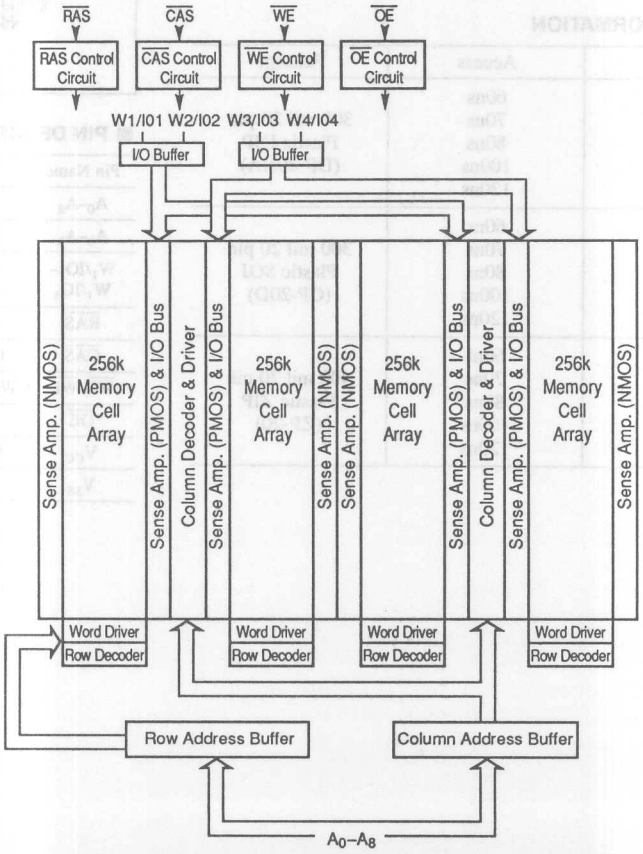
(Top View)

• HM514266AZP Series



(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	90	—	80	—	66	—	55	—	47	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	—	2	—	2	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	1	—	1	—	1	—	1	—	1	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	90	—	80	—	66	—	55	—	47	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	5	—	5	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	80	—	70	—	66	—	55	—	47	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	80	—	70	—	55	—	55	—	47	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-In, Data-Out)	$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1], [14]

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Set-Up Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Set-Up Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Delay Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

• Read Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Set-Up Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	20	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-Off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

• Write Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-Up Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-In Set-Up Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

• Refresh Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-Up Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

• Write Per Bit (15), (16)

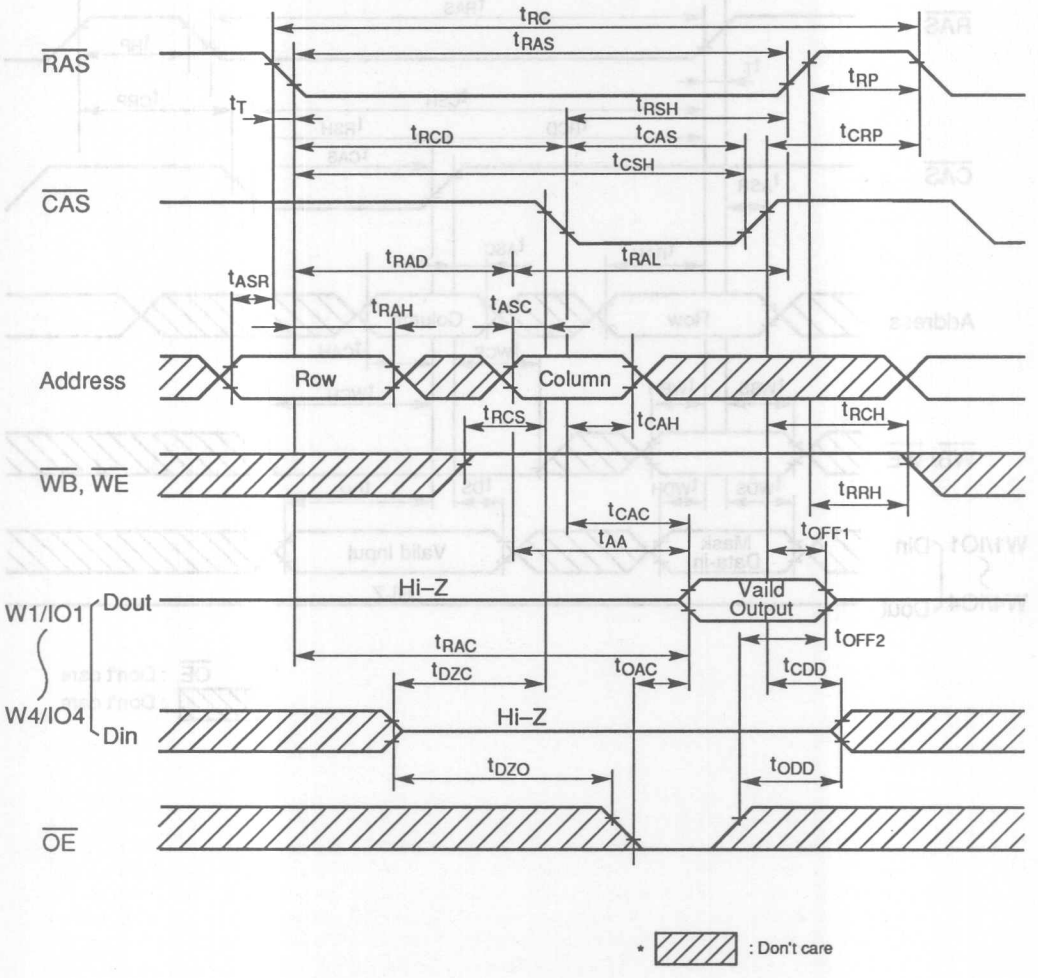
Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Per Bit Setup Time	t_{WBS}	0	—	0	—	0	—	0	—	0	—	ns	
Write Per Bit Hold Time	t_{WBH}	10	—	10	—	12	—	15	—	15	—	ns	
Write Per Bit Selection Setup Time	t_{WDS}	0	—	0	—	0	—	0	—	0	—	ns	
Write Per Bit Selection Hold Time	t_{WDH}	10	—	10	—	12	—	15	—	15	—	ns	

NOTES:

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
15. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
16. The data bits to which the write operation is applied can be specified by keeping Wi/IOi high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

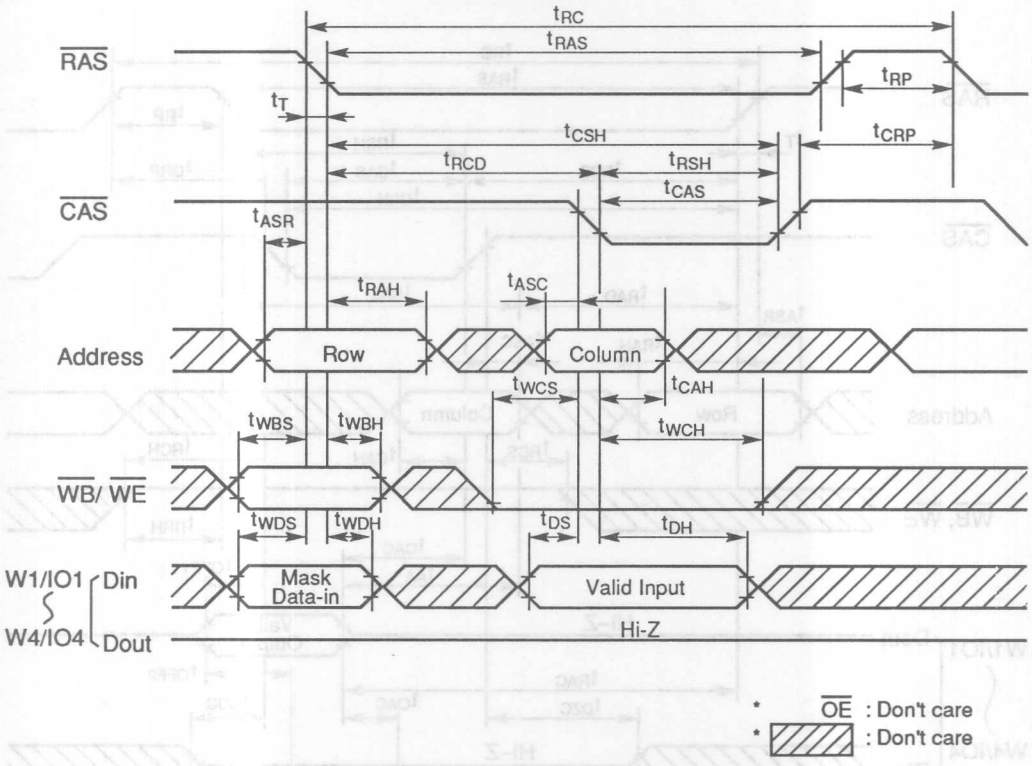
■ TIMING WAVEFORMS

• Read Cycle

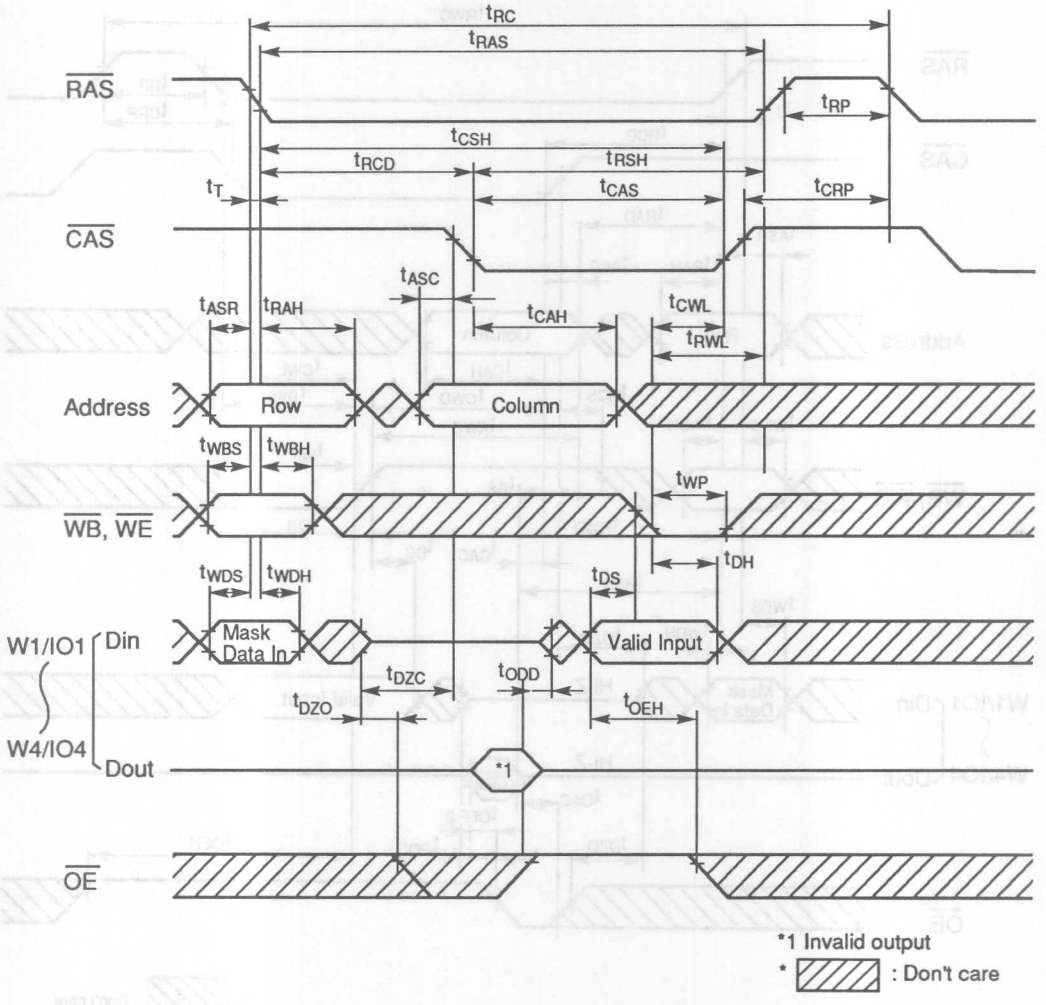


• : Don't care

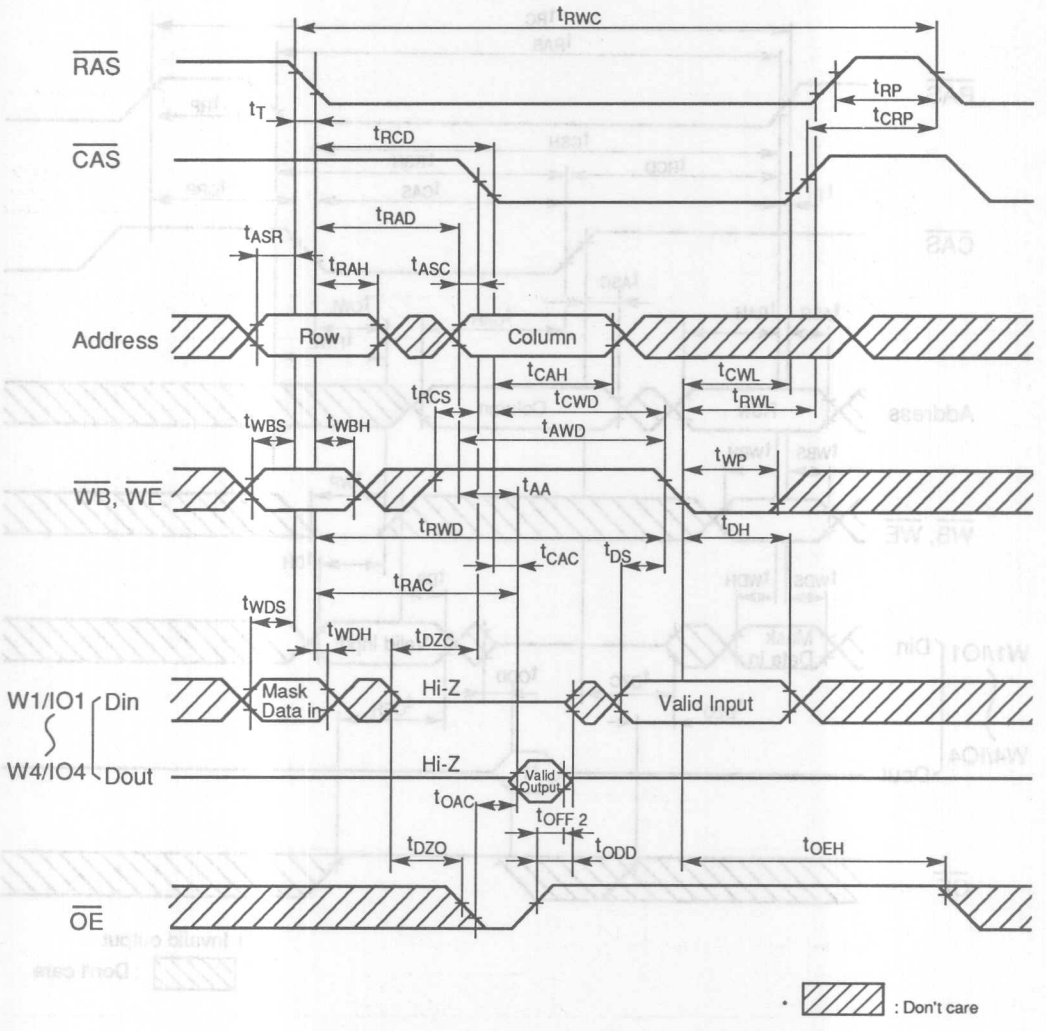
• **Early Write Cycle**



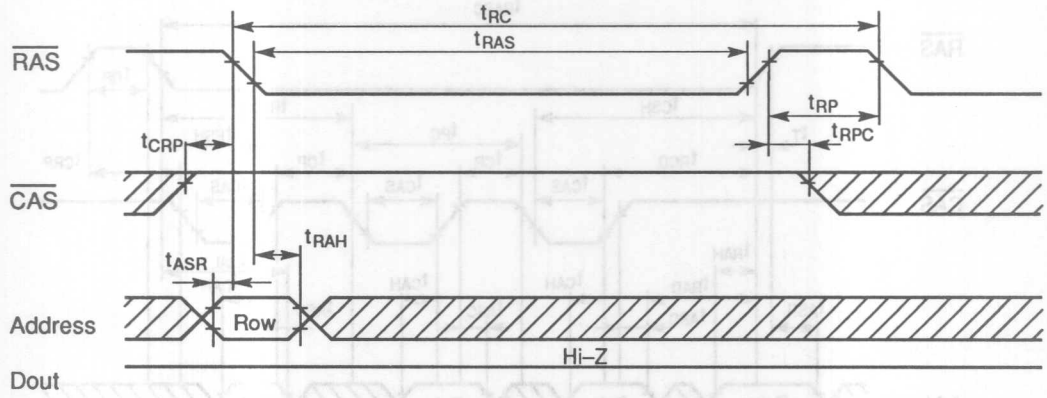
• **Delayed Write Cycle**



• **Read-Modify-Write Cycle**



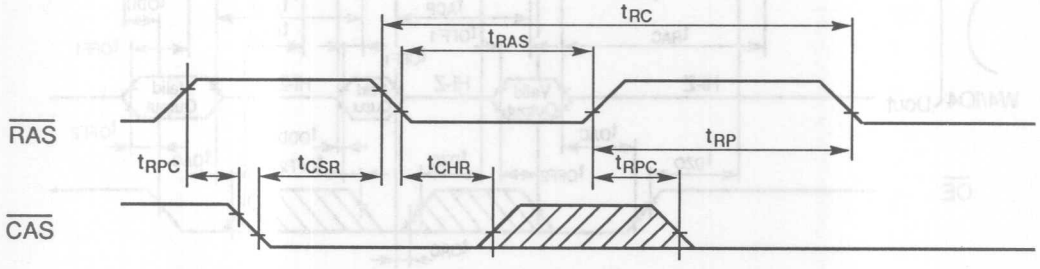
• **$\overline{RAS}$-Only Refresh Cycle**



1 $\overline{OE}$, $\overline{WE}$: Don't care

2 : Don't care

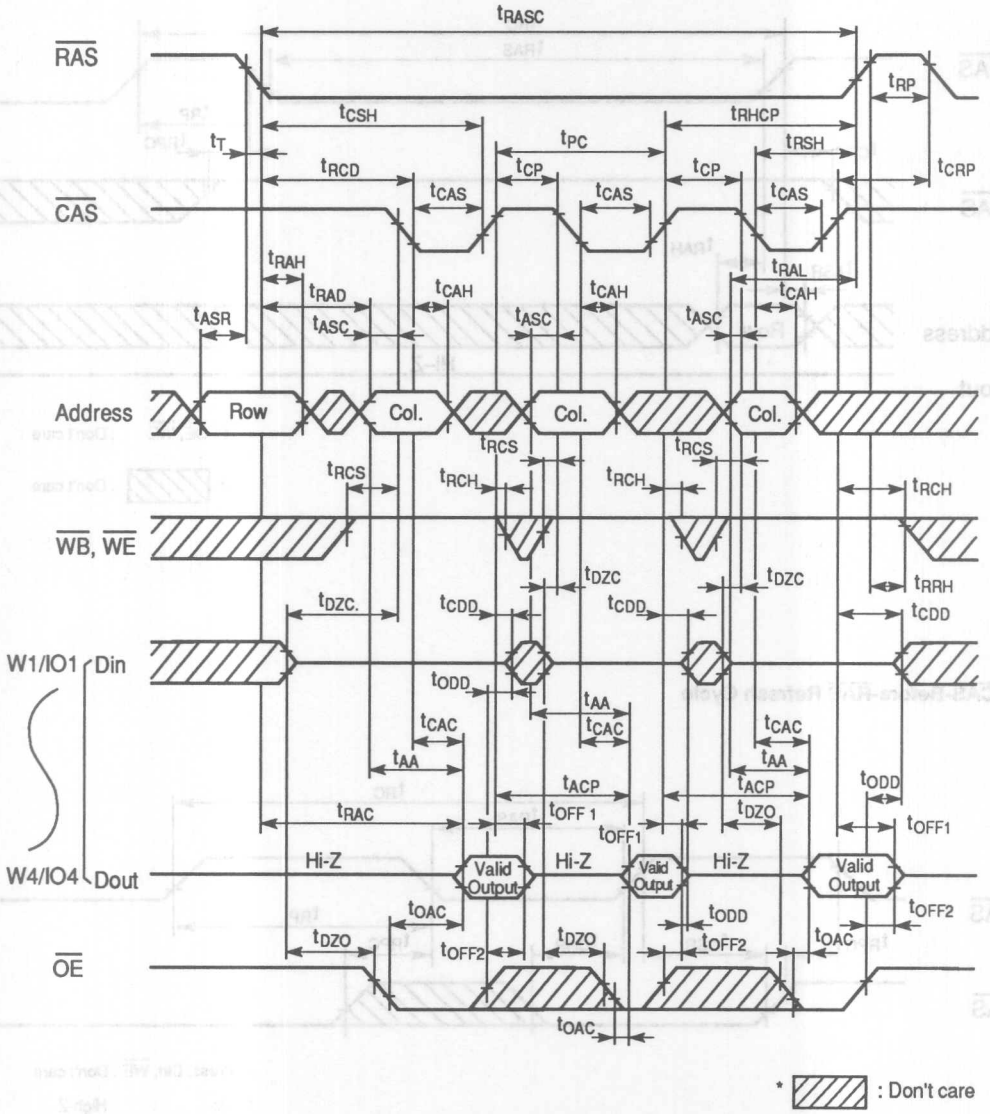
• **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle**



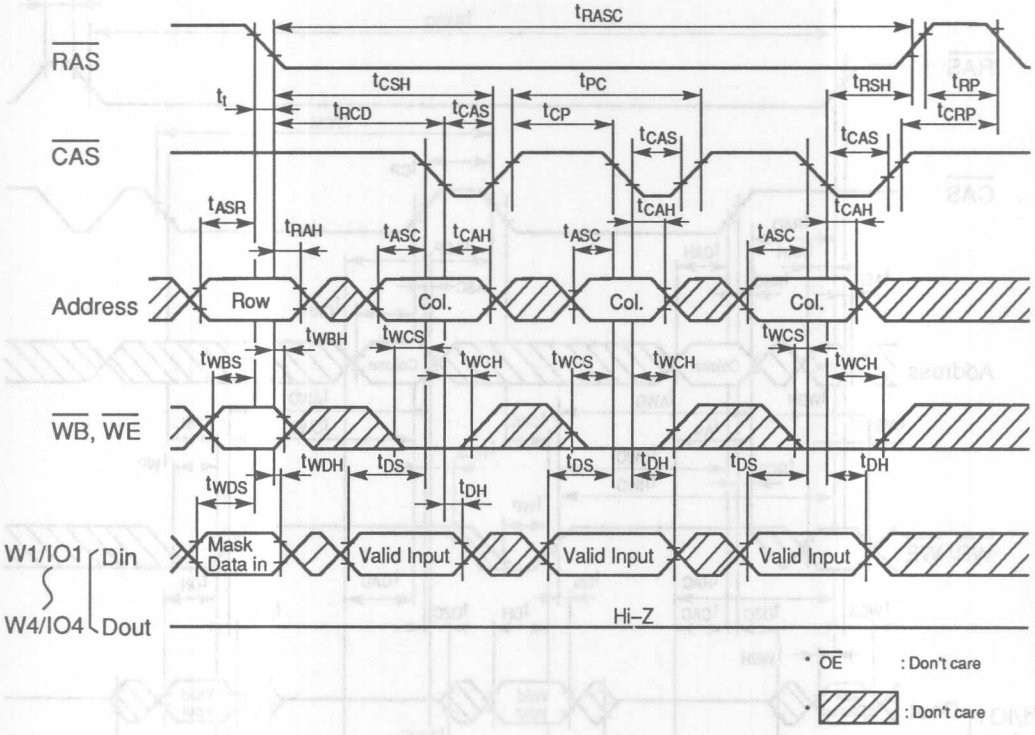
Address, Din, $\overline{WE}$: Don't care

Dout: High-Z

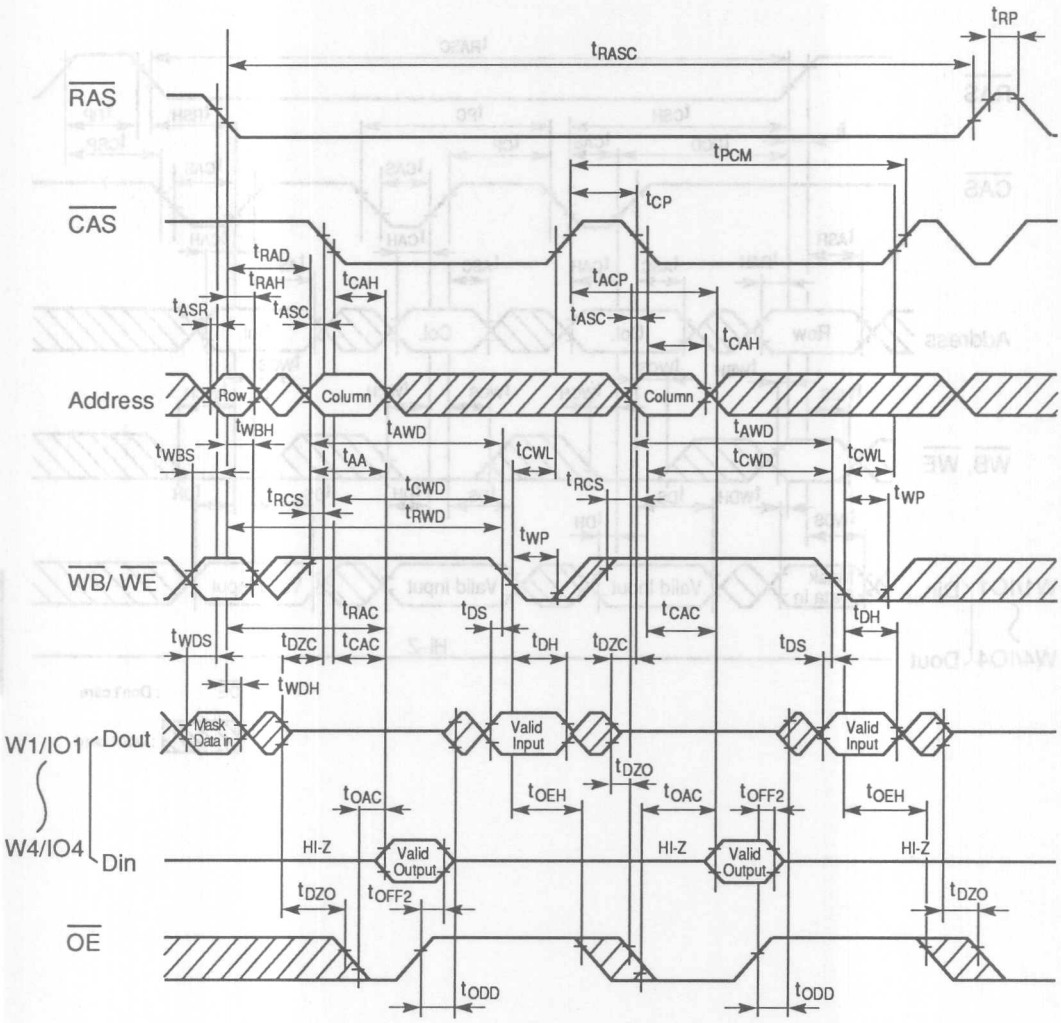
• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



• : Don't care

HM511000S Series
HM511000A Series

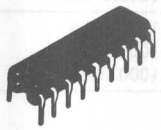
1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511000S/A series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000S/A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000S/A offers Fast Page Mode as a high speed access mode.

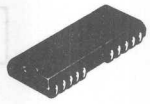
Multiplexed address input permits the HM511000S/A to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511000SP Series
HM511000AP Series



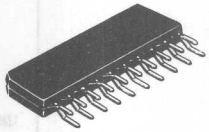
(DP-18C)

HM511000SJP Series
HM511000AJP Series



(CP-20D)

HM511000SZP Series
HM511000AZP Series



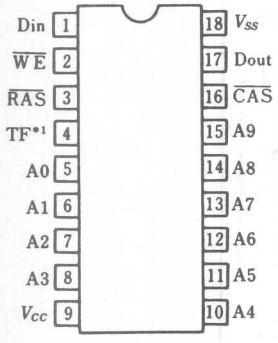
(ZP-20)

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11 mW standby, 385/330/275 mW active
- Single 5V supply (±10%)
- Fast page mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

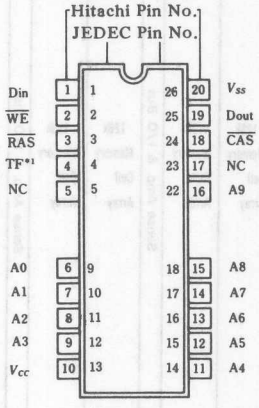
Pin Arrangement

HM511000SP Series
HM511000AP Series



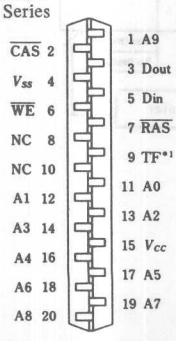
(Top View)

HM511000SJP Series
HM511000AJP Series



(Top View)

HM511000SZP Series
HM511000AZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

Note)

***1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.**

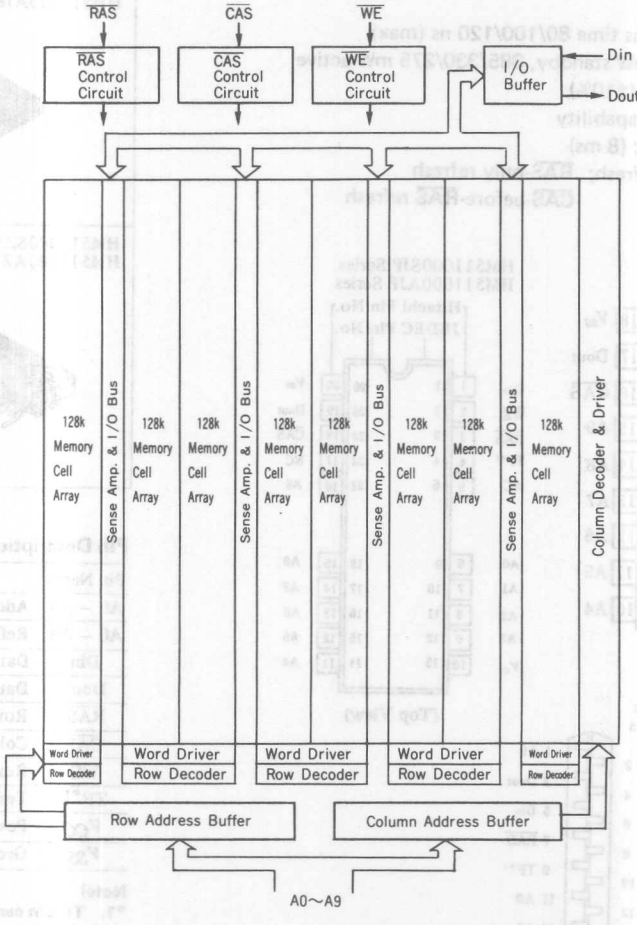
Ordering Information

Type No.	Access Time	Package
HM511000P-8S	80ns	300 mil 18-pin Plastic DIP
HM511000P-10S	100ns	
HM511000P-12S	120ns	
HM511000JP-8S	80ns	300 mil 20-pin Plastic SOJ
HM511000JP-10S	100ns	
HM511000JP-12S	120ns	
HM511000ZP-8S	80ns	400 mil 20-pin Plastic ZIP
HM511000ZP-10S	100ns	
HM511000ZP-12S	120ns	

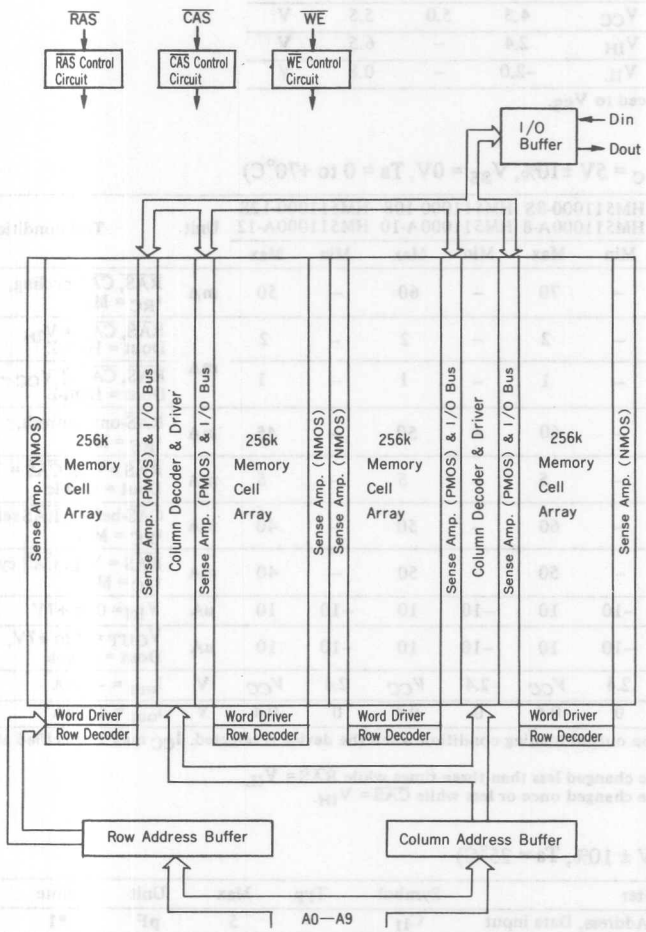
Type No.	Access Time	Package
HM511000AP-8	80ns	300 mil 18-pin Plastic DIP
HM511000AP-10	100ns	
HM511000AP-12	120ns	
HM511000AJP-8	80ns	300 mil 20-pin Plastic SOJ
HM511000AJP-10	100ns	
HM511000AJP-12	120ns	
HM511000AZP-8	80ns	400 mil 20-pin Plastic ZIP
HM511000AZP-10	100ns	
HM511000AZP-12	120ns	

Block Diagram

HM511000S Series



HM511000A Series



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Test condition	Note
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min	*1,*2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2V Dout = High-Z CMOS interface	
Refresh current	I_{CC3}	–	60	–	50	–	45	mA	$\overline{RAS}$-only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	*1
Refresh current	I_{CC6}	–	60	–	50	–	40	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min.	
Fast page mode current	I_{CC7}	–	50	–	50	–	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min	*1,*3
Input leakage	I_{LI}	–10	10	–10	10	–10	10	μA	V_{IN} = 0 to +7V	
Output leakage	I_{LO}	–10	10	–10	10	–10	10	μA	V_{OUT} = 0 to +7V, Dout = disable	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = –5mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10%)

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	25	–	25	–	30	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	*7
Refresh period	t_{REF}	–	8	–	8	–	8	ms	

Read Cycle

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	–	25	–	25	–	30	ns	*3,*4
Access time from address	t_{AA}	–	40	–	45	–	55	ns	*3,*5
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	45	–	55	–	ns	
Output buffer turn-off time	t_{OFF}	–	20	–	25	–	30	ns	*6

Write Cycle

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	*10
Write command hold time	t_{WCH}	20	–	20	–	25	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	25	–	30	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	*11
Data-in hold time	t_{DH}	20	–	20	–	25	–	ns	*11

Read-Modify-Write Cycle

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	190	–	220	–	255	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	100	–	120	–	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	25	–	25	–	30	–	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	45	–	55	–	ns	*10

Refresh Cycle

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	10	–	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	55	–	55	–	65	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	15	–	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	–	100000	–	100000	–	100000	ns	*13
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	50	–	50	–	60	ns	*14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	–	50	–	60	–	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511000-8S HM511000A-8		HM511000-10S HM511000A-10		HM511000-12S HM511000A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast page mode read-write cycle time	t_{PCM}	85	–	85	–	100	–	ns	

Notes) *1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).

*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).

*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between V_{IH} and V_{IL}.

*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

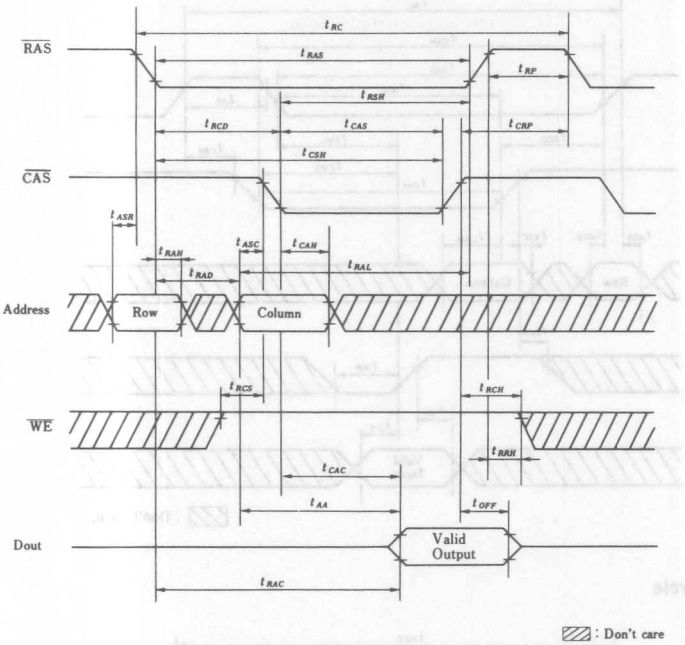
*12. An initial pause of 100μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycle.

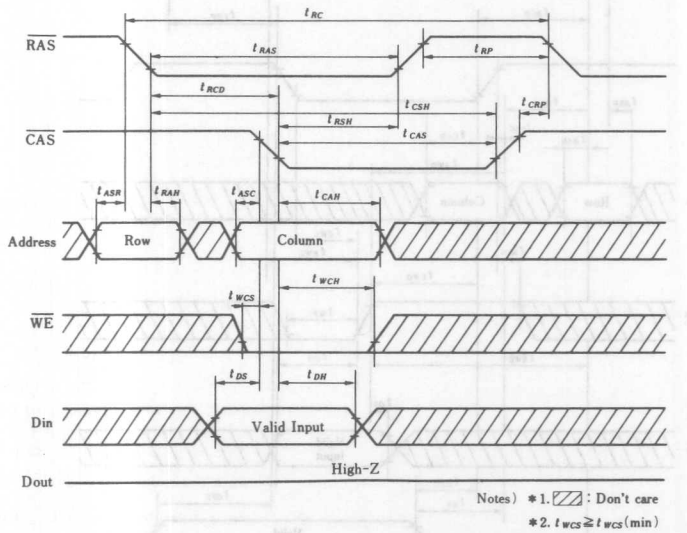
*14. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

Timing Waveforms

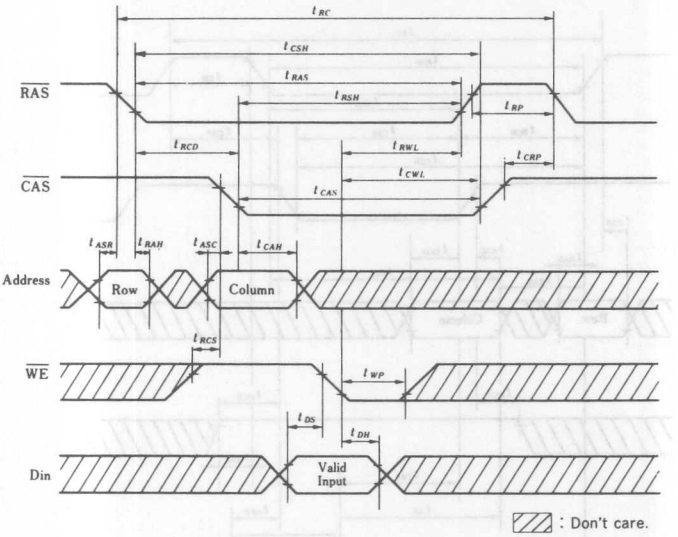
Read Cycle



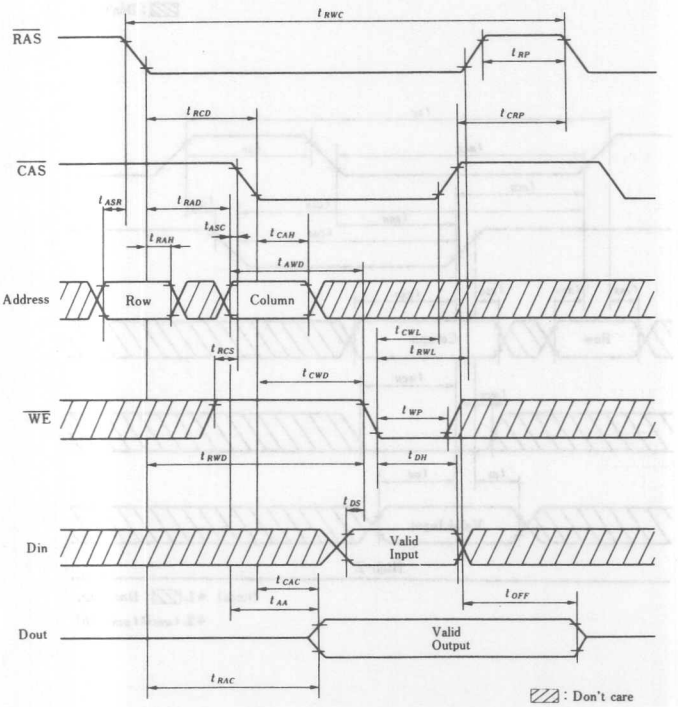
Early Write Cycle



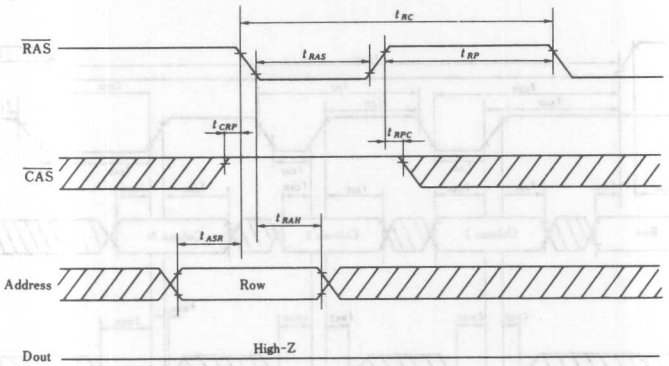
Delayed Write Cycle



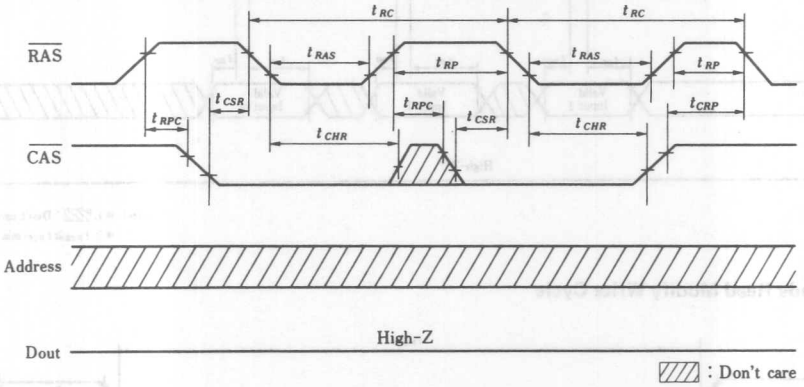
Read-Modify-Write Cycle



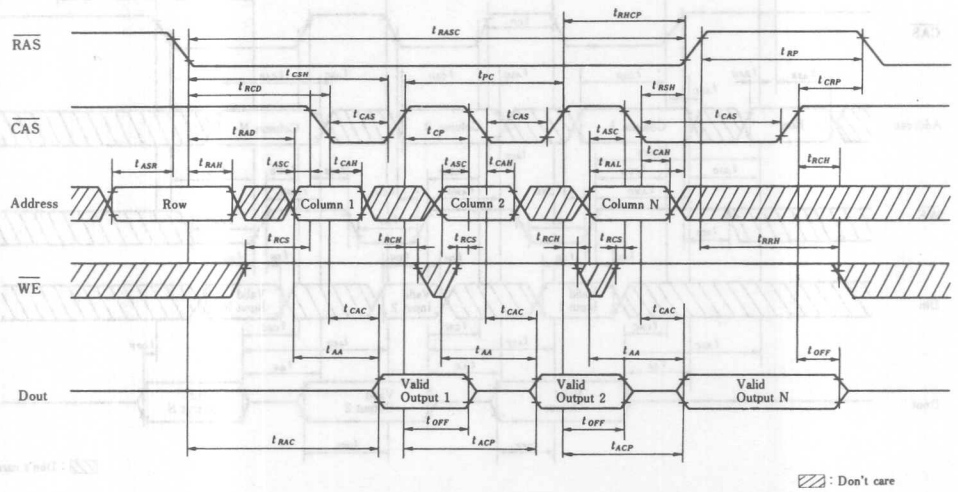
RAS-Only Refresh Cycle



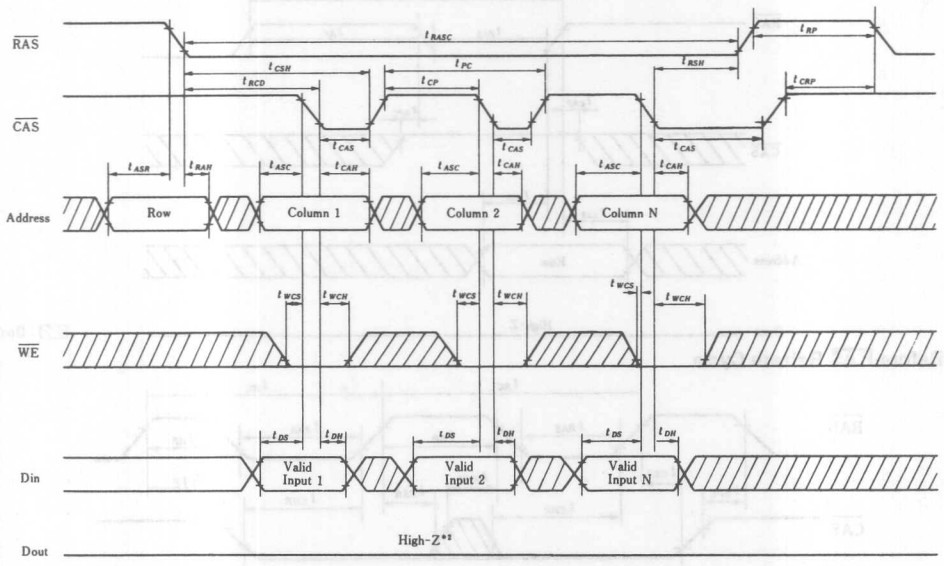
CAS-Before-RAS Refresh Cycle



Fast Page Mode Read Cycle

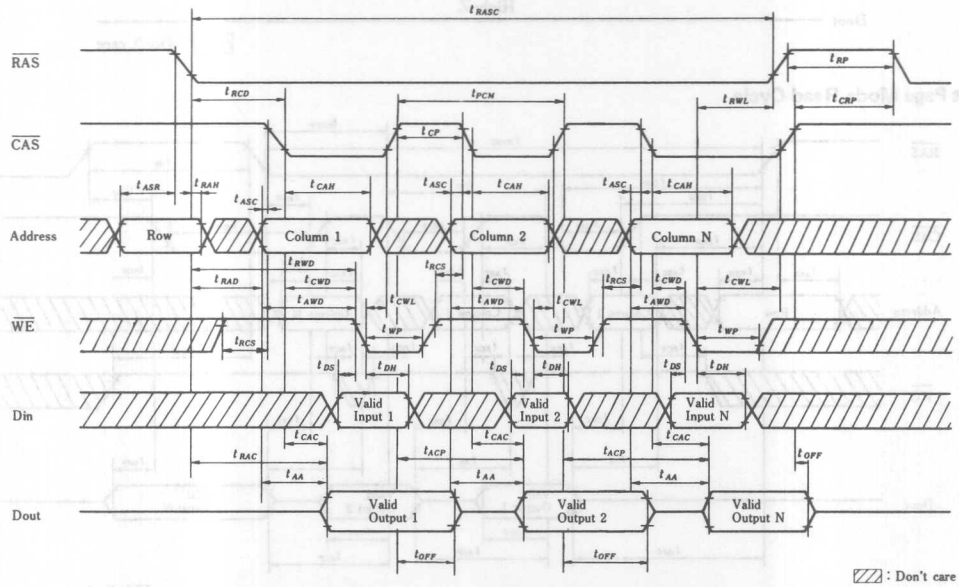


Fast Page Mode Write Cycle



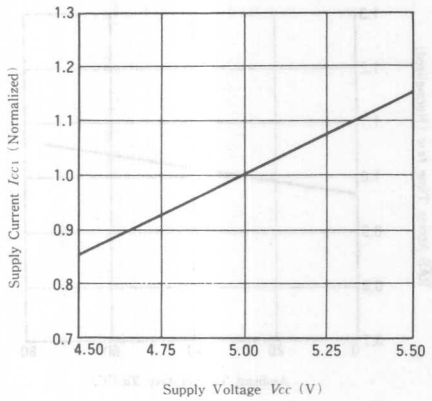
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$ (min)

Fast Page Mode Read Modify Write Cycle

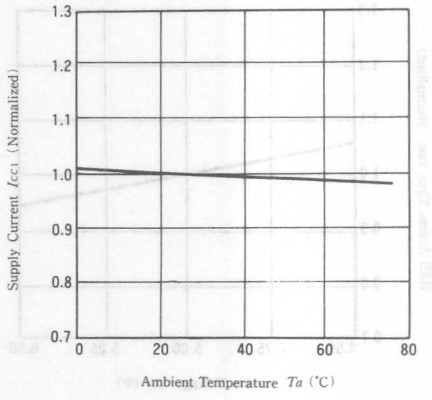


▨ : Don't care

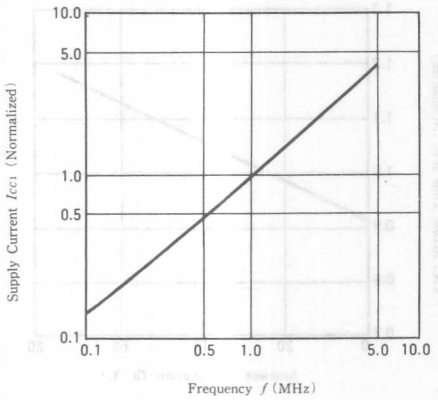
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



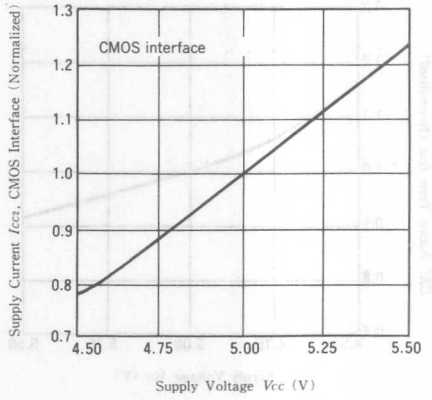
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



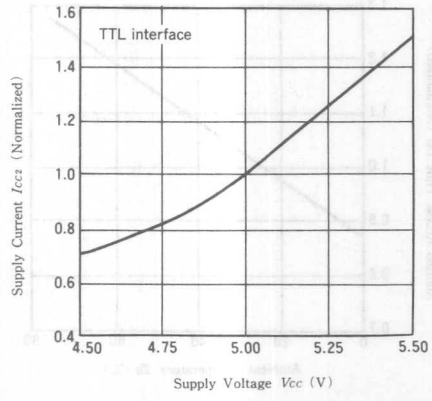
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



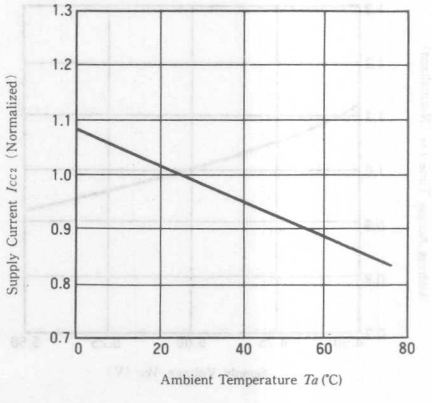
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



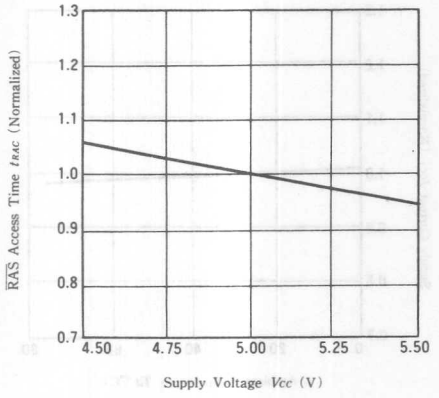
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



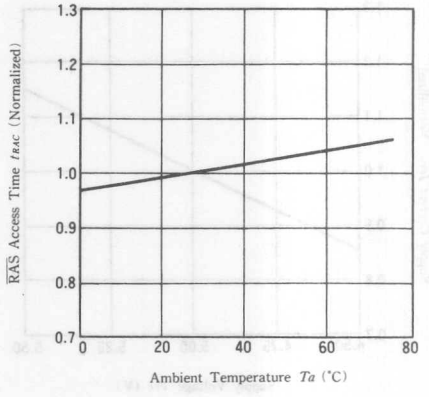
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



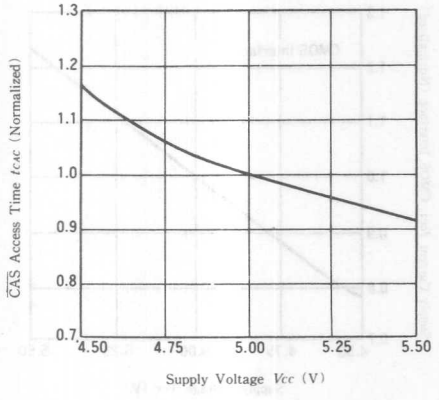
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



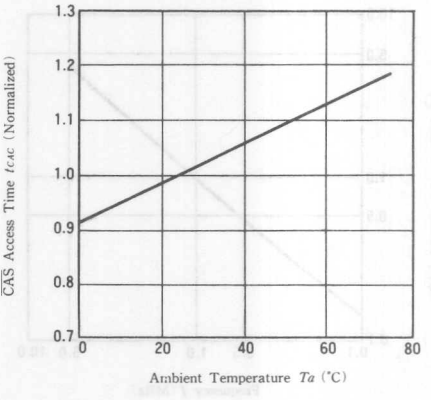
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



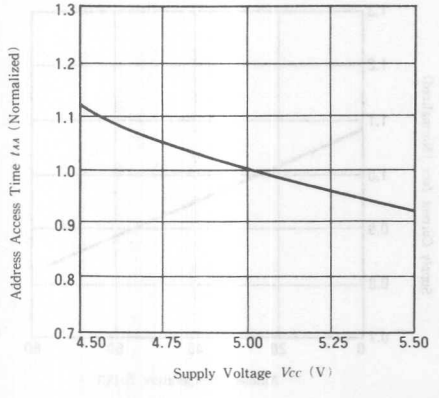
$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



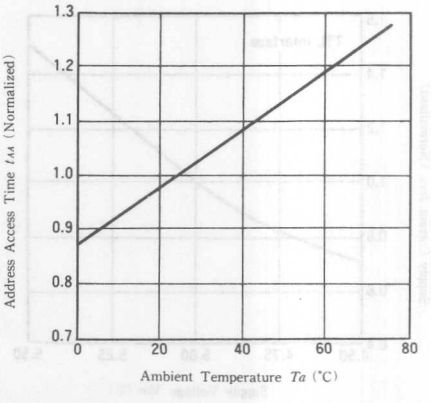
$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM511000ALP/ALJP/ALZP-8/10/12 — Preliminary

1,048,576-Word × 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM511000ALP/ALJP/ALZP family is a CMOS dynamic RAM organized 1,048,576 word × 1-bit. HM511000ALP/ALJP/ALZP has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM511000ALP/ALJP/ALZP offers Fast Page Mode as a high speed access mode.

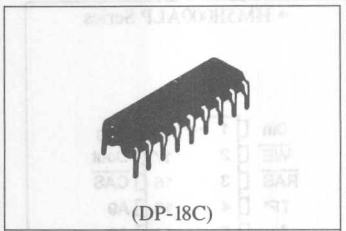
Multiplexed address input permits the HM511000ALP/ALJP/ALZP to be packaged in standard 18-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

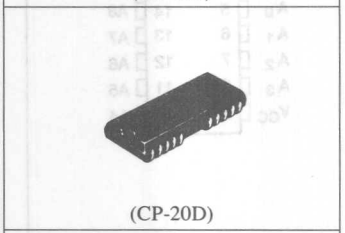
- Single 5V (±10%)
- High Speed
  - Access Time . . . . . .80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .385/330/275mW (max.)
  - Standby Mode . . . . . .1.7mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycles . . . . . .(64 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

■ ORDERING INFORMATION

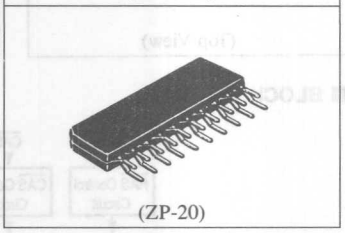
Part No.	Access	Package
HM511000ALP-8	80ns	300 mil 18 pin
HM511000ALP-10	100ns	Plastic DIP
HM511000ALP-12	120ns	(DP-18C)
HM511000ALJP-8	80ns	300 mil 20 pin
HM511000ALJP-10	100ns	Plastic SOJ
HM511000ALJP-12	120ns	(CP-20D)
HM511000ALZP-8	80ns	400 mil 20 pin
HM511000ALZP-10	100ns	Plastic ZIP
HM511000ALZP-12	120ns	(ZP-20)



(DP-18C)



(CP-20D)



(ZP-20)

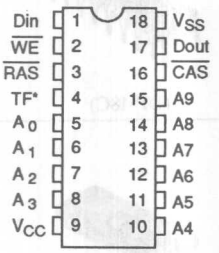
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
D_{IN}	Data-In
D_{OUT}	Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
TF	Test Function*
V_{CC}	Power Supply (+5V)
V_{SS}	Ground

* TF pin can be connected with any lines on P.C. board. However, the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

■ PIN ARRANGEMENT

• HM511000ALP Series



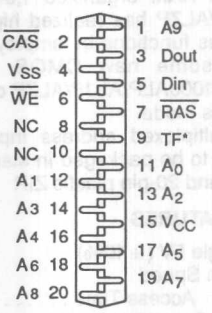
(Top View)

• HM511000ALJP Series



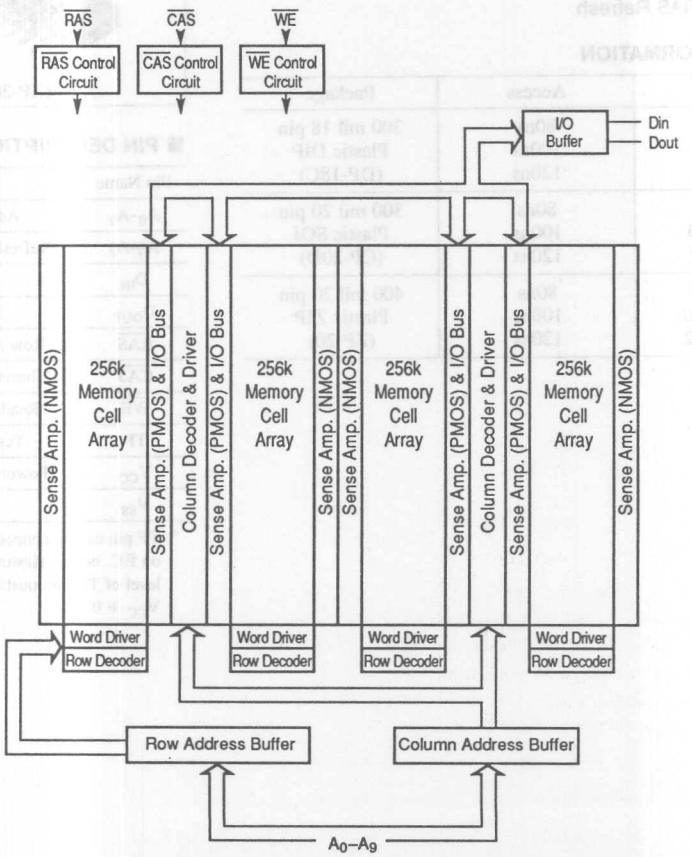
(Top View)

• HM511000ALZP Series



(Bottom View)

■ BLOCK DIAGRAM



HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	70	—	60	—	50	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High Z	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{OUT} = High Z	—	300	—	300	—	300	μA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	60	—	50	—	45	mA	2
Battery Back-Up Current	I_{CC4}	t_{RC} = 125μs, $\overline{CAS}$ Before $\overline{RAS}$ Cycling	—	300	—	300	—	300	μA	4
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	60	—	50	—	40	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	50	—	50	—	40	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.

2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

4. t_{RAS} = t_{RAS} min. to 1 μs
Input voltage: All pins ≤ V_{CC} − 0.2V or ≤ 0.2V.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address, Data-In)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-Out)	C_O	—	7	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1], [12]

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-Up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-Up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	64	—	64	—	64	ms	

• Read Cycle

Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	—	20	—	25	—	30	ns	6

• Write Cycle

Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Write Cycle Time	t_{RWC}	190	—	220	—	225	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

• Refresh Cycle

Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

• Fast Page Mode Read-Modify-Write Cycle

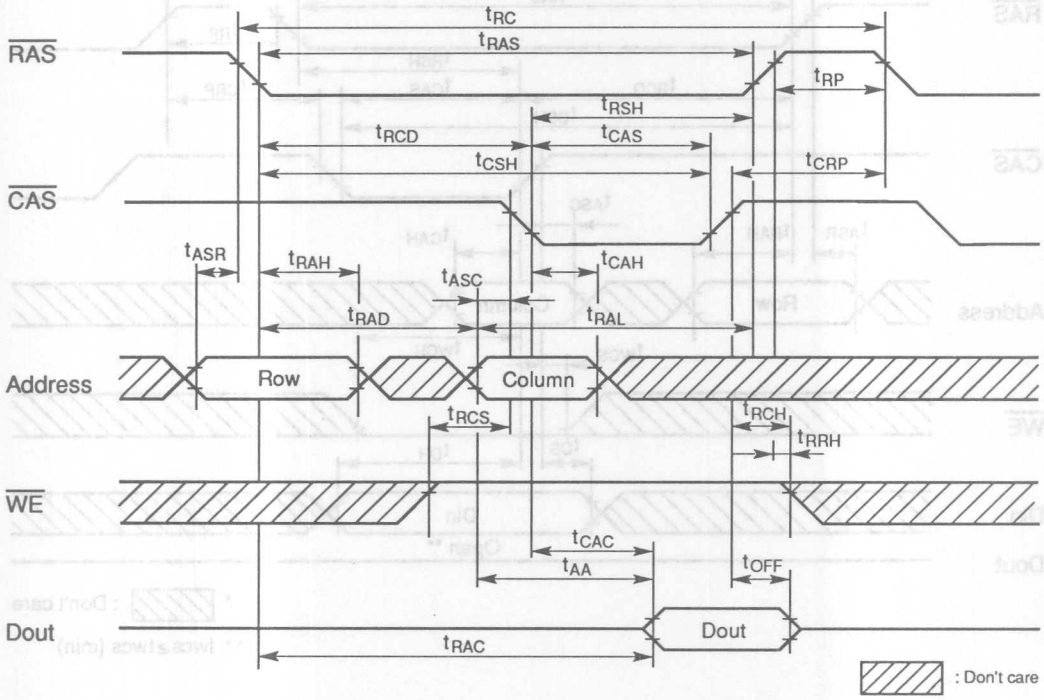
Parameter	Symbol	HM511000AL-8		HM511000AL-10		HM511000AL-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Read-Write Cycle Time	t_{PCM}	85	—	85	—	100	—	ns	

NOTES:

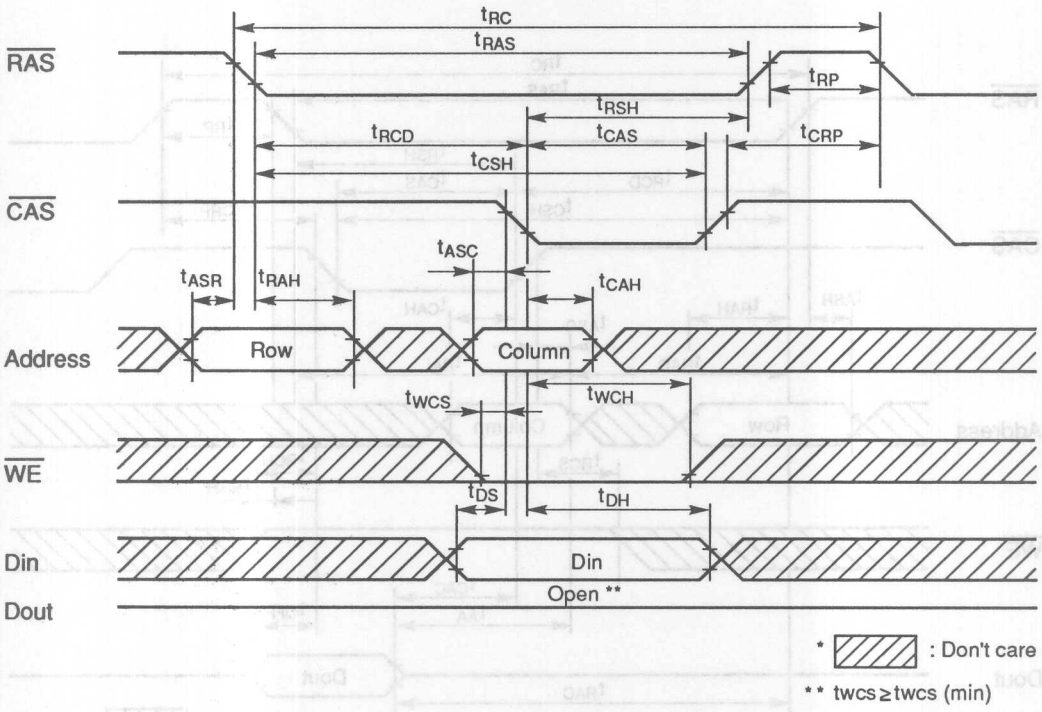
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycles.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.

■ TIMING WAVEFORMS

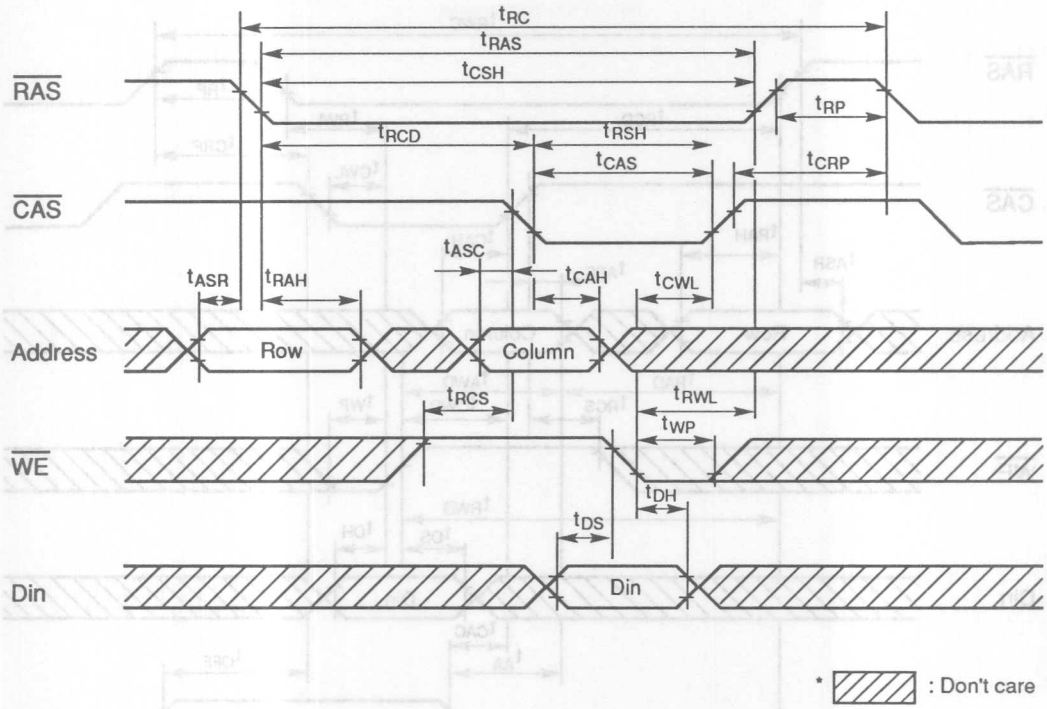
• **Read Cycle**



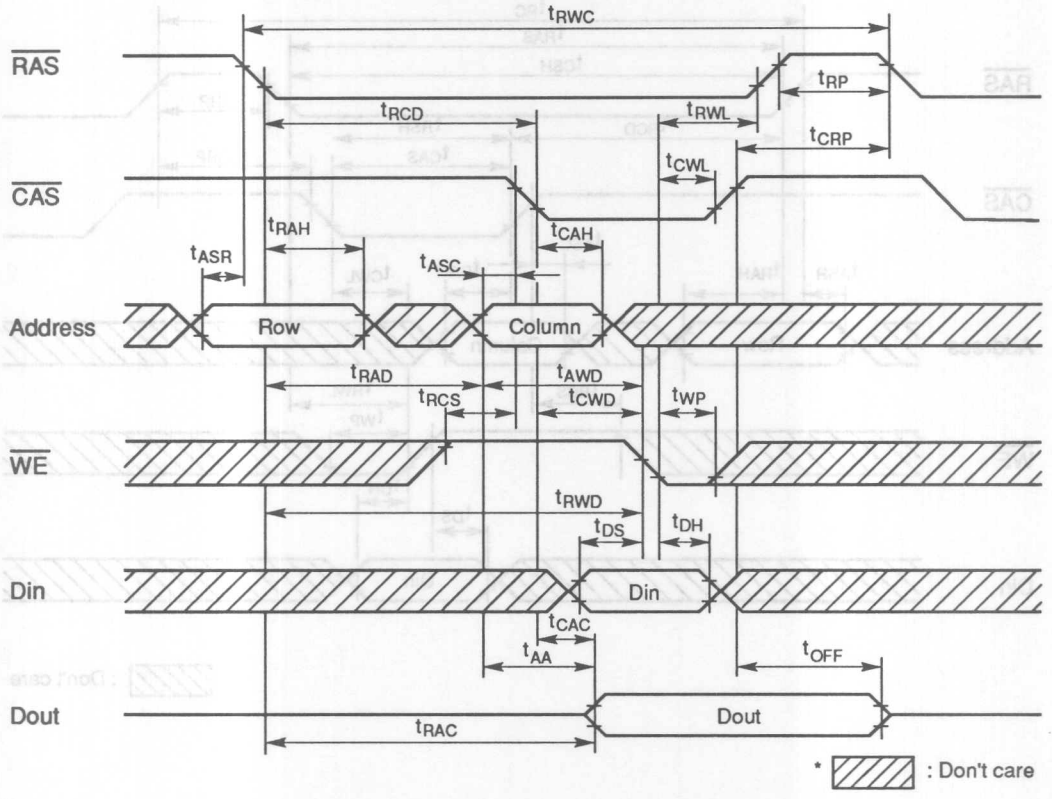
• **Early Write Cycle**



• **Delayed Write Cycle**

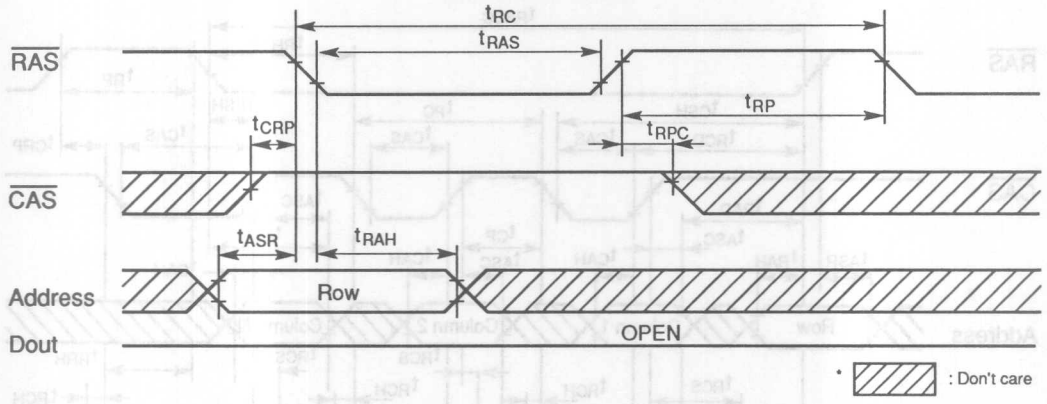


• **Read-Modify-Write Cycle**

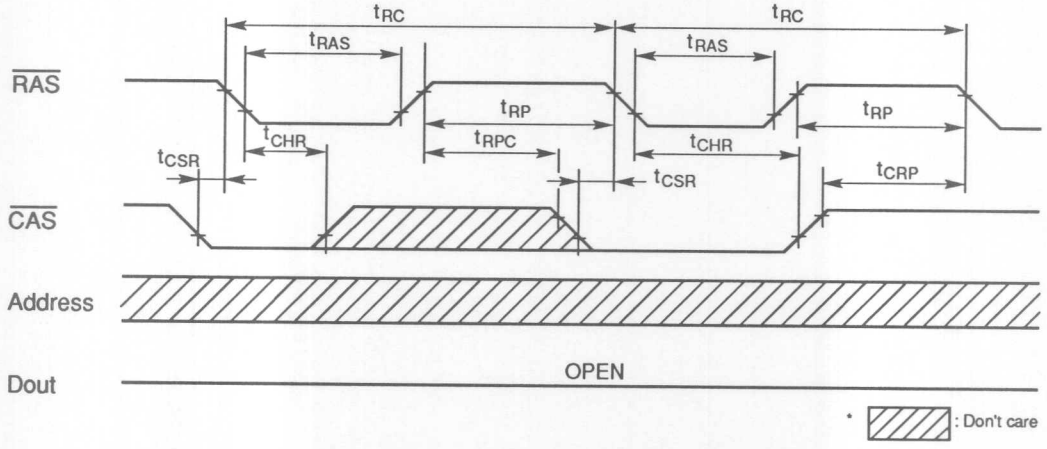


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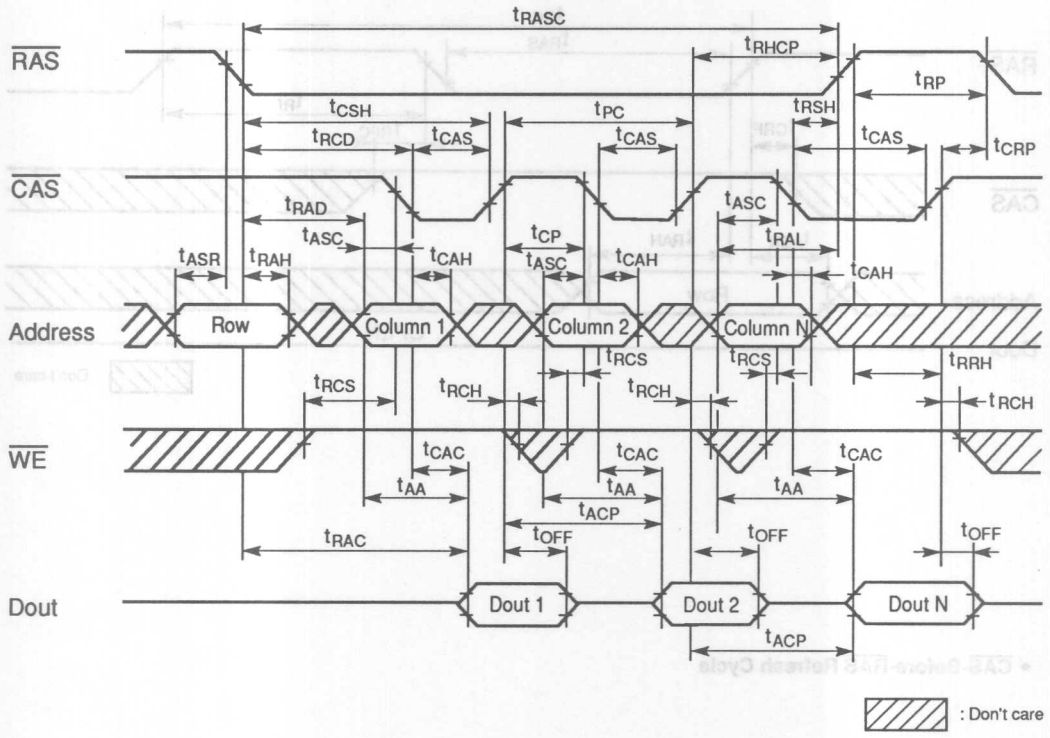
• $\overline{RAS}$-Only Refresh Cycle



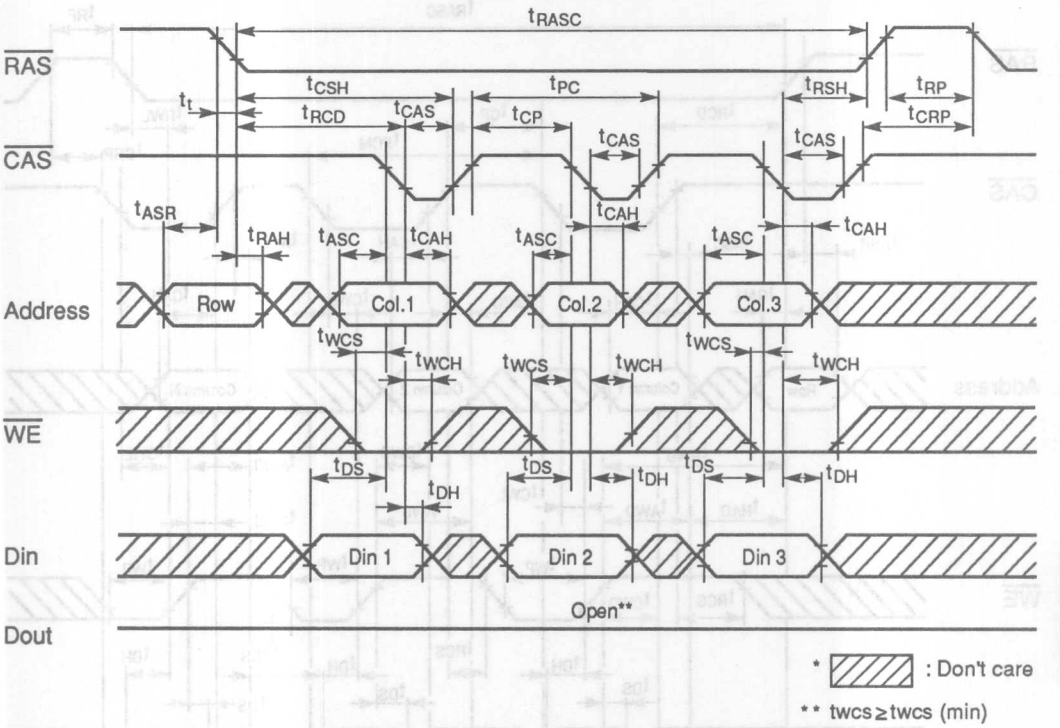
• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



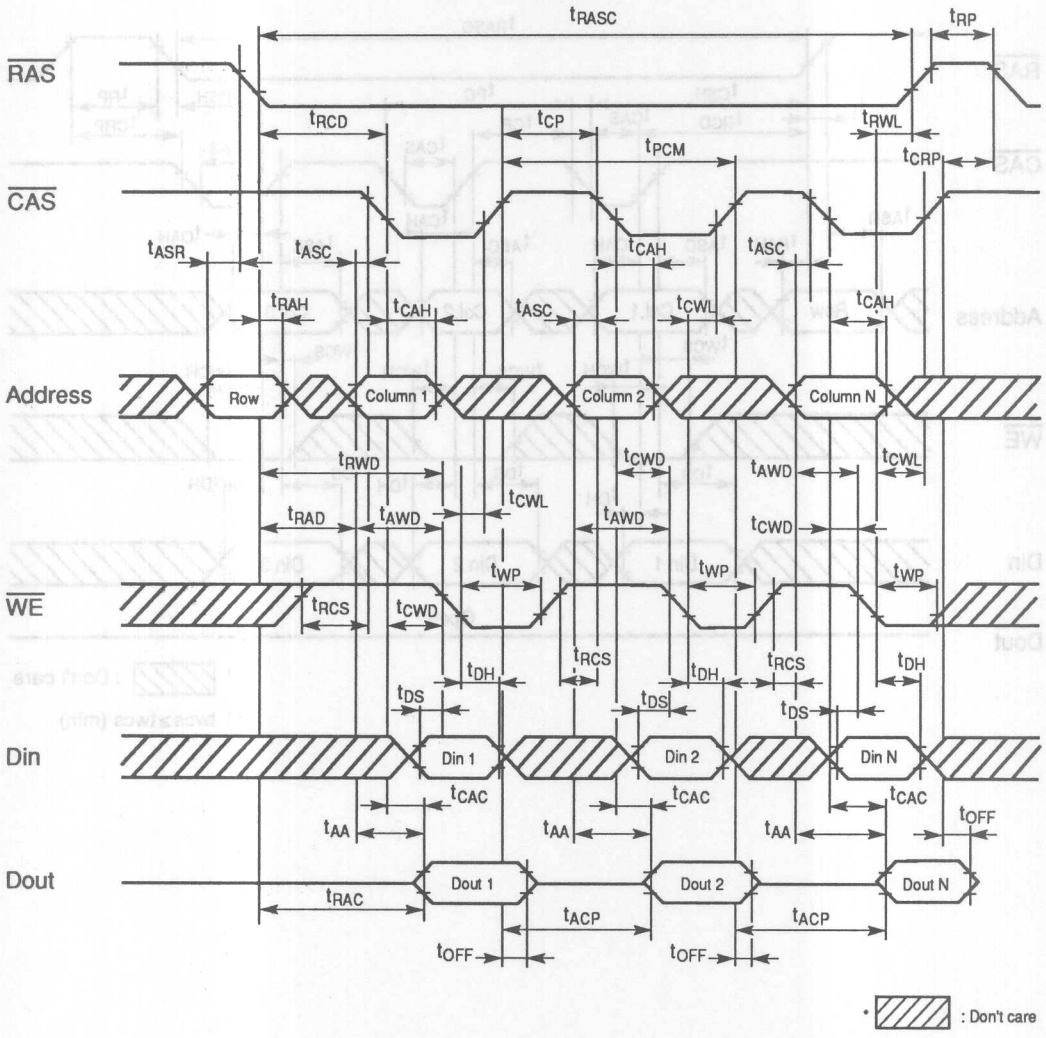
• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



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HM511000H Series

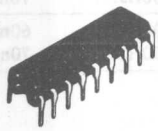
1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511000H series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000H has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000H offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511000H to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511000HP Series



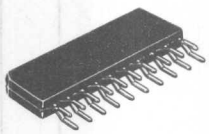
(DP-18C)

HM511000HZP Series



(CP-20D)

HM511000HJP Series



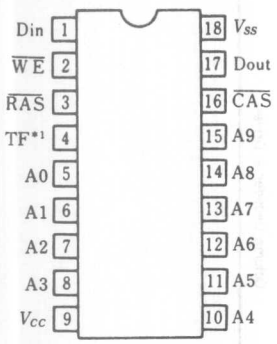
(ZP-20)

Features

- High speed; Access time 60ns/70ns (max)
- Low power; 11 mW standby, 495mW/440mW active
- Single 5V supply (±10%)
- Fast page mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

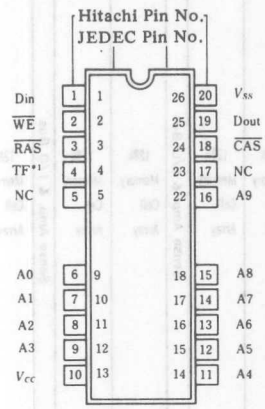
Pin Arrangement

- **HM511000HP Series**



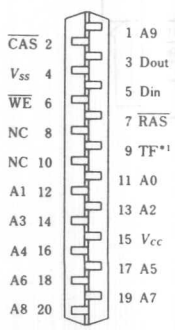
(Top View)

- **HM511000HJP Series**



(Top View)

- **HM511000HZP Series**



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

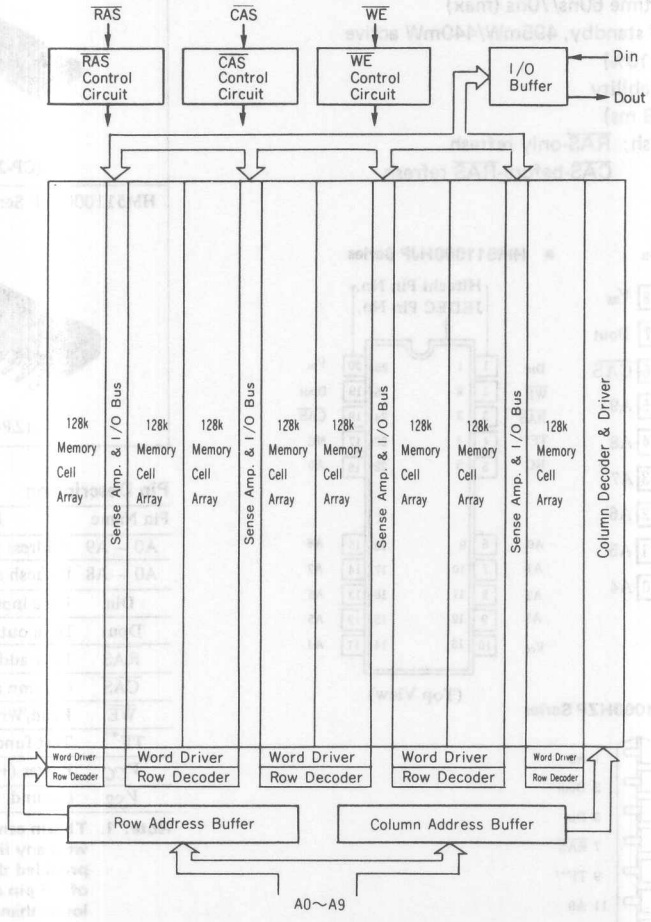
Note: 1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} +0.5V.

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Ordering Information

Type No.	Access Time	Package
HM511000HP-6	60ns	300-mil 18-pin Plastic DIP
HM511000HP-7	70ns	
HM511000HJP-6	60ns	300-mil 20-pin Plastic SOJ
HM511000HJP-7	70ns	
HM511000HZP-6	60ns	400-mil 20-pin Plastic ZIP
HM511000HZP-7	70ns	

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	$Topr$	0 to +70	°C
Storage temperature	$Tstg$	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511000H-6 Min	HM511000H-6 Max	HM511000H-7 Min	HM511000H-7 Max	Unit	Test condition	Note
Operating current	I_{CC1}	–	90	–	80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min	*1,*2
Standby current	I_{CC2}	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z TTL interface	
		–	1	–	1		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} − 0.2V Dout = High-Z CMOS interface	
Refresh current	I_{CC3}	–	90	–	80	mA	$\overline{RAS}$-only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	*1
Refresh current	I_{CC6}	–	90	–	80	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min	
Fast page mode current	I_{CC7}	–	90	–	80	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min	*1,*3
Input leakage	I_{LI}	−10	10	−10	10	μA	V_{IN} = 0 to +7V	
Output leakage	I_{LO}	−10	10	−10	10	μA	V_{OUT} = 0 to +7V, Dout = disable	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = −5mA	
	V_{OL}	0	0.4	0	0.4	V	Iout = 4.2mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10%)

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	125	–	140	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	–	60	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	–	70	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	*7
Refresh period	t_{REF}	–	8	–	8	ms	

Read Cycle

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	20	ns	*3,*4
Access time from address	t_{AA}	–	30	–	35	ns	*3,*5
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns	
Output buffer turn-off time	t_{OFF}	–	20	–	20	ns	*6

Write Cycle

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	–	0	–	ns	*10
Write command hold time	t_{WCH}	15	–	15	–	ns	
Write command pulse width	t_{WP}	10	–	10	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	*11
Data-in hold time	t_{DH}	15	–	15	–	ns	*11

Read-Modify-Write Cycle

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	150	–	165	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60	–	70	–	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20	–	20	–	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	30	–	35	–	ns	*10

Refresh Cycle

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-RAS refresh)	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15	–	15	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	45	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	–	100000	–	100000	ns	*13
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	40	–	45	ns	*14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	–	45	–	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511000H-6		HM511000H-7		Unit	Note
		Min	Max	Min	Max		
Fast page mode read-write cycle time	t_{PCM}	70	–	75	–	ns	

Notes) *1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).

*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).

*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between V_{IH} and V_{IL}.

*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

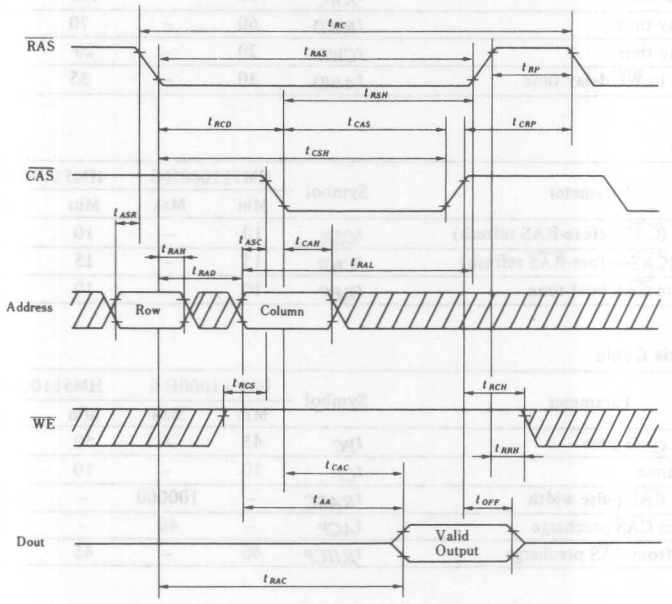
*12. An initial pause of 100μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycle.

*14. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

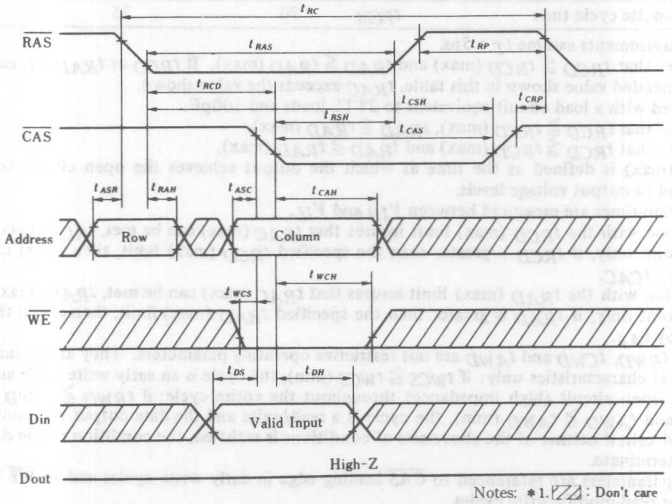
Timing Waveforms

Read Cycle



▨ : Don't care

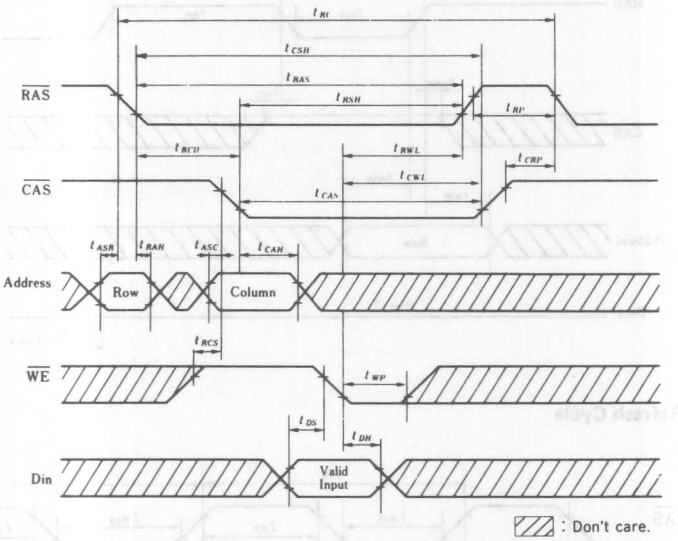
Early Write Cycle



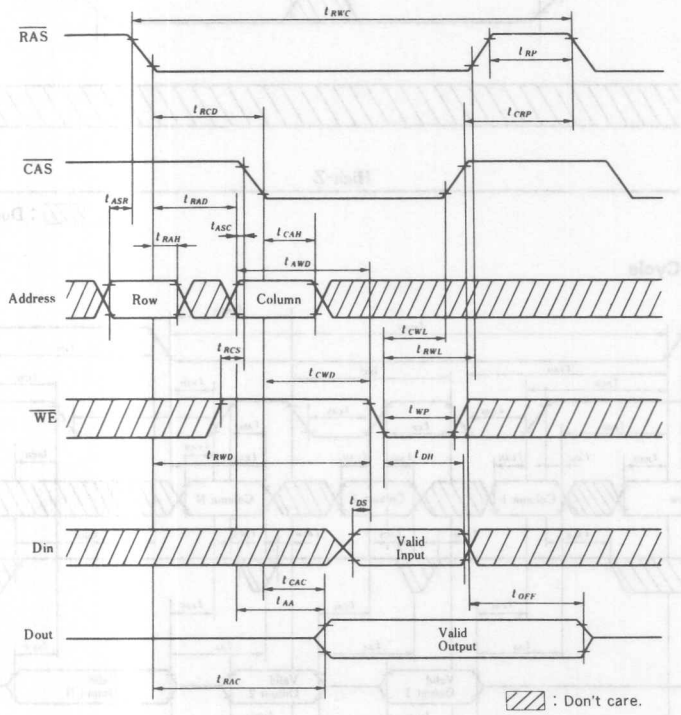
Notes: *1. ▨ : Don't care

*2. $t_{WCS} \geq t_{WCS}$(min)

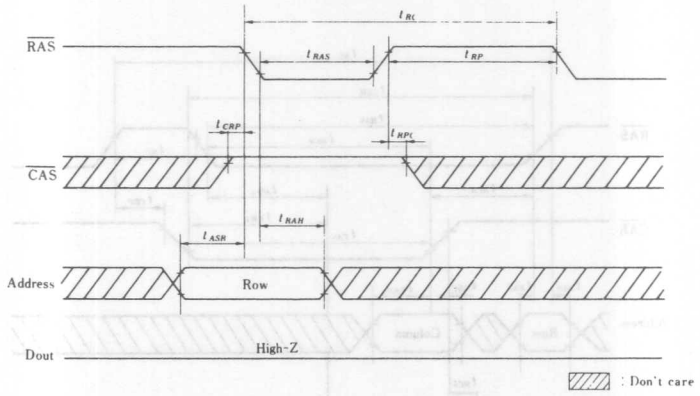
Delayed Write Cycle



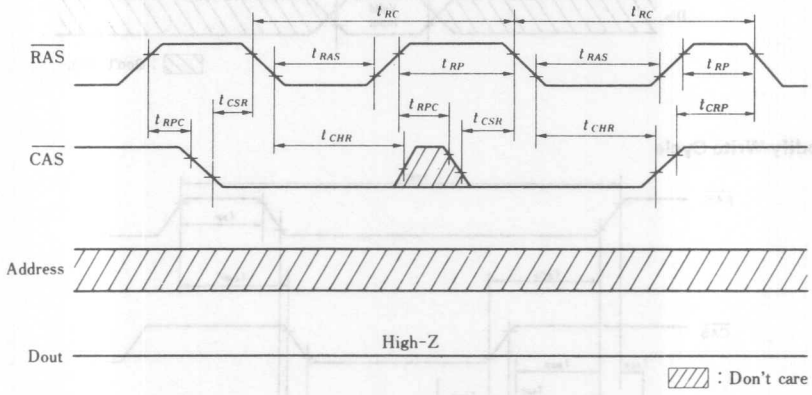
Read-Modify-Write Cycle



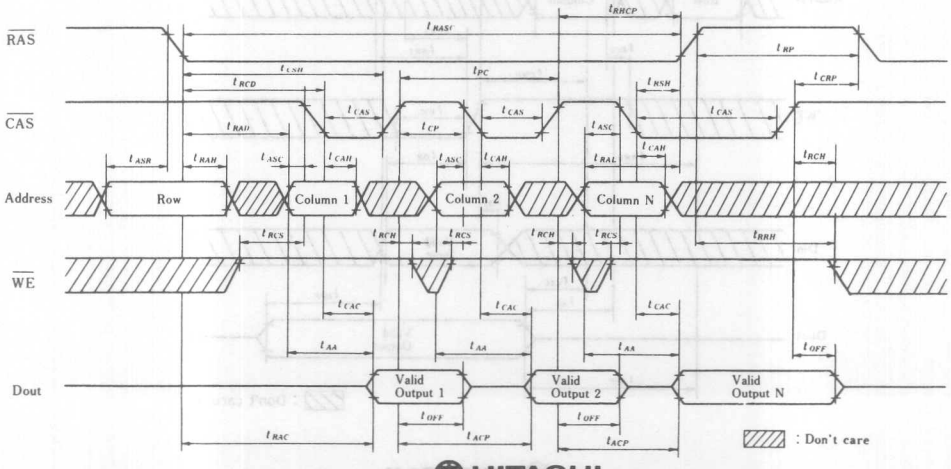
$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle

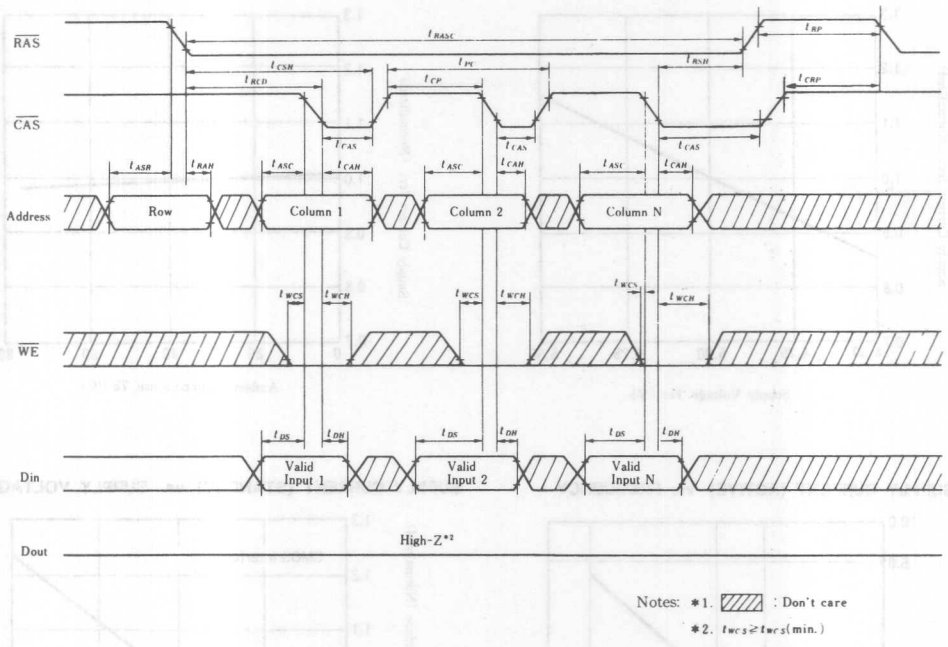


Fast Page Mode Read Cycle



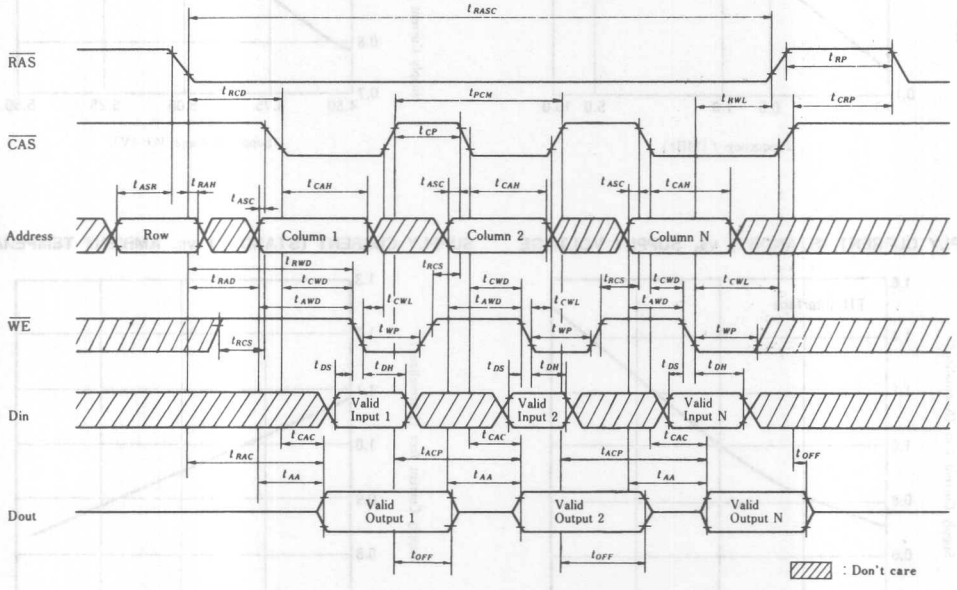
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Fast Page Mode Write Cycle

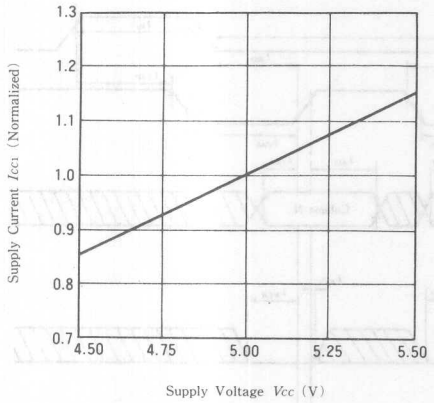


Notes: *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$(min.)

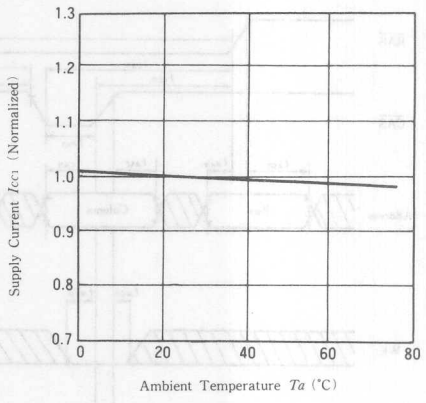
Fast Page Mode Read-Modify-Write Cycle



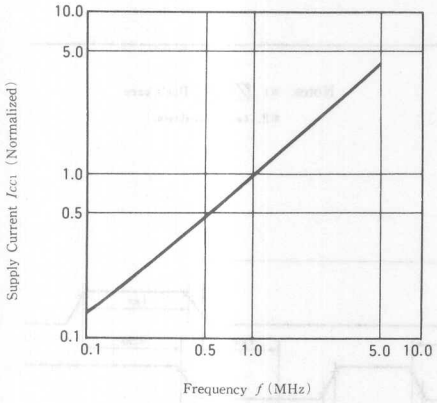
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



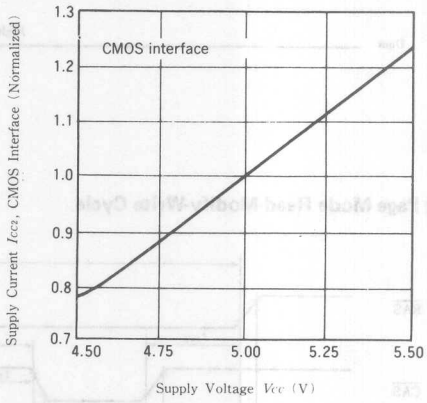
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



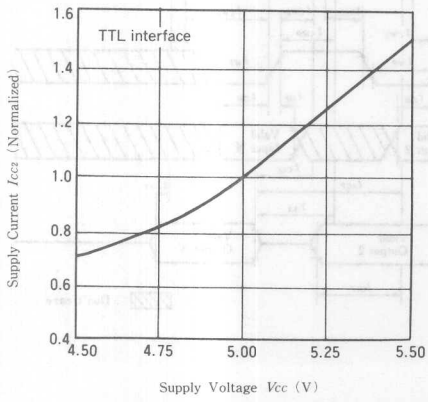
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



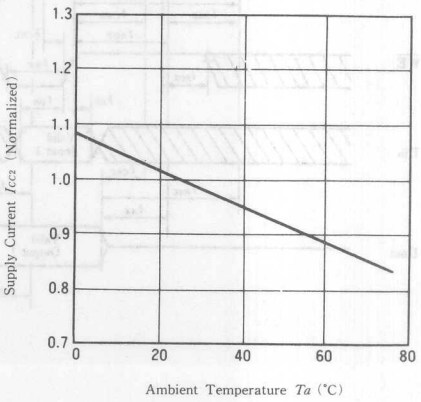
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



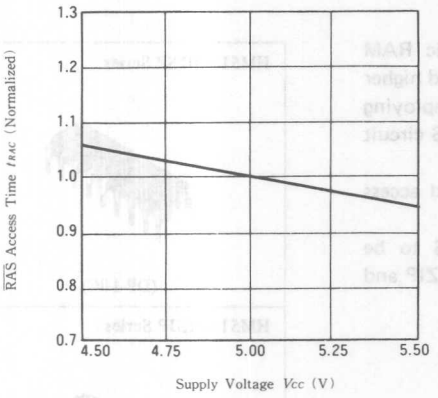
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



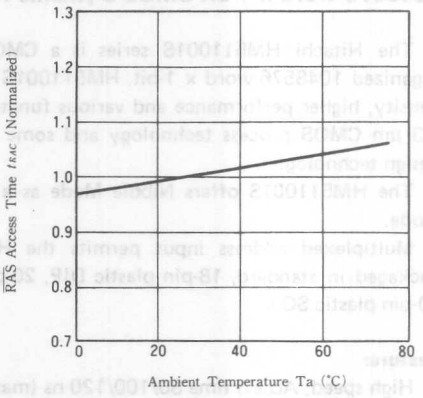
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



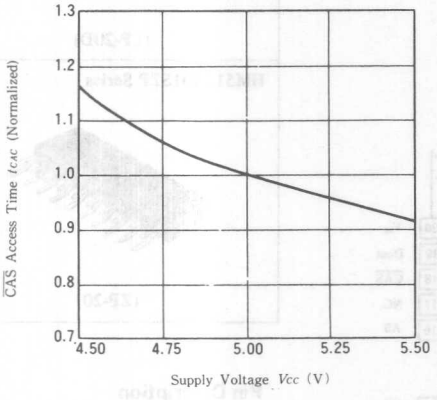
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



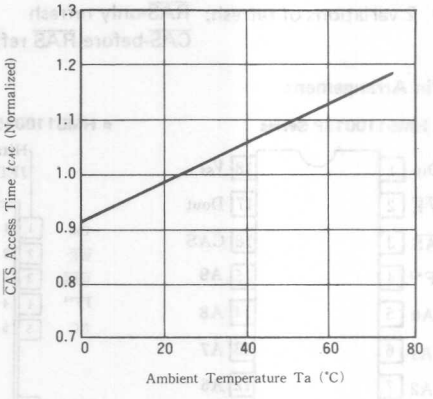
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



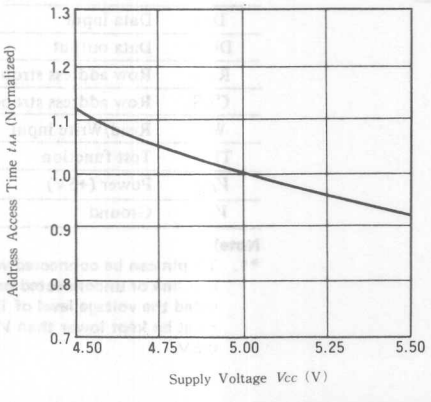
$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



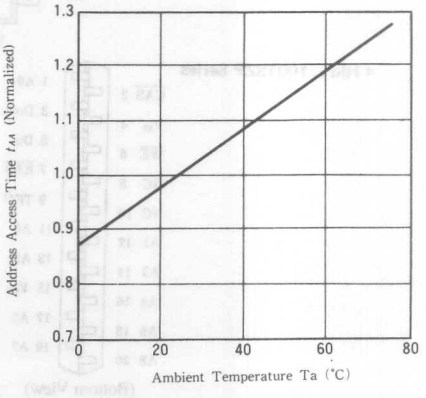
$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM511001S Series

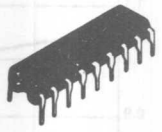
1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511001S series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511001S has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511001S offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM511001S to be packaged in standard, 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511001SP Series



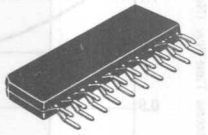
(DP-18C)

HM51101SJP Series



(CP-20D)

HM511001SZP Series



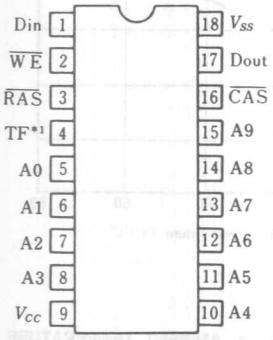
(ZP-20)

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11 mW standby, 385/330/275 mW active
- Single 5V supply (±10%)
- Nibble mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

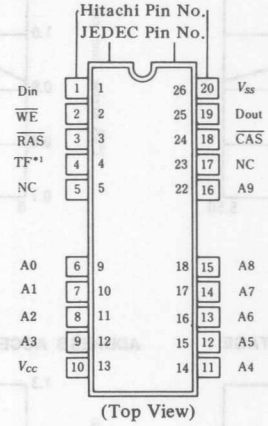
Pin Arrangement

• **HM511001SP Series**



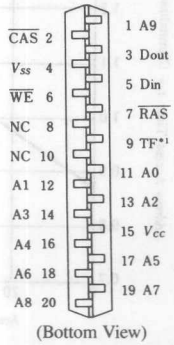
(Top View)

• **HM511001SJP Series**



(Top View)

• **HM511001SZP Series**



(Bottom View)

Pin Description

Symbol	Function
A0 – A9	Address input
A0 – A8	Refresh address input
A9	Nibble address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Row address strobe
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

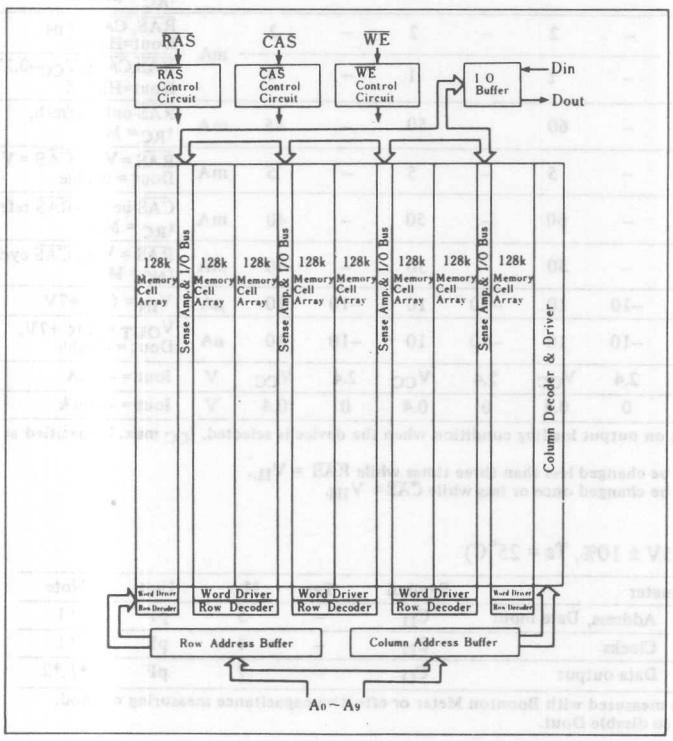
Note)

***1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.**

Ordering Information

Type No.	Access Time	Package
HM511001P-8S	80ns	300 mil 18-pin Plastic DIP
HM5110001P-10S	100ns	
HM5110001P-12S	120ns	
HM511001JP-8S	80ns	300 mil 20-pin Plastic SOJ
HM511001JP-10S	100ns	
HM511001JP-12S	120ns	
HM511001ZP-8S	80ns	400 mil 20-pin Plastic ZIP
HM511001ZP-10S	100ns	
HM511001ZP-12S	120ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Test condition		Note
		Min	Max	Min	Max	Min	Max				
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min		*1,*2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$=V_{IH} Dout=High-Z	TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$,$\overline{CAS}$≧V_{CC}–0.2V Dout=High-Z	CMOS interface	
Refresh current	I_{CC3}	–	60	–	50	–	45	mA	$\overline{RAS}$-only refresh, t_{RC} = Min		*2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable		*1
Refresh current	I_{CC6}	–	60	–	50	–	40	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min.		
Nibble mode current	I_{CC8}	–	50	–	50	–	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{NC} = Min		*1,*3
Input leakage	I_{LI}	–10	10	–10	10	–10	10	μA	V_{IN} = 0 to +7V		
Output leakage	I_{LO}	–10	10	–10	10	–10	10	μA	V_{OUT} = 0 to +7V, Dout = disable		
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5mA		
	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2mA		

Notes) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)*1,*10

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10000	50	10000	60	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	40	25	50	25	60	ns	7
$\overline{RAS}$ hold time	t_{RSH}	40	–	50	–	60	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
Refresh period	t_{REF}	–	8	–	8	–	8	ms	

Read Cycle

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	2,3
Access time from $\overline{CAS}$	t_{CAC}	–	40	–	50	–	60	ns	3,4
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Output buffer turn-off delay	t_{OFF}	–	20	–	25	–	30	ns	5

Write Cycle

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	8
Write command hold time	t_{WCH}	20	–	20	–	25	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	25	–	30	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in hold time	t_{DH}	20	–	20	–	25	–	ns	9

Read-Modify-Write Cycle

Parameter	Symbol	HM511001-8S		HM511001-10S		MH511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	190	–	210	–	245	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	90	–	110	–	ns	8
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	–	40	–	50	–	ns	8

Refresh Cycle

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	10	–	ns	

Nibble Mode Cycle

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Nibble mode access time	t_{NAC}	–	25	–	25	–	30	ns	
Nibble mode cycle time	t_{NC}	45	–	45	–	50	–	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10	–	10	–	10	–	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCA}	25	–	25	–	30	–	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25	–	25	–	30	–	ns	

Nibble Mode Read-Modify-Write

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Nibble mode read-modify-write cycle time	t_{NRWC}	65	–	65	–	75	–	ns	
Nibble mode write command $\overline{CAS}$ lead time	t_{NCWL}	20	–	20	–	25	–	ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay time	t_{NCWD}	20	–	20	–	25	–	ns	

Notes)

*1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).

*5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*6. Transition times are measured between V_{IH} and V_{IL}.

*7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

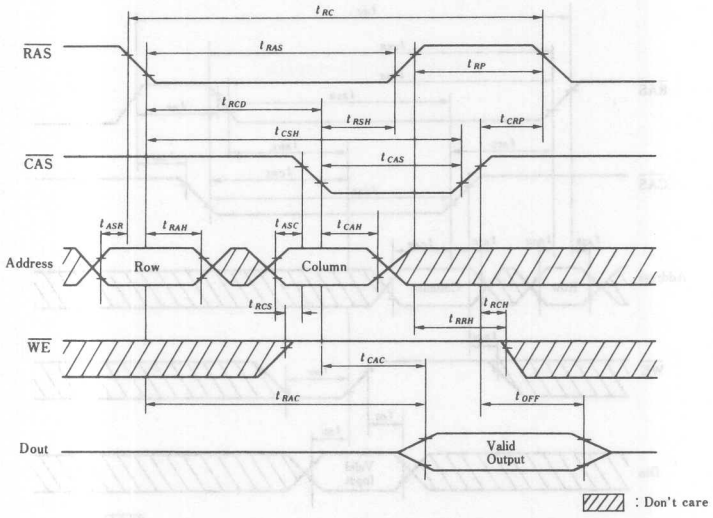
*8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min) and $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

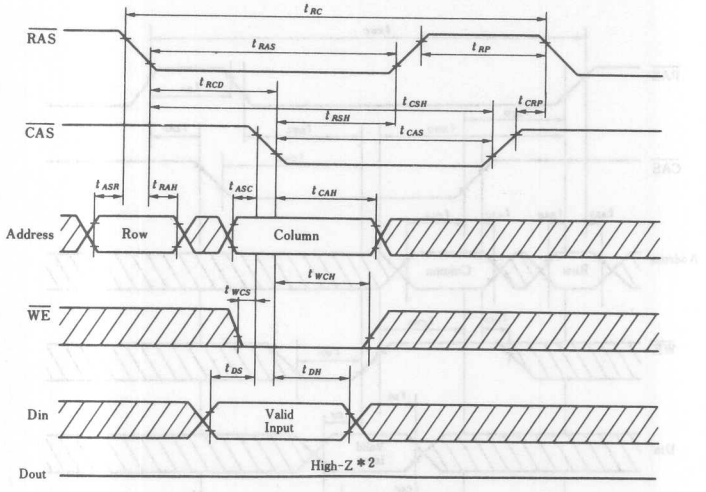
*10. An initial pause of 100μs is required after power-up followed by eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

Read Cycle

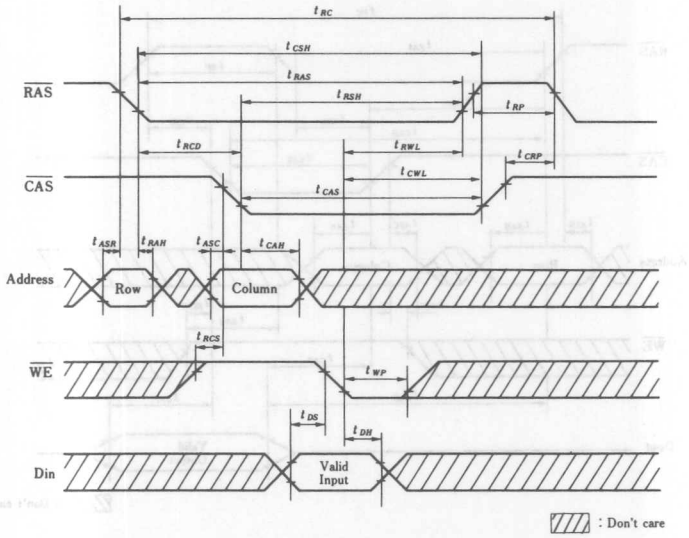


Early Write Cycle

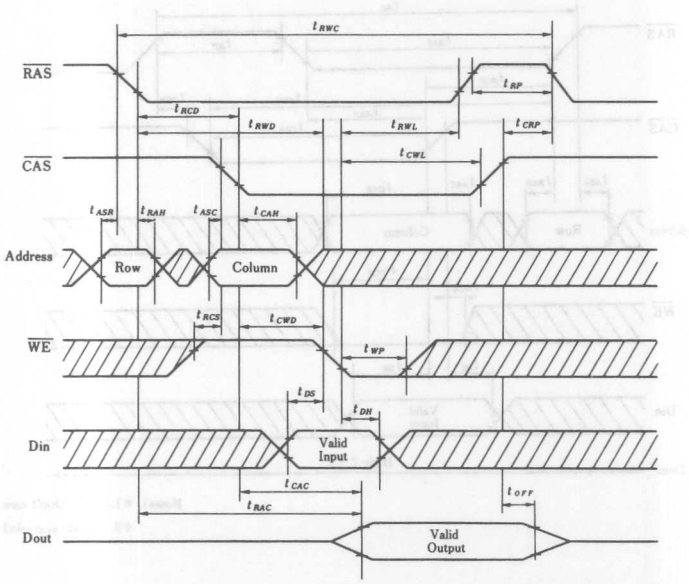


Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

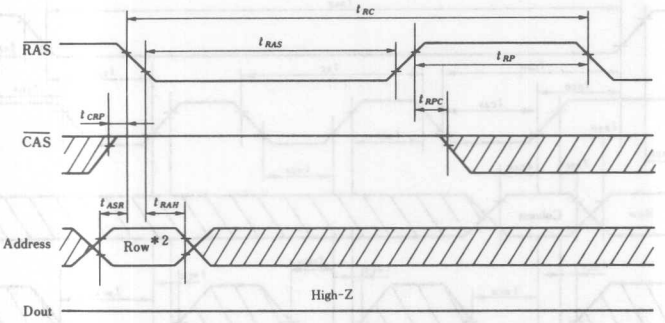
Delayed Write Cycle



Read-Modify-Write Cycle

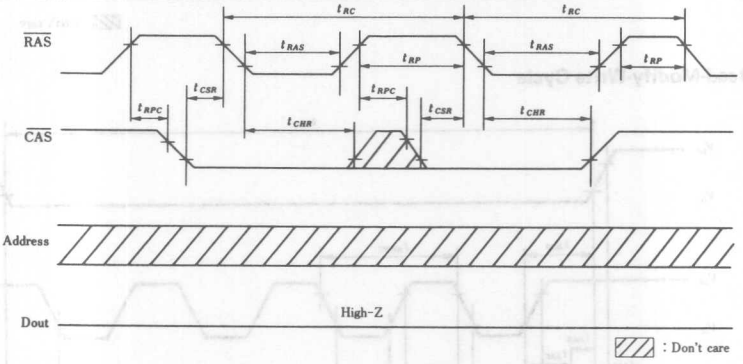


$\overline{RAS}$-Only Refresh Cycle

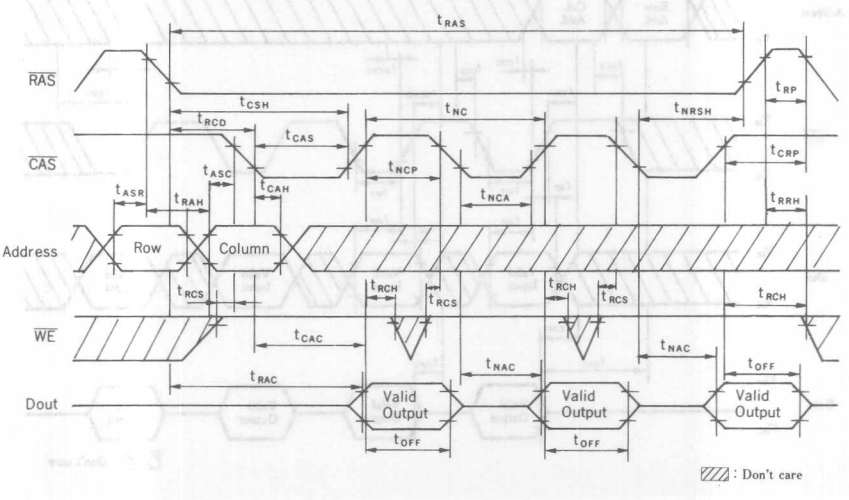


Notes) *1. ▨: Don't care
*2. Refresh Address
A0-A8(AX0-AX8)

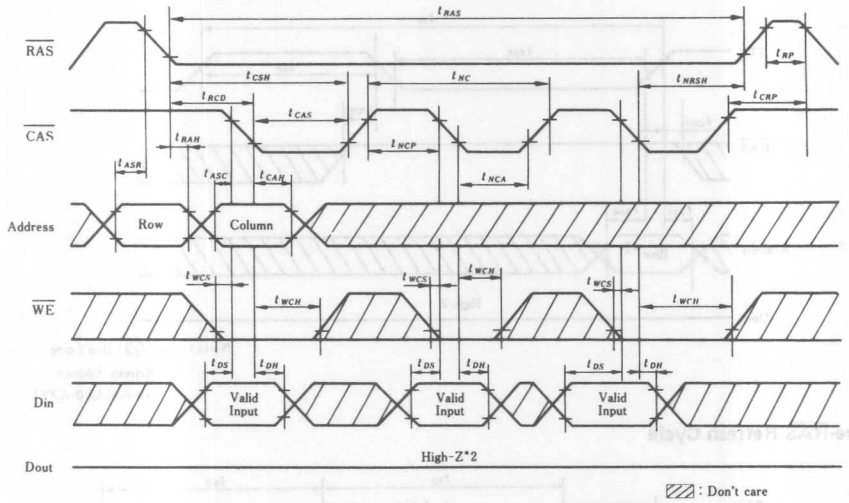
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



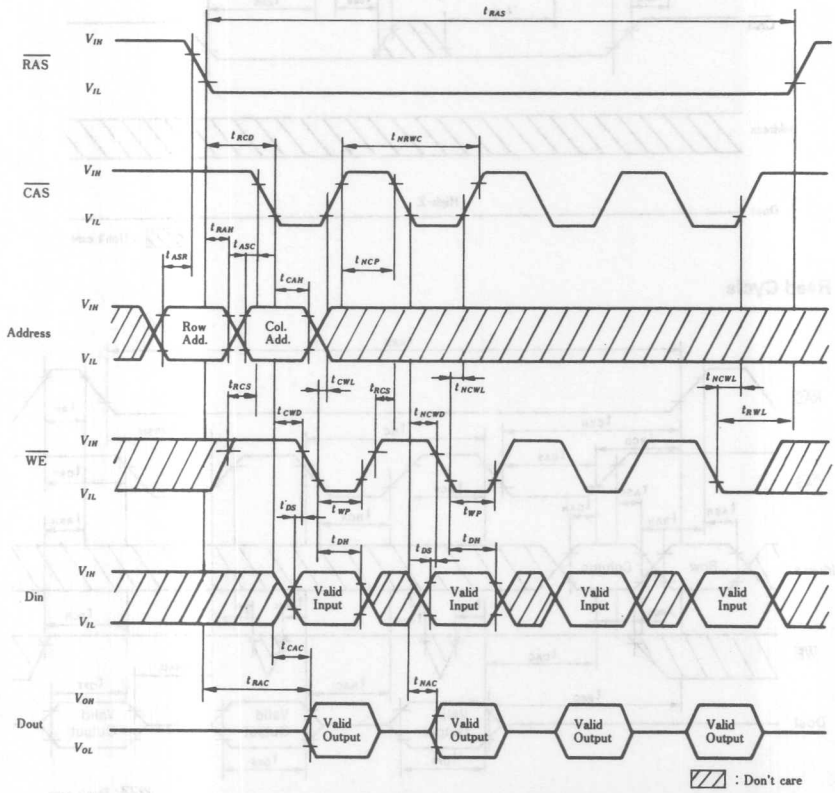
Nibble Mode Read Cycle



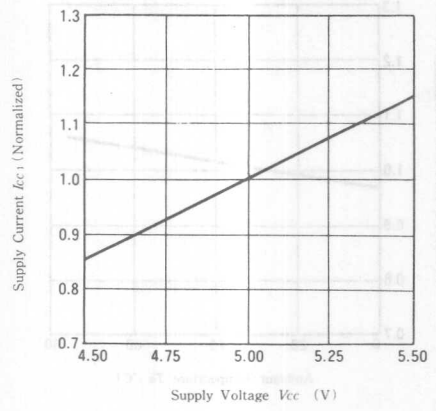
Nibble Mode Write Cycle



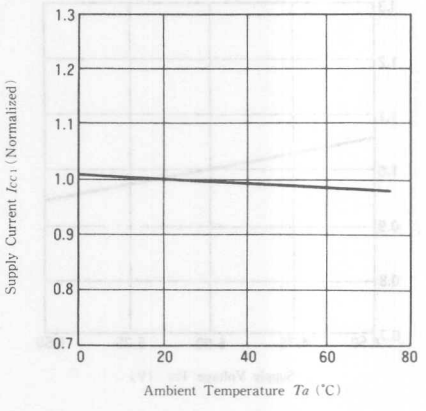
Nibble Mode Read-Modify-Write Cycle



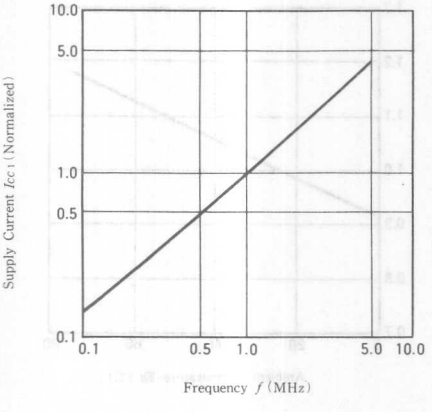
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



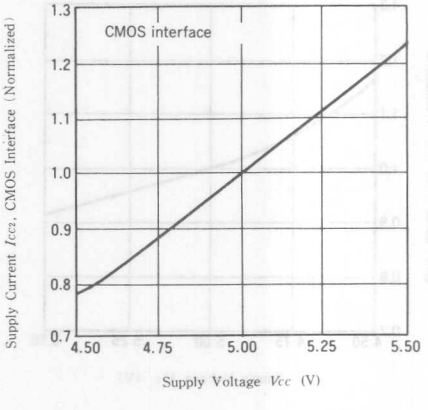
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



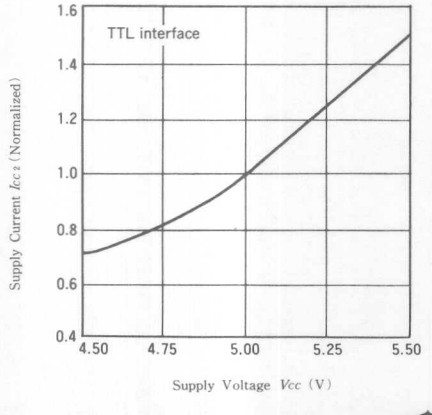
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



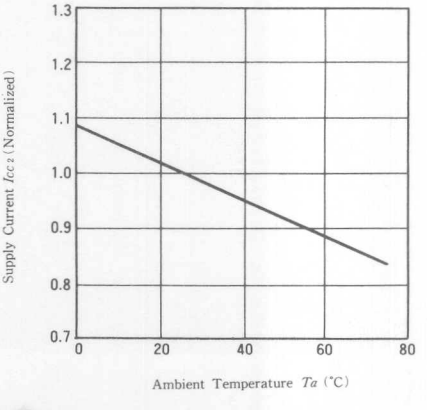
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



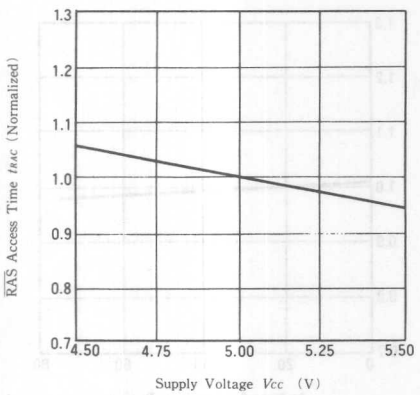
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



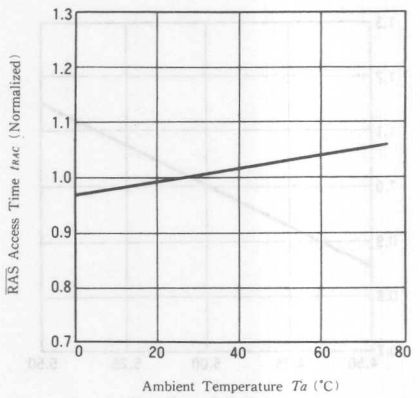
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



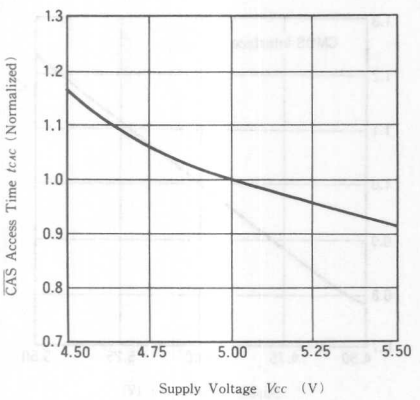
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



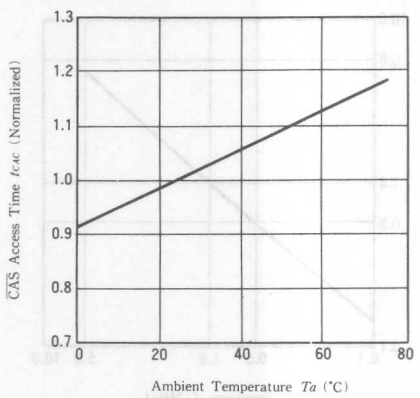
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



HM511001A Series

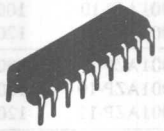
1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511001A series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511001A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511001A offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM511001A to be packaged in standard, 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511001AP Series



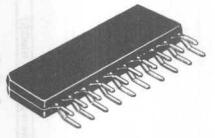
(DP-18C)

HM511001AJP Series



(CP-20D)

HM511001AZP Series



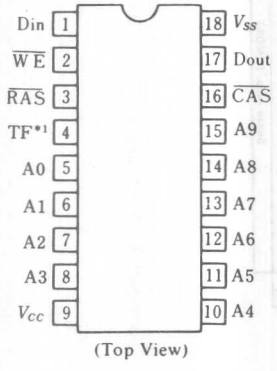
(ZP-20)

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11 mW standby, 385/330/275 mW active
- Single 5V supply (±10%)
- Nibble mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

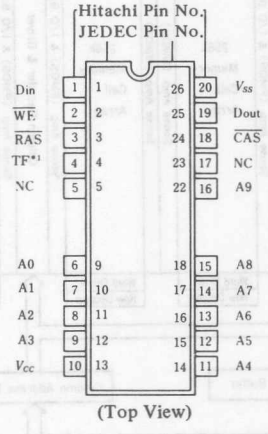
Pin Arrangement

- **HM511001AP Series**



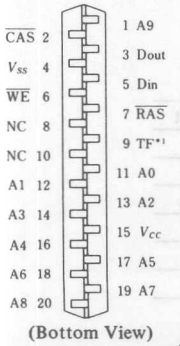
(Top View)

- **HM511001AJP Series**



(Top View)

- **HM511001AZP Series**



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
A9	Nibble address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Row address input
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

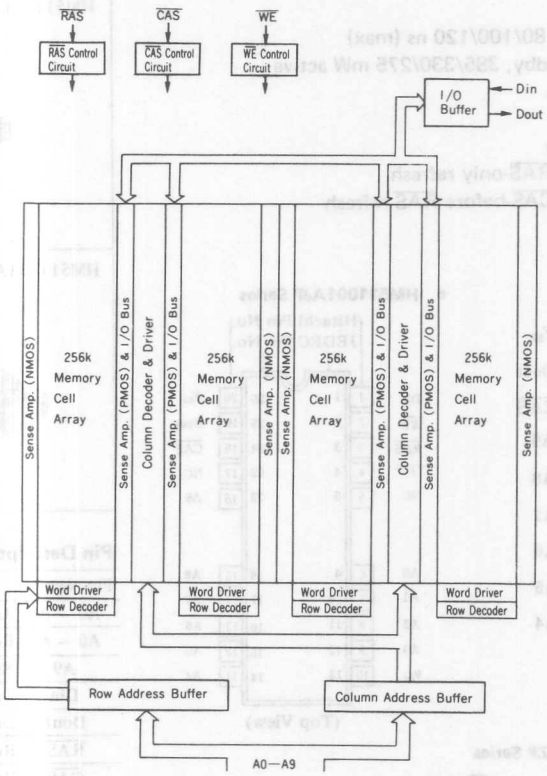
Note: 1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

HITACHI

Ordering Information

Type No.	Access Time	Package
HM511001AP-8	80ns	300 mil 18-pin Plastic DIP
HM511001AP-10	100ns	
HM511001AP-12	120ns	
HM511001AJP-8	80ns	300 mil 20-pin Plastic SOJ
HM511001AJP-10	100ns	
HM511001AJP-12	120ns	
HM511001AZP-8	80ns	400 mil 20-pin Plastic ZIP
HM511001AZP-10	100ns	
HM511001AZP-12	120ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	*Iout*	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	*Topr*	0 to +70	°C
Storage temperature	*Tstg*	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Test condition	Note
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min	*1,*2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$,$\overline{CAS}$≧V_{CC}−0.2V Dout = High-Z CMOS interface	
Refresh current	I_{CC3}	–	70	–	60	–	50	mA	$\overline{RAS}$-only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	*1
Refresh current	I_{CC6}	–	60	–	50	–	40	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min.	
Nibble mode current	I_{CC8}	–	50	–	50	–	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{NC} = Min	*1,*3
Input leakage	I_{LI}	−10	10	−10	10	−10	10	μA	V_{IN} = 0 to +7V	
Output leakage	I_{LO}	−10	10	−10	10	−10	10	μA	V_{OUT} = 0 to +7V, Dout = disabled	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = −5mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1, *2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)*1,*10

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference lvels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	*7
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	*11
$\overline{RAS}$ hold time	t_{RSH}	25	–	25	–	30	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	*6
Refresh period	t_{REF}	–	8	–	8	–	8	ms	

Read Cycle

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	–	25	–	25	–	30	ns	*3,*4
Access time from address	t_{AA}	–	40	–	45	–	55	ns	*3,*4
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	45	–	55	–	ns	
Output buffer turn-off delay	t_{OFF}	–	20	–	25	–	30	ns	*5

Write Cycle

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	*8
Write command hold time	t_{WCH}	20	–	20	–	25	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	25	–	30	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	*9
Data-in hold time	t_{DH}	20	–	20	–	25	–	ns	*9

Read-Modify-Write Cycle

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	190	–	210	–	245	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	90	–	110	–	ns	*8
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	25	–	25	–	30	–	ns	*8
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	45	–	55	–	ns	*8

Refresh Cycle

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	10	–	ns	

Nibble Mode Cycle

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble mode access time	t_{NAC}	–	25	–	25	–	30	ns	
Nibble mode cycle time	t_{NC}	45	–	45	–	50	–	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10	–	10	–	10	–	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCA}	25	–	25	–	30	–	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25	–	25	–	30	–	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511001A-8		HM511001A-10		HM511001A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble mode read-modify-write cycle time	t_{NRWC}	65	–	65	–	75	–	ns	
Nibble mode write command $\overline{CAS}$ lead time	t_{NCWL}	20	–	20	–	25	–	ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay time	t_{NCWD}	20	–	20	–	25	–	ns	

Notes)

*1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).

*5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*6. Transition times are measured between V_{IH} and V_{IL}.

*7. Operation with the t_{RCD} (max) limit insures that tRAC (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

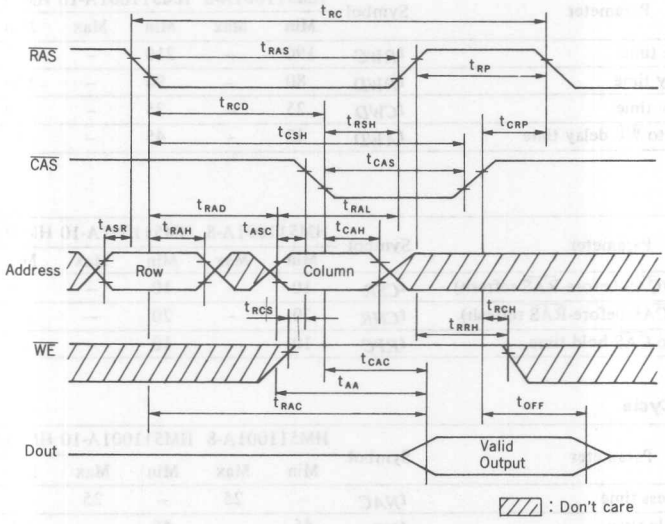
*9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

*10. An initial pause of 100μs is required after power-up followed by eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

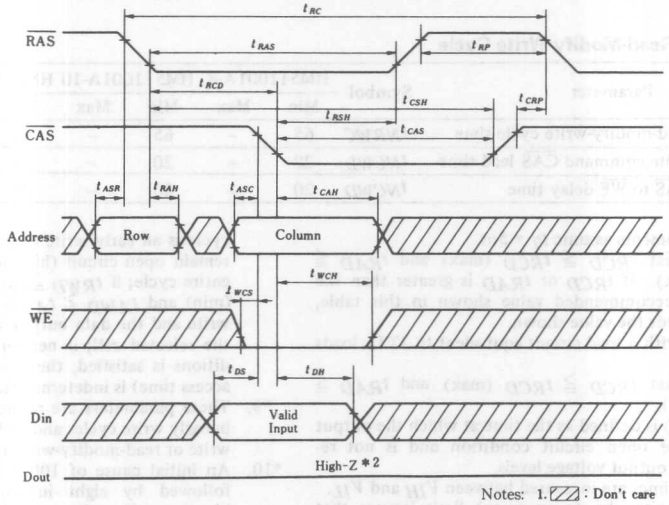
*11. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

Timing Waveforms

Read Cycle

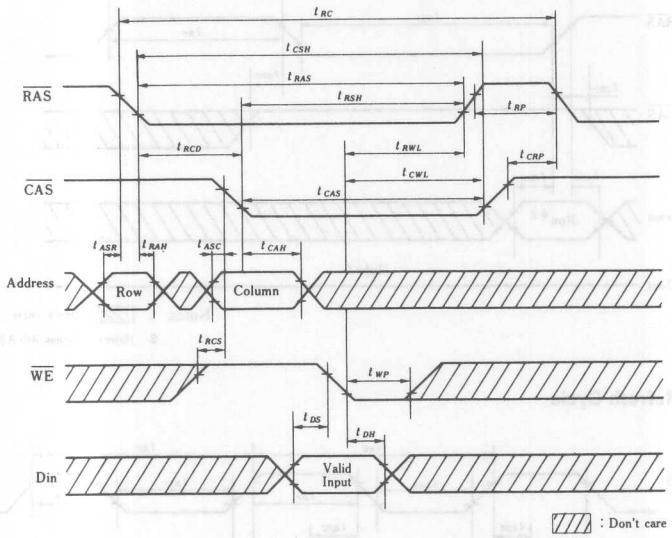


Early Write Cycle

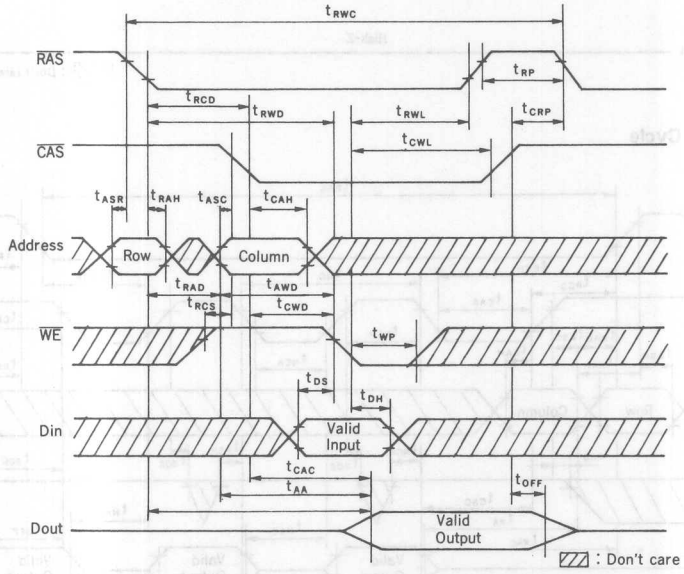


Notes: 1. ▨ : Don't care
2. $t_{WCS} \geq t_{WCS}$(min)

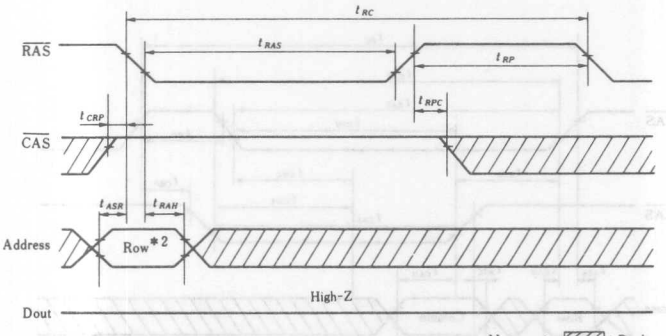
Delayed Write Cycle



Read-Modify-Write Cycle

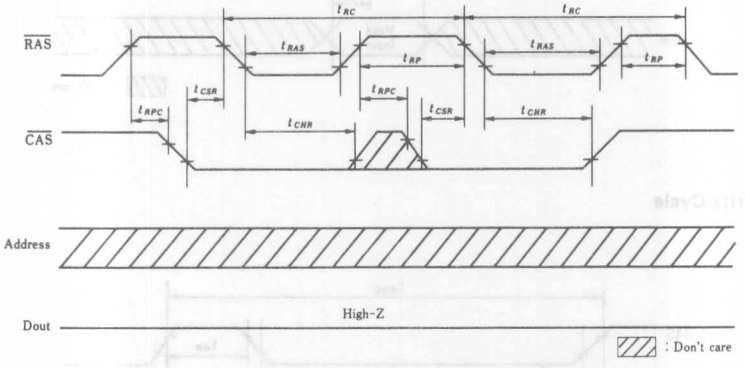


$\overline{RAS}$-Only Refresh Cycle

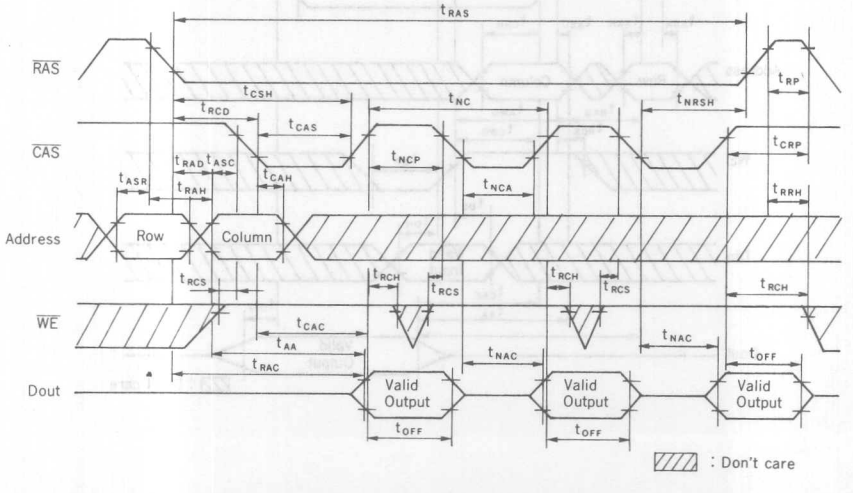


Notes: 1. ▨: Don't care
2. Refresh address A0-A8(AX0-AX8)

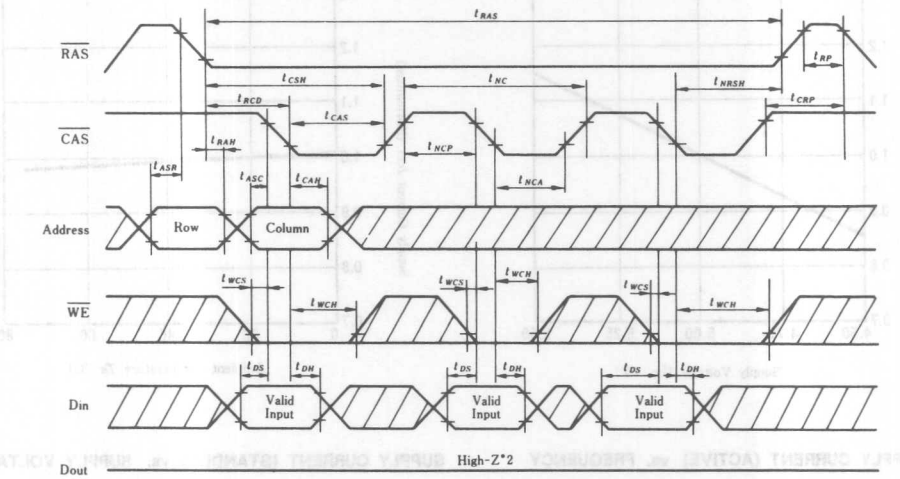
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



Nibble Mode Read Cycle

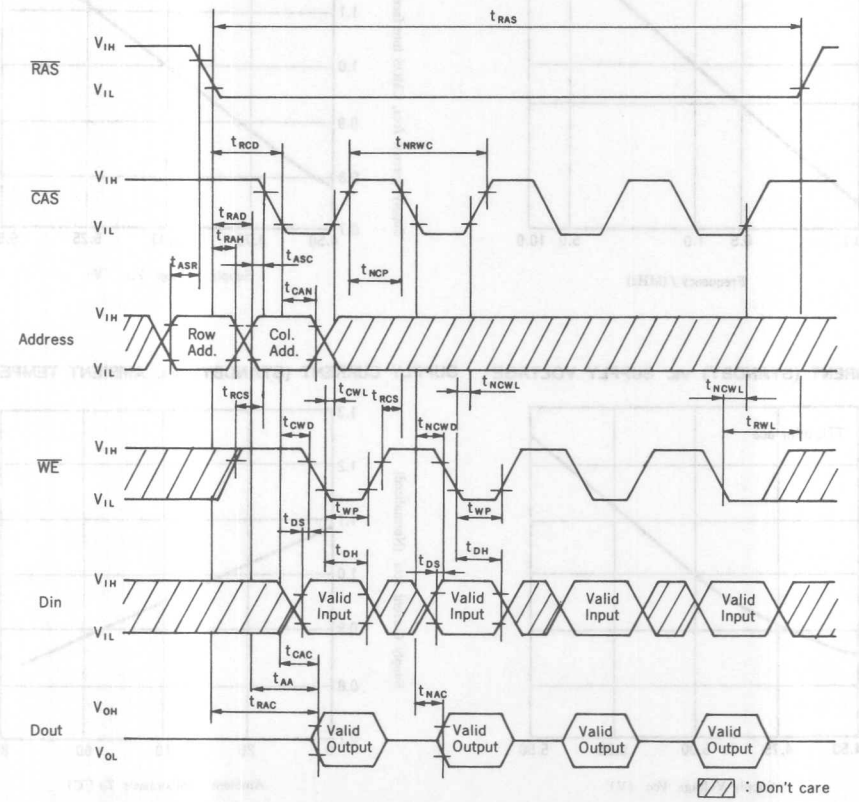


Nibble Mode Write Cycle

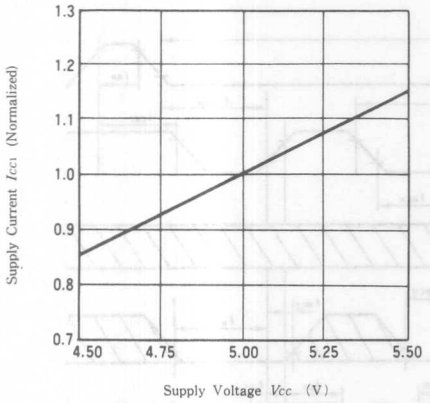


Notes: 1. ▨ : Don't care
2 $t_{WCS} \geq t_{WCS}$(min)

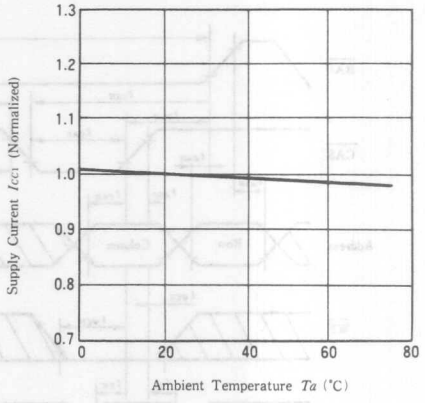
Nibble Mode Read-Modify-Write Cycle



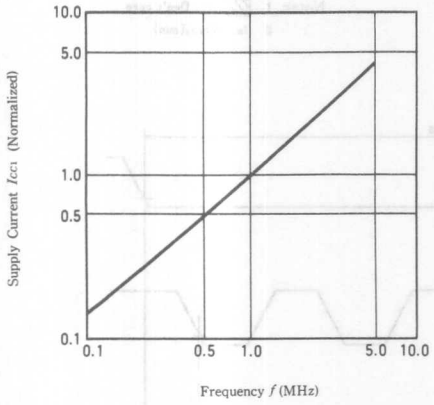
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



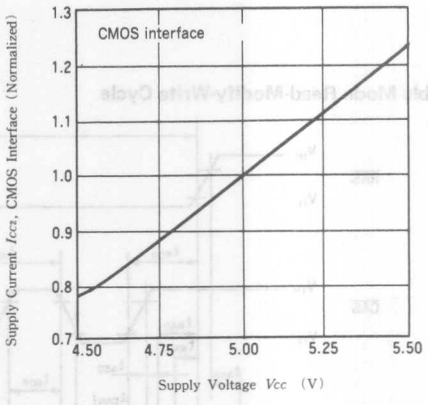
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



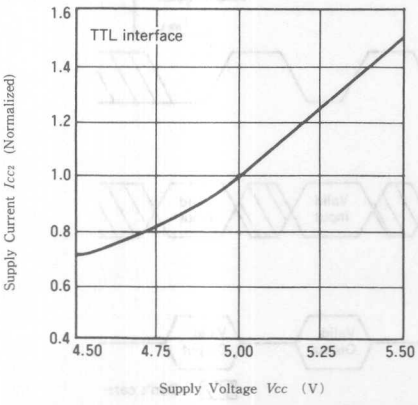
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



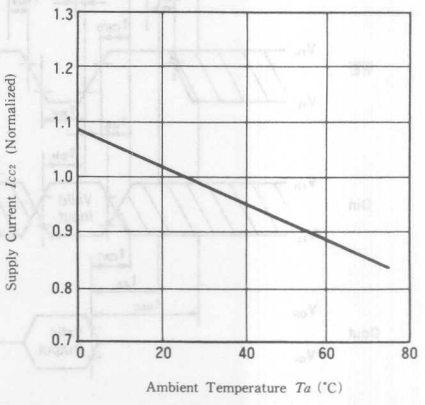
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



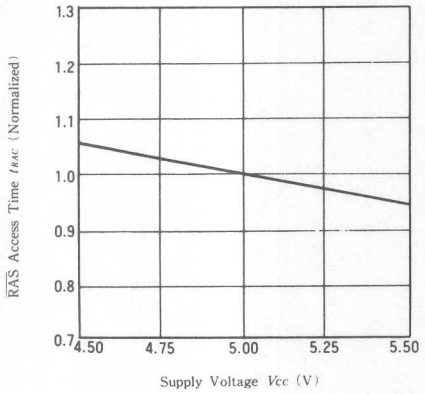
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



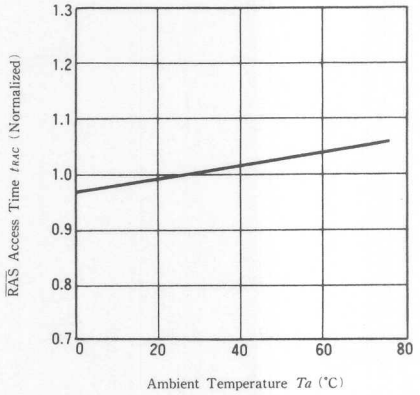
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



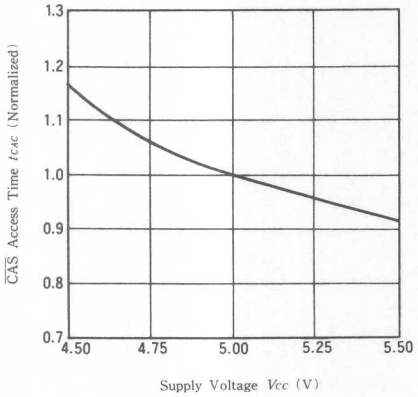
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



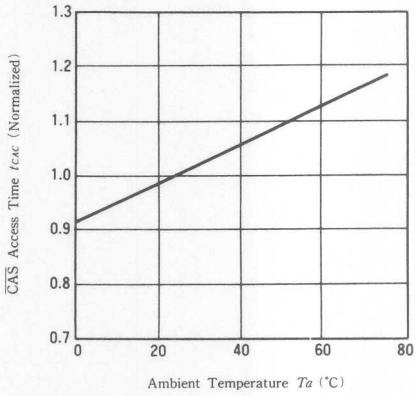
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



HM571000JP-35R/40/45

1,048,576-Word × 1-Bit (Bi CMOS) Memory

■ DESCRIPTION

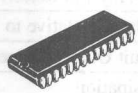
The Hitachi HM571000 is a super high speed dynamic RAM organized 1,048,576-word × 1-bit. HM571000 has realized higher density, higher performance and various functions by employing 1.3 μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM571000 offers 8 bits static column mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%) for HM571000JP-40/45
  5V (±5%) for HM571000JP-35R
- High Speed
  Access Time . . . . . .35/40/45ns (max.)
- 512 Refresh Cycles . . . . . .(4 ms)
- 2 Variations of Refresh
  $\overline{CE}$ Refresh
  Automatic Refresh
- 2 Bits Static Column Mode

■ ORDERING INFORMATION

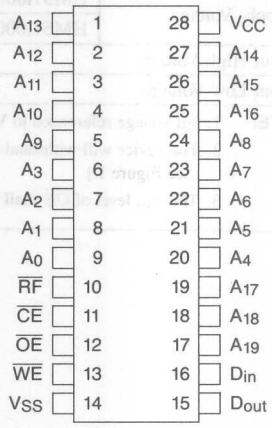
Part No.	Access	Package
HM571000JP-35R	35ns	300 mil 28 pin
HM571000JP-40	40ns	Plastic SOJ
HM571000JP-45	45ns	(CP-28DN)



(CP-28DN)

■ PIN ARRANGEMENT

HM571000JP-35R/40/45



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input for $\overline{CE}$ Refresh
A_9–A_{16}	Address Input
A_{17}–A_{19}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
D_{in}	Data-In
D_{out}	Data-Out
$\overline{RF}$	Refresh Control
V_{CC}	Power (+5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	HM571000JP-35R	V_{CC}	4.75	5.0	5.25	V	1
	HM571000JP-40/45		4.50		5.50		
Input High Voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input Low Voltage		V_{IL}	−1.0	—	0.8	V	1, 2

NOTE: 1. All voltage referenced to V_{SS}.

2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20ns at the −1.5V level. (See Figure 1.)

3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} + 0.5V.

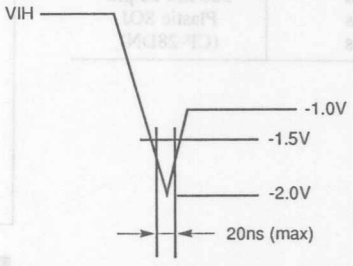


Figure 1. Undershoot of Input Voltage

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10% for HM571000JP-40/45, V_{CC} = 5V ± 5% for HM571000JP-35R)

Parameter	Symbol	Test Conditions	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Normal Operating Current	I_{CCA}		See Figure 2						mA	1
Refresh Current	I_{CCR}		See Figure 2						mA	1
Standby Current	I_{CCS}		—	5	—	5	—	5	mA	
Input Leakage Current	I_{LI}	0V < V_{in} < 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V < V_{out} < 7V D_{out} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{out} = −4mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{out} = 8mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

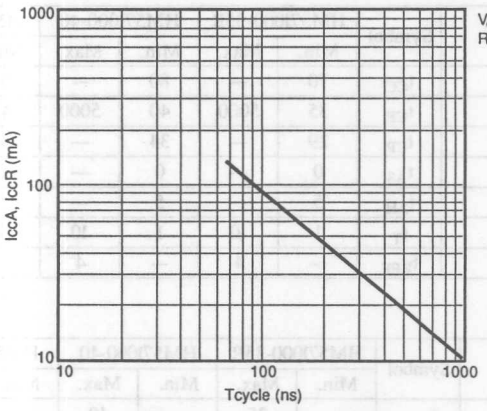


Figure 2. I_{CCA}, I_{CCR} vs. T_{cycle}

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10% for HM571000JP-40/45, V_{CC} = 5V ± 5% for HM571000JP-35R)

Parameter		Symbol	Typ.	Max.	Unit	Note
Input Capacitance	Address, Data-In	C_{in1}	—	5	pF	1
	Clock ($\overline{CE}$, $\overline{OE}$)	C_{in2}	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	C_{in3}	—	7	pF	1
Output Capacitance (Data-Out)		C_O	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10% for HM571000JP-40/45, V_{CC} = 5V ± 5% for HM571000JP-35R) (1)

• Test Conditions

- Input Pulse Levels: V_{IH} = 3.0V, V_{IL} = 0V
- Input Timing Reference Levels: High = 2.4V, Low = 0.8V (See Figure 3).
- Output Timing Reference Levels: High = 2.4V, Low = 0.4V
- Transition Time: t_T = 3ns
- Output Load: See Figure 4.

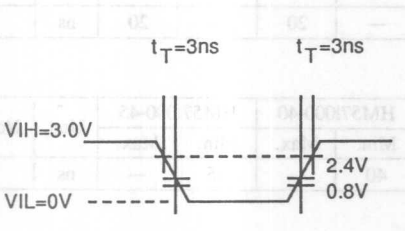


Figure 3. Input Pulse

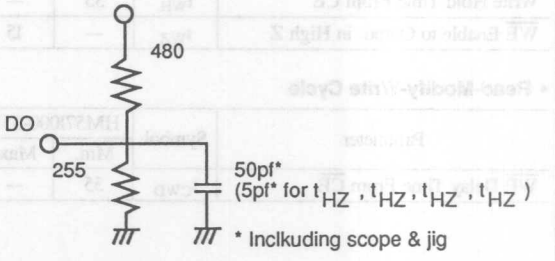


Figure 4. Output Load

*Including scope and jig.

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read/Write Cycle Time	t_{CC}	70	—	80	—	85	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ Precharge Time	t_{CP}	29	—	34	—	34	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	10	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

• Read Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time From $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time on Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time From Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time From $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

• Write Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time From $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Output in High Z	t_{WZ}	—	15	—	20	—	20	ns	

• Read-Modify-Write Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{WE}$ Delay Time From $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

• Refresh Cycle

Parameter	Symbol	HM571000-35R		HM574100-40		HM574100-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

• Static Column Mode Cycle

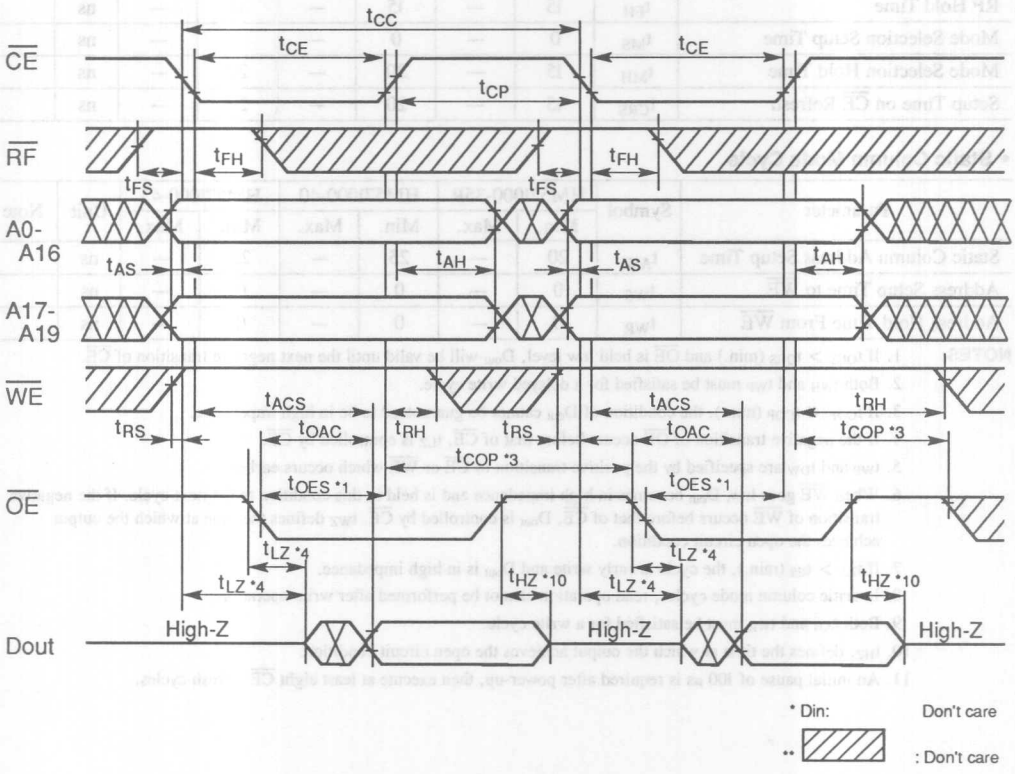
Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time From $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

NOTES:

1. If $t_{OES} > t_{OES}$ (min.) and $\overline{OE}$ is held low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min.), the condition of D_{out} cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ which occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes in high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min.), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.
10. t_{HZ}, defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.

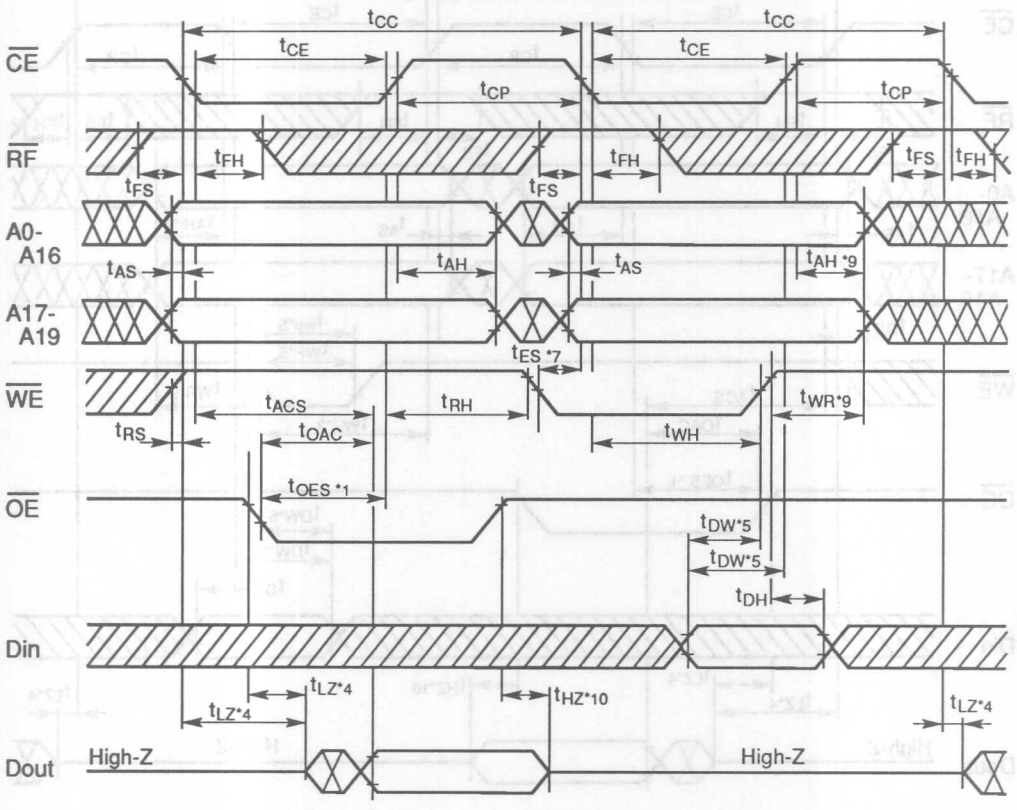
■ TIMING WAVEFORMS

• Read/Read Cycle

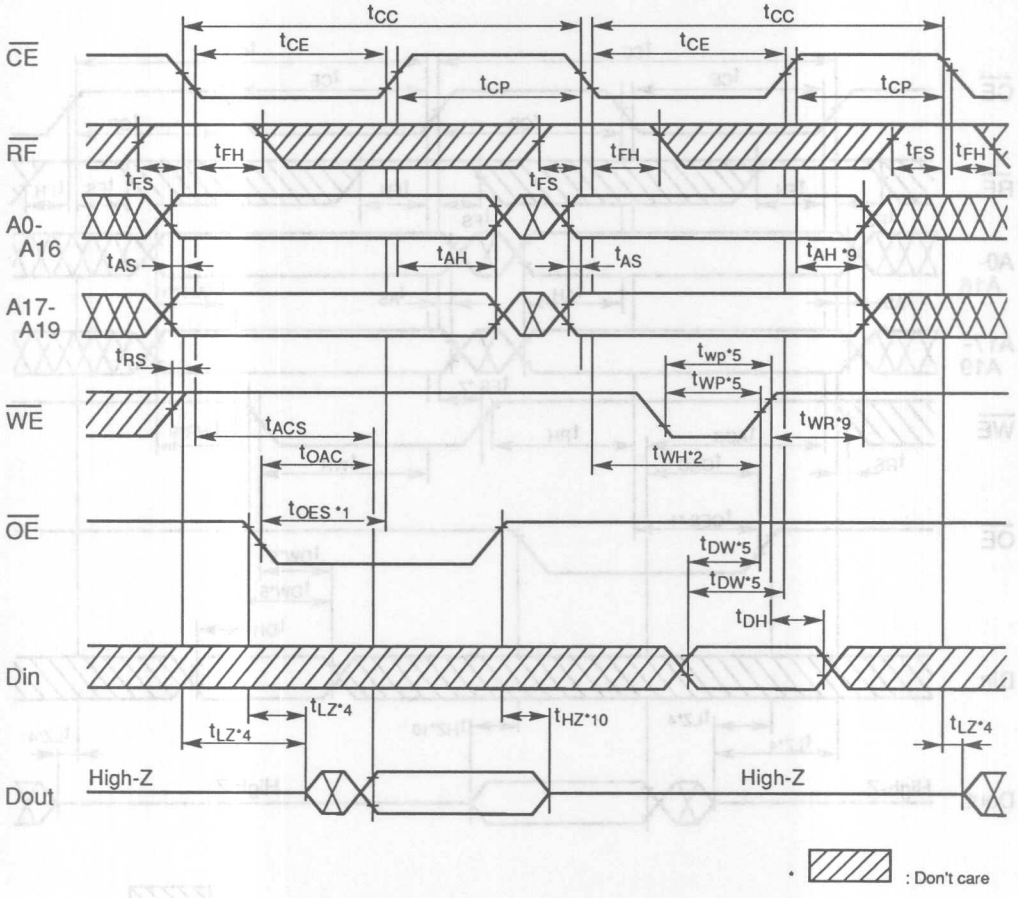


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• **Read/Early Write Cycle**

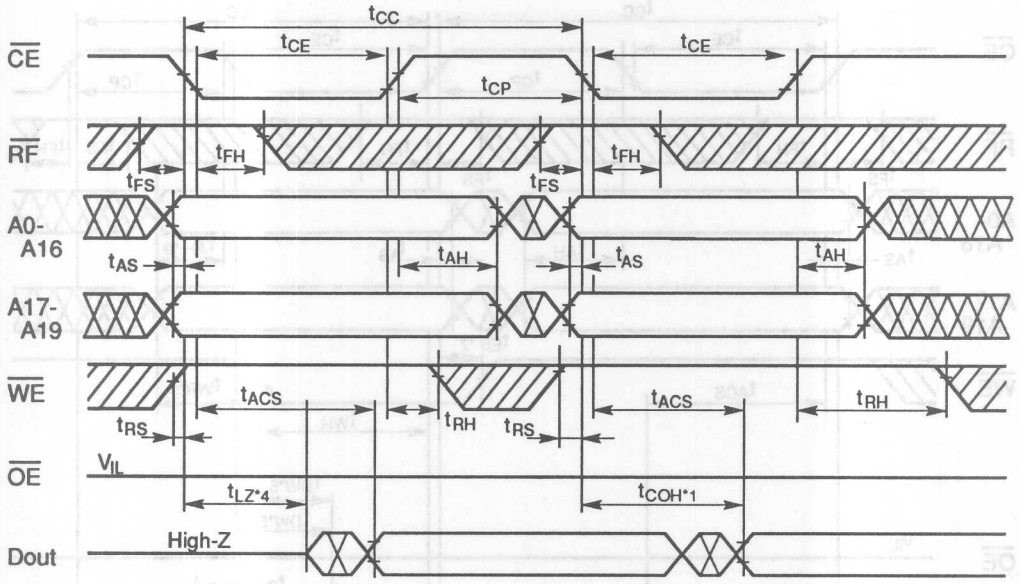


• **Read/Delayed Write Cycle**



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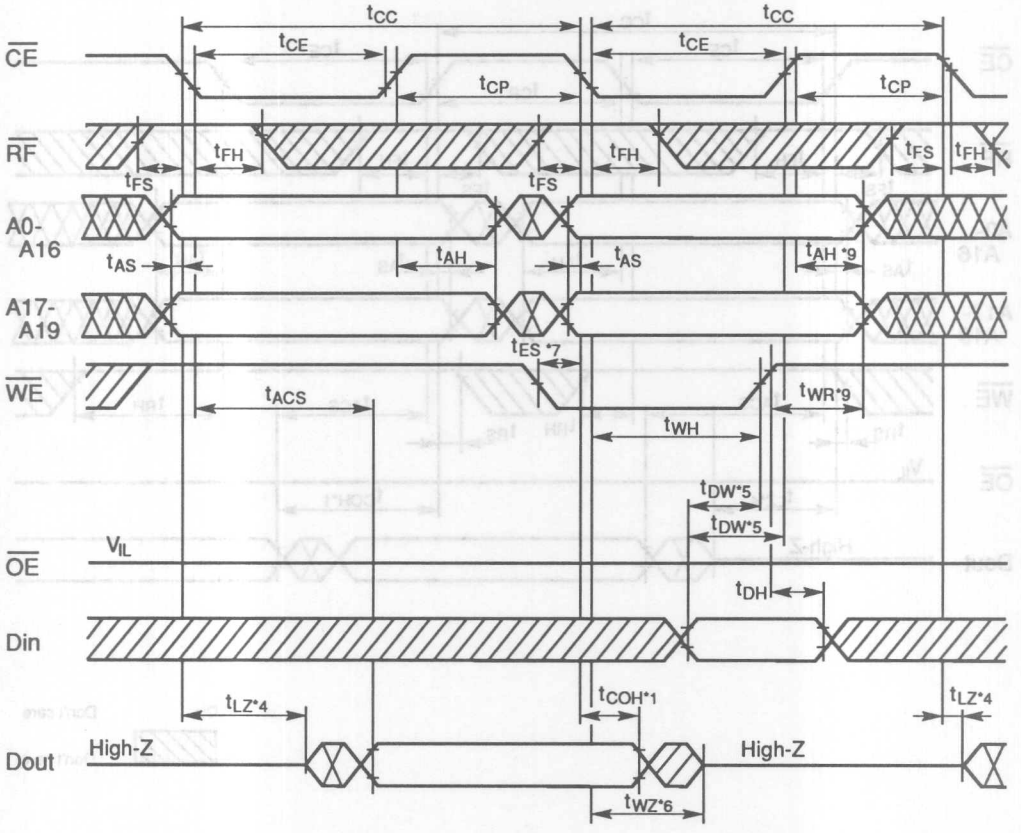
• **Read/Read Cycle** ($\overline{OE}$ = V_{IL})



* Din: Don't care

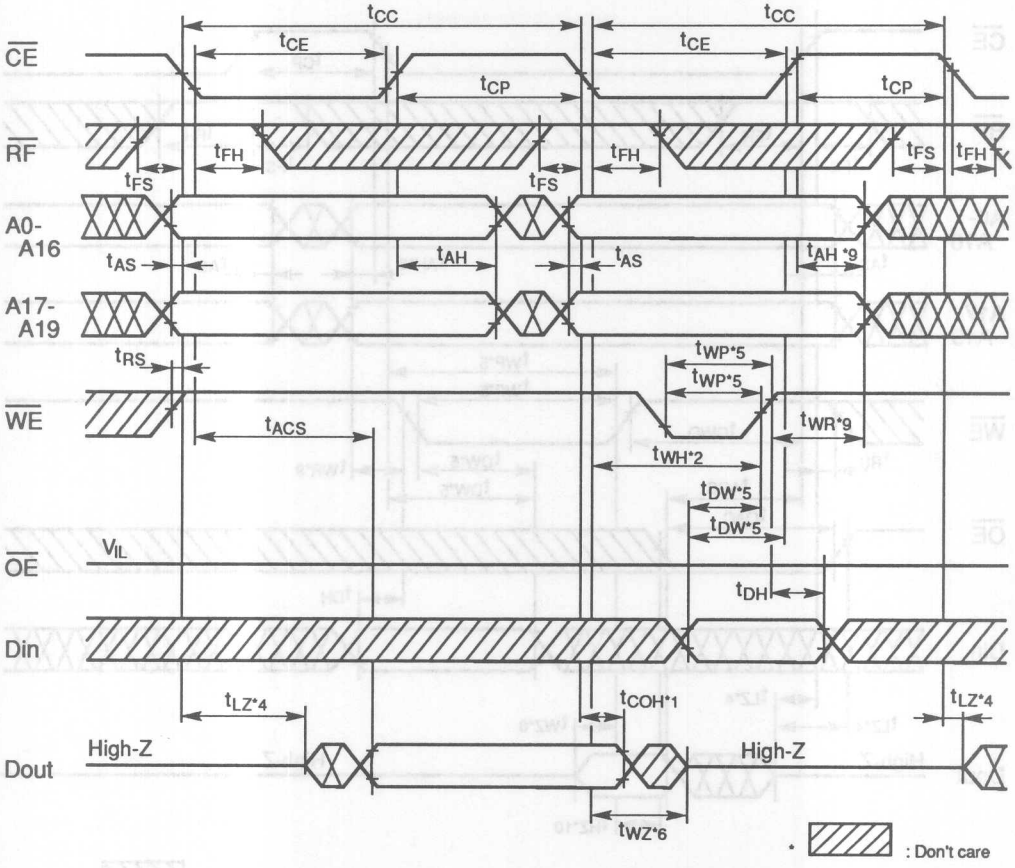
** : Don't care

• **Read/Early Write Cycle** ($\overline{OE}$ = V_{IL})

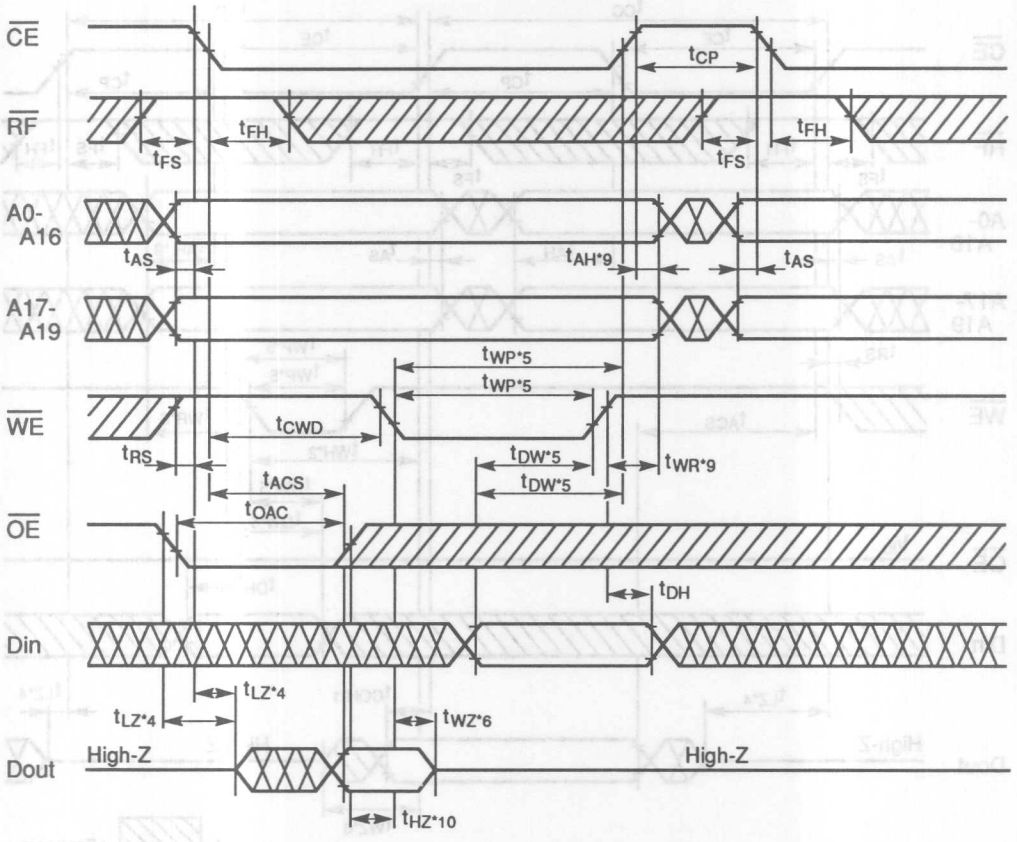


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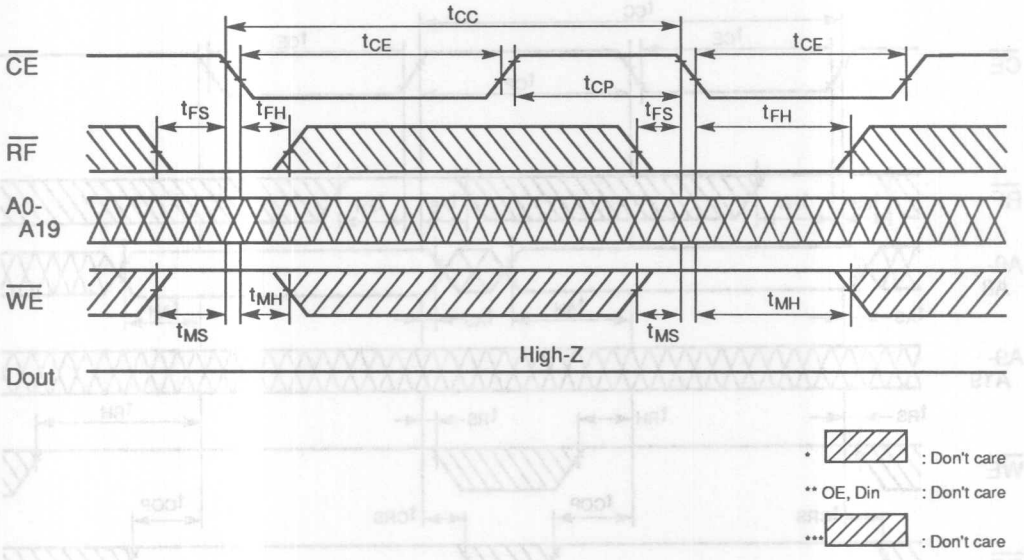
• **Read/Delayed Write Cycle** ($\overline{OE}$ = V_{IL})



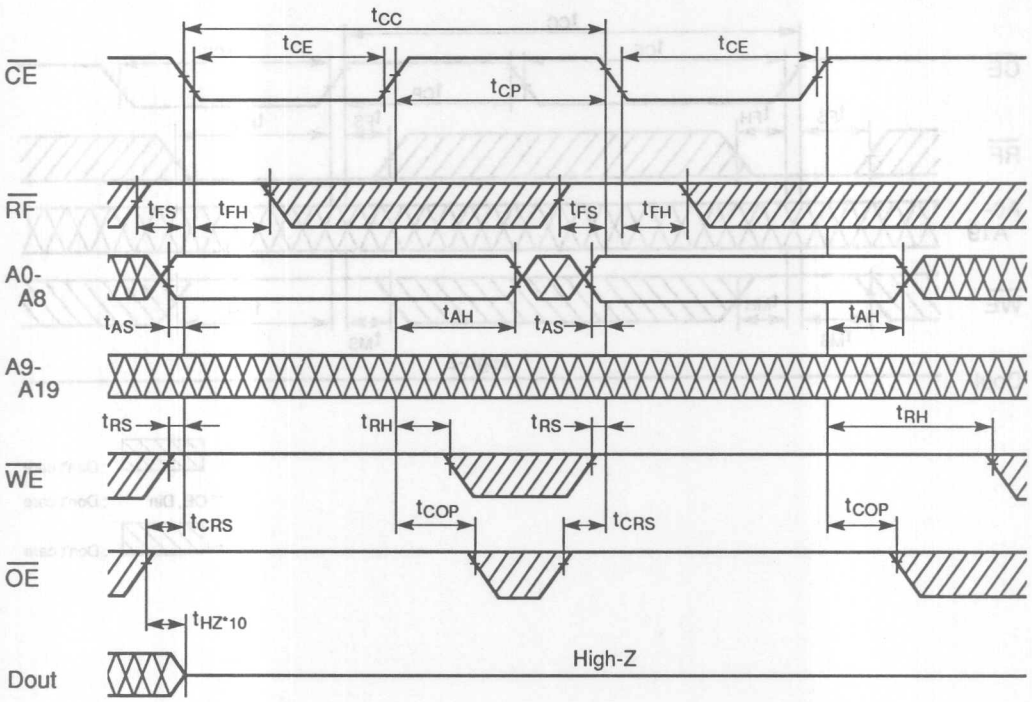
• **Read-Modify-Write Cycle**



• **Automatic Refresh Cycle**



• $\overline{CE}$ Refresh

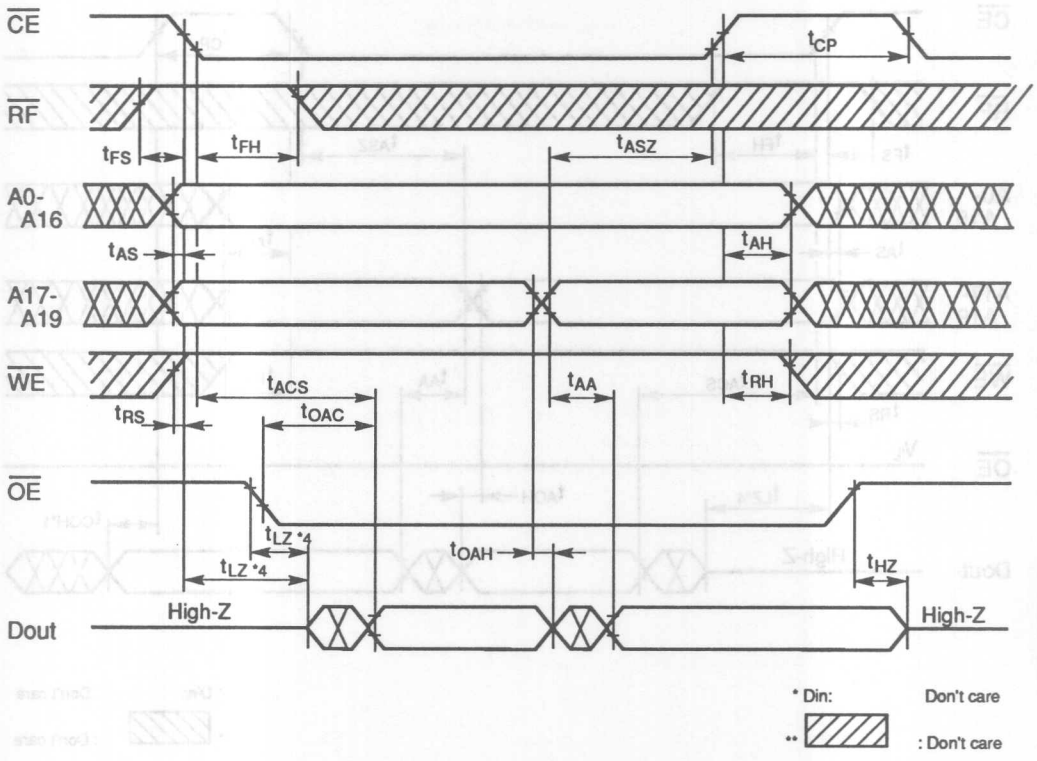


*Din : Don't care

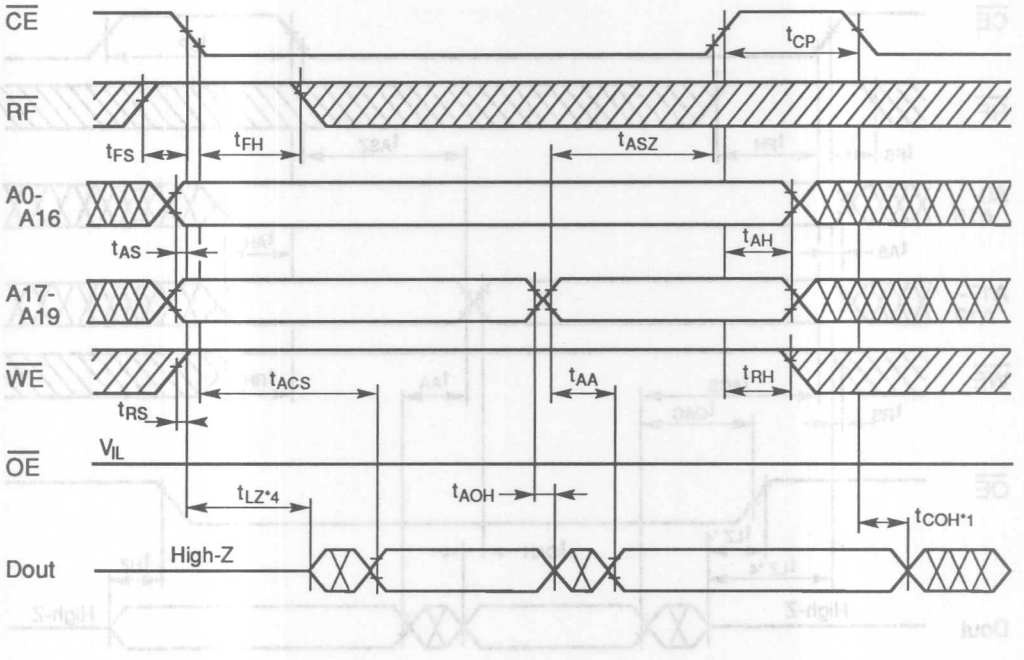
** : Don't care

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• **Static Column Mode Read Cycle**



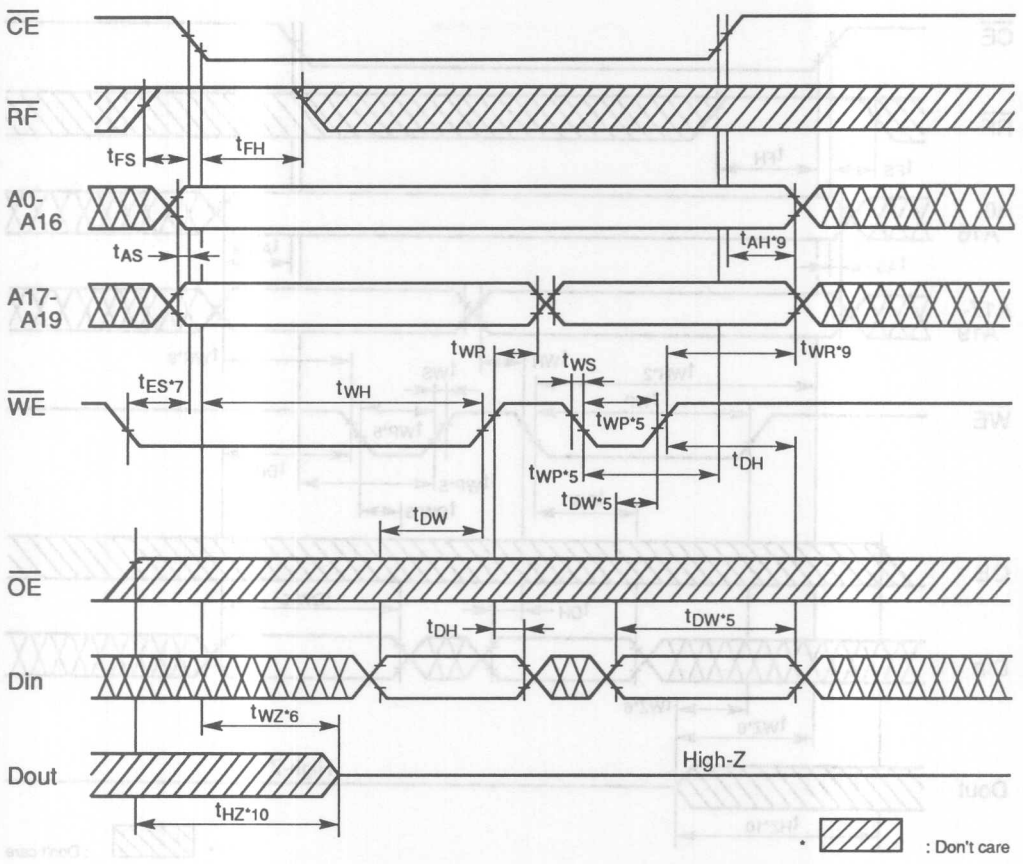
• **Static Column Mode Read Cycle** ($\overline{OE}$ = V_{IL})



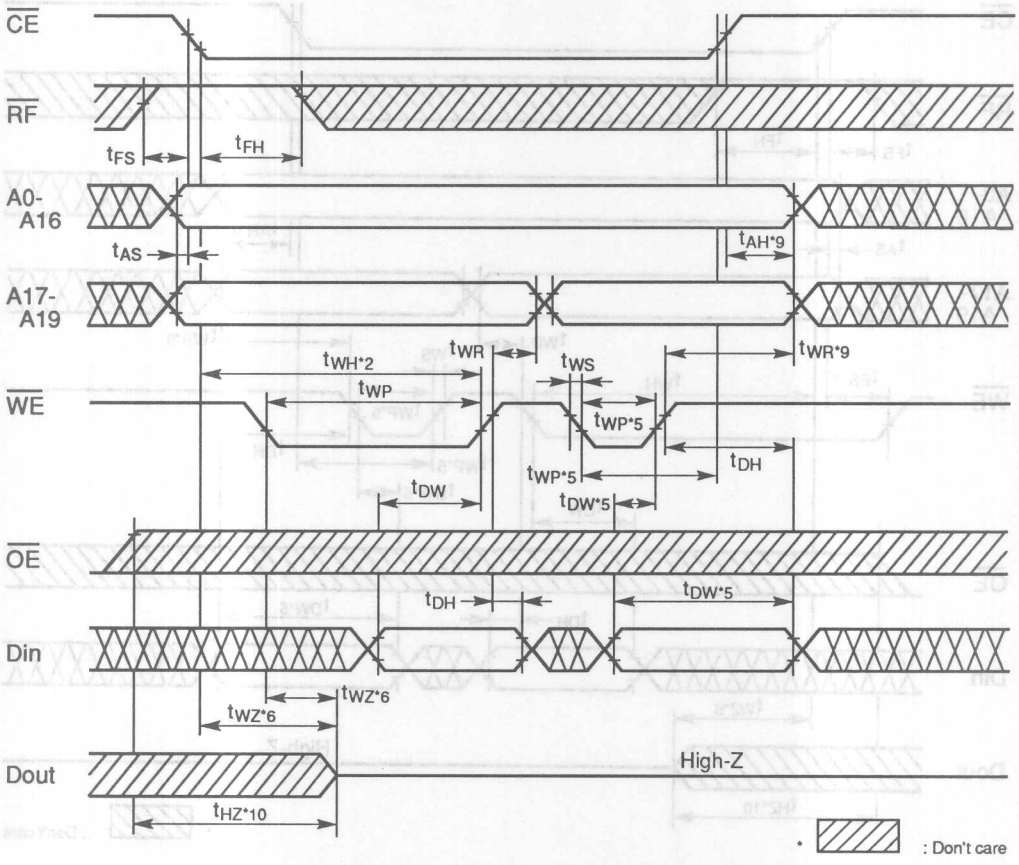
* Din: Don't care

** : Don't care

• **Static Column Mode Write Cycle** (1st Cycle = Early Write Cycle) [8]



• **Static Column Mode Write Cycle** (1st Cycle = Delayed Write Cycle) (8)



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HM574256JP-35R/40/45 — Preliminary

262,144-Word × 4-Bit (Bi CMOS)

■ DESCRIPTION

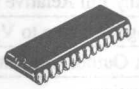
The Hitachi HM574256 is a super high speed dynamic RAM organized 262,144-word × 4-bit. HM574256 has realized higher density, higher performance and various functions by employing 1.3μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM574256 offers 2 bit static column mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%) for HM574256JP-40/45
  5V (±5%) for HM574256JP-35R
- High Speed
  Access Time . . . . . .35/40/45ns (max.)
- 512 Refresh Cycles . . . . . .(4 ms)
- 2 Variations of Refresh
  $\overline{CE}$ Refresh
  Automatic Refresh
- 2 Bits Static Column Mode

■ ORDERING INFORMATION

Part No.	Access	Package
HM574256JP-35R	35ns	300 mil 28 pin
HM574256JP-40	40ns	Plastic SOJ
HM574256JP-45	45ns	(CP-28DN)



(CP-28DN)

■ PIN ARRANGEMENT

HM574256JP-35R/40/45



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input for $\overline{CE}$ Refresh
A_9–A_{16}	Address Input
A_{17}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
I/O_1–I/O_4	Data-In/Data-Out
$\overline{RF}$	Refresh Control
V_{CC}	Power (+5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	HM574256JP-35R	V_{CC}	4.75	5.0	5.25	V	1
	HM574256JP-40/45		4.50		5.50		
Input High Voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input Low Voltage		V_{IL}	−1.0	—	0.8	V	1, 2

NOTE: 1. All voltage referenced to V_{SS}.

2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20ns at the −1.5V level. (See Figure 1.)

3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} + 0.5V.

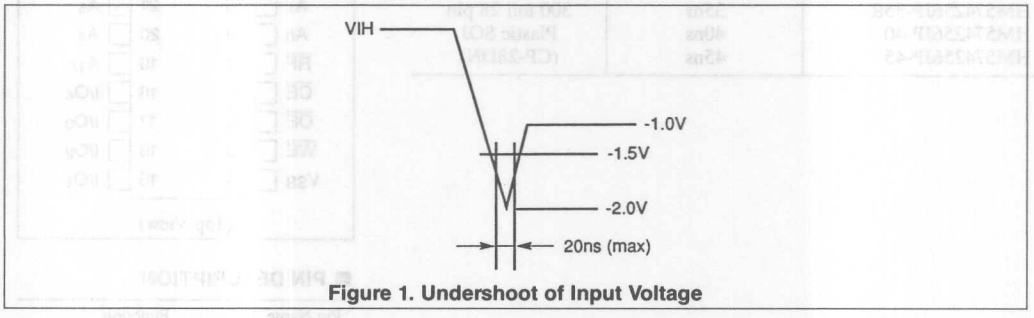


Figure 1. Undershoot of Input Voltage

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10% for HM574256JP-40/45, V_{CC} = 5V ± 5% for HM574256JP-35R)

Parameter	Symbol	Test Conditions	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Normal Operating Current	I_{CCA}		—	TBD	—	TBD	—	TBD	mA	1
Refresh Current	I_{CCR}		—	TBD	—	TBD	—	TBD	mA	1
Standby Current	I_{CCS}		—	5	—	5	—	5	mA	
Input Leakage Current	I_{LI}	0V ≤ V_{in} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{out} = −4mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{out} = 8mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%) for HM574256JP-40/45, V_{CC} = 5V ± 5% for HM574256JP-35R)

Parameter		Symbol	Typ.	Max.	Unit	Note
Input Capacitance	Address, Data-In	C_{in1}	—	5	pF	1
	Clock ($\overline{CE}$, $\overline{OE}$)	C_{in2}	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	C_{in3}	—	7	pF	1
Output Capacitance (Data-In/Data-Out)		$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10% for HM574256JP-40/45, V_{CC} = 5V ± 5% for HM574256JP-35R) (1)

• Test Conditions

- Input Pulse Levels: V_{IH} = 3.0V, V_{IL} = 0V
- Input Timing Reference Levels: High = 2.4V, Low = 0.8V (See Figure 2).
- Output Timing Reference Levels: High = 2.4V, Low = 0.4V
- Transition Time: t_T = 3ns
- Output Load: See Figure 3.

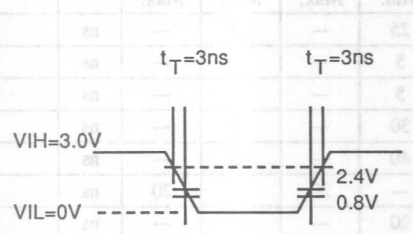


Figure 2. Input Pulse

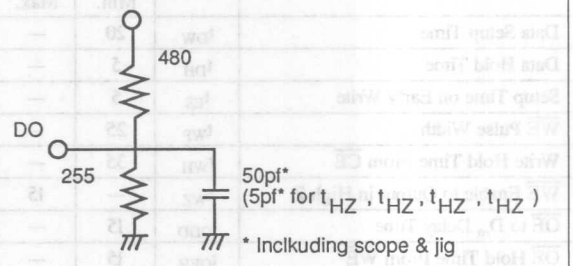


Figure 3. Output Load

*Including scope and jig.

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read/Write Cycle Time	t_{CC}	70	—	80	—	85	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ Precharge Time	t_{CP}	29	—	34	—	34	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

• Read Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time From $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time on Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time From Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time From $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

• Write Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time From $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Output in High Z	t_{WZ}	—	15	—	20	—	20	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	ns	
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
$\overline{CE}$ Setup Time From D_{in}	t_{DZC}	0	—	0	—	0	—	ns	

• Read-Modify-Write Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{WE}$ Delay Time From $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

• Refresh Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

• Static Column Mode Cycle

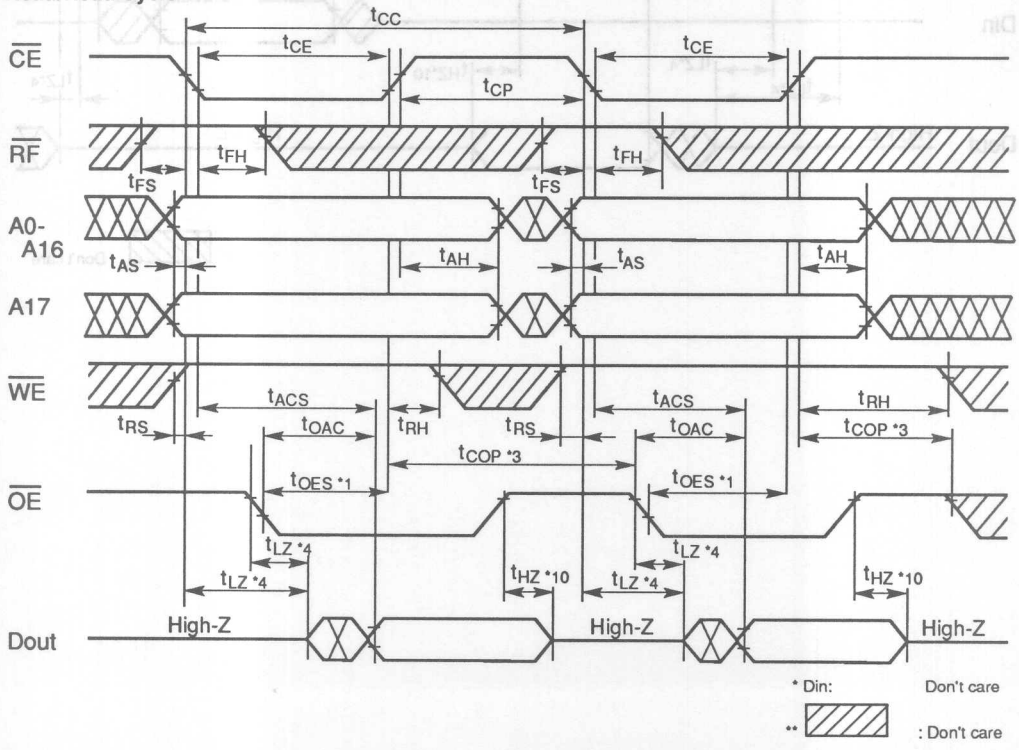
Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time From $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

NOTES:

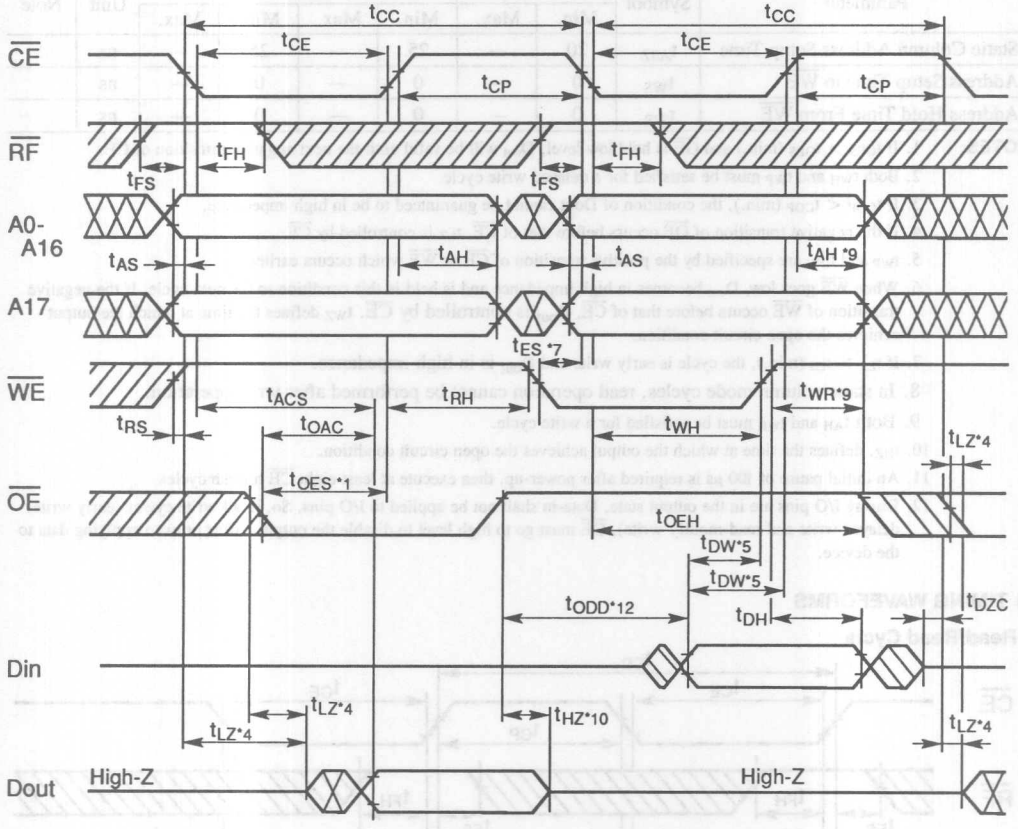
1. If $t_{OES} > t_{OES}$ (min.) and $\overline{OE}$ is held low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min.), the condition of Dout cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ which occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes in high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min.), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.
10. t_{HZ}, defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. During I/O pins are in the output state, Data-in shall not be applied to I/O pins. So, in all write cycles (early write, delayed write and read-modify-write), $\overline{OE}$ must go to high level to disable the output buffer prior to applying data to the device.

■ TIMING WAVEFORMS

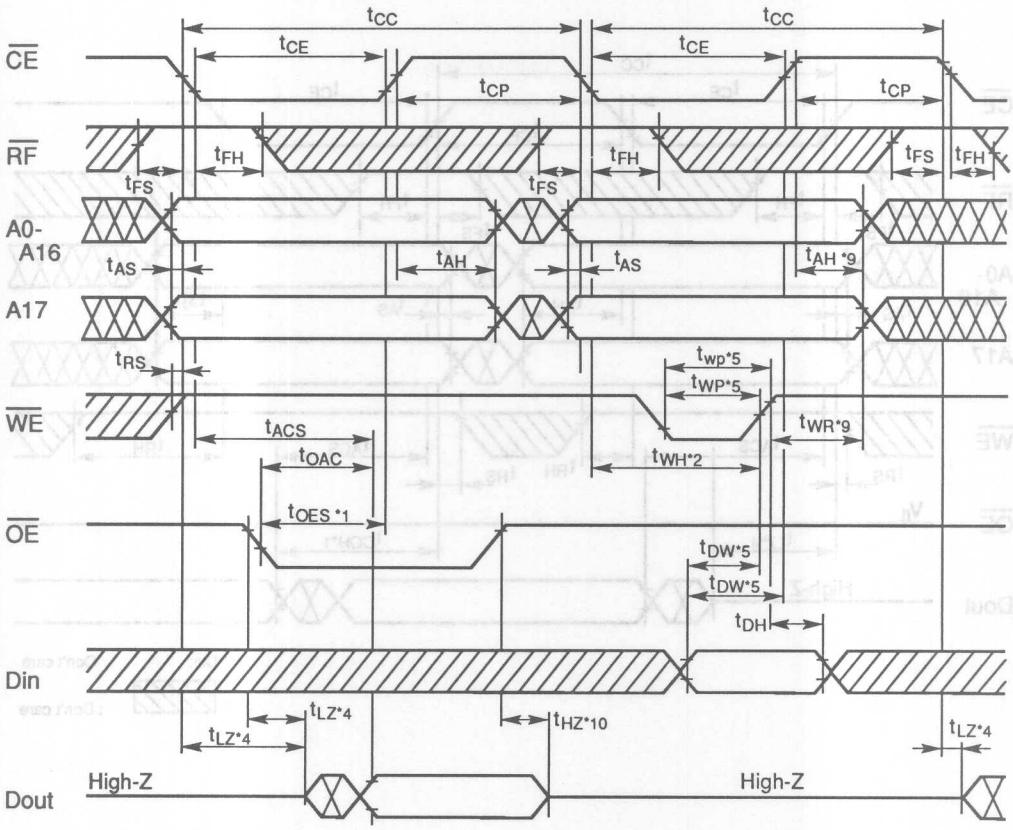
• Read/Read Cycle



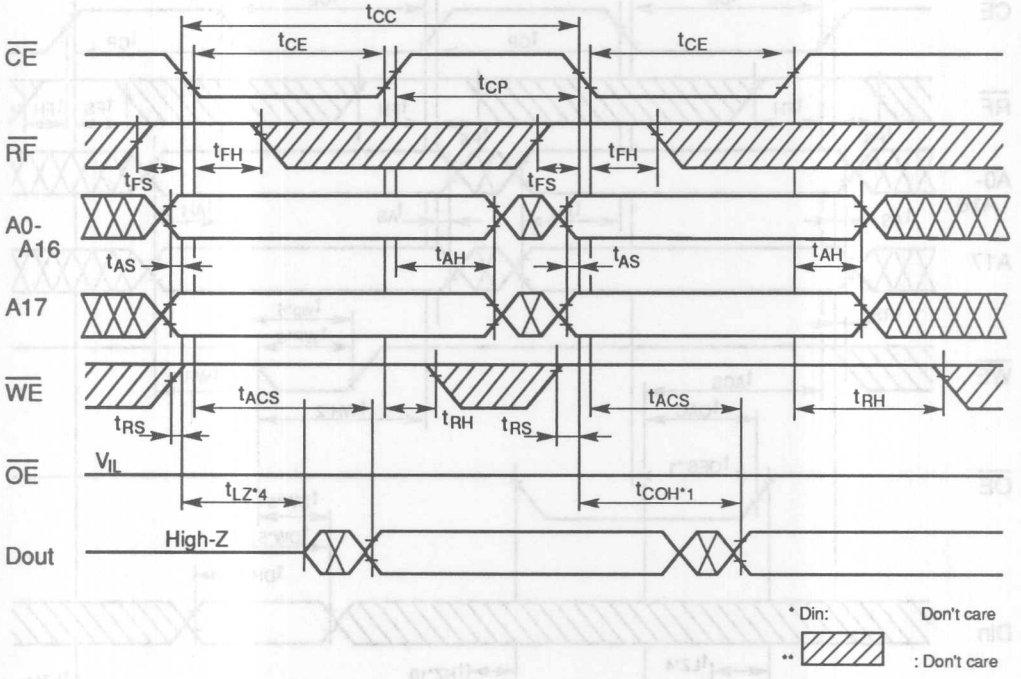
• **Read/Early Write Cycle**



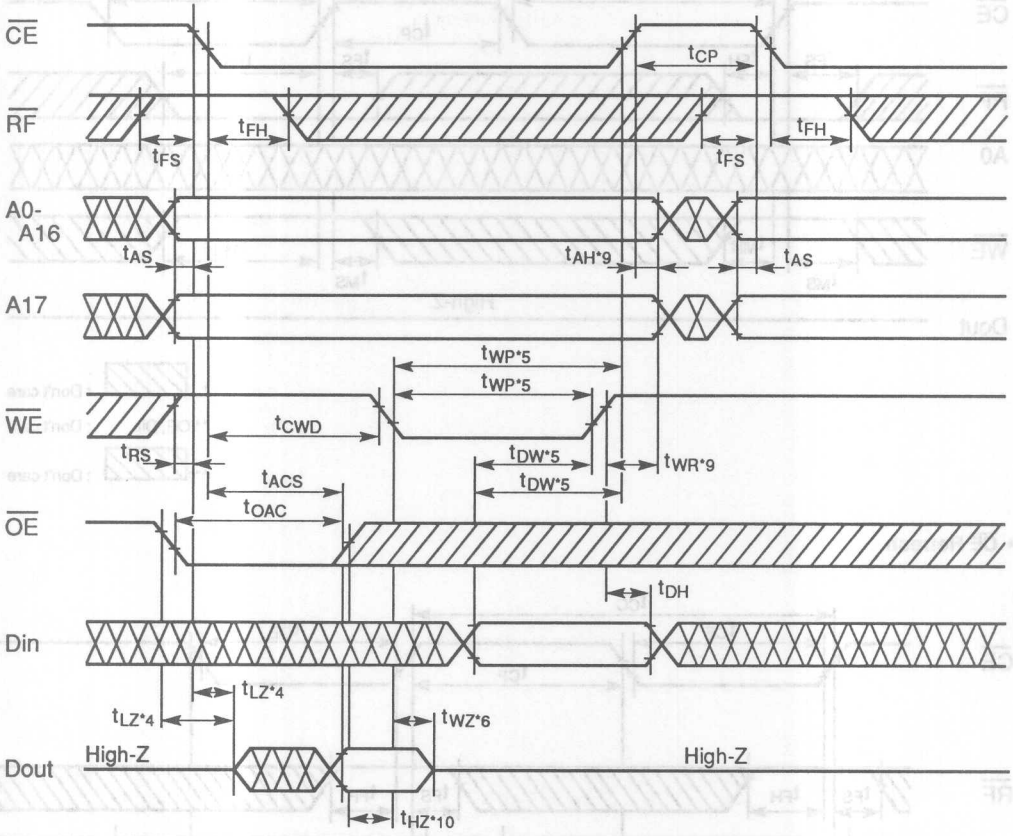
• **Read/Delayed Write Cycle**



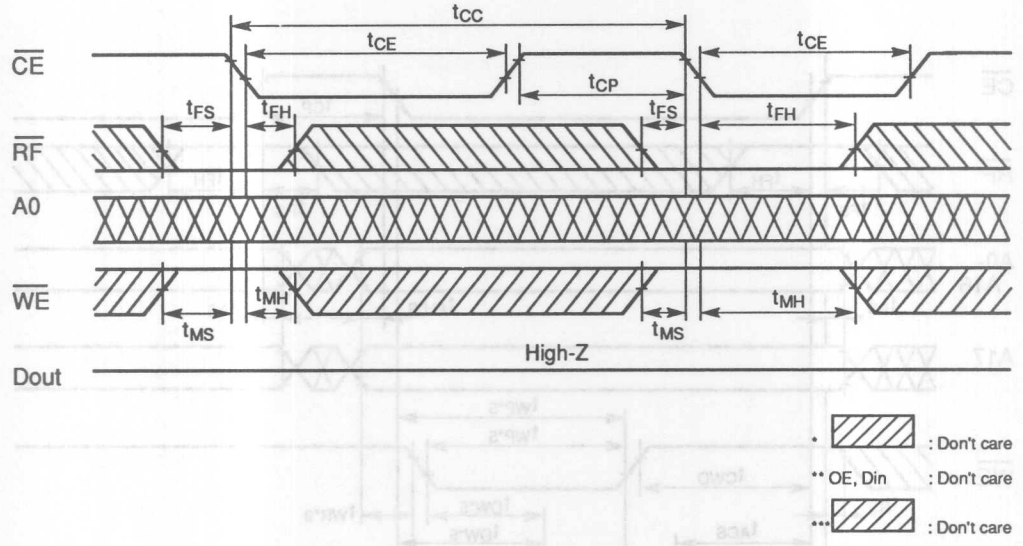
• **Read/Read Cycle** ($\overline{OE}$ = V_{IL})



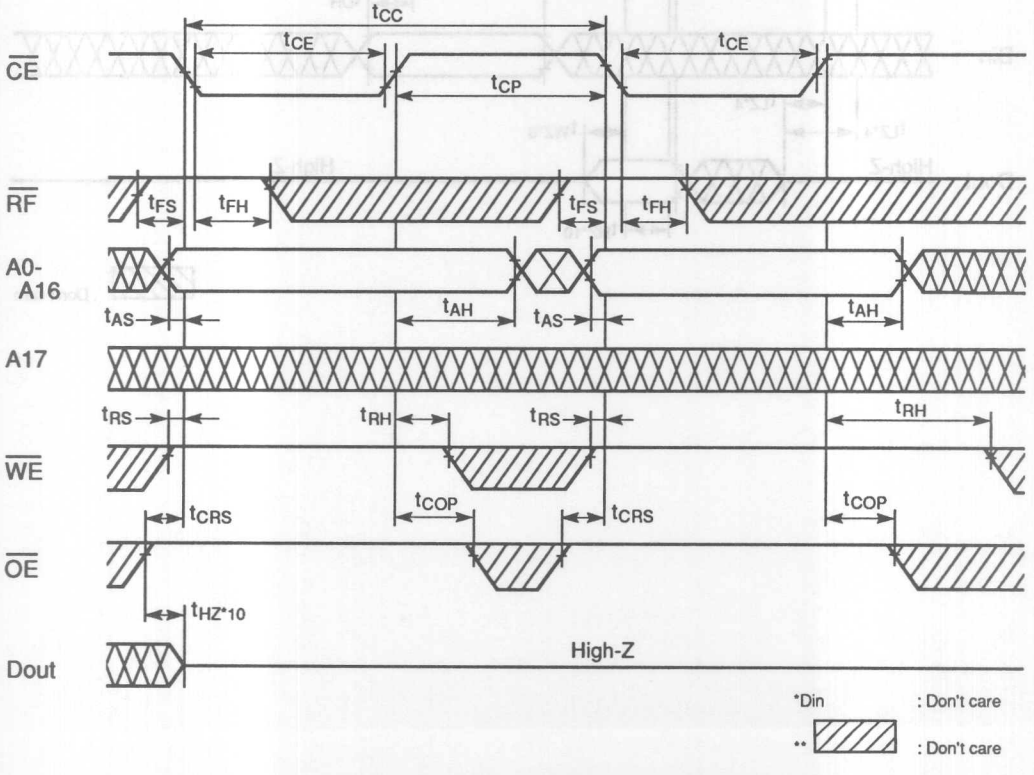
• **Read-Modify-Write Cycle**



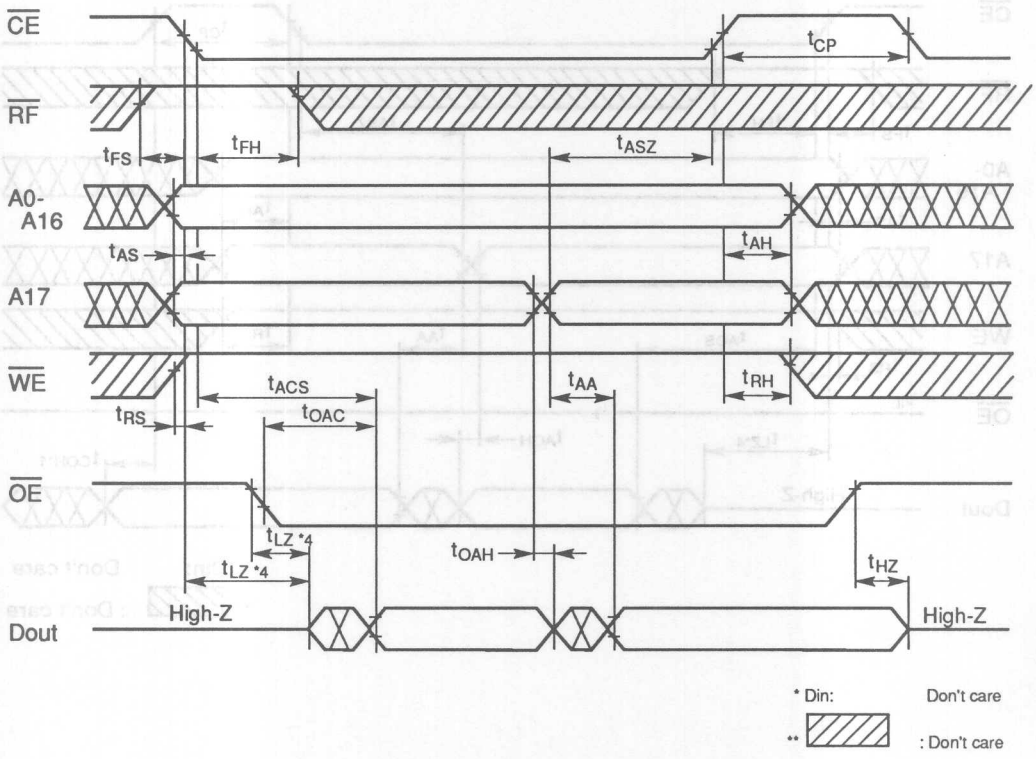
• **Automatic Refresh Cycle**



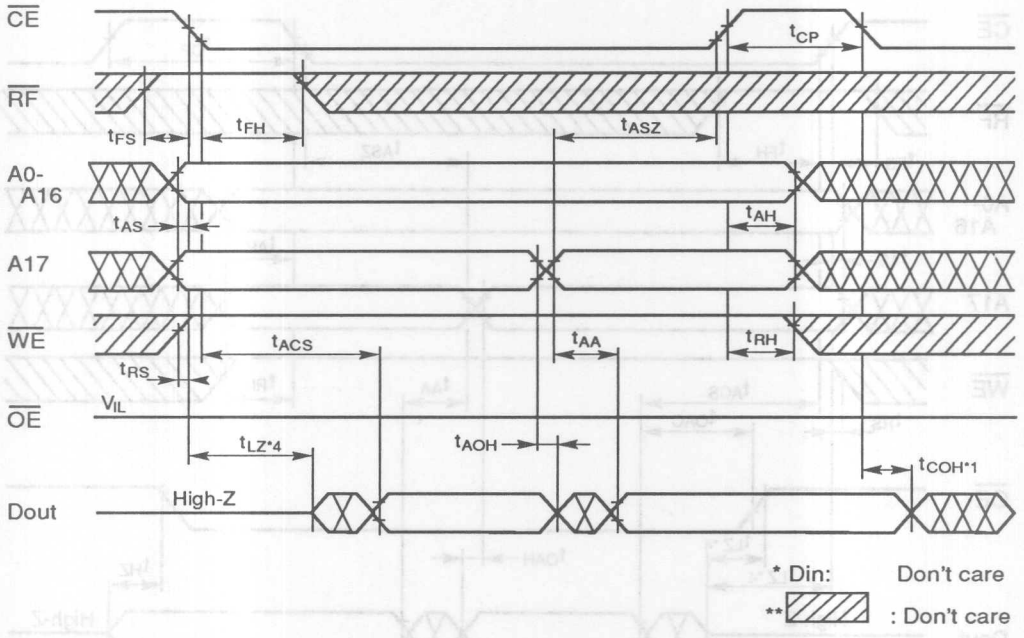
• **$\overline{CE}$ Refresh**



• **Static Column Mode Read Cycle**

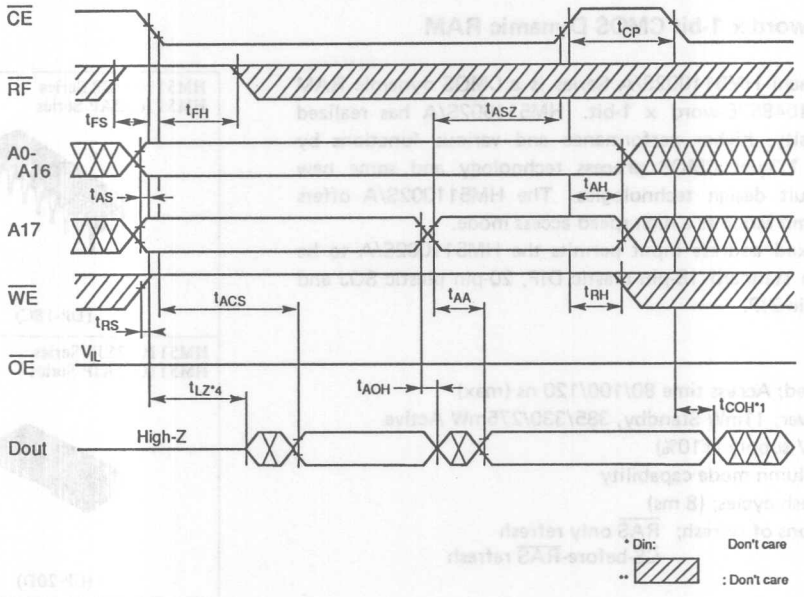


• **Static Column Mode Read Cycle** ($\overline{OE}$ = V_{IL})

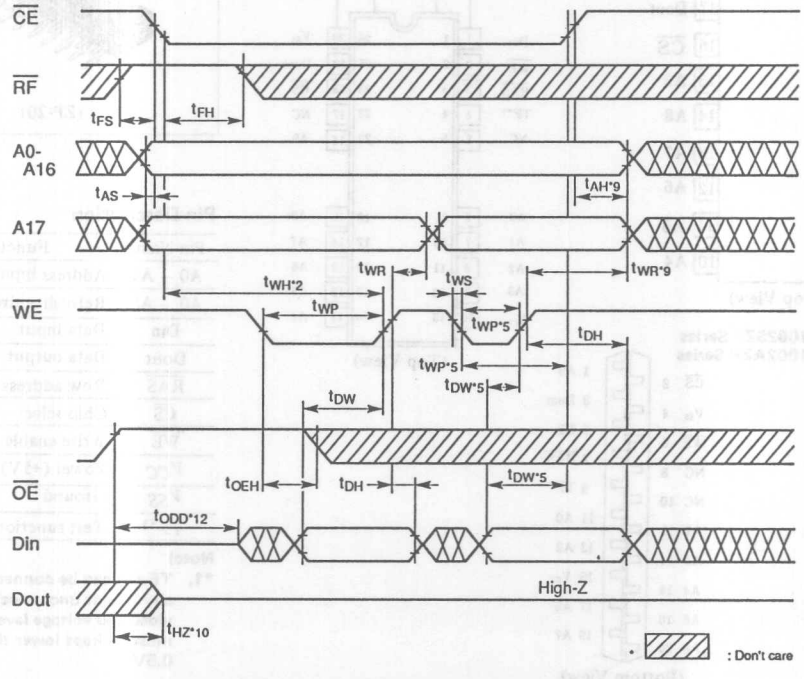


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• **Static Column Mode Write Cycle** (1st Cycle = Early Write Cycle) (8)



• **Static Column Mode Write Cycle** (1st Cycle = Delayed Write Cycle) (8)



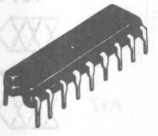
HM511002S Series
HM511002A Series

1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511002S/A Series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511002S/A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM511002S/A offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM511002S/A to be packaged in standard 18-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM511002SP Series
HM511002AP Series



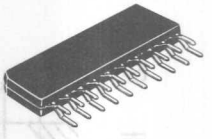
(DP-18C)

HM511002SJP Series
HM511002AJP Series



(CP-20D)

HM511002SZP Series
HM511002AZP Series



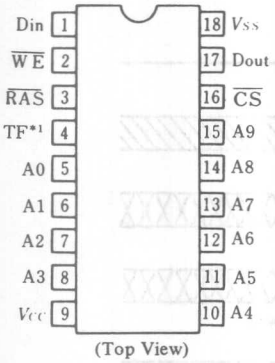
(ZP-20)

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11mW Standby, 385/330/275mW Active
- Single 5V supply (±10%)
- Static column mode capability
- 512 refresh cycles; (8 ms)
- 2 variations of refresh; $\overline{RAS}$ only refresh
  $\overline{CS}$-before-$\overline{RAS}$ refresh

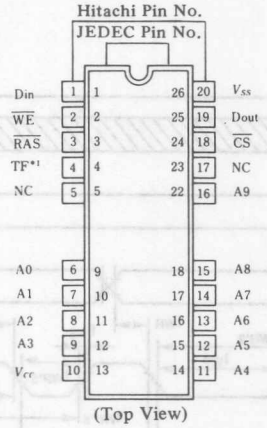
Pin Arrangement

• **HM511002SP Series**
HM511002AP Series



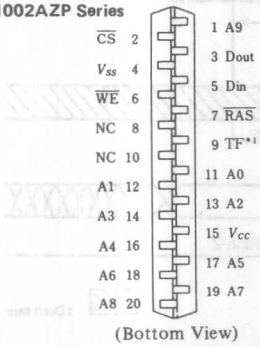
(Top View)

• **HM511002SJP Series**
HM511002AJP Series



(Top View)

• **HM511002SZP Series**
HM511002AZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power (+5V)
V_{SS}	Ground
TF*1	Test function

Note)

***1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.**

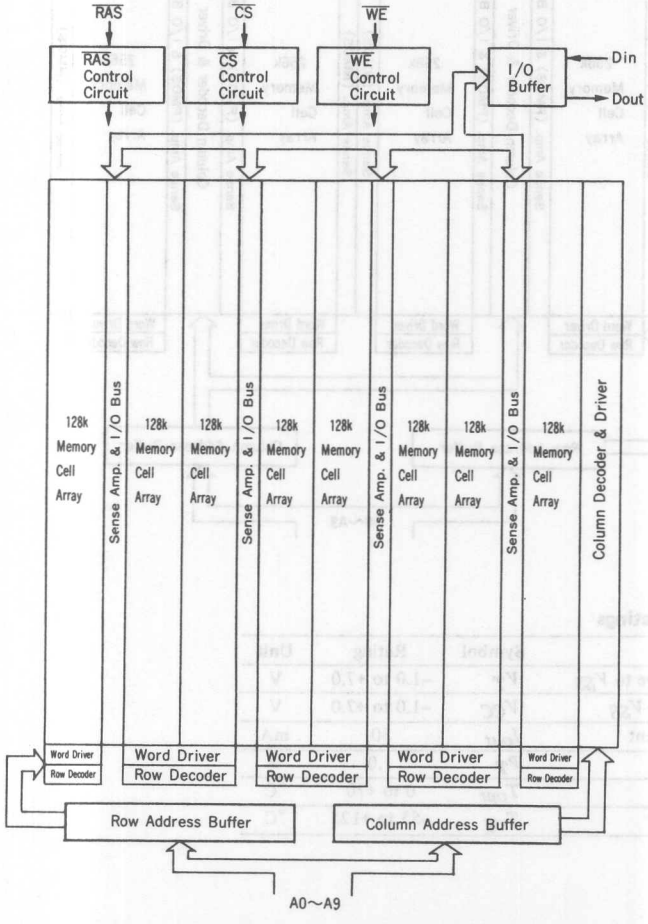
Ordering Information

Type No.	Access Time	Package
HM511002P-8S	80ns	300 mil 18-pin Plastic DIP
HM511002P-10S	100ns	
HM511002P-12S	120ns	
HM511002JP-8S	80ns	300 mil 20-pin Plastic SOJ
HM511002JP-10S	100ns	
HM511002JP-12S	120ns	
HM511002ZP-8S	80ns	400 mil 20-pin Plastic ZIP
HM511002ZP-10S	100ns	
HM511002ZP-12S	120ns	

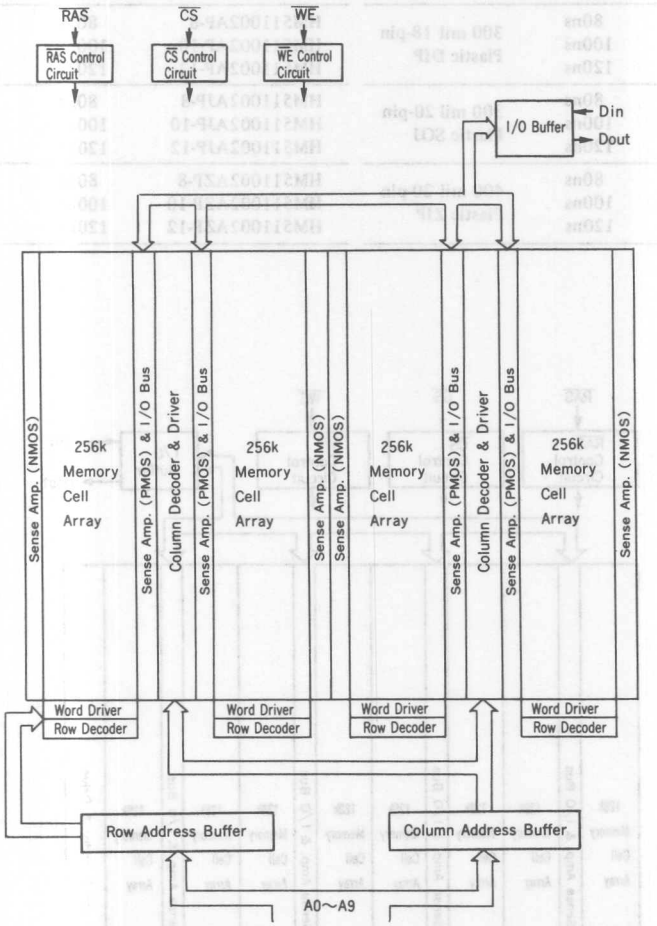
Type No.	Access Time	Package
HM511002AP-8	80ns	300 mil 18-pin Plastic DIP
HM511002AP-10	100ns	
HM511002AP-12	120ns	
HM511002AJP-8	80ns	300 mil 20-pin Plastic SOJ
HM511002AJP-10	100ns	
HM511002AJP-12	120ns	
HM511002AZP-8	80ns	400 mil 20-pin Plastic ZIP
HM511002AZP-10	100ns	
HM511002AZP-12	120ns	

Block Diagram

HM511002S Series



HM511002A Series



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Test condition	Note
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = Min	*1,*2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$, $\overline{CS} \geq V_{CC}$–0.2V Dout = High-Z CMOS interface	
Refresh current	I_{CC3}	–	60	–	50	–	45	mA	$\overline{RAS}$-only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, Dout = enable	*1
Refresh current	I_{CC6}	–	60	–	50	–	40	mA	$\overline{CS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min.	
Static column mode current	I_{CC9}	–	60	–	50	–	40	mA	t_{SC} = Min	*3
Input leakage	I_{LI}	–10	10	–10	10	–10	10	µA	V_{IN} = 0 to +7V	
Output leakage	I_{LO}	–10	10	–10	10	–10	10	µA	V_{OUT} = 0 to +7V, Dout = disable	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2mA	

Note) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[*1,*17]

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ pulse width	t_{SP}	25	10000	30	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address setup time	t_{ASW}	0	–	0	–	0	–	ns	
Column address hold time	t_{AHW}	20	–	25	–	25	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	55	25	70	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSL}	25	–	30	–	30	–	ns	
$\overline{CS}$ hold time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	10	–	10	–	10	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	*7
Refresh period	t_{REF}	–	8	–	8	–	8	ms	

Read Cycle

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	*2,*3
Access time from $\overline{CS}$	t_{ACS}	–	25	–	30	–	30	ns	*3,*4
Access time from address	t_{AA}	–	40	–	50	–	55	ns	*3,*5,*14
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	55	–	ns	
$\overline{RAS}$ to column address hold time	t_{AHR}	15	–	15	–	15	–	ns	*16
Output hold time from address	t_{AOH}	5	–	5	–	5	–	ns	
Output buffer turn-off time	t_{OFF}	–	20	–	25	–	30	ns	*6
Column address hold time to $\overline{RAS}$ on read	t_{AR}	80	–	100	–	120	–	ns	

Write Cycle

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	*10
Write command hold time	t_{WCH}	20	–	25	–	25	–	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	75	–	95	–	115	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	25	–	30	–	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	*11
Data-in hold time	t_{DH}	20	–	25	–	25	–	ns	*11
Data-in hold time to $\overline{RAS}$	t_{DHR}	75	–	95	–	115	–	ns	
Column address hold time or $\overline{RAS}$ on write	t_{AWR}	75	–	95	–	115	–	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM51100A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	190	–	220	–	255	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	100	–	120	–	ns	*10
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	25	–	30	–	30	–	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	50	–	55	–	ns	*10
Output hold time from $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	ns	

Refresh Cycle

Parameter	Symbol	HM511002-8S HM511002A-8		HM51102-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{ZRH}	10	–	10	–	10	–	ns	

SC Mode Cycle

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{SC}$ mode cycle time	t_{SC}	45	–	55	–	60	–	ns	
$\overline{SC}$ mode $\overline{RAS}$ pulse width	t_{RASC}	–	100000	–	100000	–	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	90	–	110	–	135	–	ns	
$\overline{SC}$ mode $\overline{CS}$ precharge time	t_{SI}	10	–	10	–	15	–	ns	
Write invalid time	t_{WI}	10	–	10	–	15	–	ns	

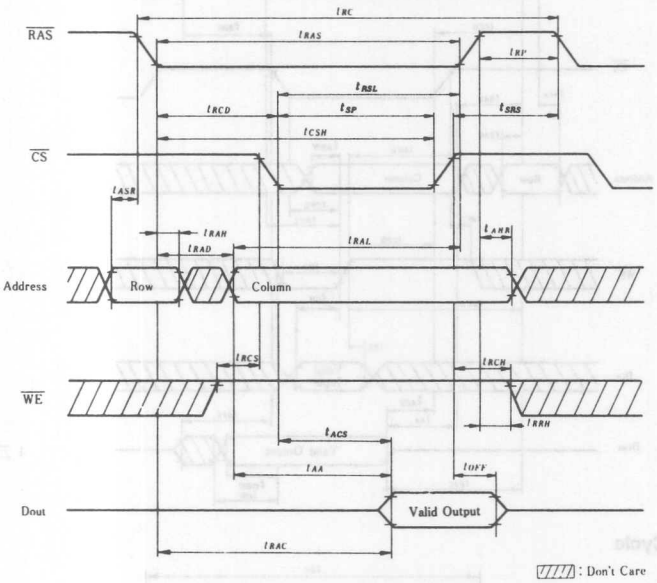
SC Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM511002-8S HM511002A-8		HM511002-10S HM511002A-10		HM511002-12S HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{SC}$ mode cycle time on read-write	t_{SRW}	90	–	105	–	120	–	ns	*12
Access time from previous $\overline{WE}$	t_{ALW}	–	85	–	100	–	115	ns	*3,*13
Previous $\overline{WE}$ to column address delay time	t_{LWAD}	25	45	25	50	30	60	ns	*15
Column address hold time to previous $\overline{WE}$	t_{AHLW}	85	–	100	–	115	–	ns	
Output enable time from $\overline{WE}$	t_{OW}	–	30	–	30	–	35	ns	

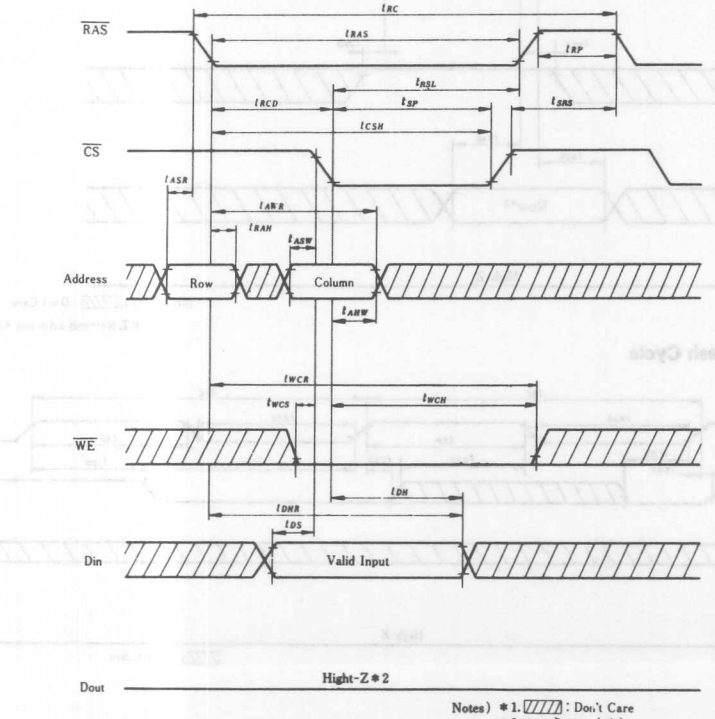
Notes)
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T.
13. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geqq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} is defined as the time at which the column address hold.
17. An initial pause of 100μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

- **Read Cycle**

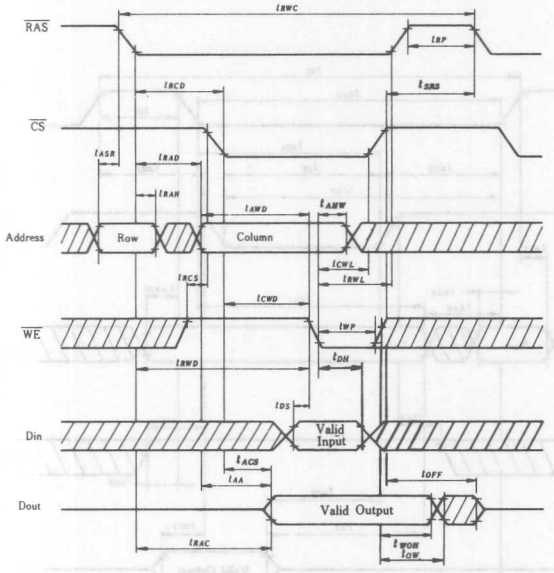


- **Early Write Cycle**



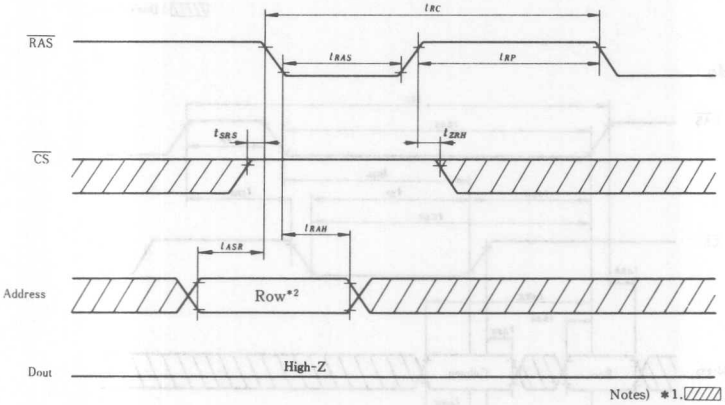
Notes) *1. : Don't Care
*2. $t_{WCS} \geq t_{WCS}$ (min)

• Read-Modify-Write Cycle



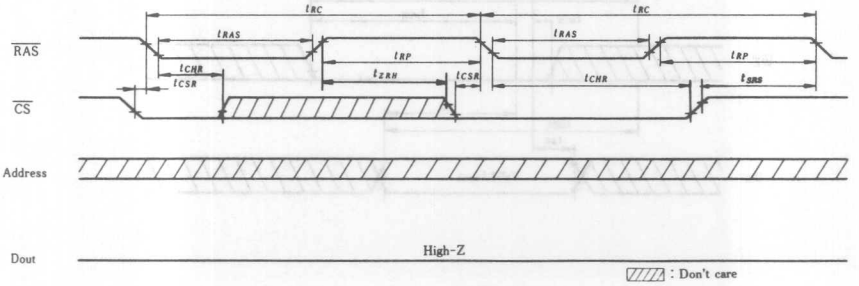
1 ▨: Don't Care

• RAS-Only Refresh Cycle



Notes) *1. ▨: Don't Care
*2. Refresh address A0-A8(AX0-AX8)

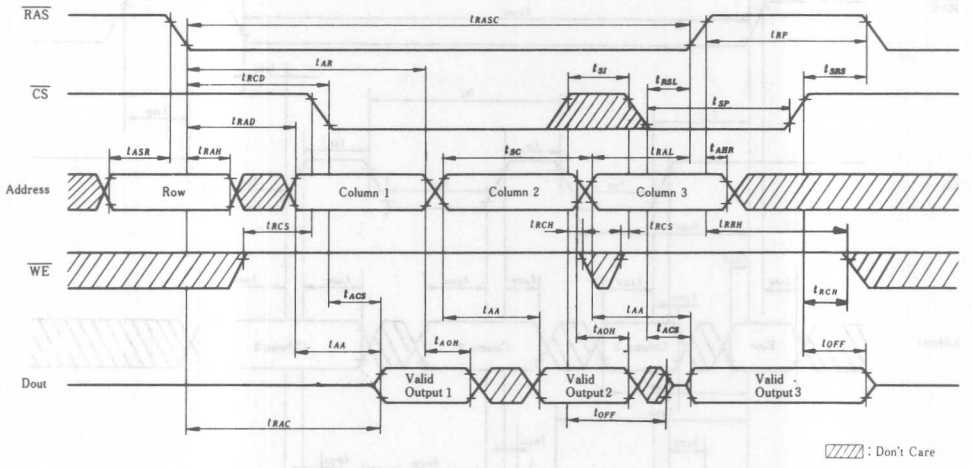
• CS-before-RAS Refresh Cycle



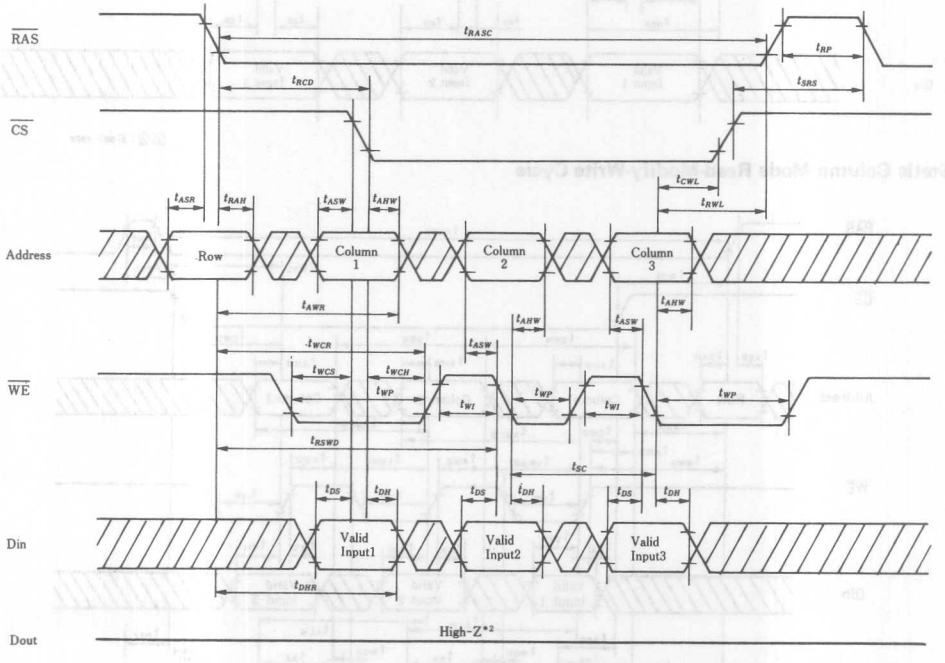
▨: Don't care

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• Static Column Mode Read Cycle

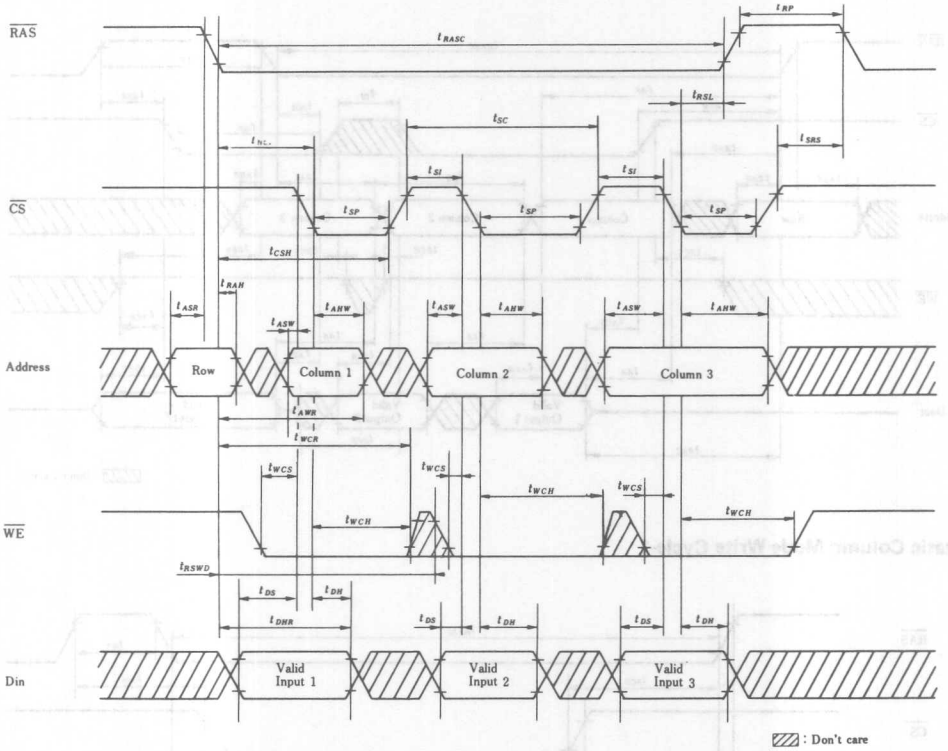


• Static Column Mode Write Cycle-1

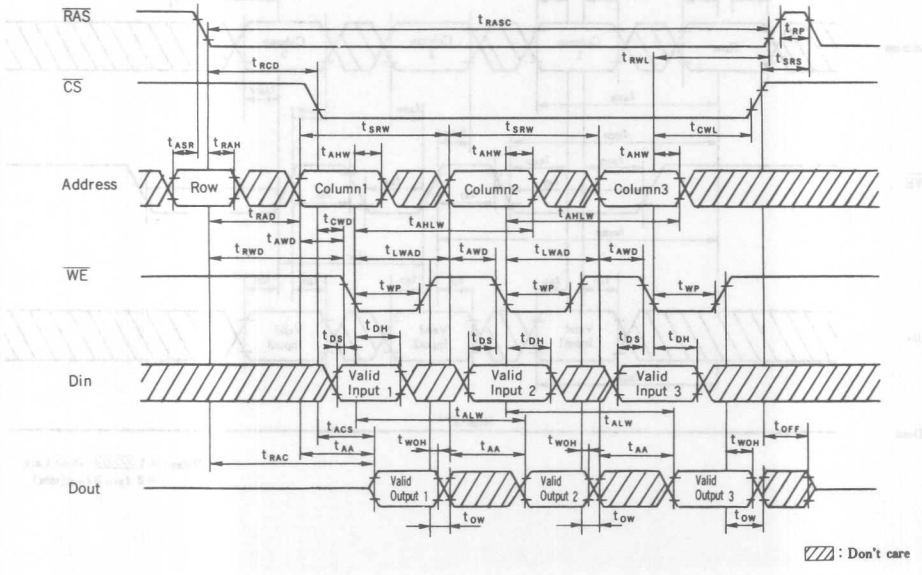


Notes) *1 : Don't Care
*2 $t_{WCS} \geqq t_{WCS}$(min)

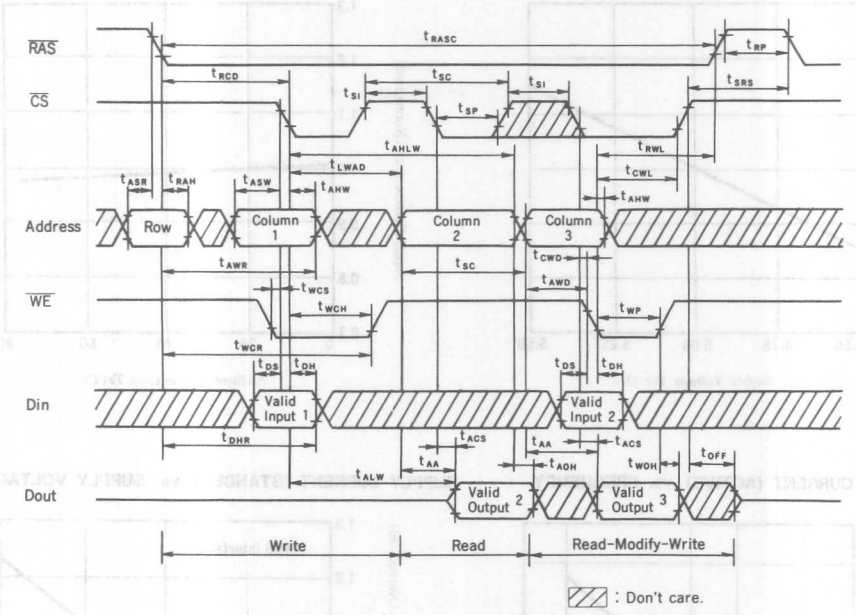
• Static Column Mode Write Cycle-2



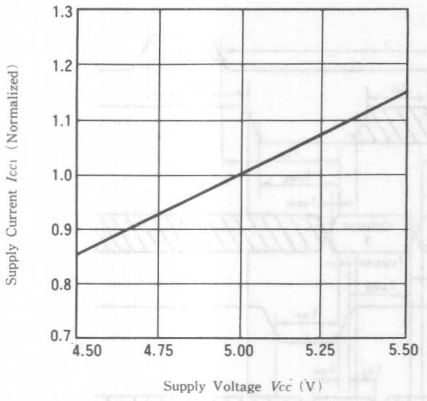
• Static Column Mode Read-Modify-Write Cycle



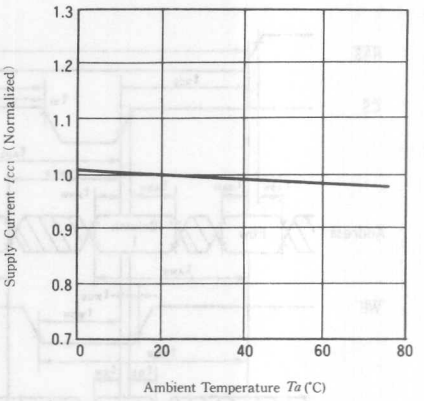
• Static Column Mode Mixed Cycle



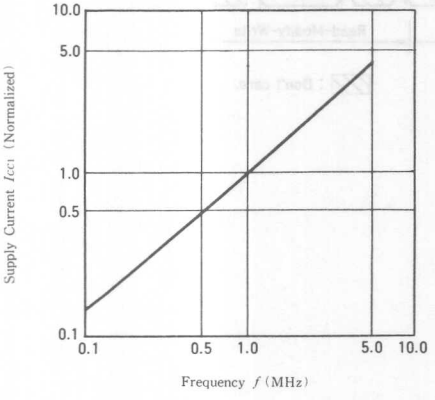
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



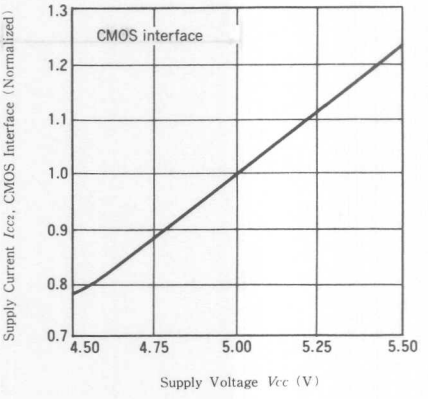
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



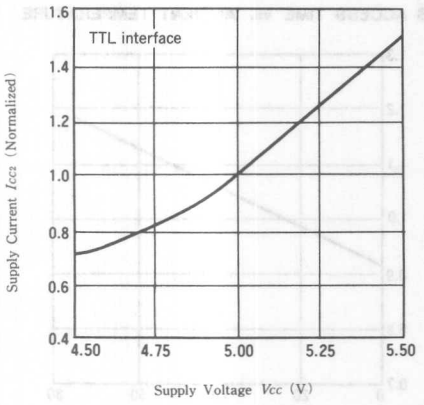
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



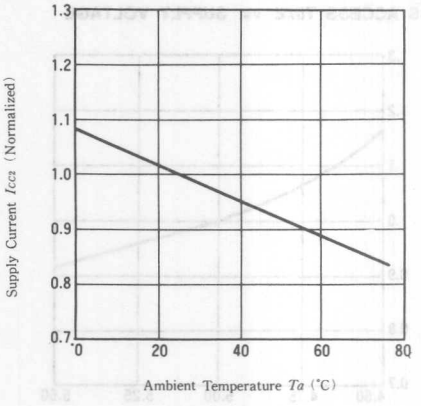
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



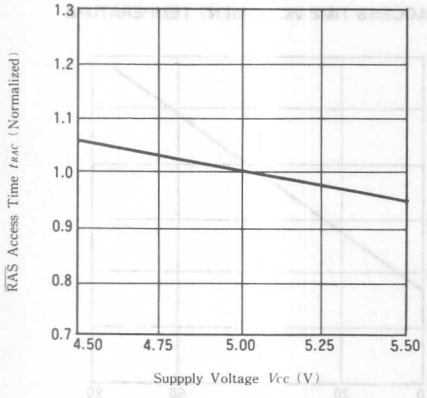
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



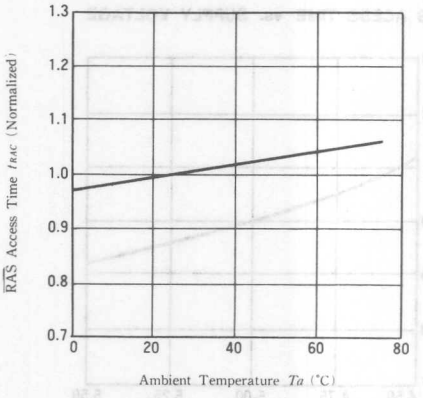
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



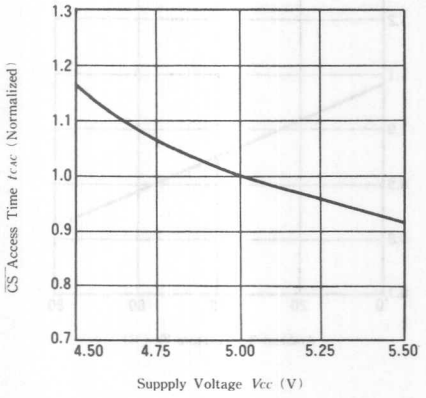
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



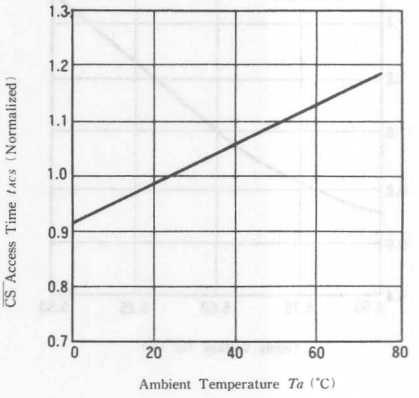
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



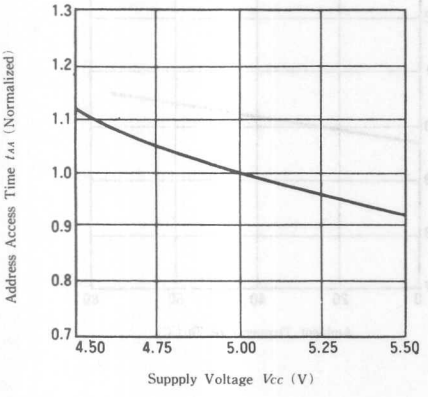
$\overline{CS}$ ACCESS TIME vs. SUPPLY VOLTAGE



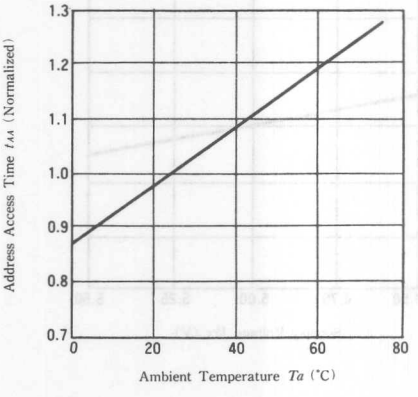
$\overline{CS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



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HB56A18A/AT/B-6H/7H/8A/10A/12A

1,048,576-Word × 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A18 is a 1M × 8 dynamic RAM module, mounted eight 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A18 is 30-pin single in-line package having Lead types (HB56A18A, HB56A18AT), socket type (HB56A18B). Therefore, the HB56A18 makes high density mounting possible without surface mount technology. The HB56A18 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

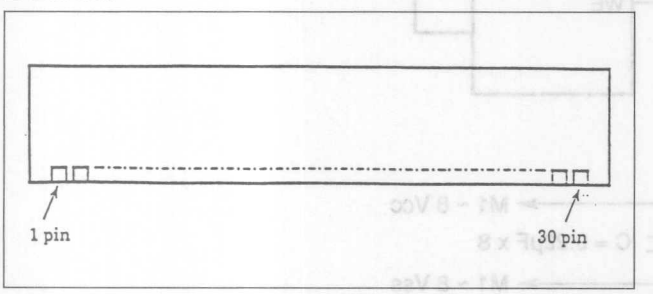
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . .60/70/80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .3.96/3.52/3.08/2.64/2.20W (max.)
  - Standby Mode. . . . . .88mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-Pin SIP Lead Type	30-Pin SIP Low Profile Lead Type	30-Pin SIMM Socket Type
60ns	HB56A18A-6H	HB56A18AT-6H	HB56A18B-6H
70ns	HB56A18A-7H	HB56A18AT-7H	HB56A18B-7H
80ns	HB56A18A-8A	HB56A18AT-8A	HB56A18B-8A
100ns	HB56A18A-10A	HB56A18AT-10A	HB56A18B-10A
120ns	HB56A18A-12A	HB56A18AT-12A	HB56A18B-12A

■ PIN OUT

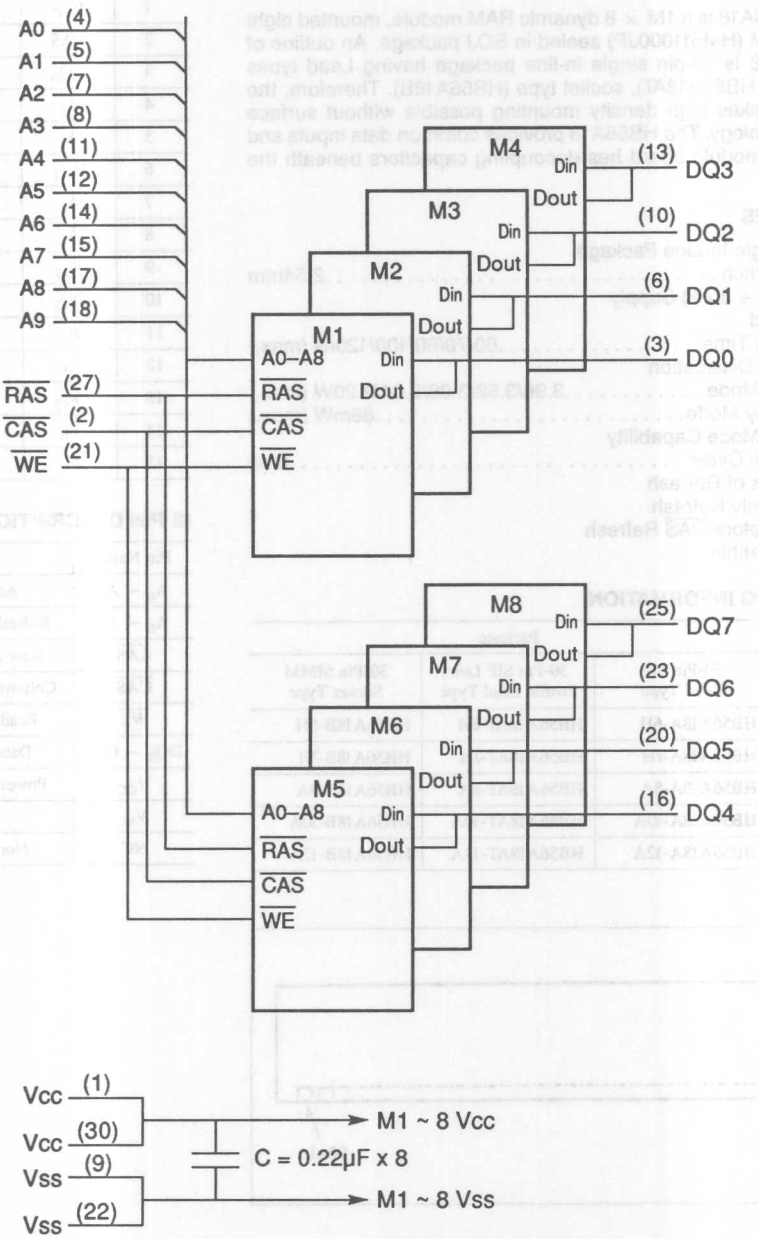


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

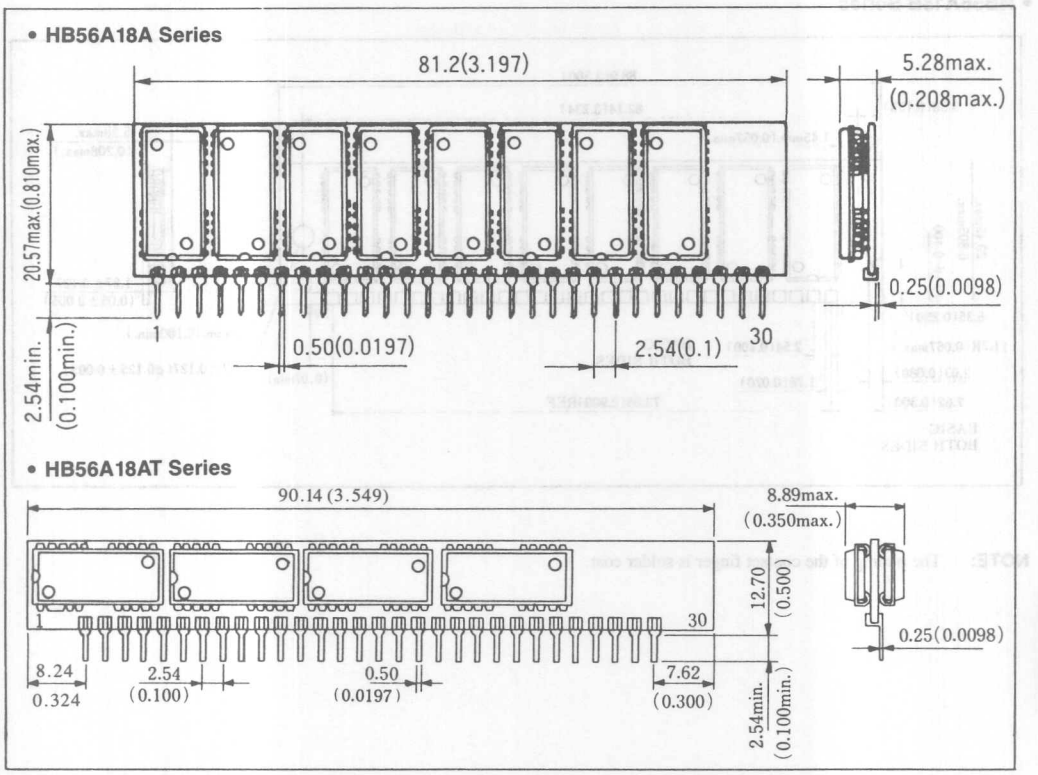
■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_9	Address Input
A_0 ~ A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0 ~ DQ_7	Data-In/Data-Out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

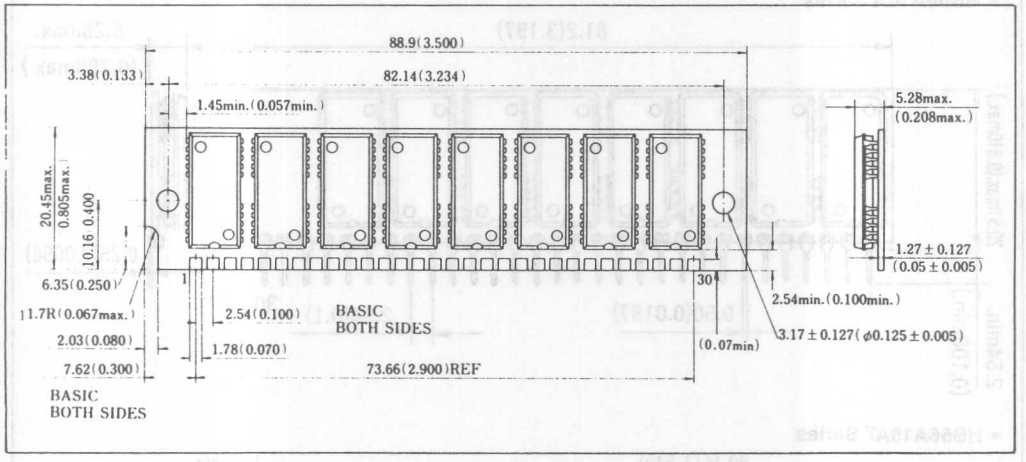
■ BLOCK DIAGRAM



■ PHYSICAL OUTLINE



- **HB56A18B Series**



NOTE: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	Input	V_{IN}	−1.0 to + 7.0	V
	Output	V_{OUT}	−1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56A18A/AT/B										Unit	Note
			-6H		-7H		-8A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	720	—	640	—	560	—	480	—	400	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	—	16	—	16	—	16	—	16	—	16	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	8	—	8	—	8	—	8	—	8	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	720	—	640	—	480	—	400	—	360	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	40	—	40	—	40	—	40	—	40	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	720	—	640	—	480	—	400	—	320	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	720	—	640	—	400	—	400	—	320	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	55	pF	1
Input Capacitance (Clock)	C_{I2}	—	70	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS

Please show at HM511000H series or HM511000A series about AC Characteristics. But don't use by Derayed Write Cycle, because the HB56A18 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min.)).

HB56C18A/AT/B-8A/10A/12A

1,048,576-Word × 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56C18 is a 1M × 8 static column mode dynamic RAM module, mounted eight 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C18 is 30-pin single in-line package having Lead types (HB56C18A, HB56C18AT), socket type (HB56C18B). Therefore, the HB56C18 makes high density mounting possible without surface mount technology. The HB56C18 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

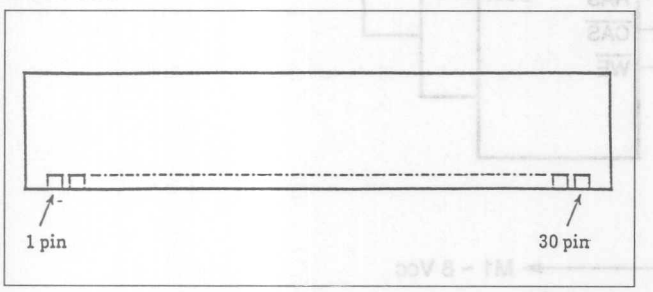
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time. . . . . 80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 3080/2640/2200mW (max.)
  - Standby Mode. . . . . 88mW (max.)
- Static Column Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-Pin SIP Lead Type	30-Pin SIP Low Profile Lead Type	30-Pin SIP Socket Type
80ns	HB56C18A-8A	HB56C18AT-8A	HB56C18B-8A
100ns	HB56C18A-10A	HB56C18AT-10A	HB56C18B-10A
120ns	HB56C18A-12A	HB56C18AT-12A	HB56C18B-12A

■ PIN OUT

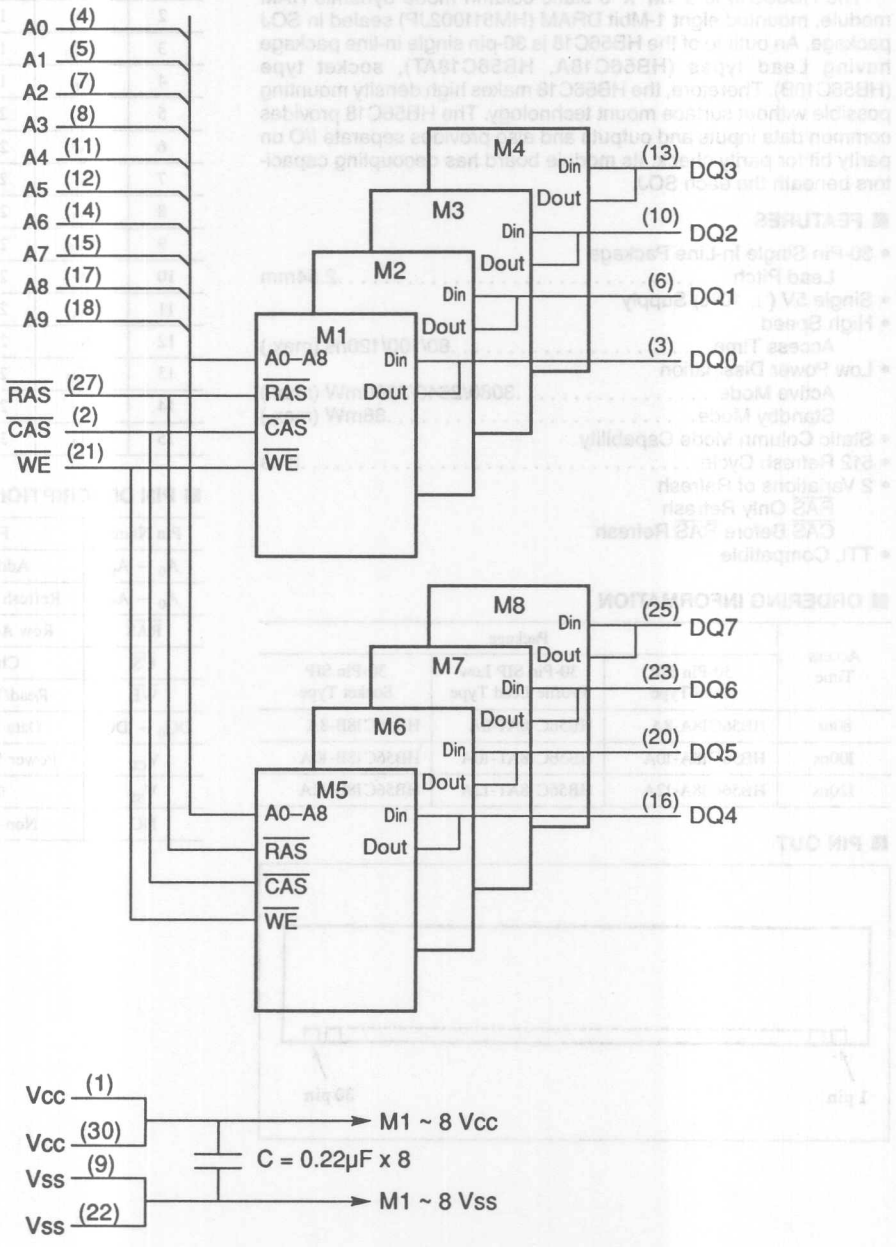


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

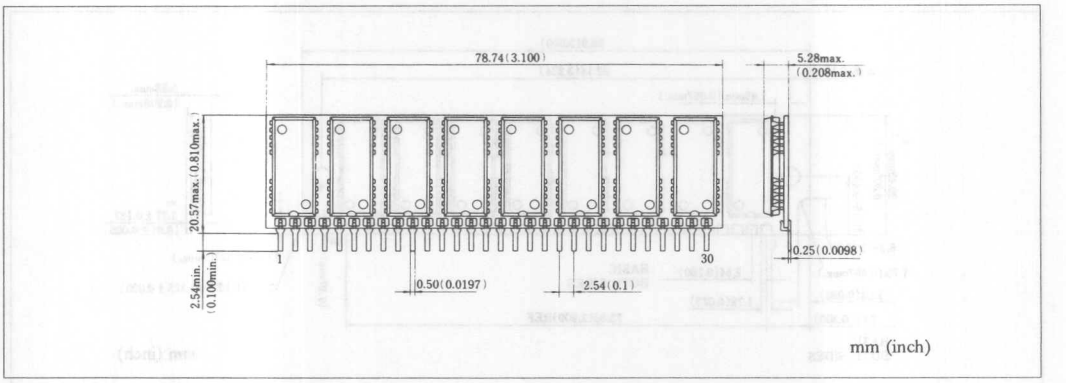
Pin Name	Function
A_0 ~ A_9	Address Input
A_0 ~ A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Read/Write Enable
DQ_0 ~ DQ_7	Data-In/Data-Out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

■ BLOCK DIAGRAM

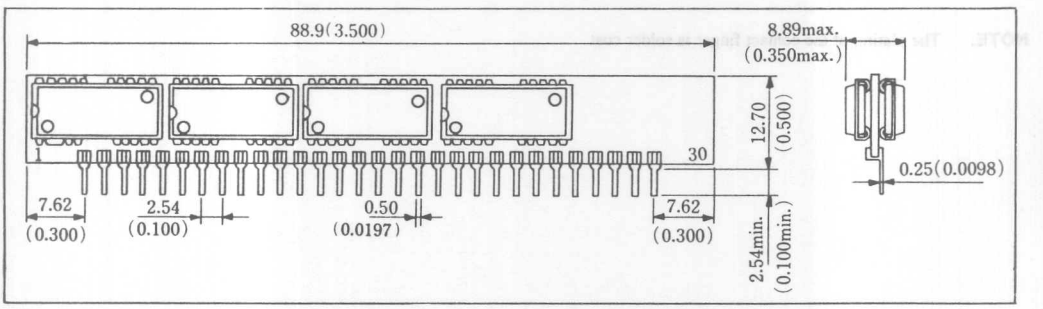


■ PHYSICAL OUTLINE

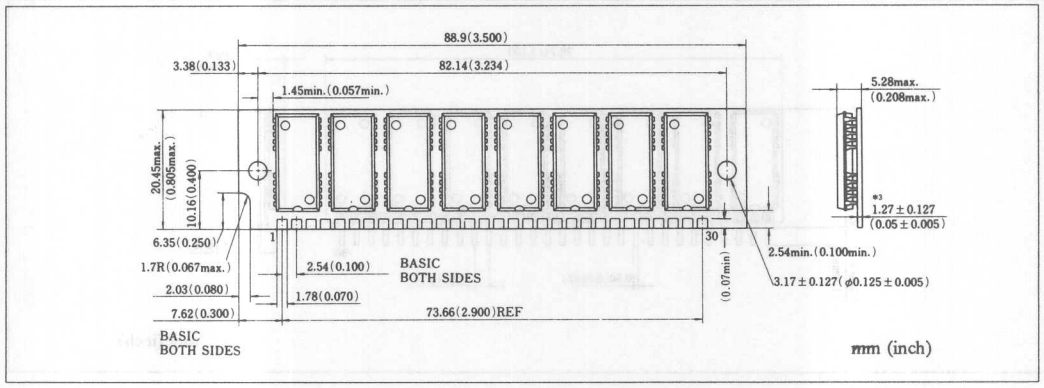
• HB56C18A Series



• HB56C18AT Series



• **HB56C18B Series**



NOTE: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56C18A/AT/B						Unit	Note
			-8A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	560	—	480	—	400	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} D_{OUT} = High-Z	—	16	—	16	—	16	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	8	—	8	—	8	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	480	—	400	—	360	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL} D_{OUT} = Enable	—	40	—	40	—	40	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	480	—	400	—	320	mA	
Static Column Mode Current	I_{CC9}	Static Column Mode t_{PC} = Min.	—	480	—	400	—	320	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	55	pF	1
Input Capacitance (Clock)	C_{I2}	—	70	pF	1, 2
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS

Please show at HM511002H series about AC Characteristics. But don't use by Derayed Write Cycle, because the HB56C18 provides common data inputs and outputs. Please use by Early Write Cycle. (t_{WCS} ≥ t_{WCS} (min.)).

HB56A19A/AT/B-6H/7H/8A/10A/12A

1,048,576-Word × 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A19 is a 1M × 9 dynamic RAM module, mounted nine 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A19 is 30-pin single in-line package having Lead types (HB56A19A, HB56A19AT), Socket type (HB56A19B). Therefore, the HB56A19 makes high density mounting possible without surface mount technology. The HB56A19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

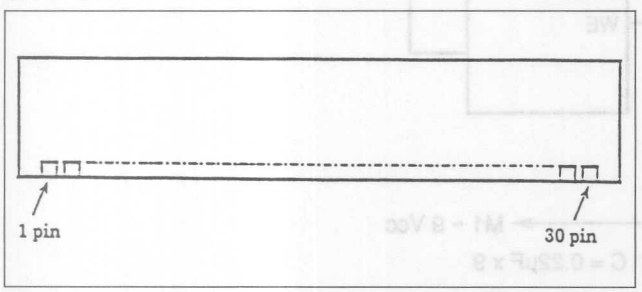
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . 60/70/80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 4455/3960/3465/2970/2475mW (max.)
  - Standby Mode . . . . . 99mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-Pin SIP Lead Type	30-Pin SIP Low Profile Lead Type	30-Pin SIMM Socket Type
60ns	HB56A19A-6H	HB56A19AT-6H	HB56A19B-6H
70ns	HB56A19A-7H	HB56A19AT-7H	HB56A19B-7H
80ns	HB56A19A-8A	HB56A19AT-8A	HB56A19B-8A
100ns	HB56A19A-10A	HB56A19AT-10A	HB56A19B-10A
120ns	HB56A19A-12A	HB56A19AT-12A	HB56A19B-12A

■ PIN OUT

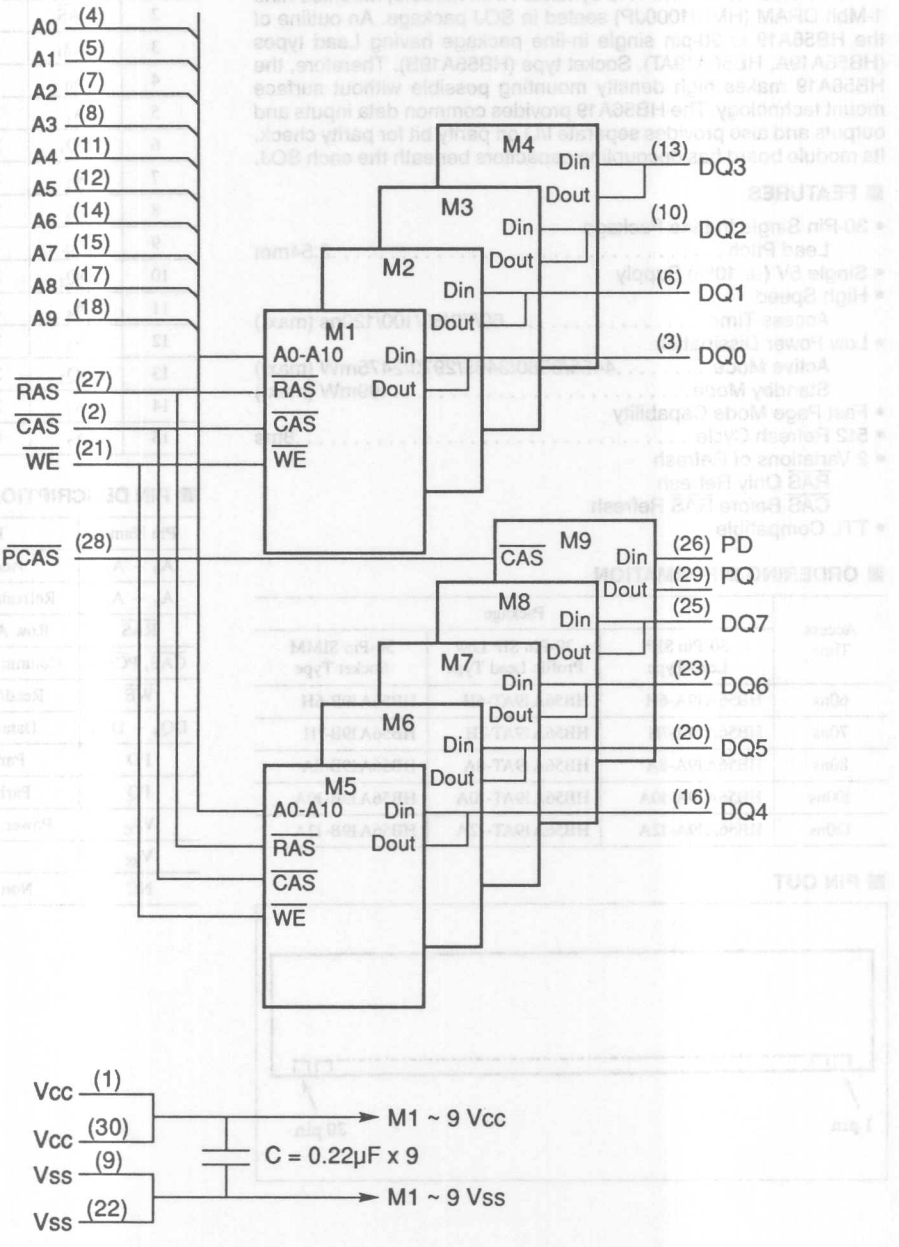


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

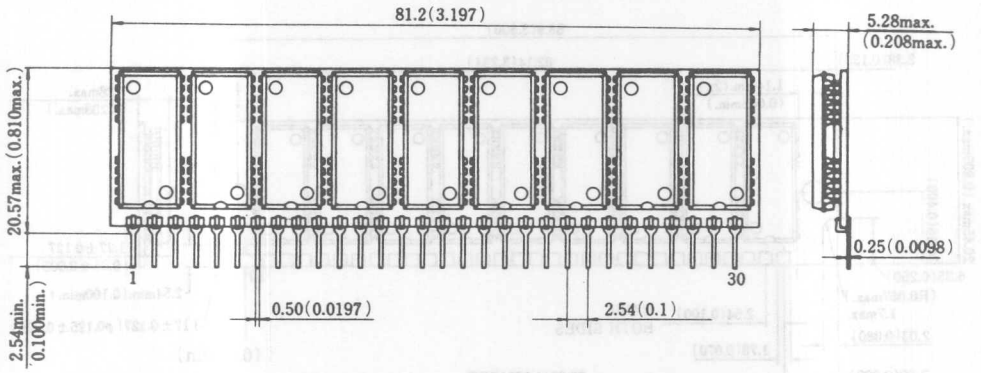
Pin Name	Function
A_0 ~ A_9	Address Input
A_0 ~ A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0 ~ DQ_7	Data-In/Data-Out
PD	Parity Data-In
PQ	Parity Data-Out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

■ BLOCK DIAGRAM

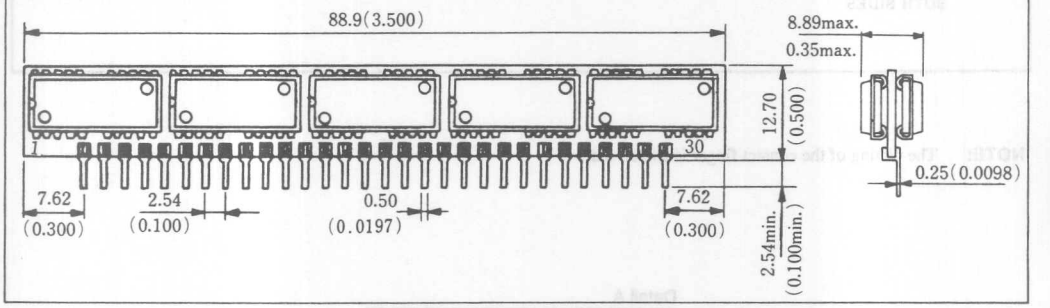


■ PHYSICAL OUTLINE

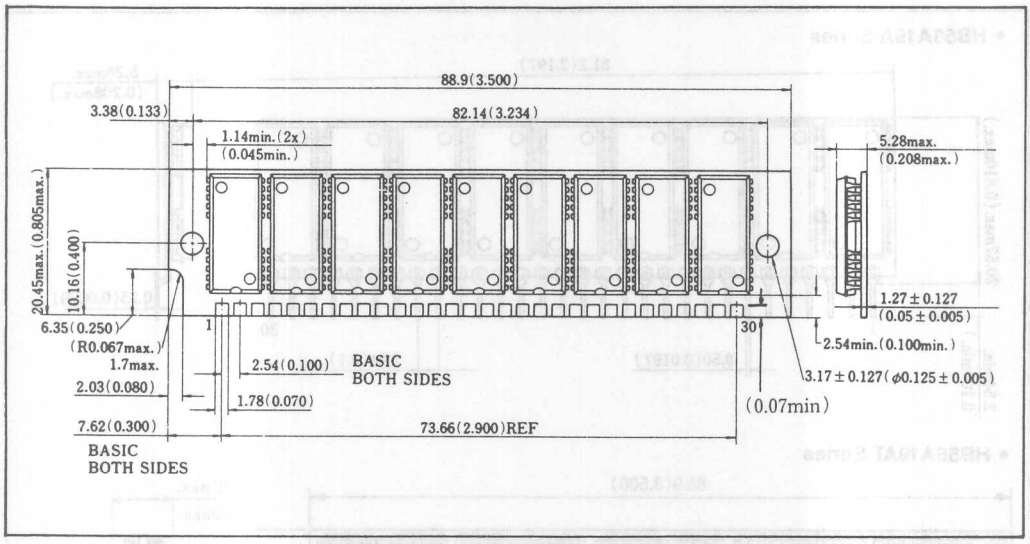
• **HB56A19A Series**



• **HB56A19AT Series**

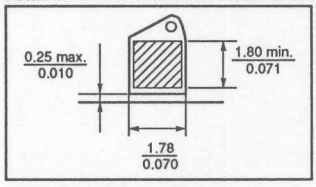


• **HB56A19B Series**



NOTE: The plating of the contact finger is solder coat.

Detail A



Note: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	Input	V_{IN}	−1.0 to + 7.0	V
	Output	V_{OUT}	−1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	9	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56A19A/AT/B										Unit	Note
			-6H		-7H		-8A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	810	—	720	—	630	—	540	—	450	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	—	18	—	18	—	18	—	18	—	18	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	9	—	9	—	9	—	9	—	9	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	810	—	720	—	540	—	450	—	405	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	45	—	45	—	45	—	45	—	45	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	810	—	720	—	540	—	450	—	360	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	810	—	720	—	450	—	450	—	360	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	60	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	pF	1
Input/Output Capacitance (DQ_0-DQ_7)	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1, 2
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS

Please show at HM511000H series or HM511000A series about AC Characteristics. But don't use by Derayed Write Cycle, because the HB56A19 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min.)).

HB56C19A/AT/B-8A/10A/12A

1,048,576-Word × 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56C19 is a 1M × 9 static column mode dynamic RAM module, mounted nine 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C19 is 30-pin single in-line package having Lead types (HB56C19A, HB56C19AT), Socket type (HB56C19B). Therefore, the HB56C19 makes high density mounting possible without surface mount technology. The HB56C19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

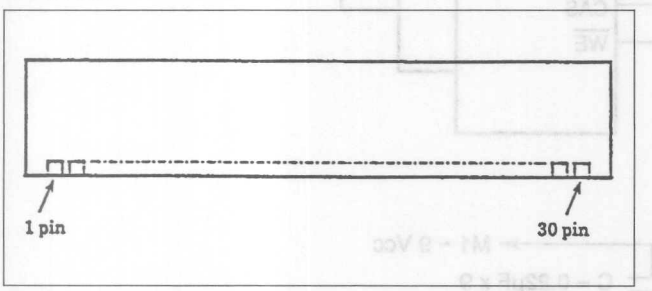
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . 80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 3465/2970/2475mW (max.)
  - Standby Mode . . . . . 99mW (max.)
- Static Column Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-Pin SIP Lead Type	30-Pin SIP Low Profile Lead Type	30-Pin SIMM Socket Type
80ns	HB56C19A-8A	HB56C19AT-8A	HB56C19B-8A
100ns	HB56C19A-10A	HB56C19AT-10A	HB56C19B-10A
120ns	HB56C19A-12A	HB56C19AT-12A	HB56C19B-12A

■ PIN OUT

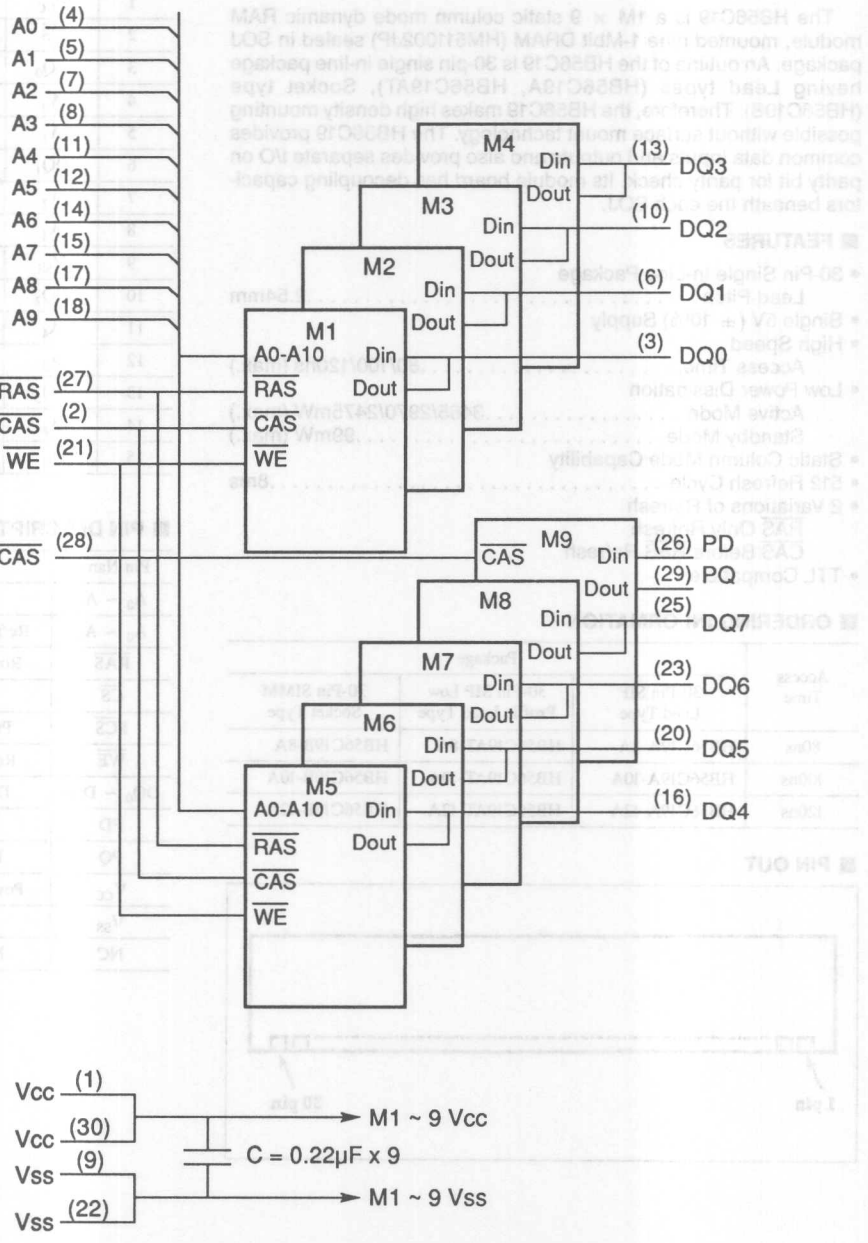


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$P\overline{CS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

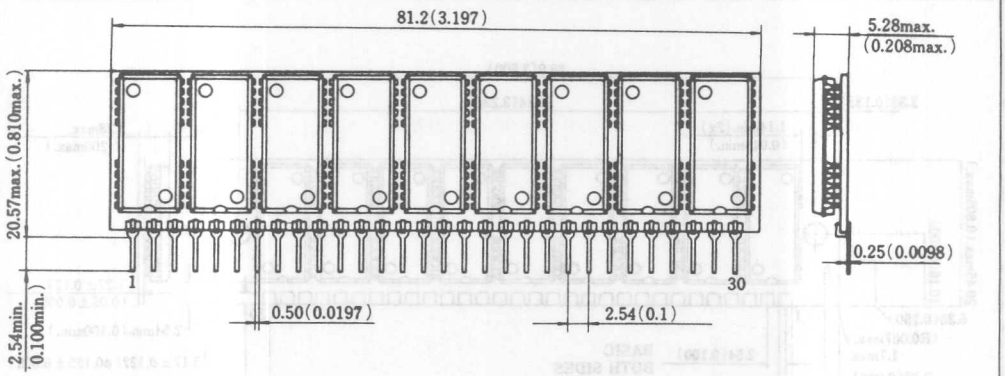
Pin Name	Function
$A_0 \sim A_9$	Address Input
$A_0 \sim A_8$	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$P\overline{CS}$	Parity Chip Select
$\overline{WE}$	Read/Write Enable
$DQ_0 \sim DQ_7$	Data-In/Data-Out
PD	Parity Data-In
PQ	Parity Data-Out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

■ BLOCK DIAGRAM

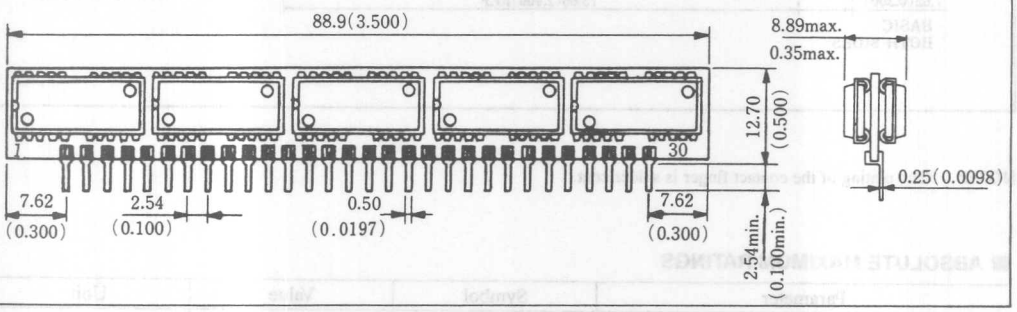


■ PHYSICAL OUTLINE

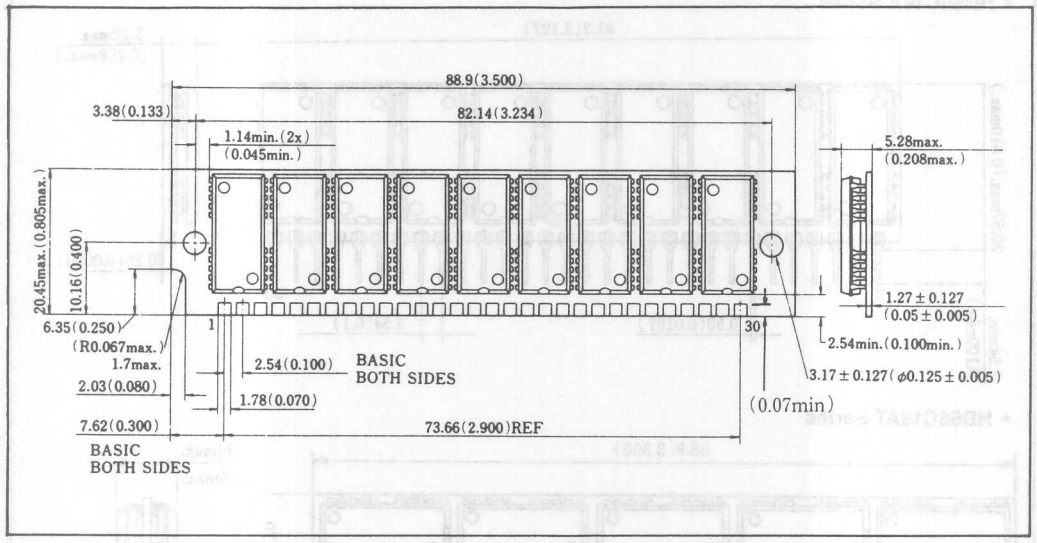
• **HB56C19A Series**



• **HB56C19AT Series**



• **HB56C19B Series**



NOTE: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	9.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **Recommended DC Operating Conditions** (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56C19A/AT/B						Unit	Note
			-8A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	630	—	540	—	450	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} D_{OUT} = High-Z	—	18	—	18	—	18	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} -0.2V D_{OUT} = High-Z	—	9	—	9	—	9	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	540	—	450	—	405	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL} D_{OUT} = Enable	—	45	—	45	—	45	mA	1
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	540	—	450	—	360	mA	
Static Column Mode Current	I_{CC9}	Static Column Mode t_{PC} = Min.	—	540	—	450	—	360	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = -5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	60	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	pF	1, 2
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS

Please show at HM511002A series about AC Characteristics. But don't use by Derayed Write Cycle, because the HB56C19 provides common data inputs and outputs. Please use by Early Write Cycle. (t_{WCS} ≥ t_{WCS} (min.)).

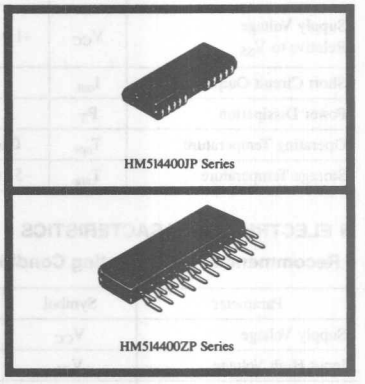
HM514100JP/ZP-8/10/12
4 Megabit DRAM

4,194,304-Word × 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word × 1 bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.



■ FEATURES

- Single 5V (±10%)
- High Speed
  Access time . . . . . .80ns/100ns/120ns (max.)
- Low power dissipation
  —Active mode . . . . . .495mW/440mW/385mW (max.)
  —Standby mode . . . . . .11mW (max.)
- Fast page mode capability
- 1,024 refresh cycles. . . . . .(16 ms)
- 3 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
  —Hidden Refresh
- Test Function

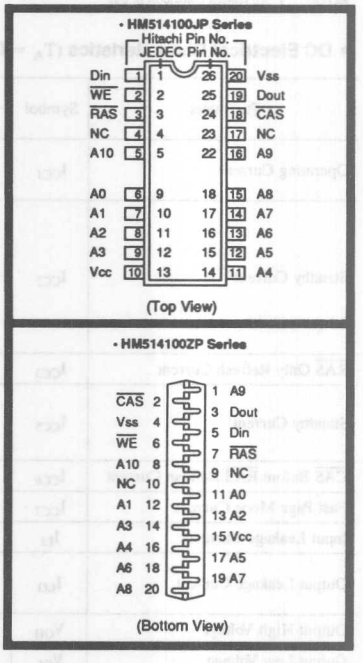
■ ORDERING INFORMATION

Part No.	Access	Package
HM514100JP-8	80ns	350 mil 20-pin Plastic SOJ
HM514100JP-10	100ns	
HM514100JP-12	120ns	
HM514100ZP-8	80ns	400 mil 20-pin Plastic ZIP
HM514100ZP-10	100ns	
HM514100ZP-12	120ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{IN}	Data-in
D_{OUT}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• **AC Characteristics** (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) [1, 12, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

■ **READ CYCLE**

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

■ WRITE CYCLE

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

• Refresh Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14, 16
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

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• Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	—	85	—	100	—	ns	

• Test Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode $\overline{WE}$ Set-up Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

• Counter Test Cycle

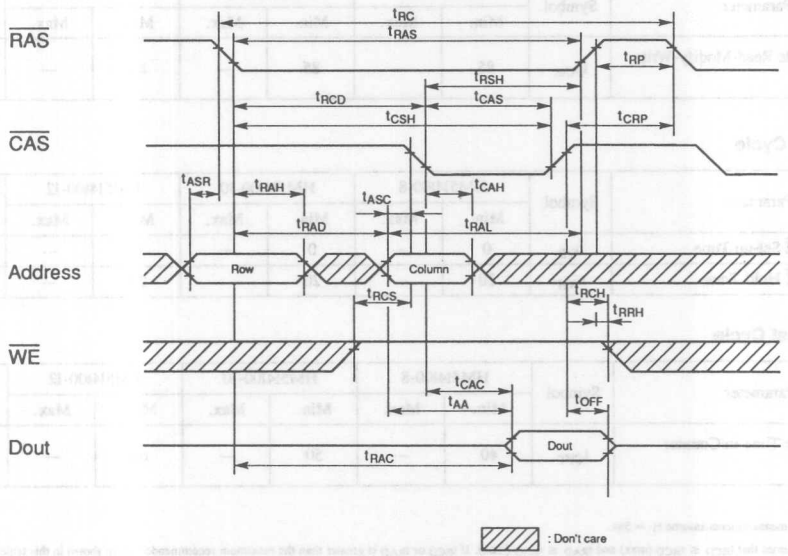
Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

NOTES:

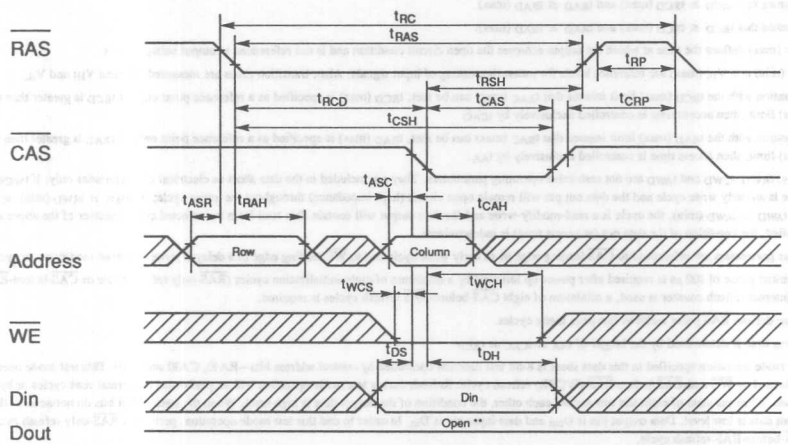
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORM

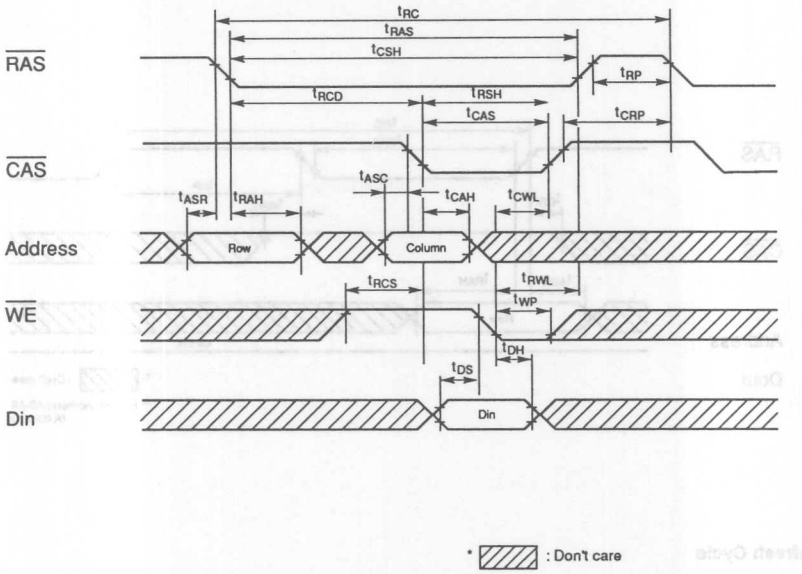
• Read Cycle



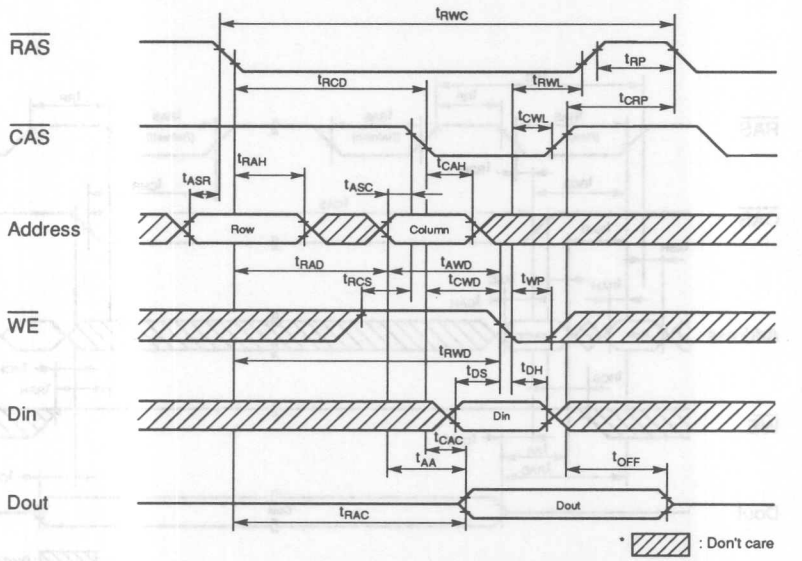
• Early Write Cycle



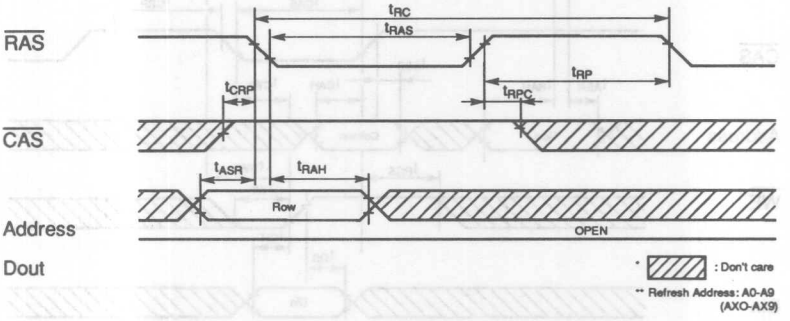
• **Delayed Write Cycle**



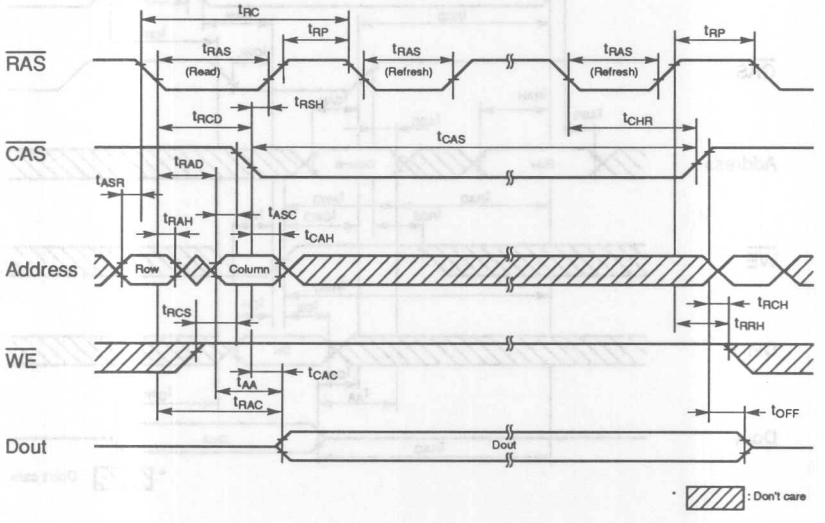
• **Read-Modify-Write Cycle**



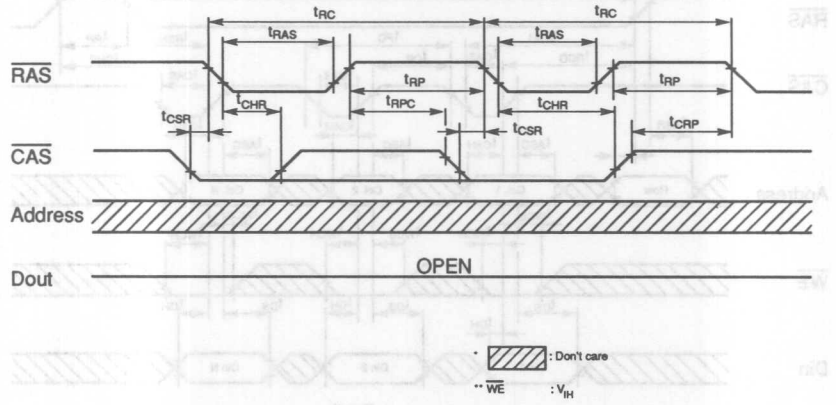
• **$\overline{RAS}$ Only Refresh Cycle**



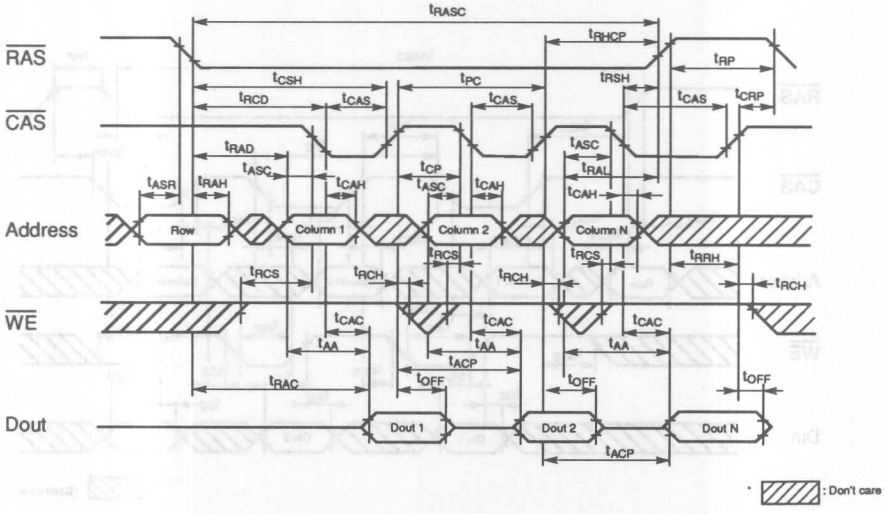
• **Hidden Refresh Cycle**



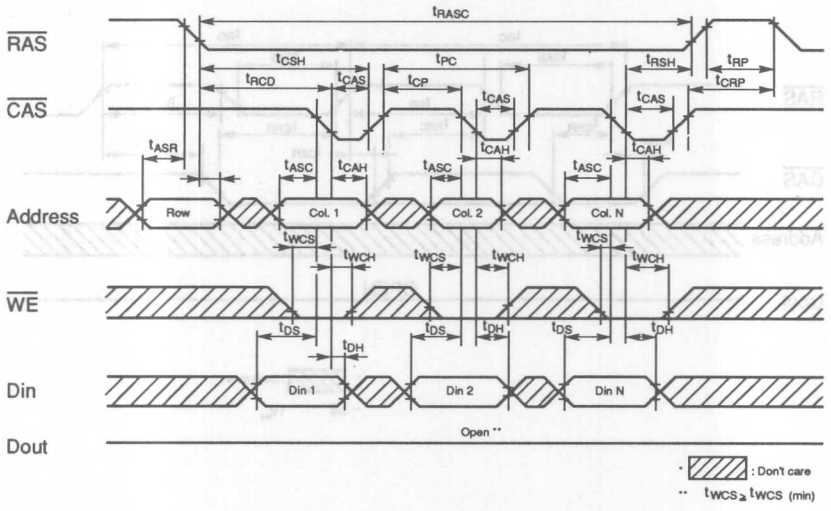
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



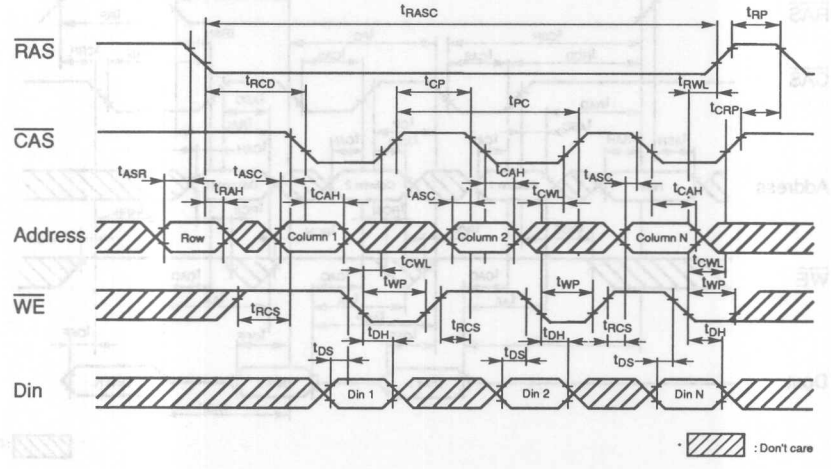
• **Fast Page Mode Read Cycle**



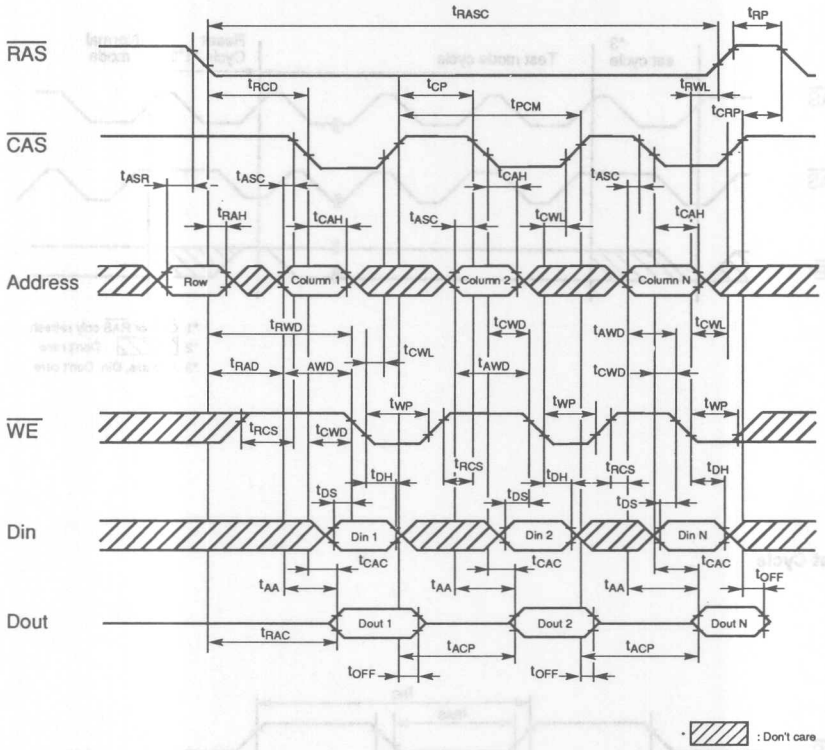
• **Fast Page Mode Early Write Cycle**



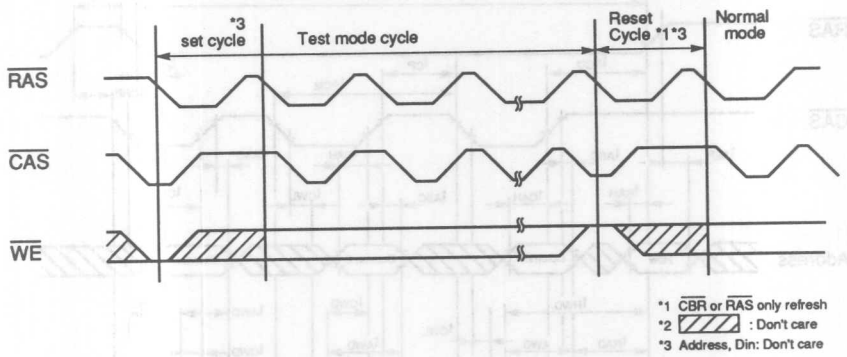
• **Fast Page Delayed Write Cycle**



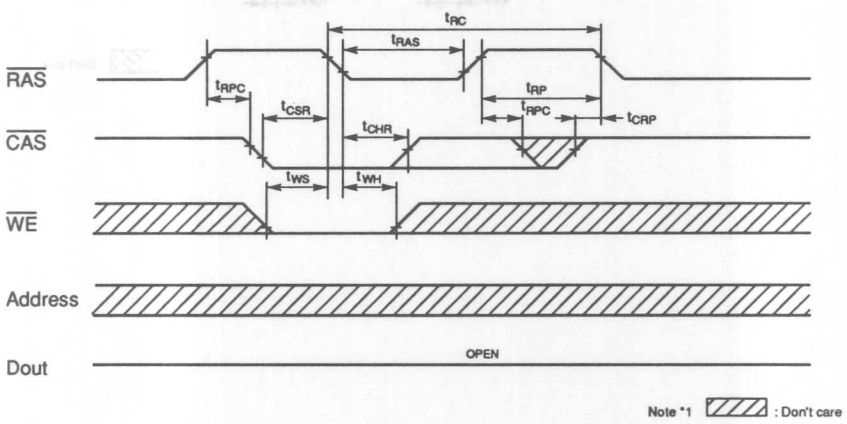
• **Fast Page Mode Read-Modify-Write Cycle**



• **Test Mode Cycle**

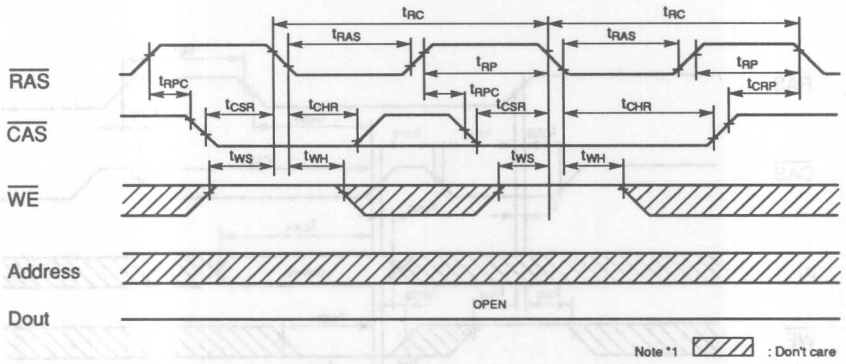


• **Test Mode Set Cycle**

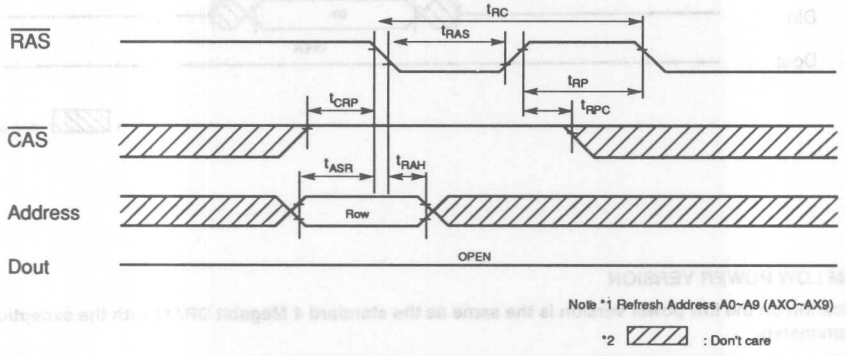


■ TEST MODE RESET CYCLE

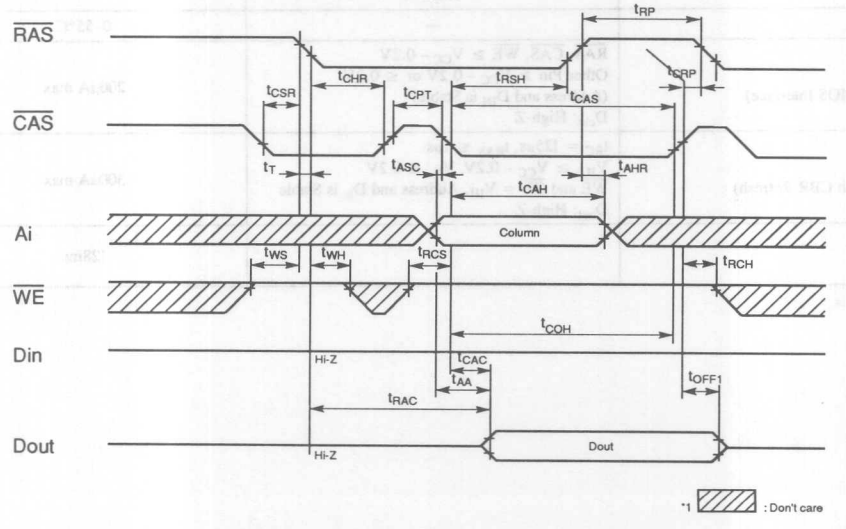
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



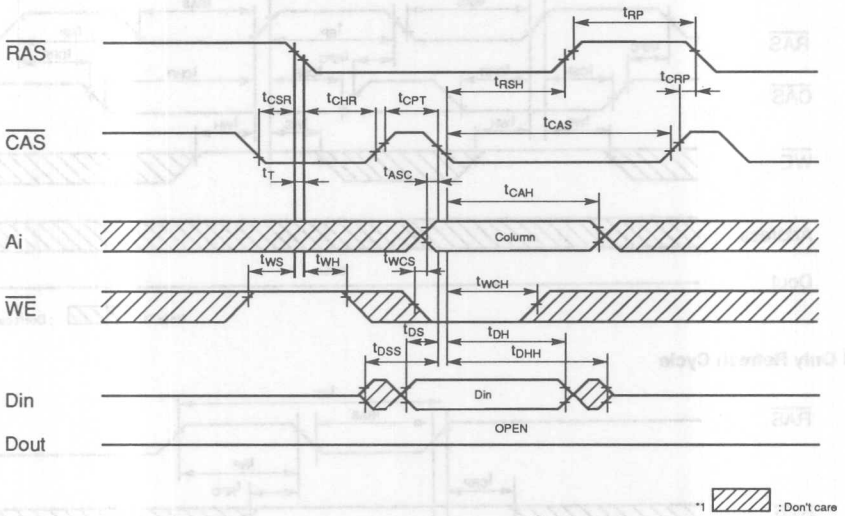
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)**



■ 4M DRAM LOW POWER VERSION

The specification on the low power version is the same as the standard 4 Megabit DRAM with the exception of the following parameters.

Item	Conditions	Spec.
Type No.	4M × 1	HM514100LJP/LZP
	1M × 4	
Temperature	—	0–55°C
I_{CC2} (Standby CMOS Interface)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} – 0.2V Other Pin ≥ V_{CC} – 0.2V or ≤ 0.2V (Address and D_{IN} is Stable) D_{out}: High-Z	200μA max
I_{CC10} (Standby with CBR Refresh)	t_{RC} = 125μs, t_{RAS} ≤ 1μs V_{IL1} ≥ V_{CC} – 0.2V, V_{IL} ≤ 0.2V $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in} is Stable D_{out}: High-Z	300μA max
Refresh t_{REF}	—	128ms

*only for 1M × 4.

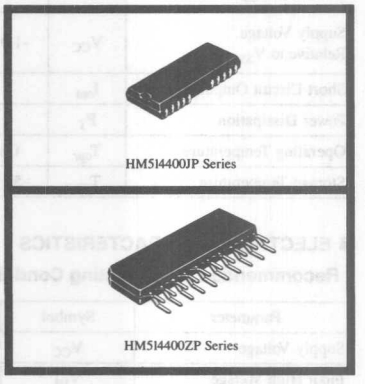
HM514100JP/ZP-7
4 Megabit DRAM

4,194,304-Word × 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word × 1 bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.



■ FEATURES

- Single 5V (±10%, –5%)
- High Speed
  Access time . . . . . .70ns (max.)
- Low power dissipation
  —Active mode . . . . . .550mW (max.)
  —Standby mode . . . . . .11mW (max.)
- Fast page mode capability
- 1,024 refresh cycles. . . . . .(16 ms)
- 3 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
  —Hidden Refresh
- Test Function

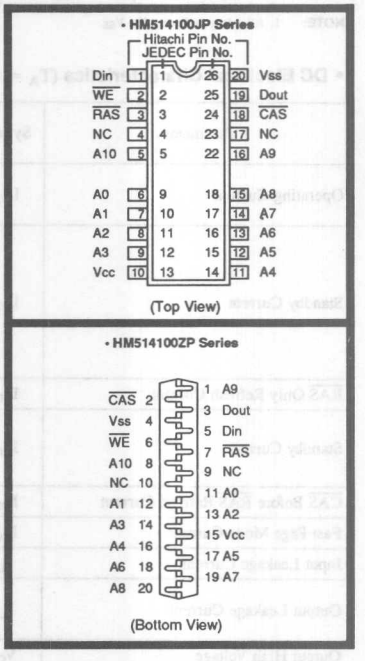
■ ORDERING INFORMATION

Part No.	Access	Package
HM514100JP-7	70ns	350 mil 20-pin Plastic SOJ
HM514100ZP-7	70ns	400 mil 20-pin Plastic ZIP

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{IN}	Data-in
D_{OUT}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, −5%, V_{SS} = 0V)

Parameter	Symbol	HM514100-7		Unit	Test Condition	Note
		Min	Max			
Operating Current	I_{CC1}	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	100	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	100	mA	t_{RC} = min	
Fast Page Mode Current	I_{CC7}	—	100	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output Low Voltage	V_{OL}	0	0.4	V	Low I_{out} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ± 10%, -5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• **AC Characteristics** (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, -5% V_{SS} = 0V) [1, 12, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	140	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	ns	7
Refresh Period	t_{REF}	—	16	ms	

■ **READ CYCLE**

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	70	ns	2, 3, 16
Access Time From $\overline{CAS}$	t_{CAC}	—	25	ns	3, 4, 14
Access Time From Address	t_{AA}	—	40	ns	3, 5, 14, 16
Read Command Set-up Time	t_{RCS}	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	ns	6

■ WRITE CYCLE

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	ns	
Data-in Set-up Time	t_{DS}	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	ns	11

■ READ-MODIFY-WRITE CYCLE

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Read-Modify-Write Cycle Time	t_{RWC}	170	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	70	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	ns	10

■ REFRESH CYCLE

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	ns	

■ FAST PAGE MODE CYCLE

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	ns	13
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	ns	14, 16
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	ns	

■ FAST PAGE MODE READ-MODIFY-WRITE CYCLE

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	—	ns	

■ TEST MODE CYCLE

Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
Test Mode $\overline{WE}$ Set-up Time	t_{WS}	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	ns	

■ COUNTER TEST CYCLE

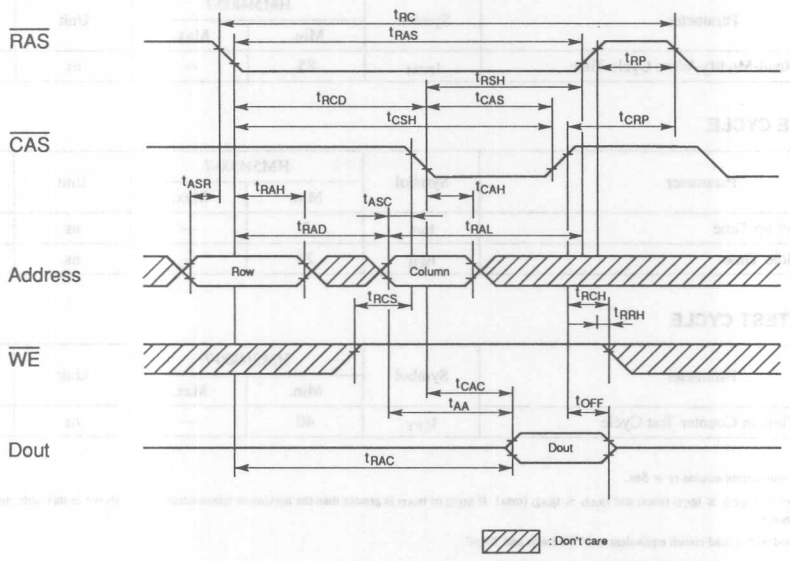
Parameter	Symbol	HM514100-7		Unit	Note
		Min.	Max.		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	ns	

NOTES:

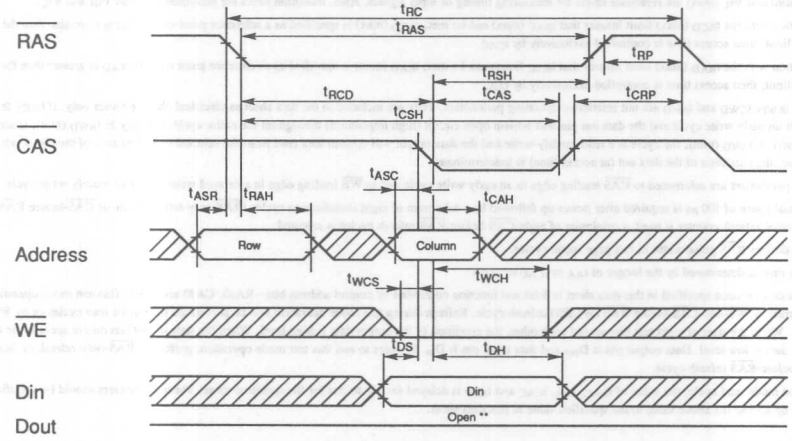
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORM

• Read Cycle



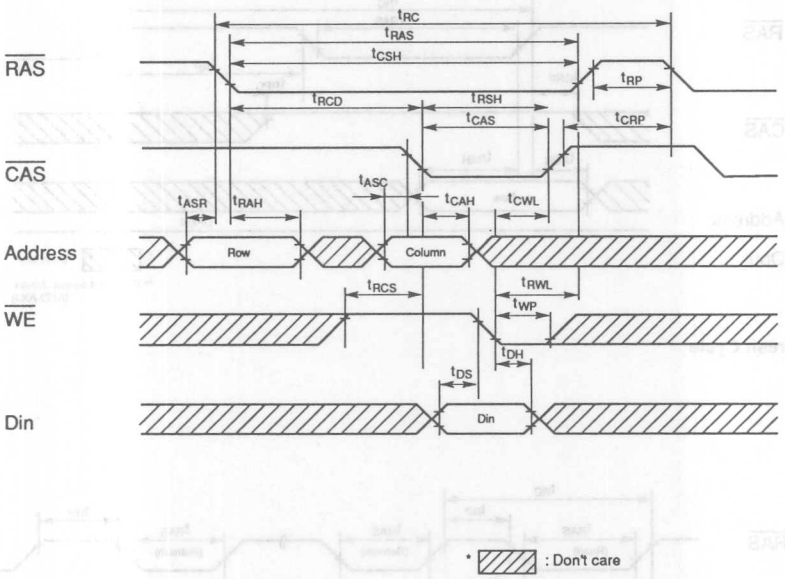
• Early Write Cycle



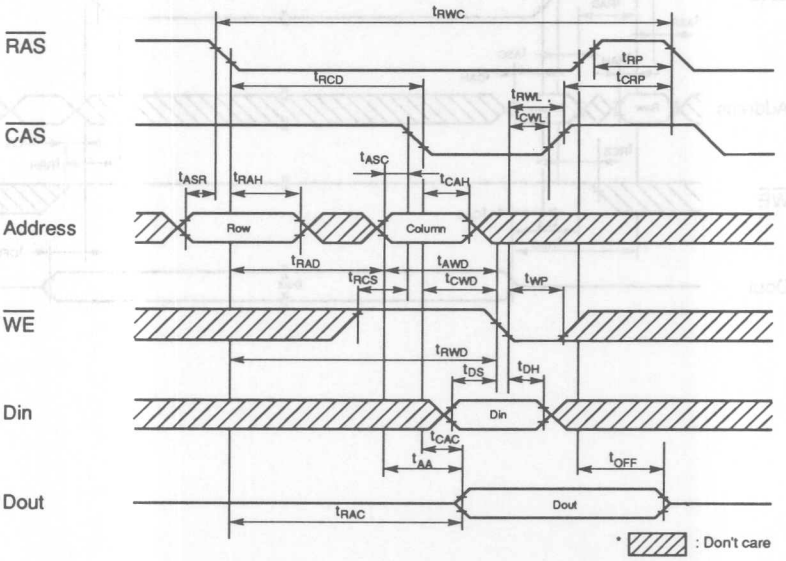
* : Don't care

** twcs ≥ twcs (min)

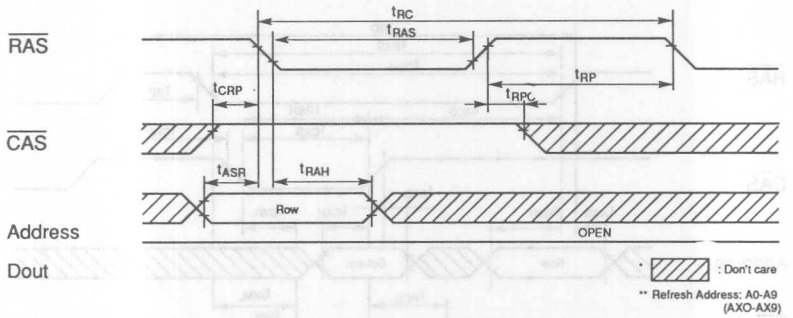
• **Delayed Write Cycle**



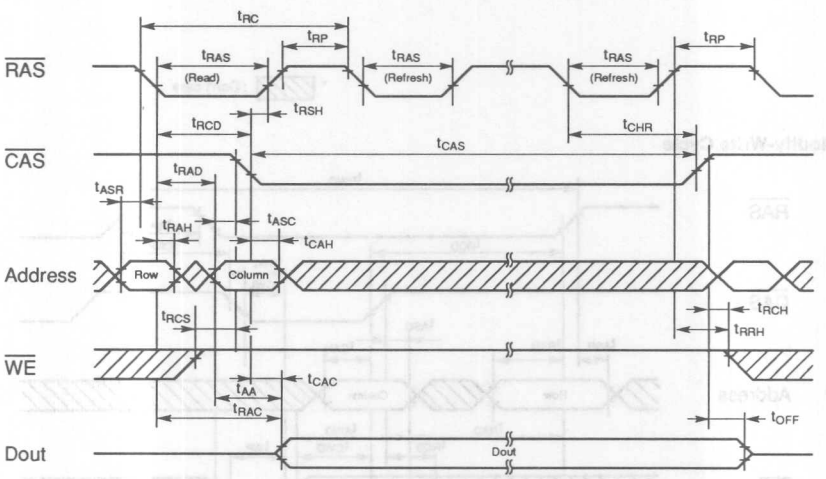
• **Read-Modify-Write Cycle**



• **$\overline{RAS}$ Only Refresh Cycle**

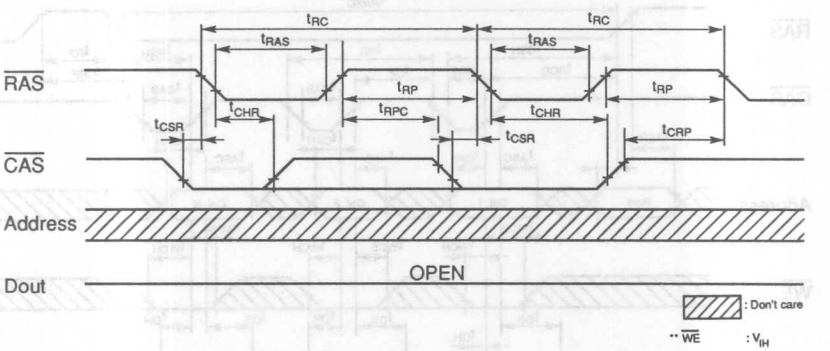


• **Hidden Refresh Cycle**

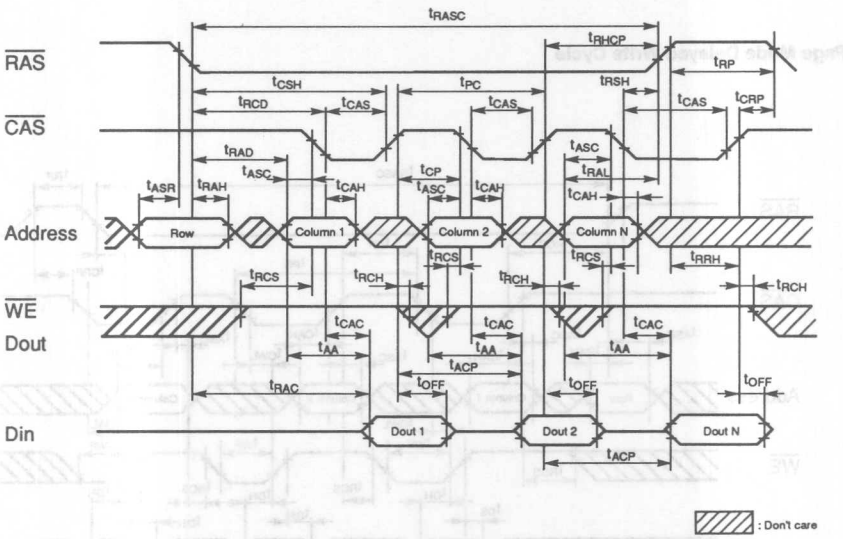


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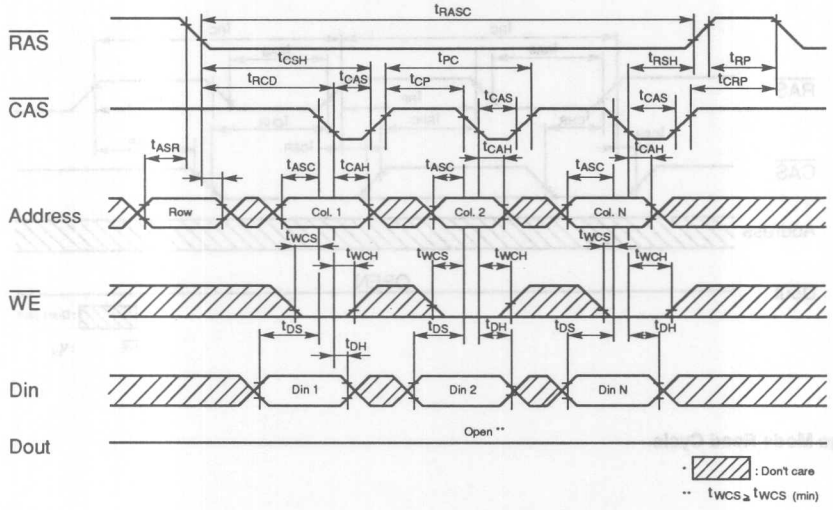
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



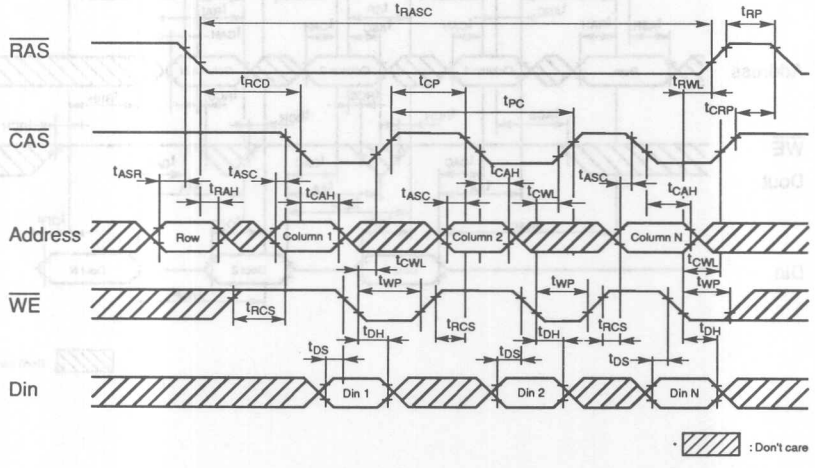
• **Fast Page Mode Read Cycle**



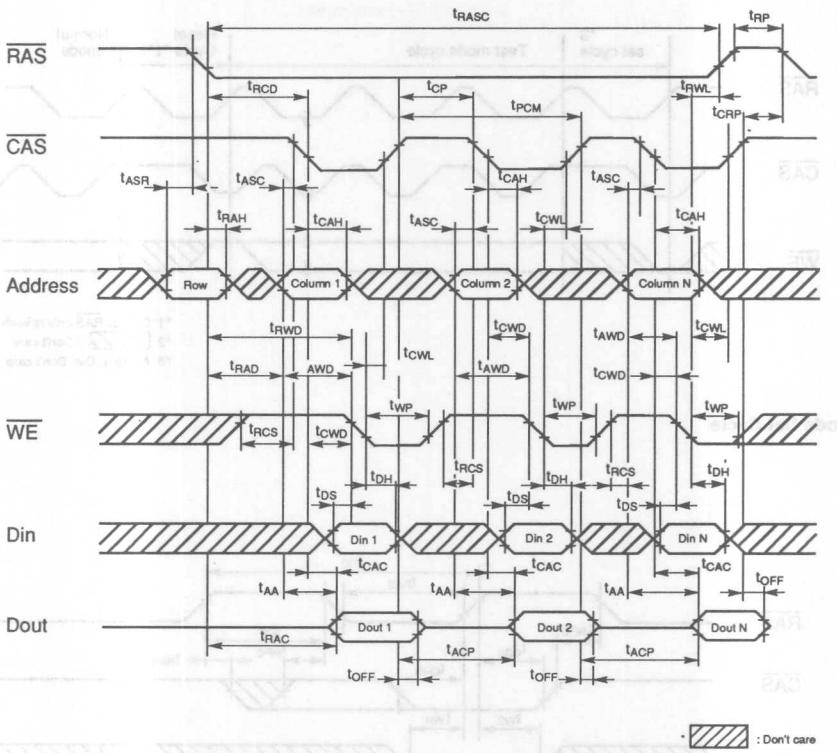
• **Fast Page Mode Early Write Cycle**



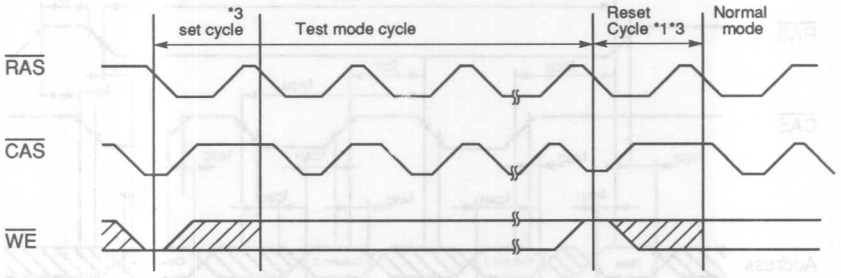
• **Fast Page Mode Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**

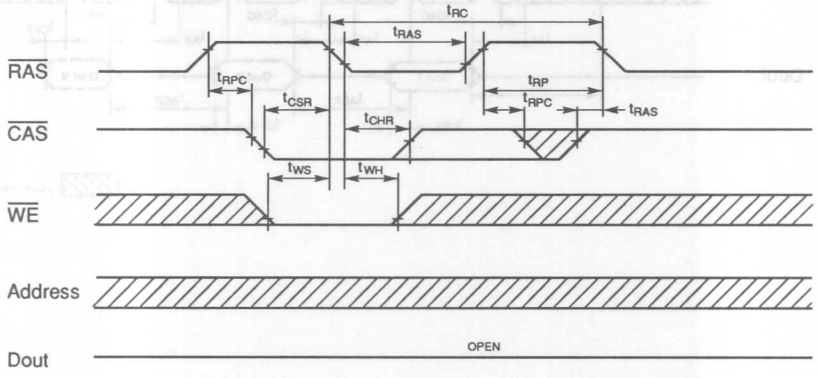


■ TEST MODE CYCLE



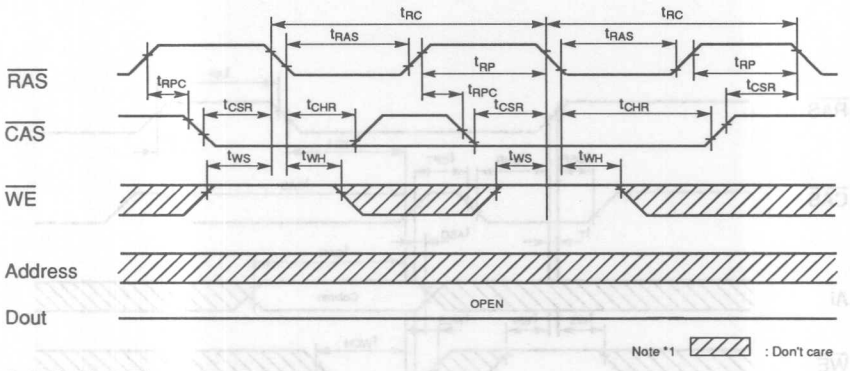
*1 $\overline{CBR}$ or $\overline{RAS}$ only refresh
*2 ▨ : Don't care
*3 Address, Din: Don't care

• **Test Mode Set Cycle**

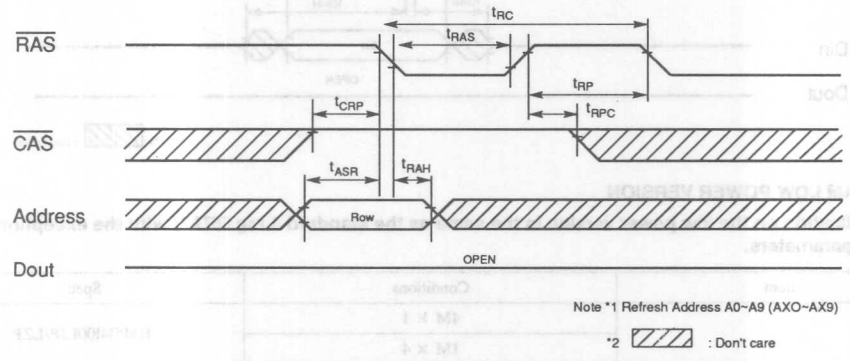


Note *1 ▨ : Don't care

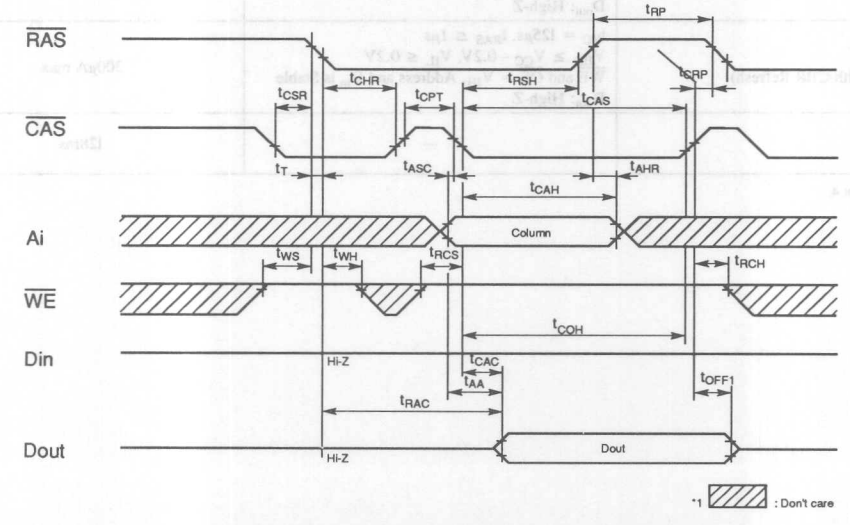
- **Test Mode Reset Cycle**
  - **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



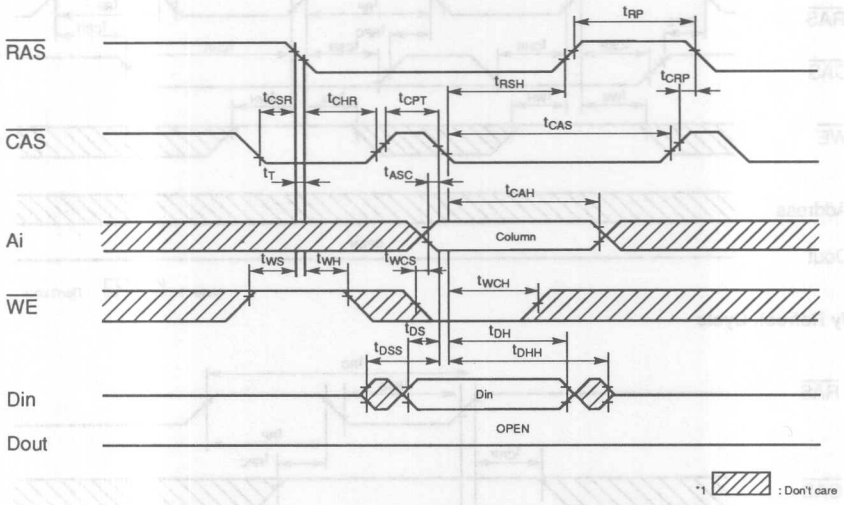
- **$\overline{RAS}$ Only Refresh Cycle**



- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)**



• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)**



■ 4M DRAM LOW POWER VERSION

The specification on the low power version is the same as the standard 4 mg DRAM with the exception of the following parameters.

Item	Conditions	Spec.
Type No.	4M × 1	HM514100LJP/LZP
	1M × 4	
Temperature	—	0–55°C
I_{CC2} (Standby CMOS Interface)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} – 0.2V Other Pin ≥ V_{CC} – 0.2V or ≤ 0.2V (Address and D_{IN} is Stable) D_{out}: High-Z	200μA max
I_{CC10} (Standby with CBR Refresh)	t_{RC} = 125μs, t_{RAS} ≤ 1μs V_{IL1} ≥ V_{CC} – 0.2V, V_{IL} ≤ 0.2V $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in} is Stable D_{out}: High-Z	300μA max
Refresh t_{REF}	—	128ms

*only for 1M × 4.

HM514100LJP/LZP-8/10/12 Low Power Version

4,194,304-Word × 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word × 1 bit. HM514100 has realized high density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (± 10%)
- High Speed
  - Access Time. . . . . .80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .495/440/385mW (max.)
  - Standby Mode . . . . . .11mW (max.)
- Fast Page Mode Capability
- 1,024 Refresh Cycles . . . . . .(16ms)
- 3 Variations of Refresh
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Back Up Operation

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514100LJP-8	80ns	350 mil 20 pin
HM514100LJP-10	100ns	Plastic SOJ
HM514100LJP-12	120ns	(CP-20D)
HM514100LZP-8	80ns	400 mil 20 pin
HM514100LZP-10	100ns	Plastic ZIP
HM514100LZP-12	120ns	(ZP-20)

■ PIN DESCRIPTION

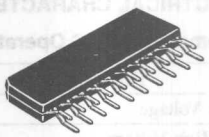
Pin Name	Function
$A_0 \sim A_{10}$	Address Input
$A_0 \sim A_9$	Refresh Address Input
D_{IN}	Data-In
D_{OUT}	Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

HM514100LJP Series



(CP-20D)

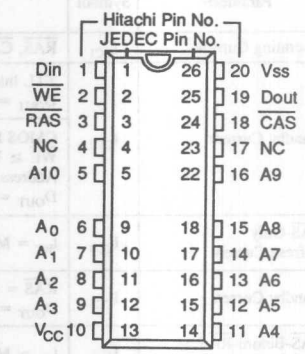
HM514100LZP Series



(ZP-20)

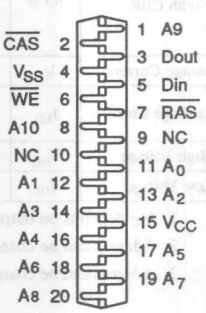
■ PIN OUT

HM514100LJP Series



(Top View)

HM514100LZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM514100-8		HM514100-10		HM514100-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	—	90	—	80	—	70	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ ≥ V_{CC} −0.2V or ≤ 0.2V, Address and D_{in}: Stable, D_{OUT} = High-Z	—	200	—	200	—	200	μA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	90	—	80	—	70	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	90	—	80	—	70	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	90	—	80	—	70	mA	1, 3
Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V, $\overline{WE}$ = V_{IH}, Address and D_{in}: Stable, D_{out} = High-Z	—	300	—	300	—	300	μA	
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address, Data-In)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-Out)	C_O	—	7	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (1), (12), (15)

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	128	—	128	—	128	ns	

• Read Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• **Write Cycle**

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

• **Read-Modify-Write Cycle**

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

• **Refresh Cycle**

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• **Fast Page Mode Cycle**

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

• **Fast Page Mode Read-Modify-Write Cycle**

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	—	85	—	100	—	ns	

• Test Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

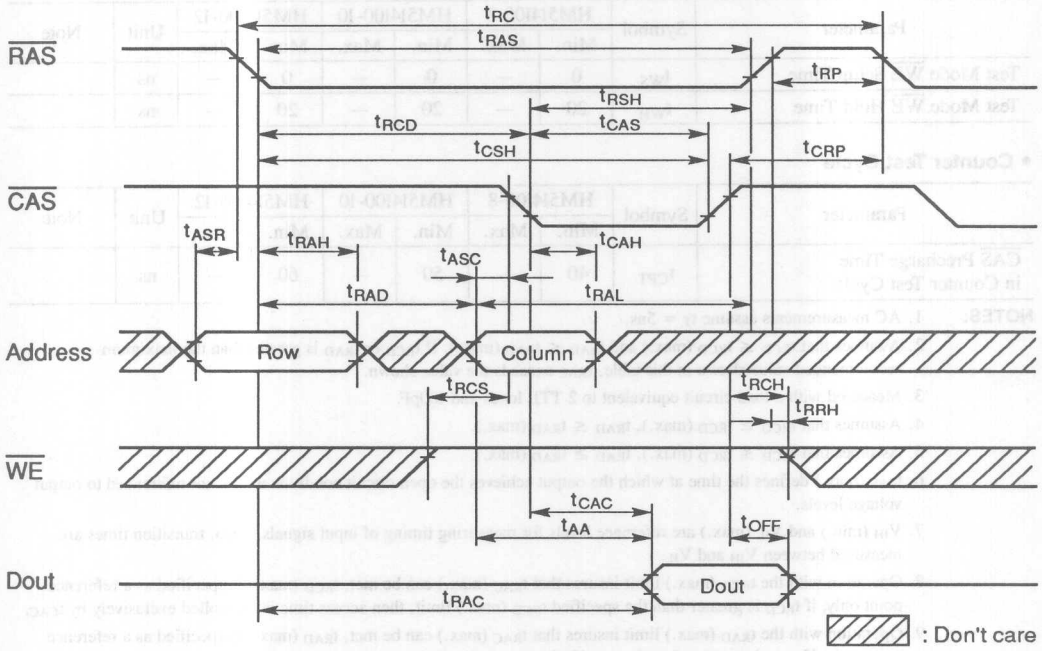
• Counter Test Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

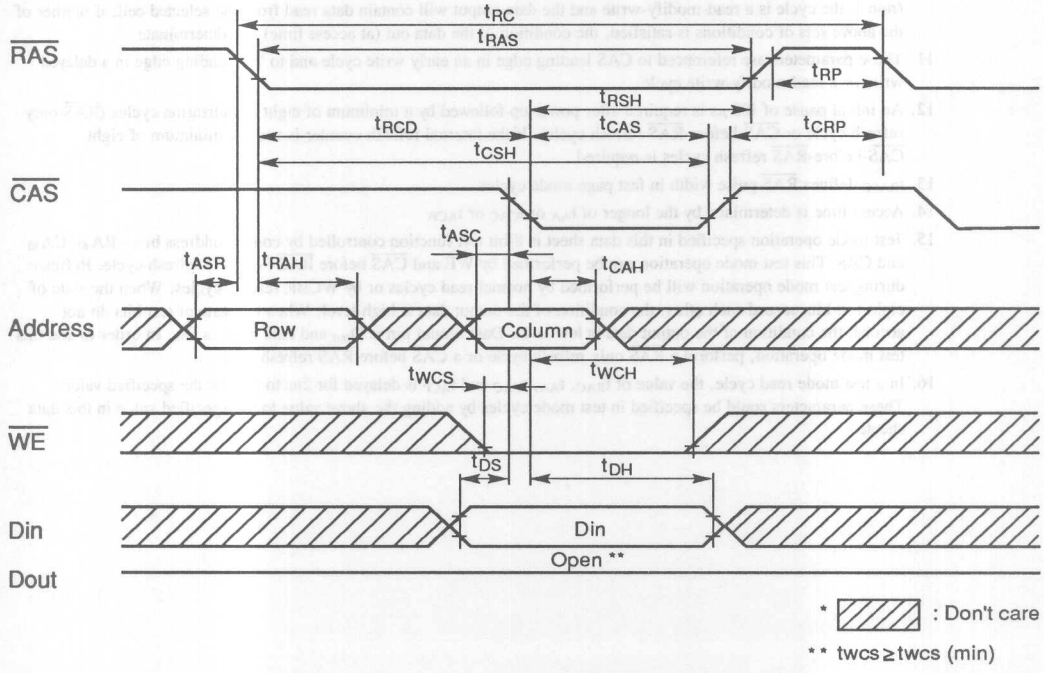
NOTES:

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA_{10}, CA_{10} and CA_0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters sould be specified in test mode cycles by adding the above value to the specified value in this data sheet.

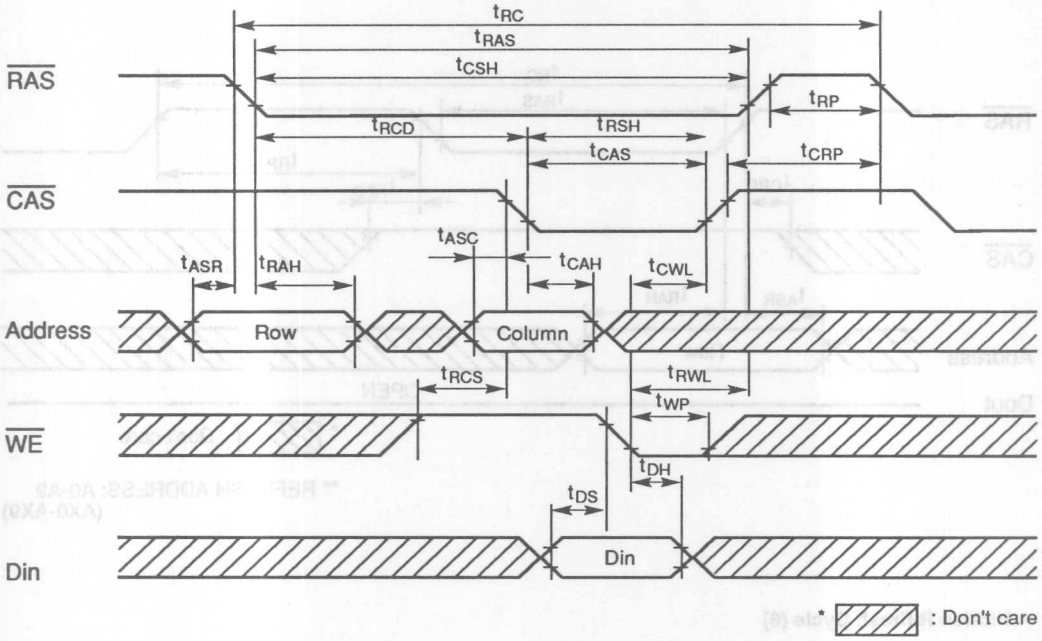
• **Read Cycle (1)**



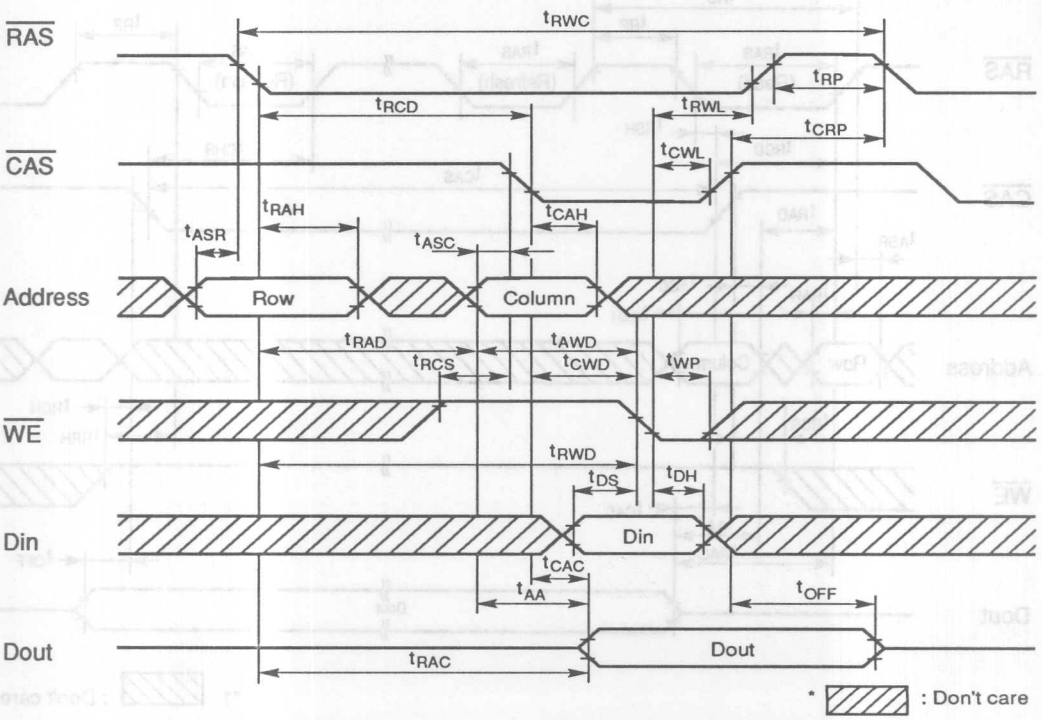
• **Early Write Cycle (2)**



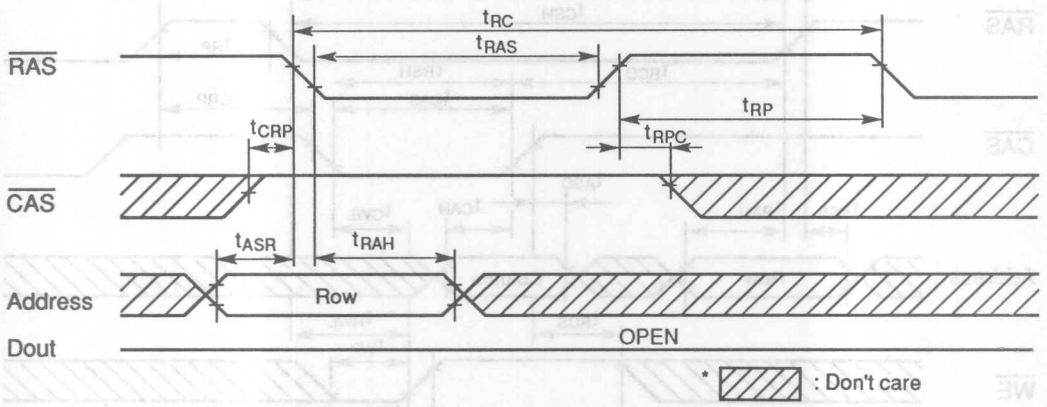
• **Delayed Write Cycle (3)**



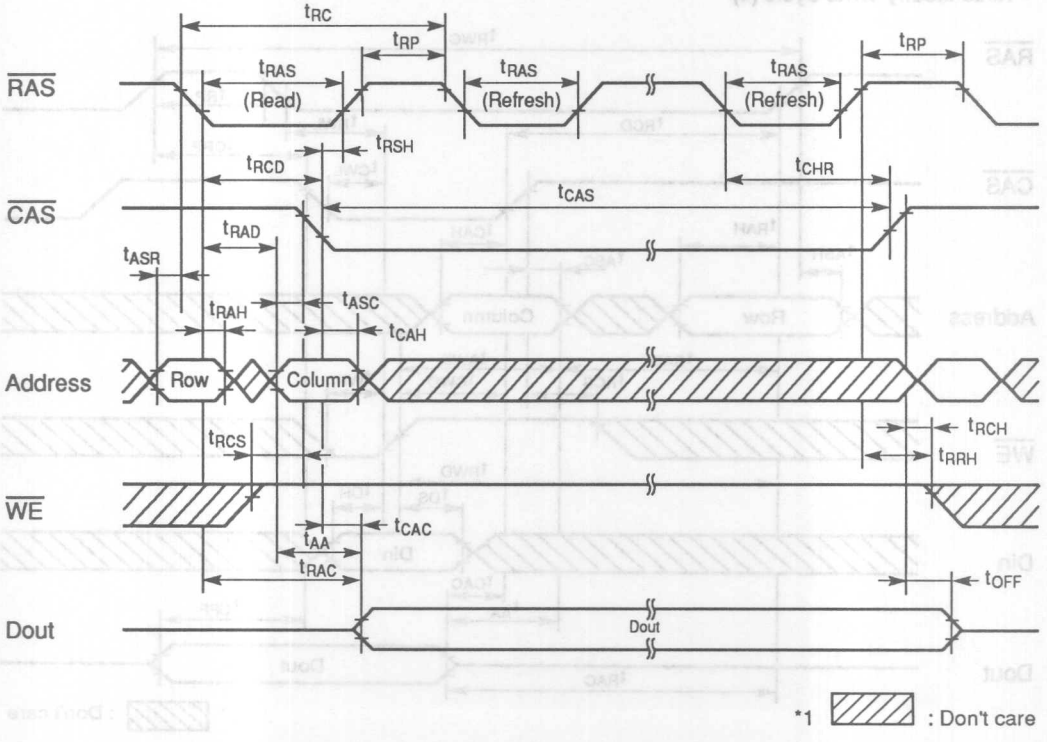
• **Read-Modify-Write Cycle (4)**



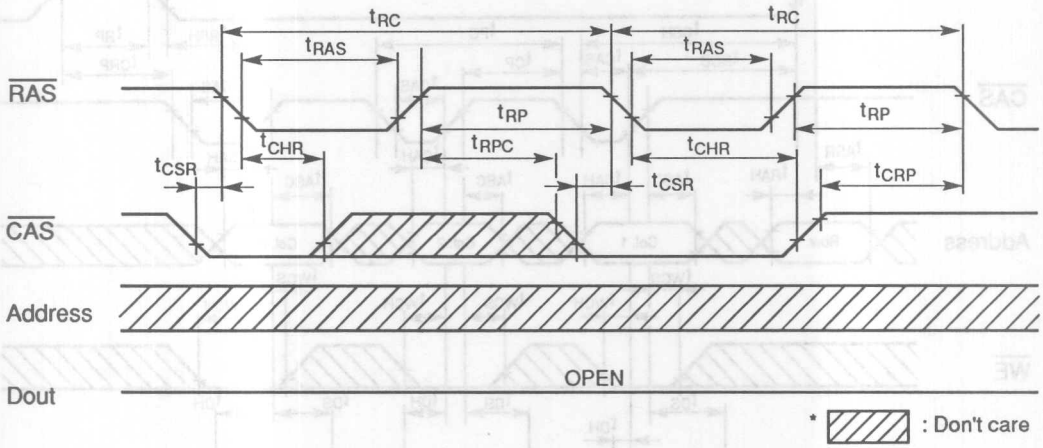
• $\overline{RAS}$-Only Refresh Cycle (5)



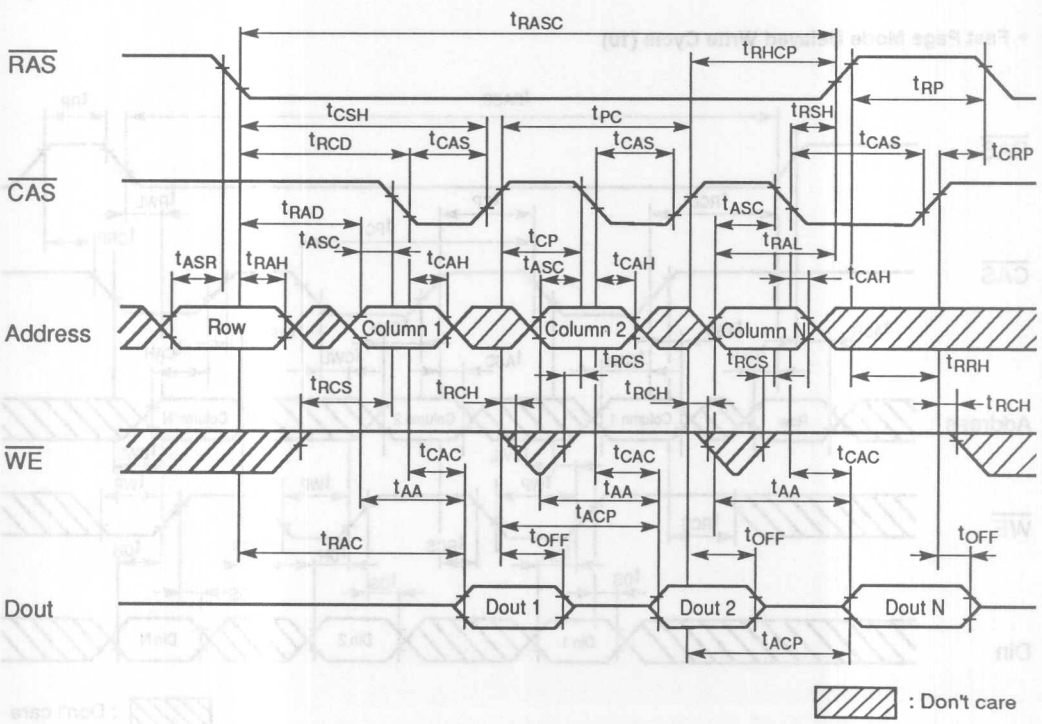
• Hidden Refresh Cycle (6)



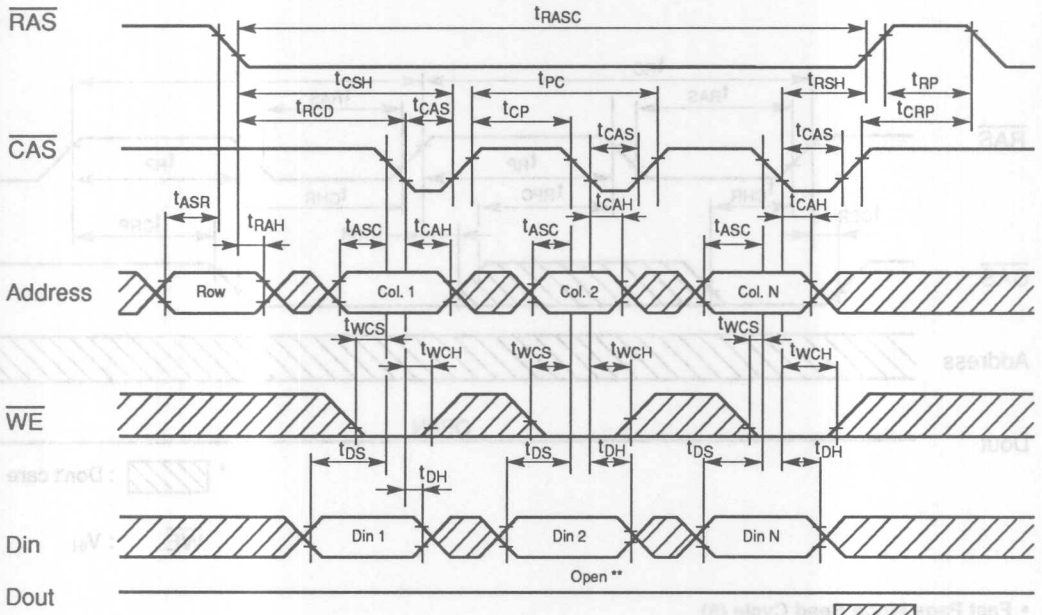
• **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (7)**



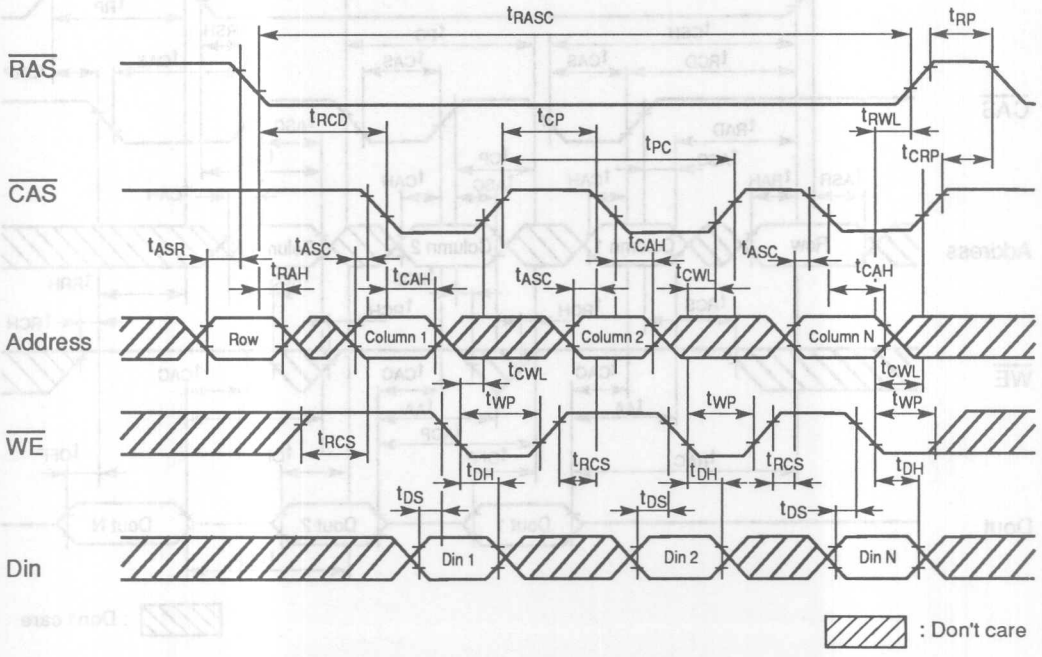
• **Fast Page Mode Read Cycle (8)**



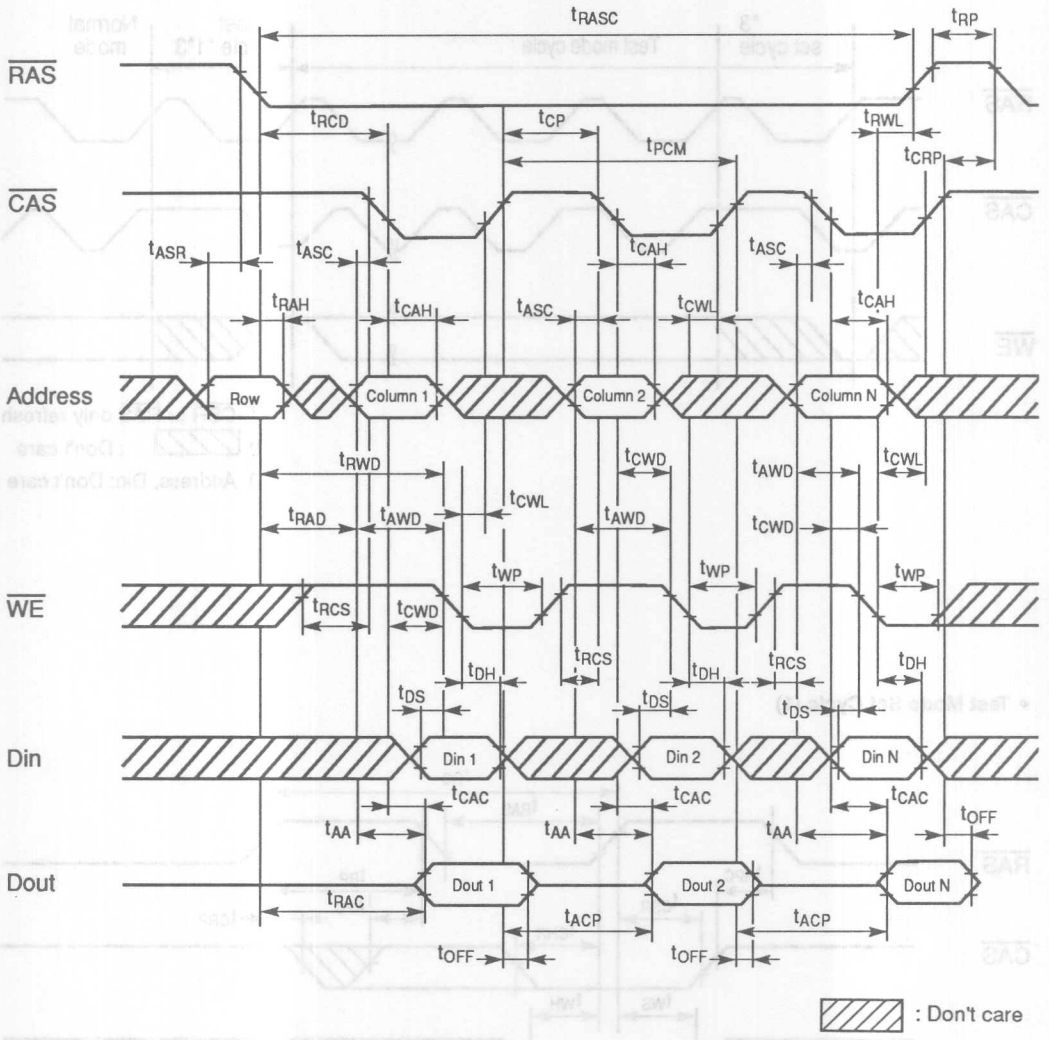
• **Fast Page Mode Early Write Cycle (9)**



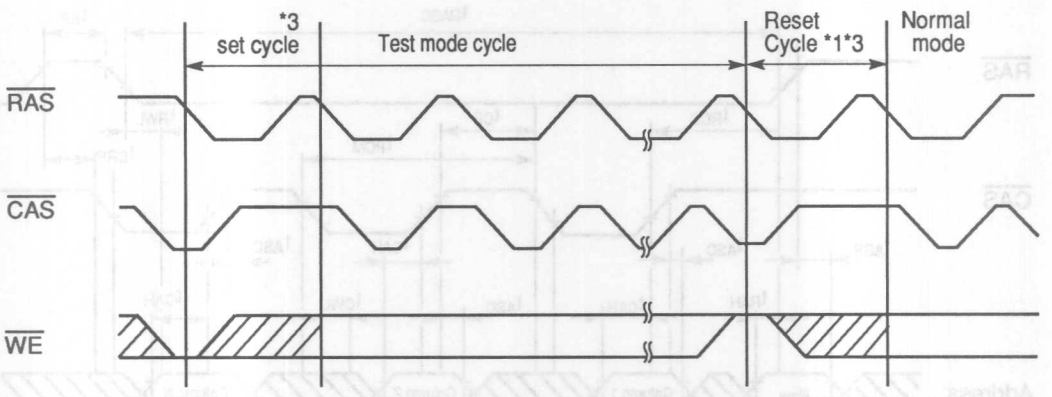
• **Fast Page Mode Delayed Write Cycle (10)**



• **Fast Page Mode Read-Modify-Write Cycle (11)**

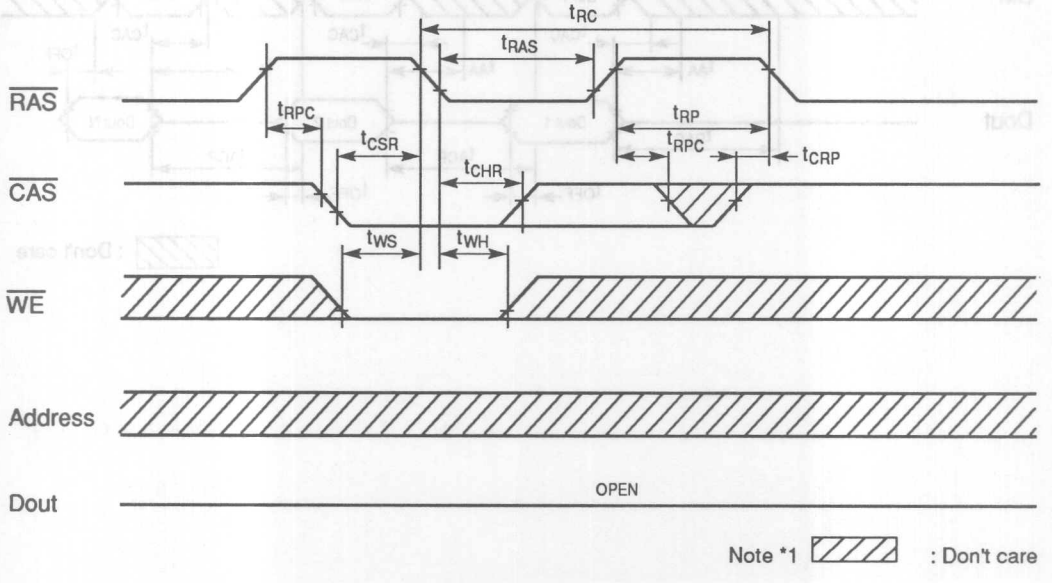


• **Test Mode Cycle**



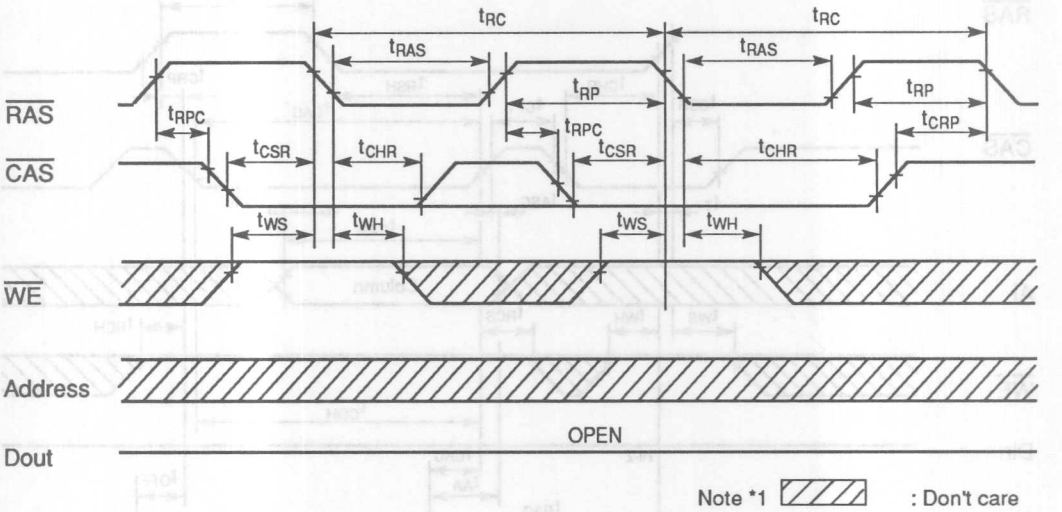
*1 $\overline{CBR}$ or $\overline{RAS}$ only refresh
*2 ▨ : Don't care
*3 Address, Din: Don't care

• **Test Mode Set Cycle (1)**

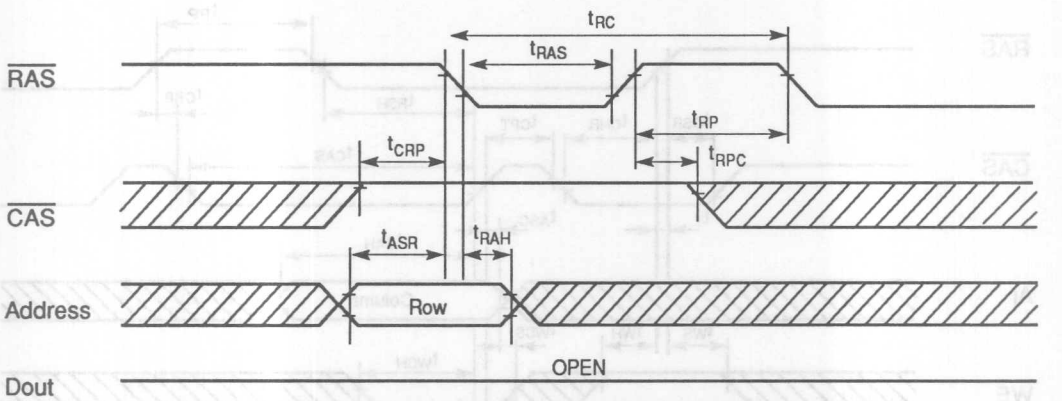


Note *1 ▨ : Don't care

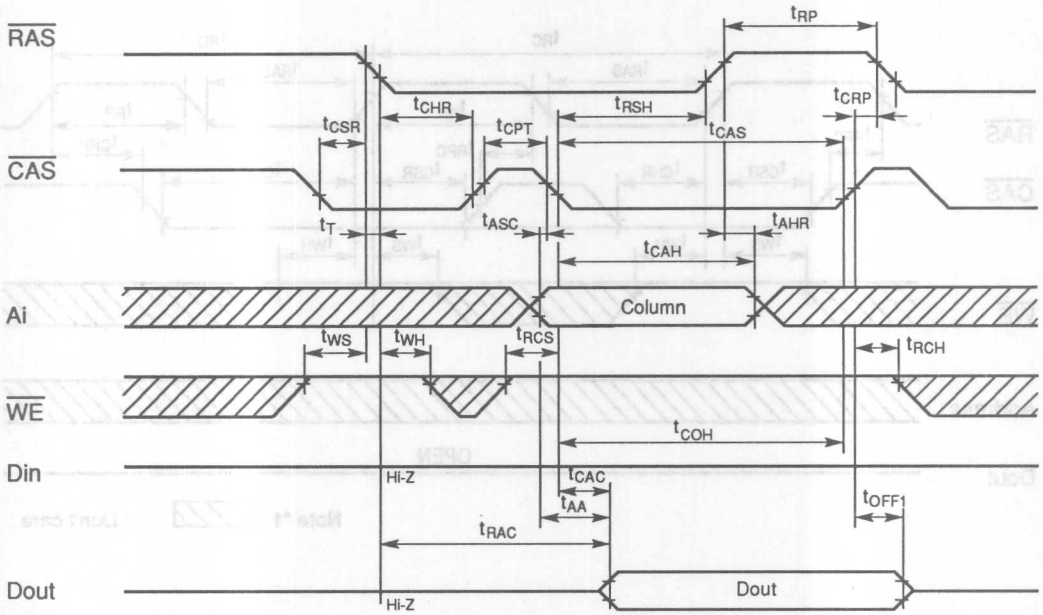
• **Test Mode Reset Cycle (2)**



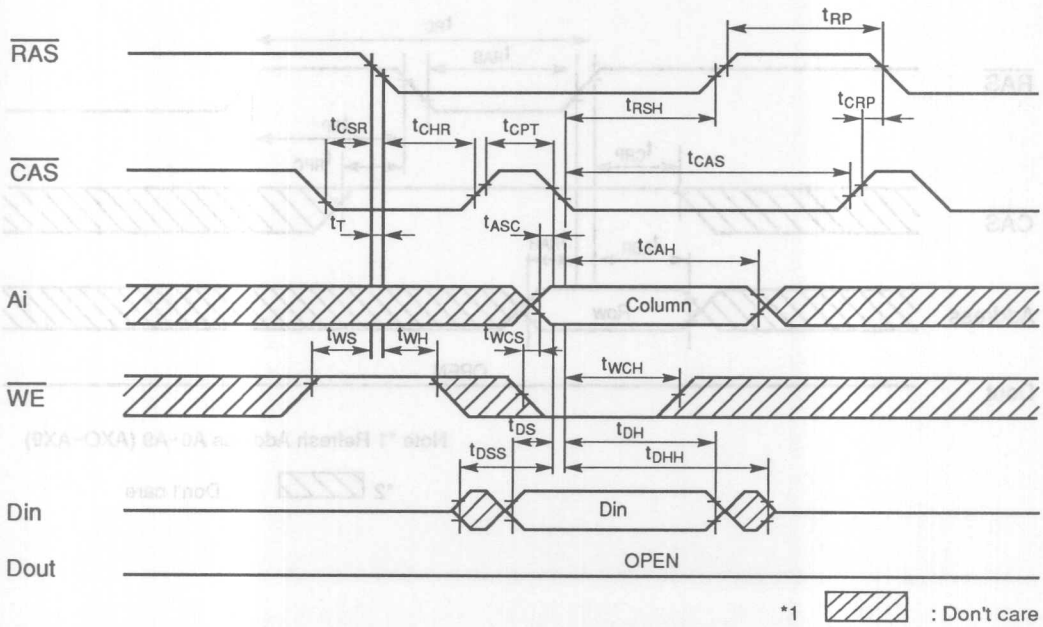
• **$\overline{\text{RAS}}$-Only Refresh Cycle**



• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



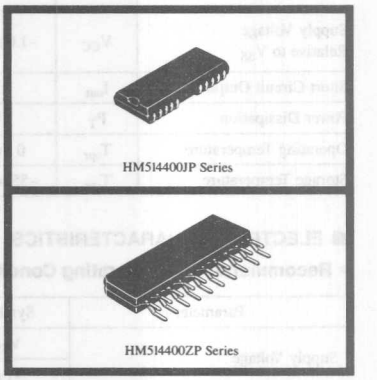
HM514400JP/ZP-8/10/12
4 Megabit DRAM

1,048,576-Word × 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word × 4 bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.



■ FEATURES

- Single 5V (± 10%)
- High Speed
  Access time. . . . . .80ns/100ns/120ns (max.)
- Low power dissipation
  —Active mode . . . . . .495mW/440mW/385mW (max.)
  —Standby mode . . . . . .11mW (max.)
- Fast page mode capability
- 1,024 refresh cycles. . . . . .(16 ms)
- 3 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
  —Hidden Refresh
- Test Function

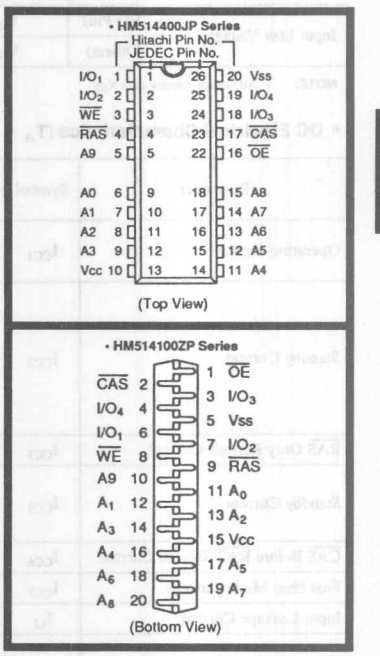
■ ORDERING INFORMATION

Part No.	Access	Package
HM514400JP-8	80ns	350 mil 20-pin Plastic SOJ
HM514400JP-10	100ns	
HM514400JP-12	120ns	
HM514400ZP-8	80ns	400 mil 20-pin Plastic ZIP
HM514400ZP-10	100ns	
HM514400ZP-12	120ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
I/O_1–I/O_4	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• **AC Characteristics** (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) [1, 14, 15, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Set-up Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

■ READ CYCLE

Parameter	Symbol	HM514400-8		HM514400-10		HM51400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16
Access Time From $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

■ WRITE CYCLE

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

■ READ-MODIFY-WRITE CYCLE

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Modify-Write Cycle Time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

■ REFRESH CYCLE

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

■ FAST PAGE MODE CYCLE

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13, 17
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	105	—	110	—	130	—	ns	

■ TEST MODE CYCLE

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode $\overline{WE}$ Set-up Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

■ COUNTER TEST CYCLE

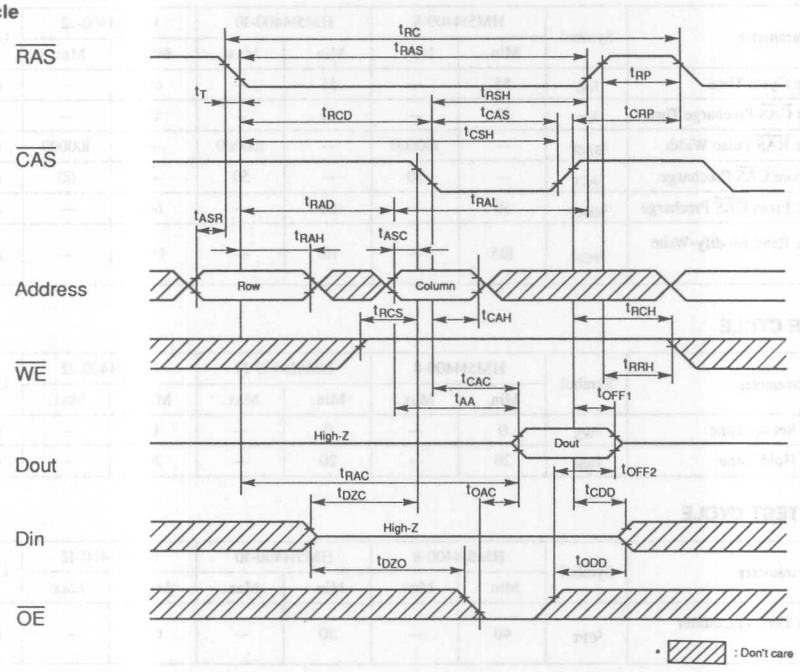
Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

NOTES:

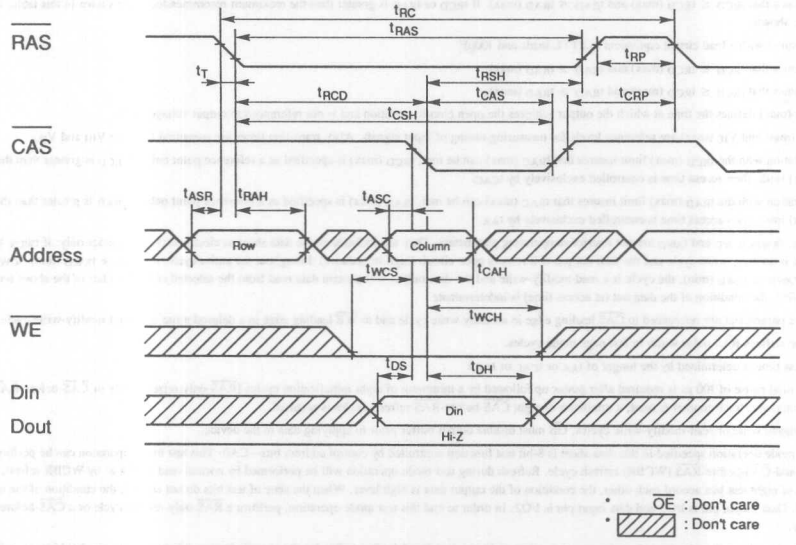
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O3 and data input pin is I/O2. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORM

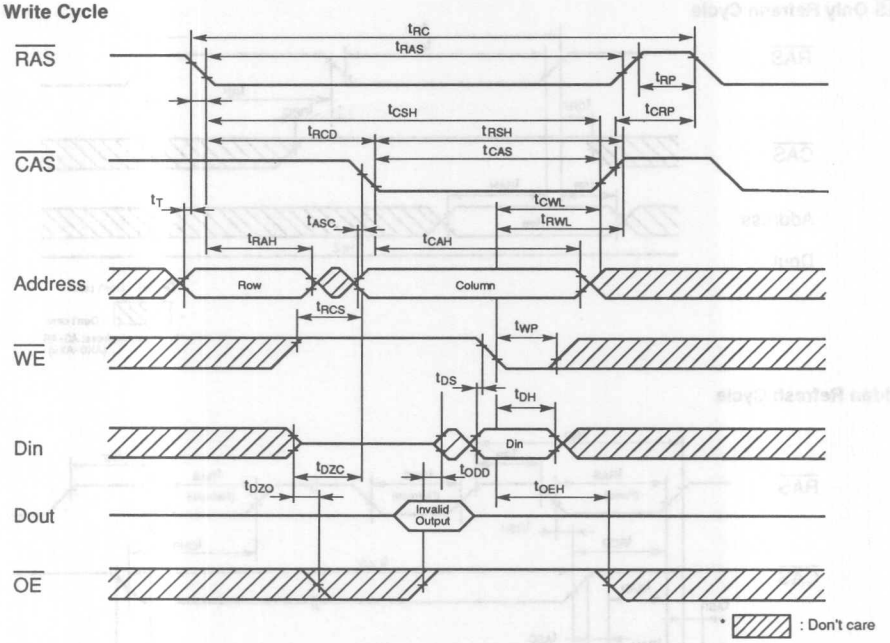
• Read Cycle



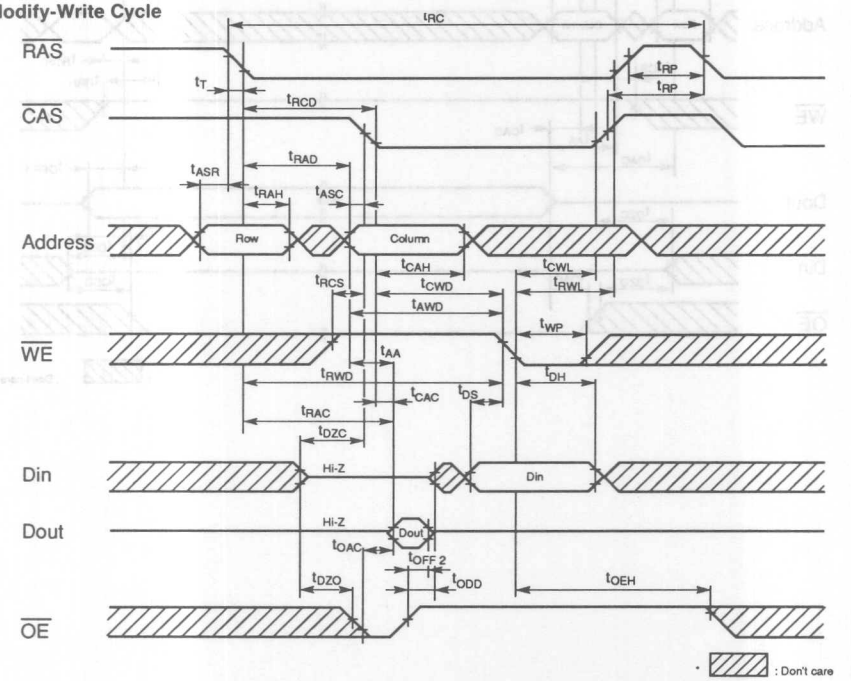
• Early Write Cycle



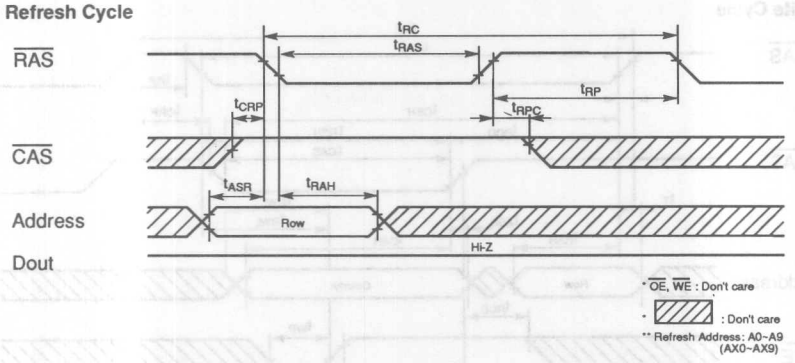
• **Delayed Write Cycle**



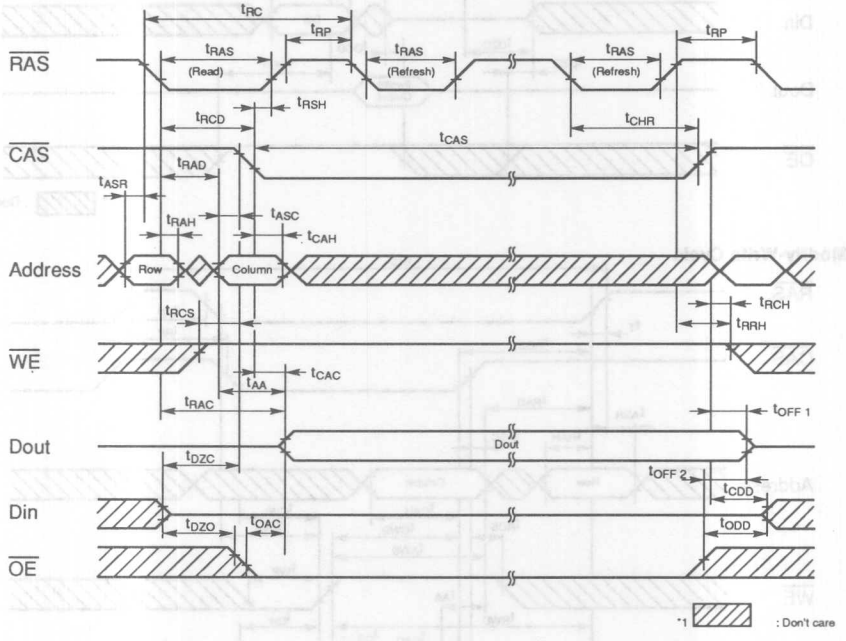
• **Read-Modify-Write Cycle**



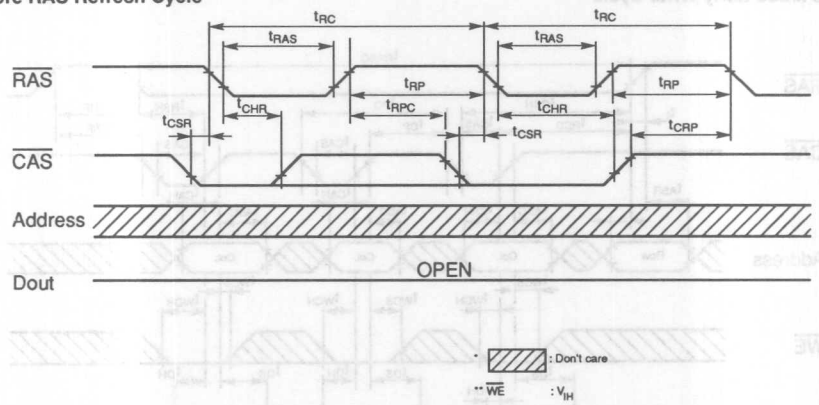
• **$\overline{RAS}$ Only Refresh Cycle**



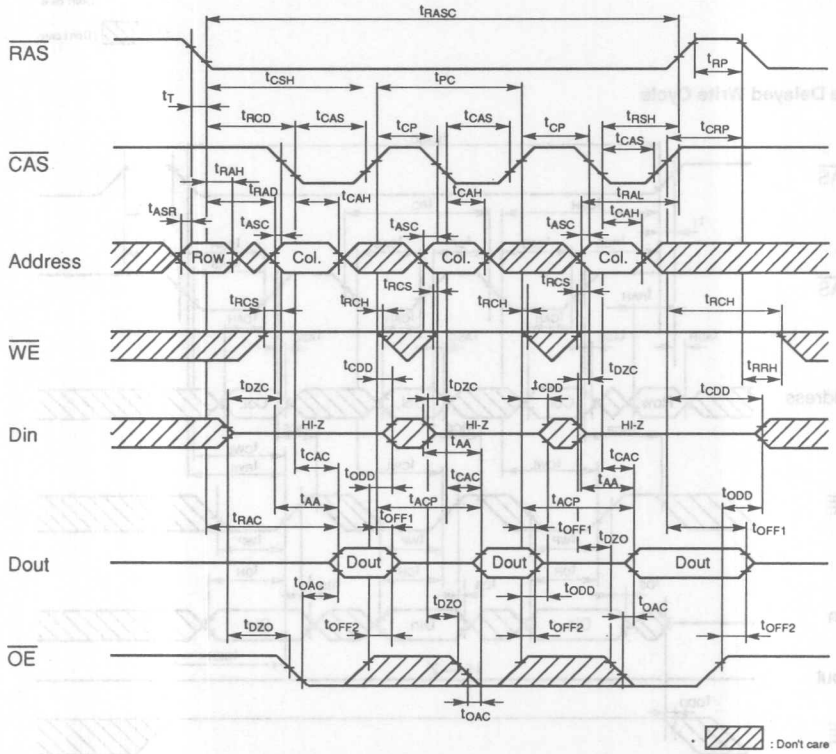
• **Hidden Refresh Cycle**



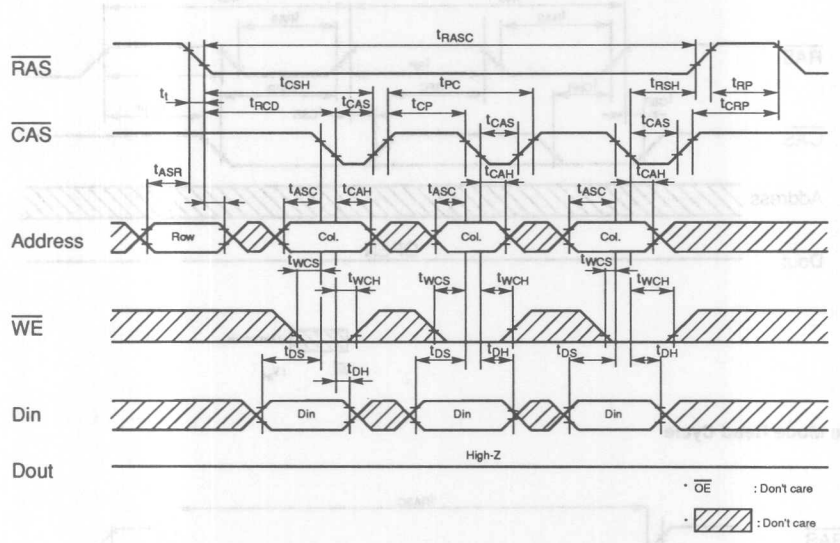
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



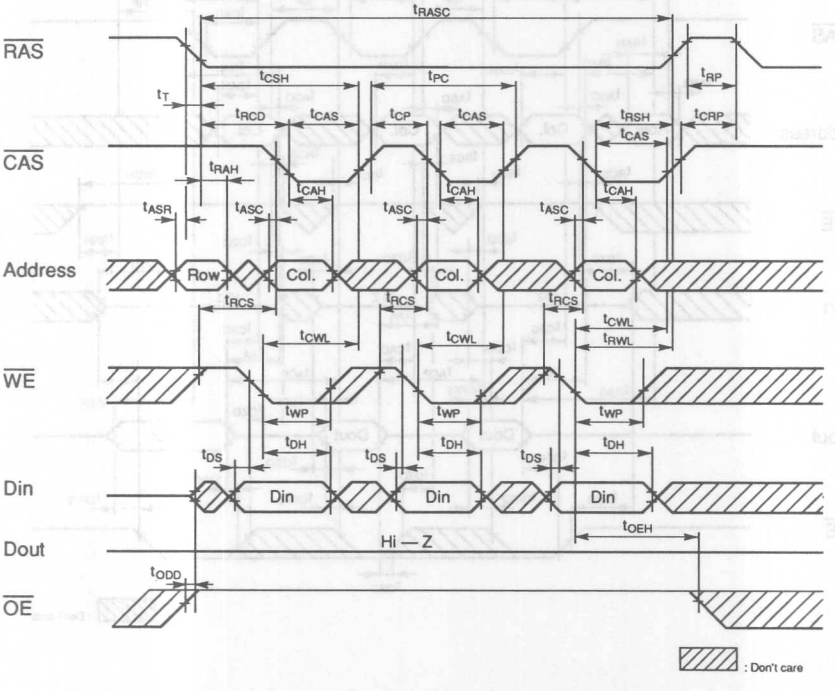
• **Fast Page Mode Read Cycle**



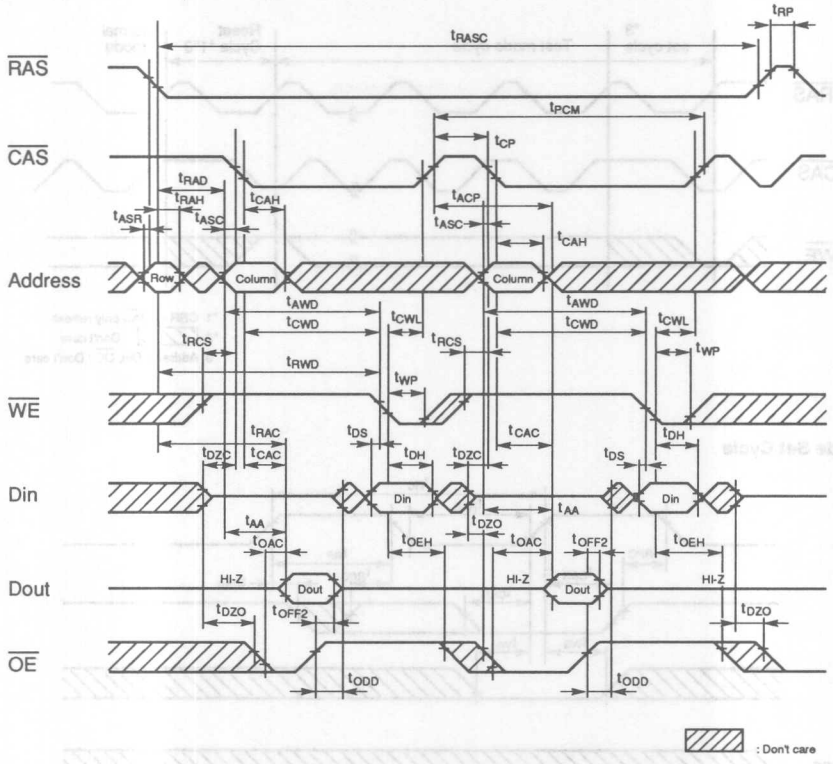
• **Fast Page Mode Early Write Cycle**



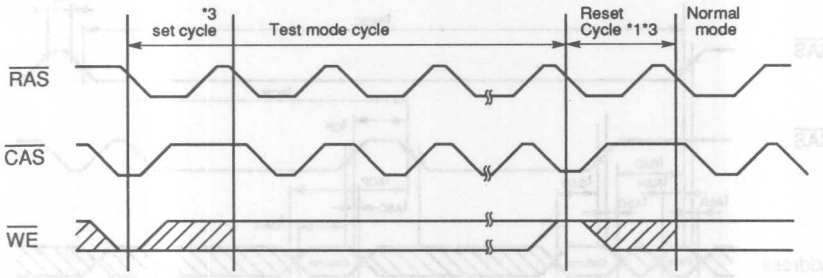
• **Fast Page Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**

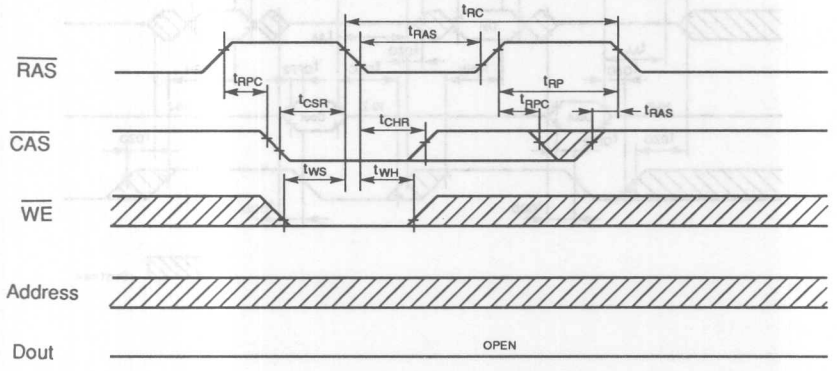


• **Test Mode Cycle**



*1 CBR or RAS only refresh
*2 ▨ : Don't care
*3 Address, Din, OE : Don't care

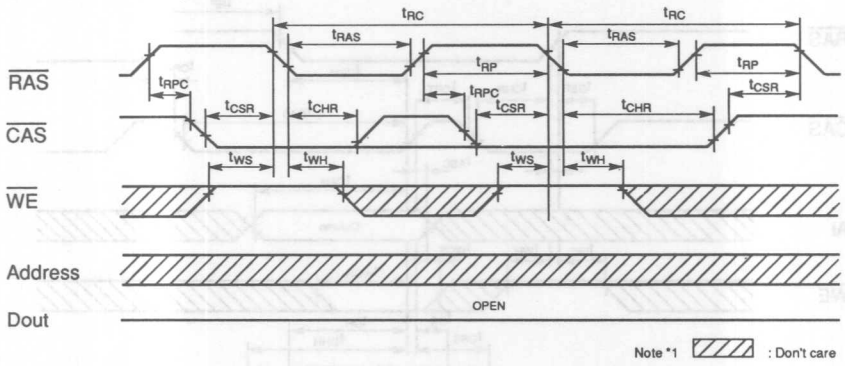
• **Test Mode Set Cycle**



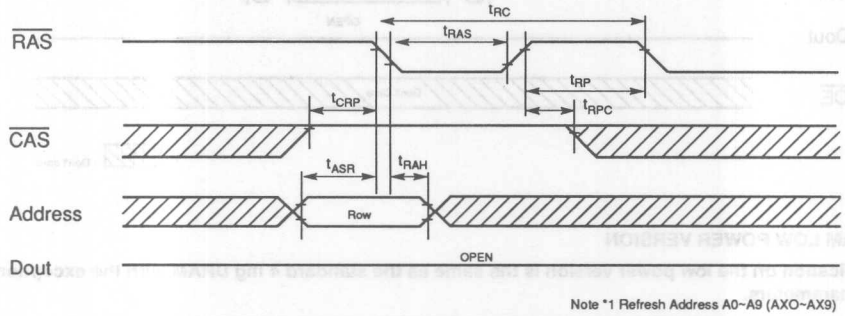
Note *1 ▨ : Don't care

- **Test Mode Reset Cycle**

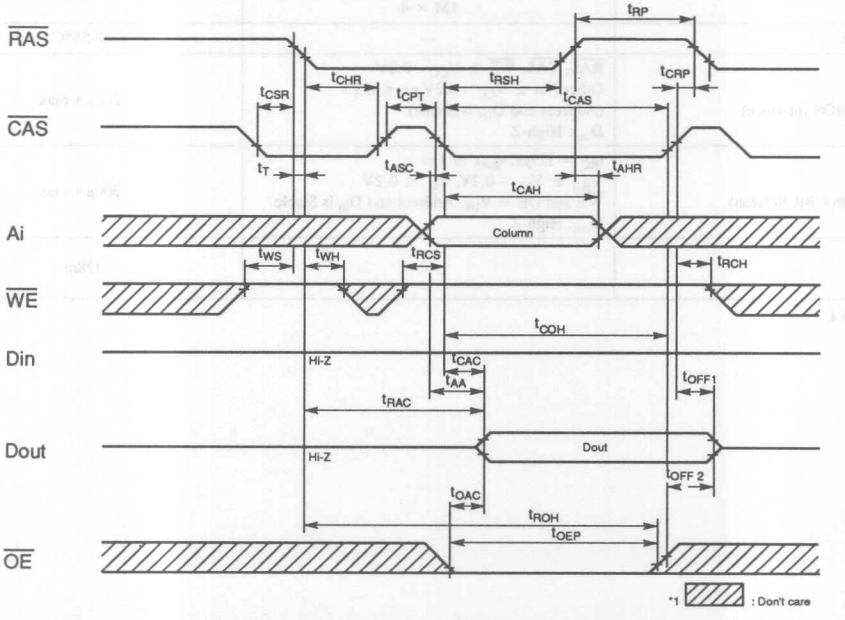
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



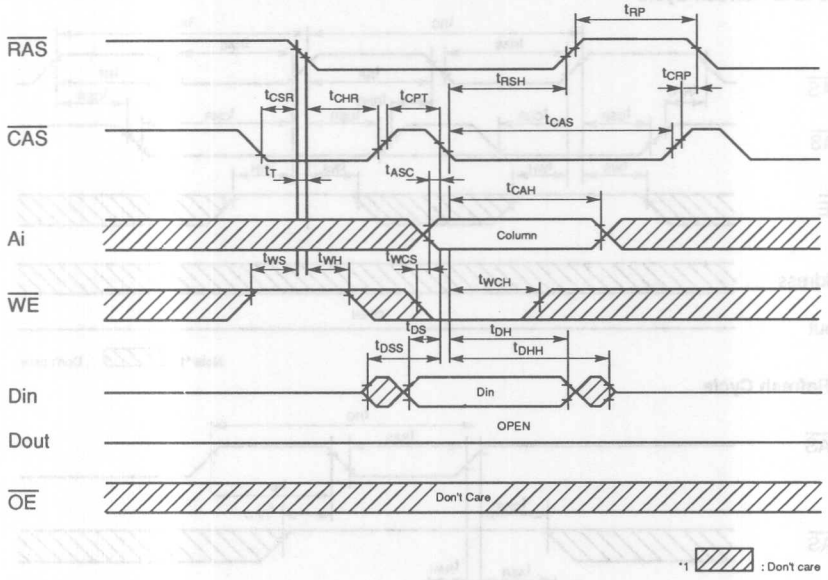
- **$\overline{RAS}$ Only Refresh Cycle**



- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)**



• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)**



■ 4M DRAM LOW POWER VERSION

The specification on the low power version is the same as the standard 4 mg DRAM with the exception of the following parameters.

Item	Conditions	Spec.
Type No.	4M × 1 1M × 4	HM514100LJP/LZP
Temperature	—	0–55°C
I_{CC2} (Standby CMOS Interface)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} – 0.2V Other Pin ≥ V_{CC} – 0.2V or ≤ 0.2V (Address and D_{IN} is Stable) D_{out}: High-Z	200μA max
I_{CC10} (Standby with CBR Refresh)	t_{RC} = 125μs, t_{RAS} ≤ 1μs V_{IL1} ≥ V_{CC} – 0.2V, V_{IL} ≤ 0.2V $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in} is Stable D_{out}: High-Z	300μA max
Refresh t_{REF}	—	128ms

*only for 1M × 4.

HM514410JP/ZP-8/10/12 — Preliminary

1,048,576-Word × 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514410 is a CMOS dynamic RAM organized 1,048,576 word × 4 bit. HM514410 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514410 offers Fast Page Mode as a high speed access mode.

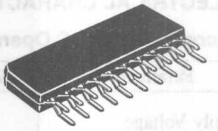
Multiplexed address input permits the HM514410 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514410JP Series



(CP-20D)

HM514410ZP Series



(ZP-20)

■ FEATURES

- Single 5V (± 10%)
- High Speed
  - Access Time. . . . . .80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .495/440/385mW (max.)
  - Standby Mode . . . . . .11mW (max.)
- Fast Page Mode Capability
- 1,024 Refresh Cycles . . . . . .(16ms)
- 3 Variations of Refresh
  - $\overline{\text{RAS}}$-Only Refresh
  - $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh
  - Hidden Refresh
- Test Function
- Write Per Bit Capability

■ ORDERING INFORMATION

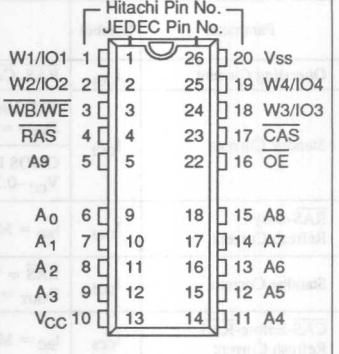
Part No.	Access Time	Package
HM514410JP-8	80ns	350 mil 20 pin
HM514410JP-10	100ns	Plastic SOJ
HM514410JP-12	120ns	(CP-20D)
HM514410ZP-8	80ns	400 mil 20 pin
HM514410ZP-10	100ns	Plastic ZIP
HM514410ZP-12	120ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_9$	Address Input
$A_0 \sim A_9$	Refresh Address Input
W_1/IO_1–W_4/IO_4	Write Select/Data-In/Data-Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WB/WE}}$	Write Per Bit/Write Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

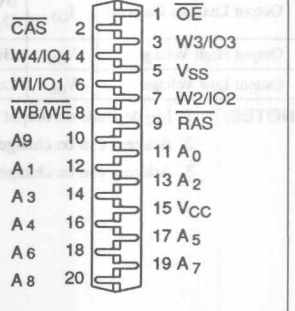
■ PIN OUT

HM514410JP Series



(Top View)

HM514410ZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM514410-8		HM514410-10		HM514410-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	—	90	—	80	—	70	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V, D_{OUT} = High-Z	—	1	—	1	—	1	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	90	—	80	—	70	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	90	—	80	—	70	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	90	—	80	—	70	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-In, Data-Out)	$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (1), (14), (15), (16)

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Set-up Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

• Read Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16, 17
Access Time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output Buffer Turn-Off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

• Write Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Modify-Write Cycle Time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

• Refresh Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Normal Mode)	t_{CPN}	10	—	10	—	15	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13, 17
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	105	—	110	—	130	—	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	80	—	85	—	100	—	ns	

• Test Mode Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

• Counter Test Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

• Write Per Bit (18), (19)

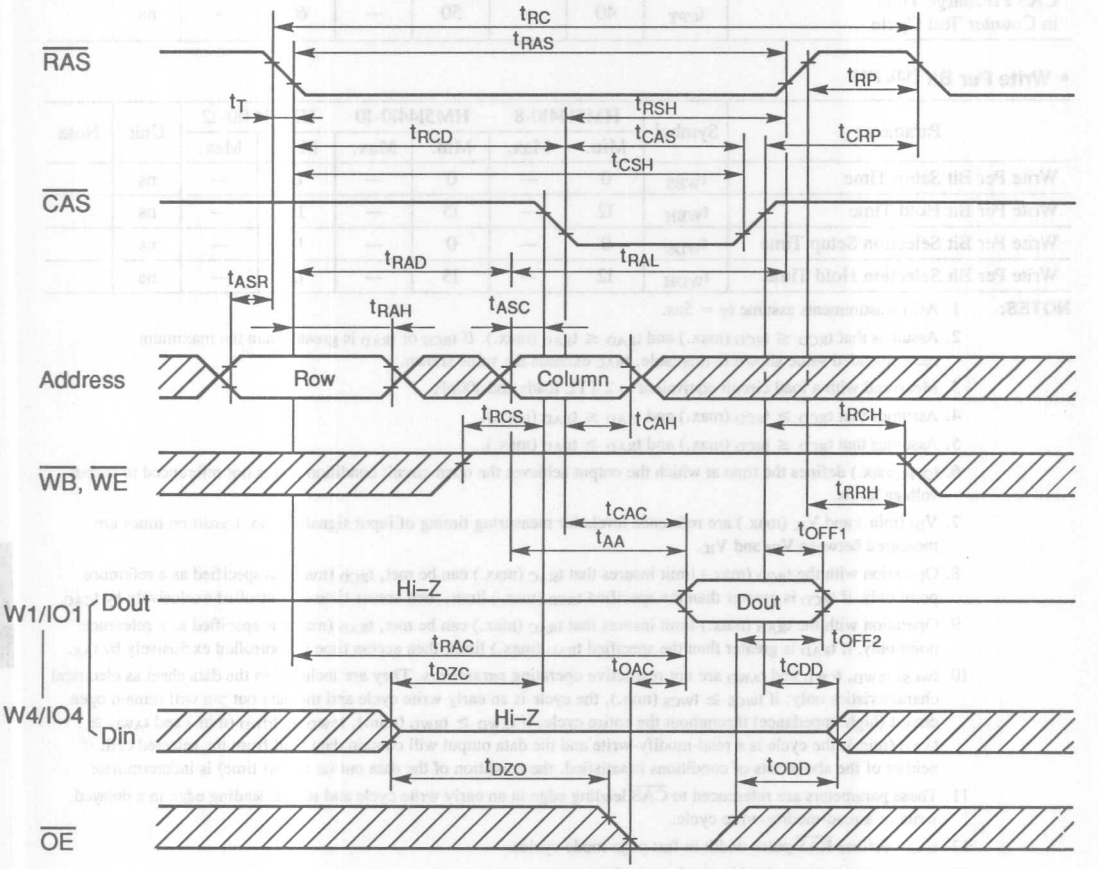
Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Per Bit Setup Time	t_{WBS}	0	—	0	—	0	—	ns	
Write Per Bit Hold Time	t_{WBH}	12	—	15	—	15	—	ns	
Write Per Bit Selection Setup Time	t_{WDS}	0	—	0	—	0	—	ns	
Write Per Bit Selection Hold Time	t_{WDH}	12	—	15	—	15	—	ns	

NOTES:

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle of $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—CAO. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
19. The data bits to which the write operation is applied can be specified by keeping $W1/IO_1$, $W2/IO_2$, $W3/IO_3$ and $W4/IO_4$ high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

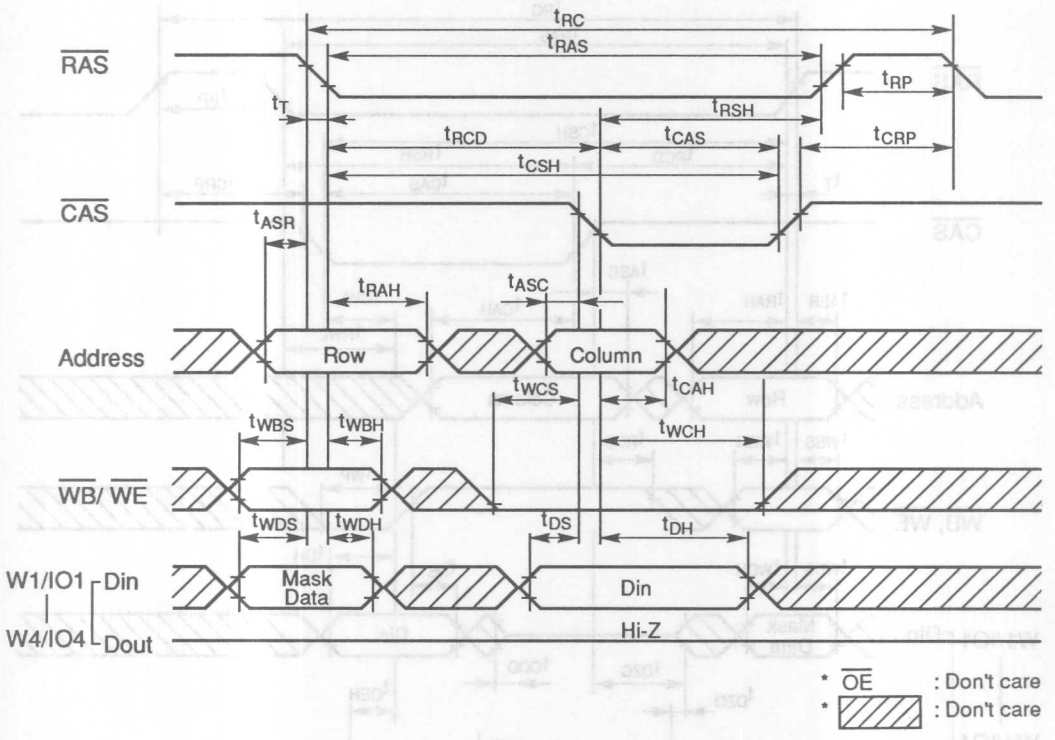
■ TIMING WAVEFORMS

• **Read Cycle (1)**

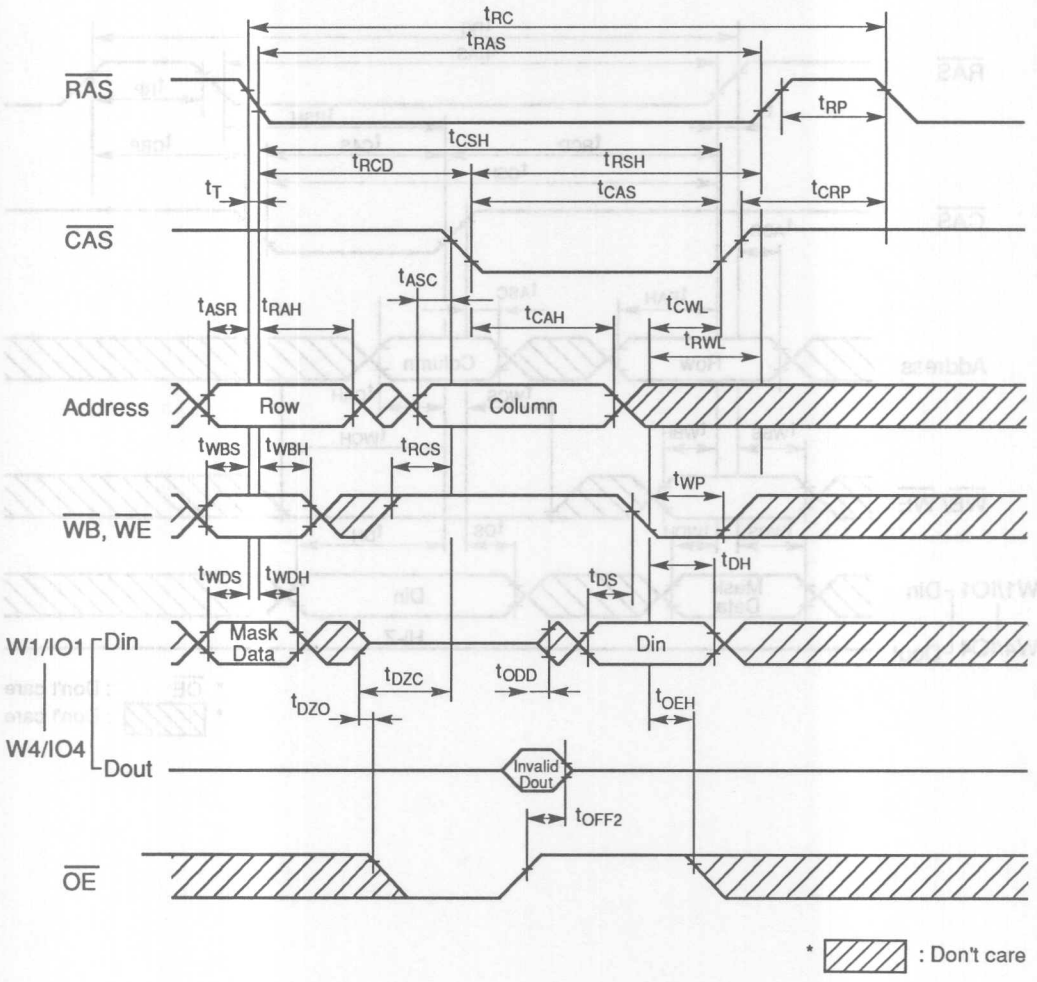


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• **Early Write Cycle (2)**

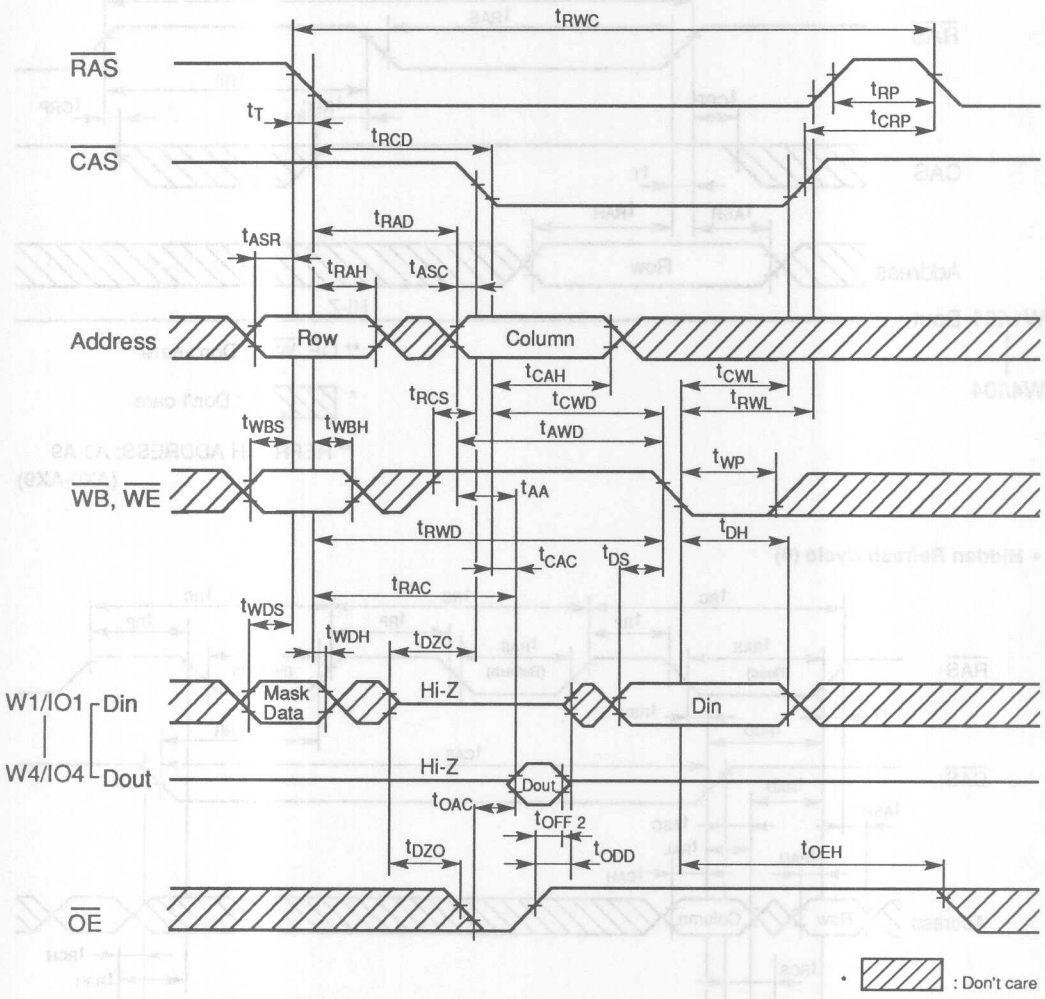


• **Delayed Write Cycle (3)**

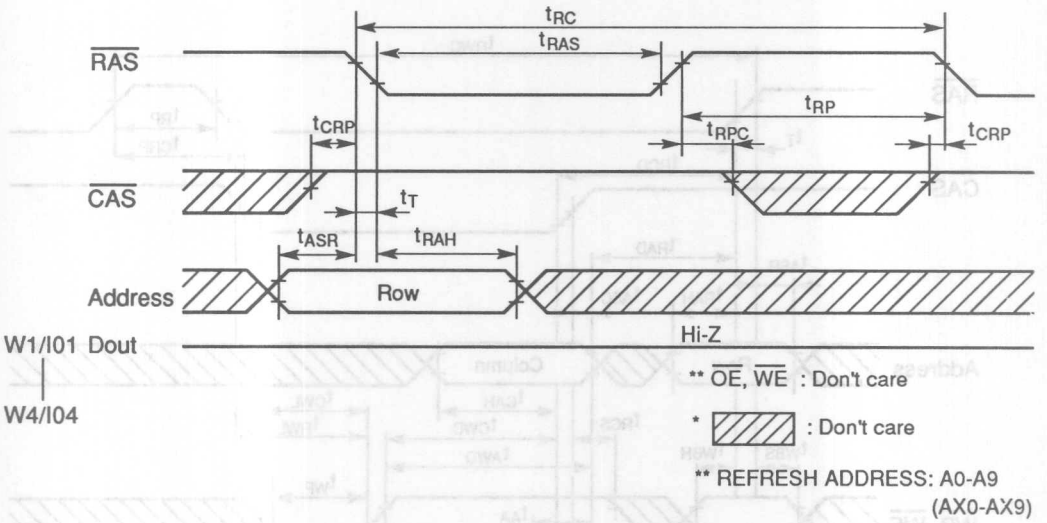


* ▨ : Don't care

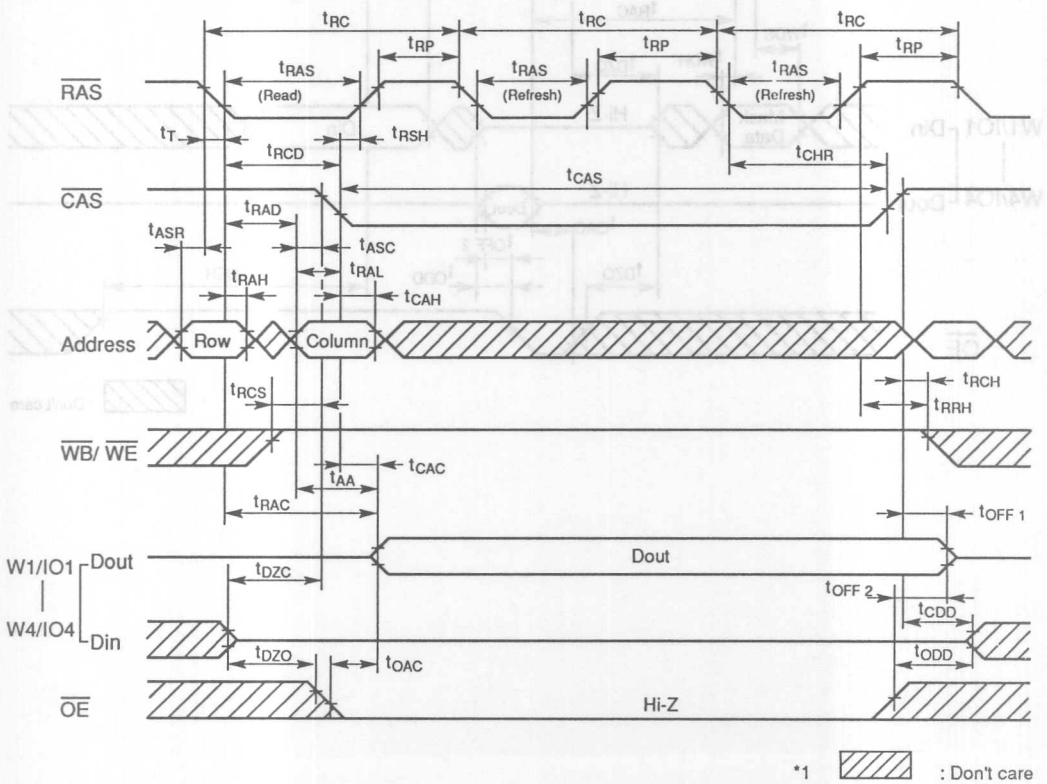
• **Read-Modify-Write Cycle (4)**



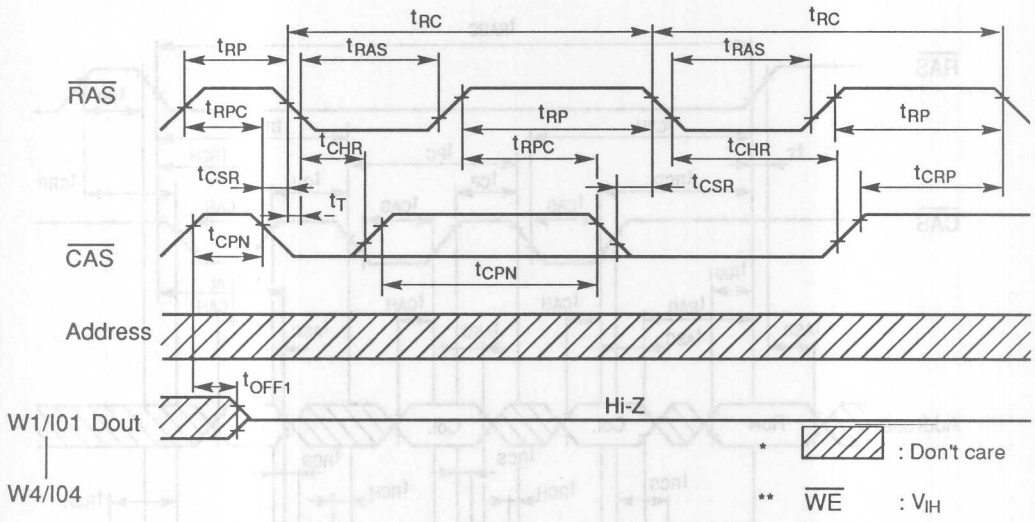
• **$\overline{RAS}$-Only Refresh Cycle (5)**



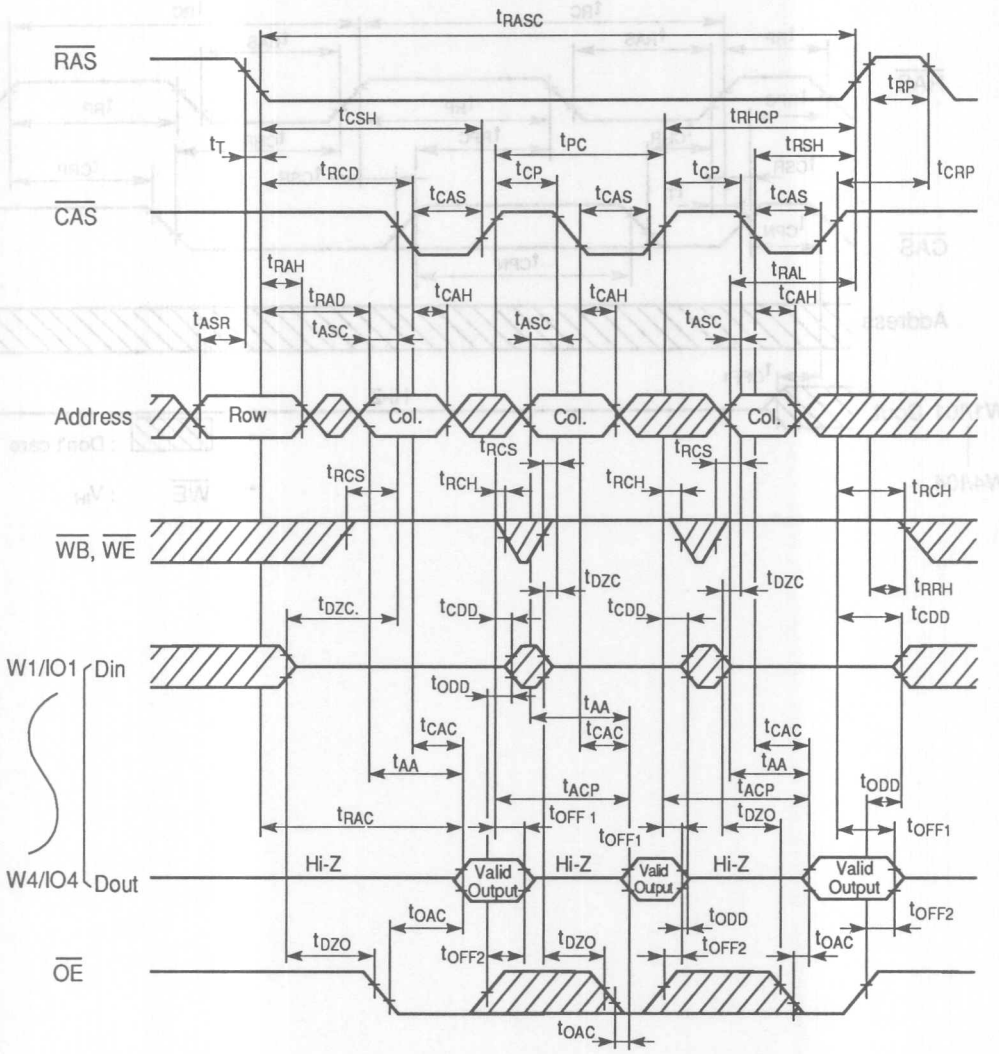
• **Hidden Refresh Cycle (6)**



• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (7)

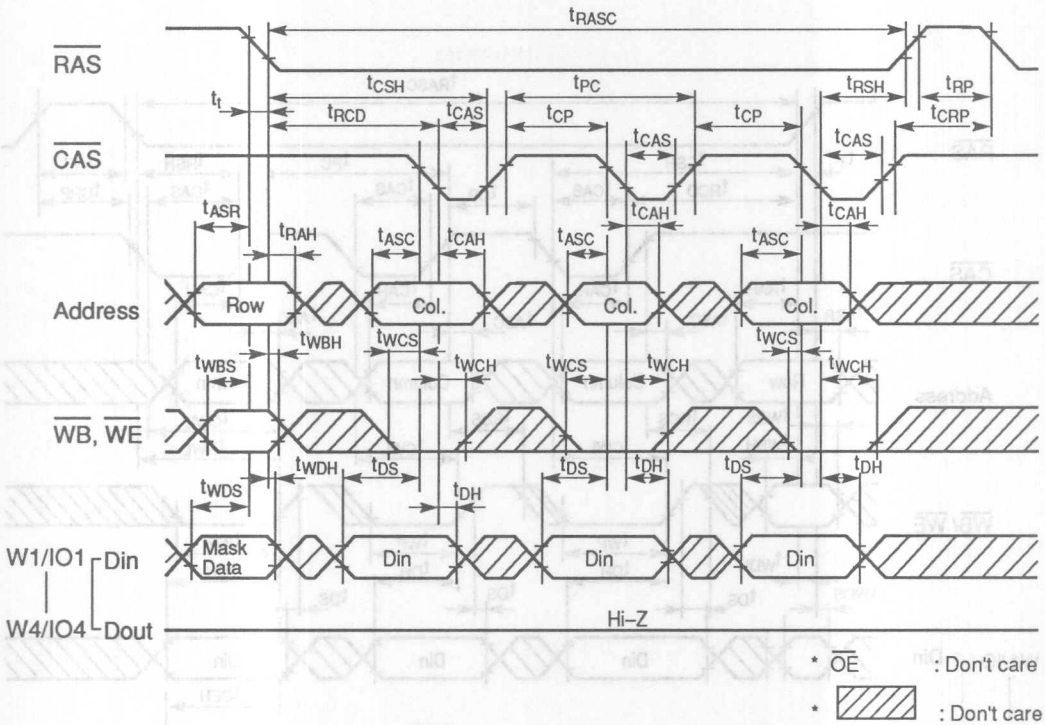


• **Fast Page Mode Read Cycle (8)**

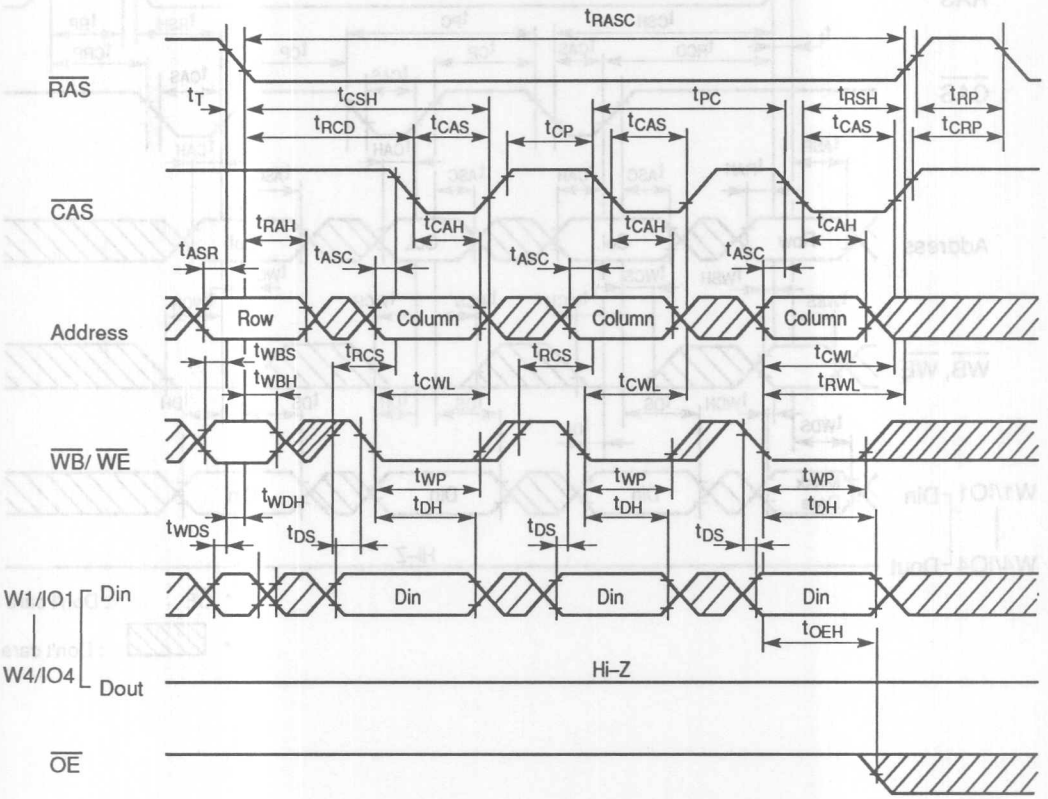


* ▨ : Don't care

• **Fast Page Mode Early Write Cycle (9)**

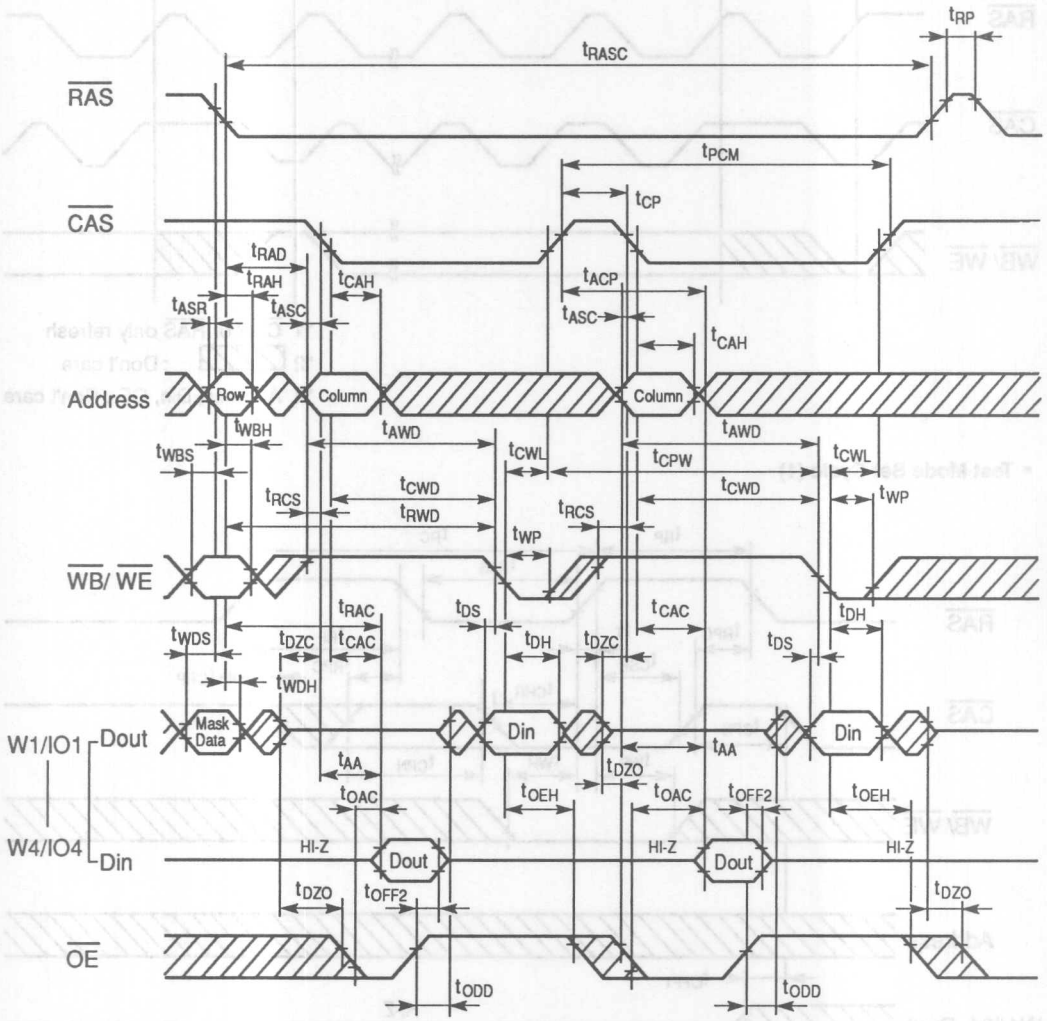


• **Fast Page Delayed Write Cycle (10)**

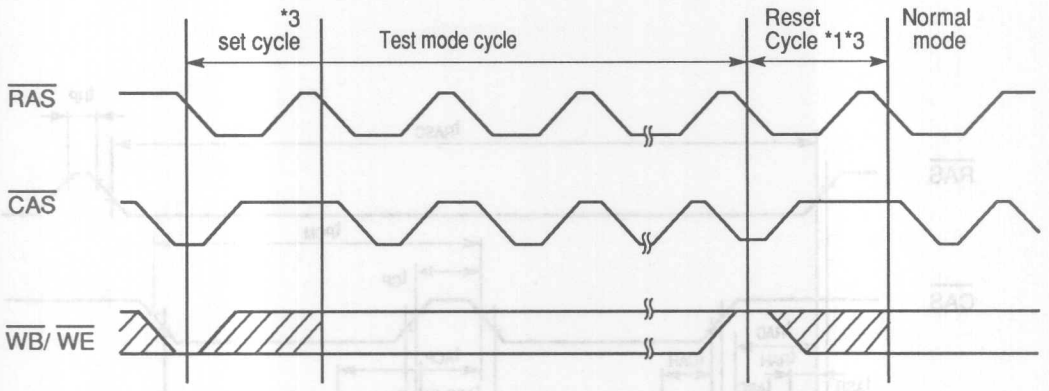


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• **Fast Page Mode Read-Modify-Write Cycle (11)**

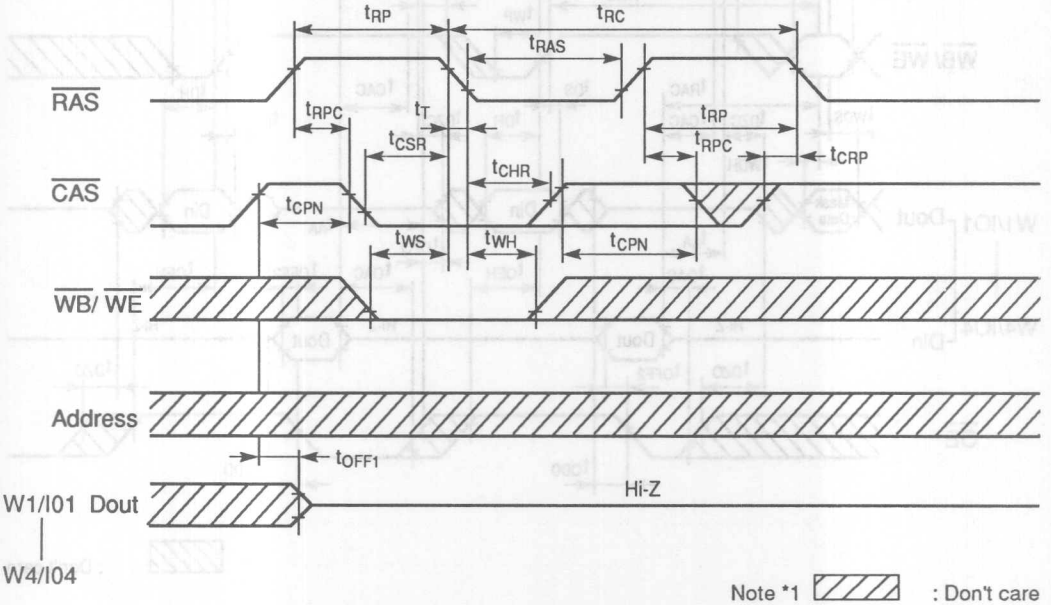


• **Test Mode Cycle**



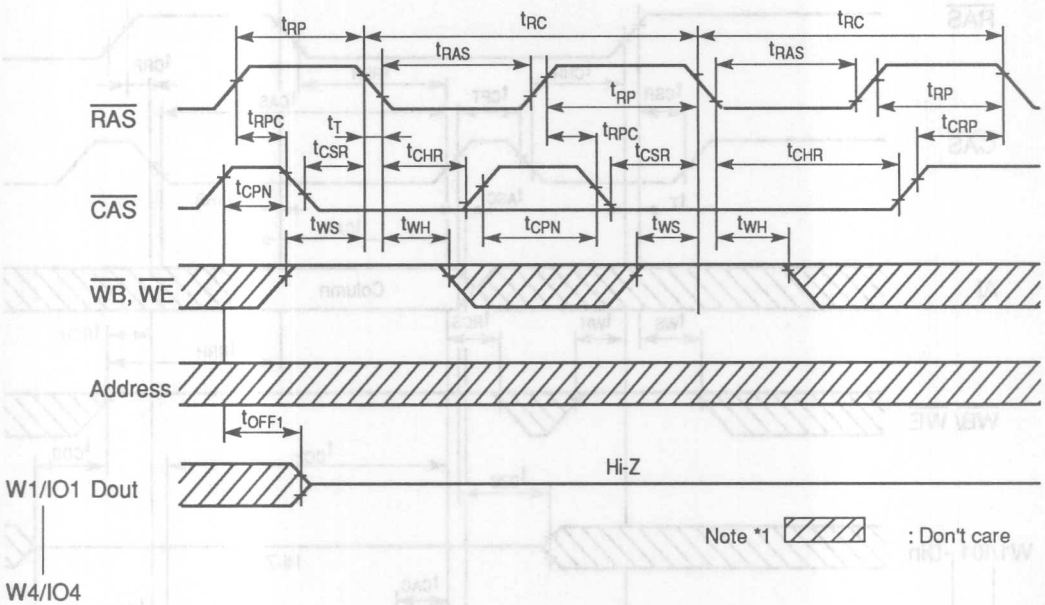
*1 $\overline{CBR}$ or $\overline{RAS}$ only refresh
*2 ▨ : Don't care
*3 Address, Din, OE : Don't care

• **Test Mode Set Cycle (1)**

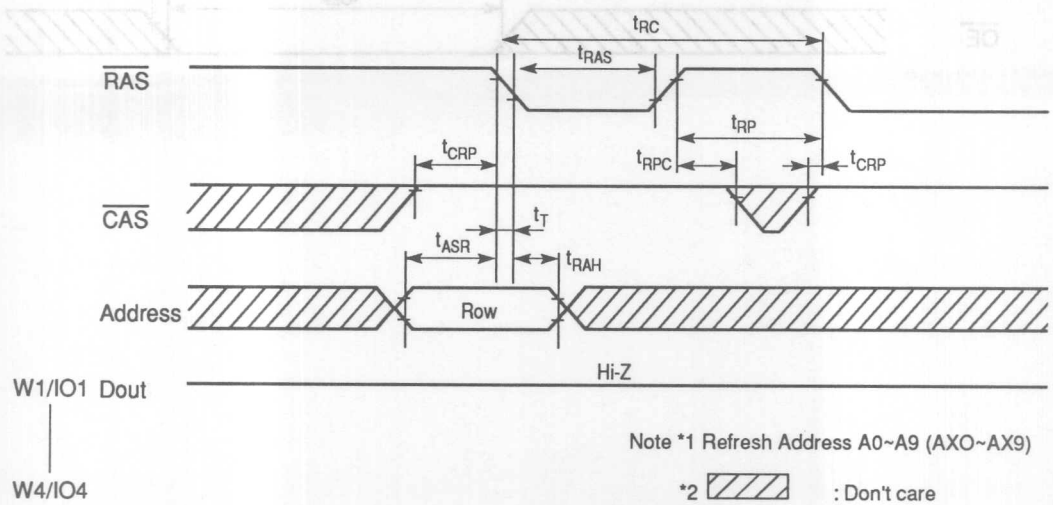


Note *1 ▨ : Don't care

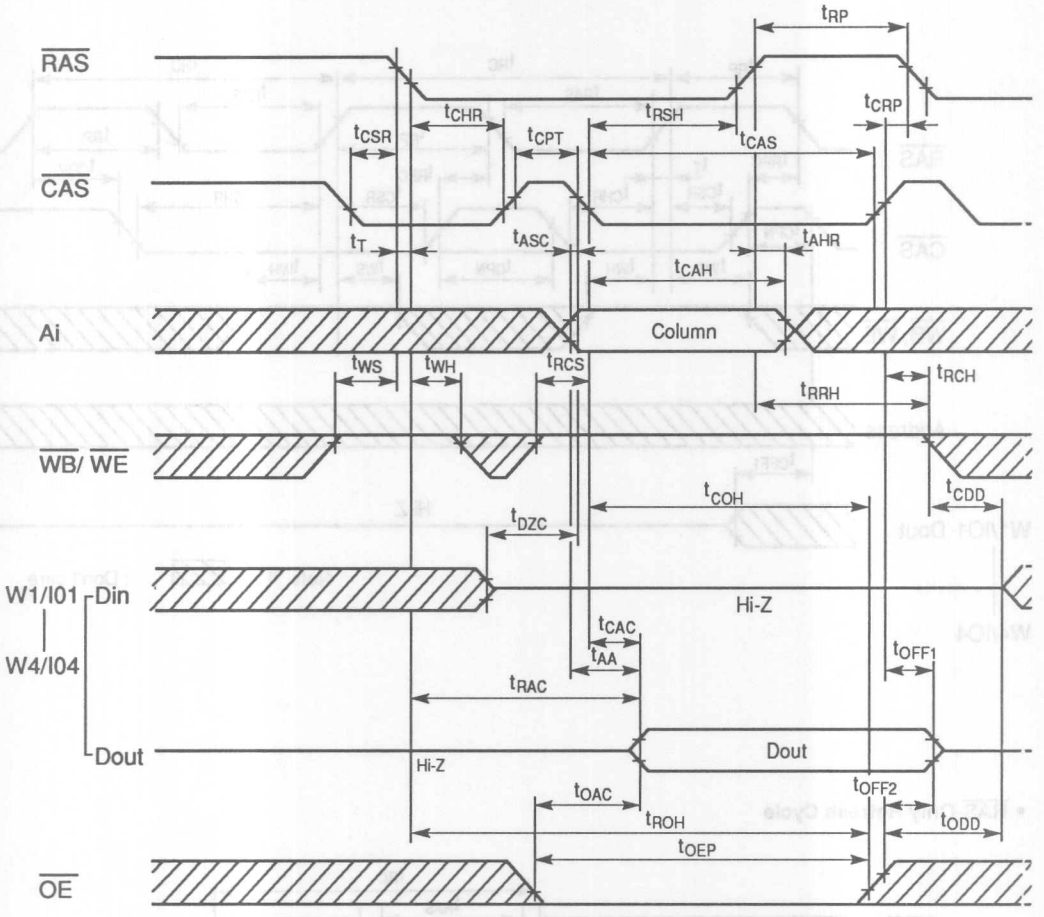
• **Test Mode Reset Cycle (2)**



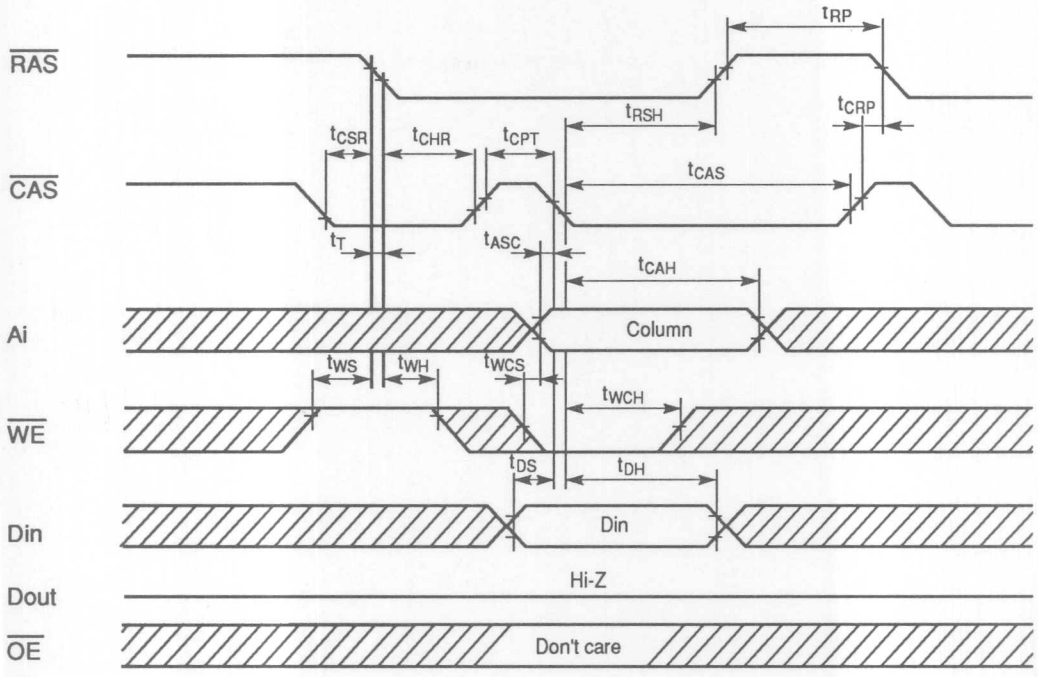
• **RAS-Only Refresh Cycle**



• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle, (READ)



• $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle, (WRITE)



*1 : Don't care

HM514400LJP/LZP-8/10/12 Low Power Version

1,048,576-Word × 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word × 4 bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (± 10%)
- High Speed
  - Access Time. . . . . .80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .495/440/385mW (max.)
  - Standby Mode . . . . . .11mW (max.)
- Fast Page Mode Capability
- 1,024 Refresh Cycles . . . . . .(16ms)
- 3 Variations of Refresh
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Back Up Operation

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514400LJP-8	80ns	350 mil 20 pin
HM514400LJP-10	100ns	Plastic SOJ
HM514400LJP-12	120ns	(CP-20D)
HM514400LZP-8	80ns	400 mil 20 pin
HM514400LZP-10	100ns	Plastic ZIP
HM514400LZP-12	120ns	(ZP-20)

■ PIN DESCRIPTION

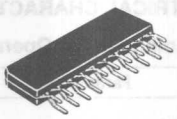
Pin Name	Function
A_0 ~ A_9	Address Input
A_0 ~ A_9	Refresh Address Input
I/O_1–I/O_4	Data-In/Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

HM514400LJP Series



(CP-20D)

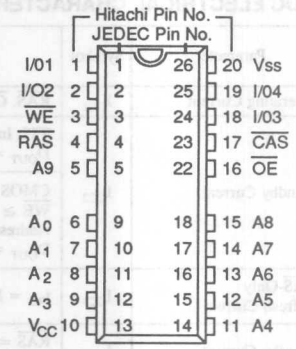
HM514400LZP Series



(ZP-20)

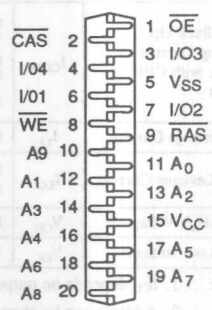
■ PIN OUT

HM514400LJP Series



(Top View)

HM514400LZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM514400-8		HM514400-10		HM514400-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	—	90	—	80	—	70	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ ≥ V_{CC} −0.2V or ≤ 0.2V, Address and D_{in}: Stable, D_{OUT} = High-Z	—	200	—	200	—	200	μA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	90	—	80	—	70	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	90	—	80	—	70	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	90	—	80	—	70	mA	1, 3
Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs, V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V, $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in}: Stable, D_{out} = High-Z	—	300	—	300	—	300	μA	
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-In, Data-Out)	$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (1), (14), (15), (16)

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Set-up Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	128	—	128	—	128	ms	

• Read Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16, 17
Access Time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	18
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output Buffer Turn-Off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

• Write Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-Modify-Write Cycle Time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

• Refresh Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13, 17
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	105	—	110	—	130	—	ns	

• Test Mode Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

• Counter Test Cycle

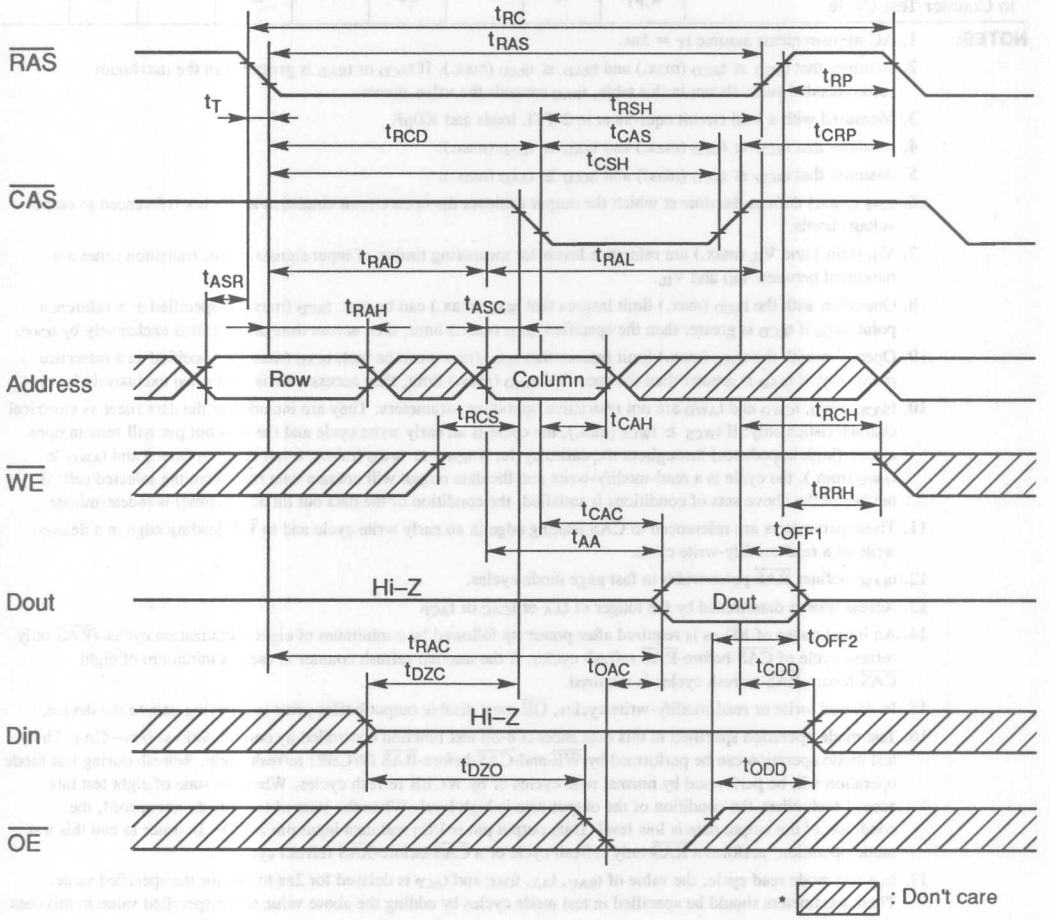
Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

NOTES:

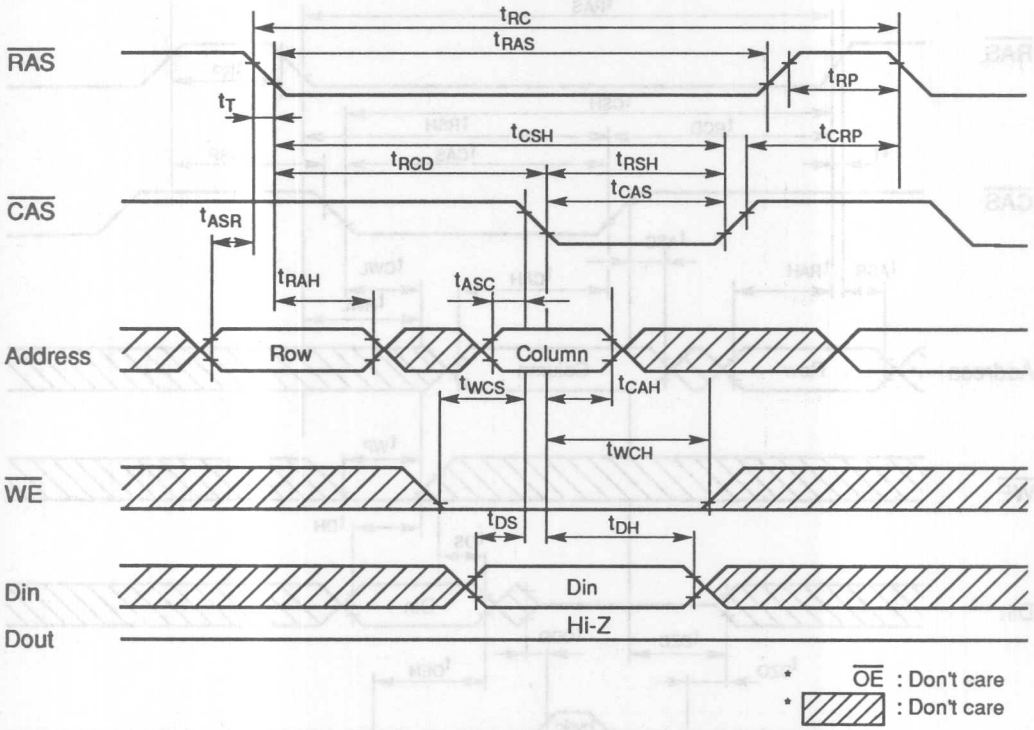
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle of $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—CA_0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

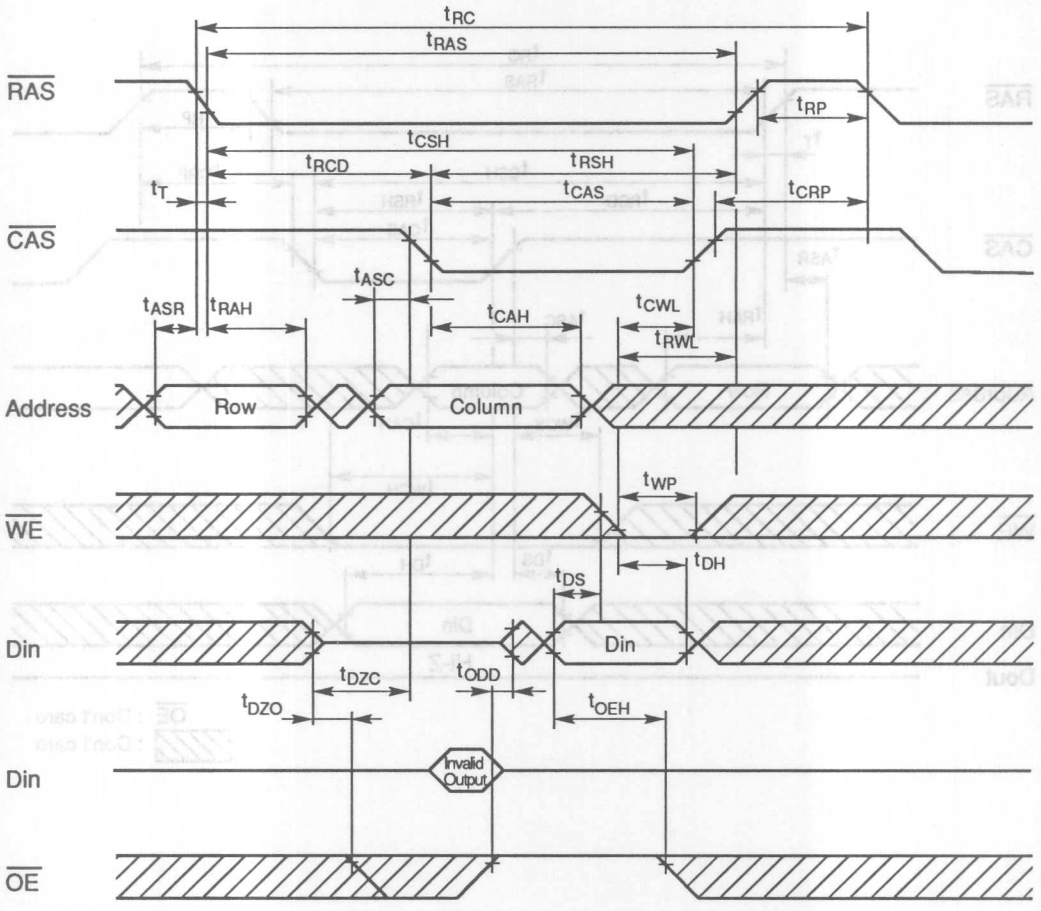
• Read Cycle (1)



• **Early Write Cycle (2)**



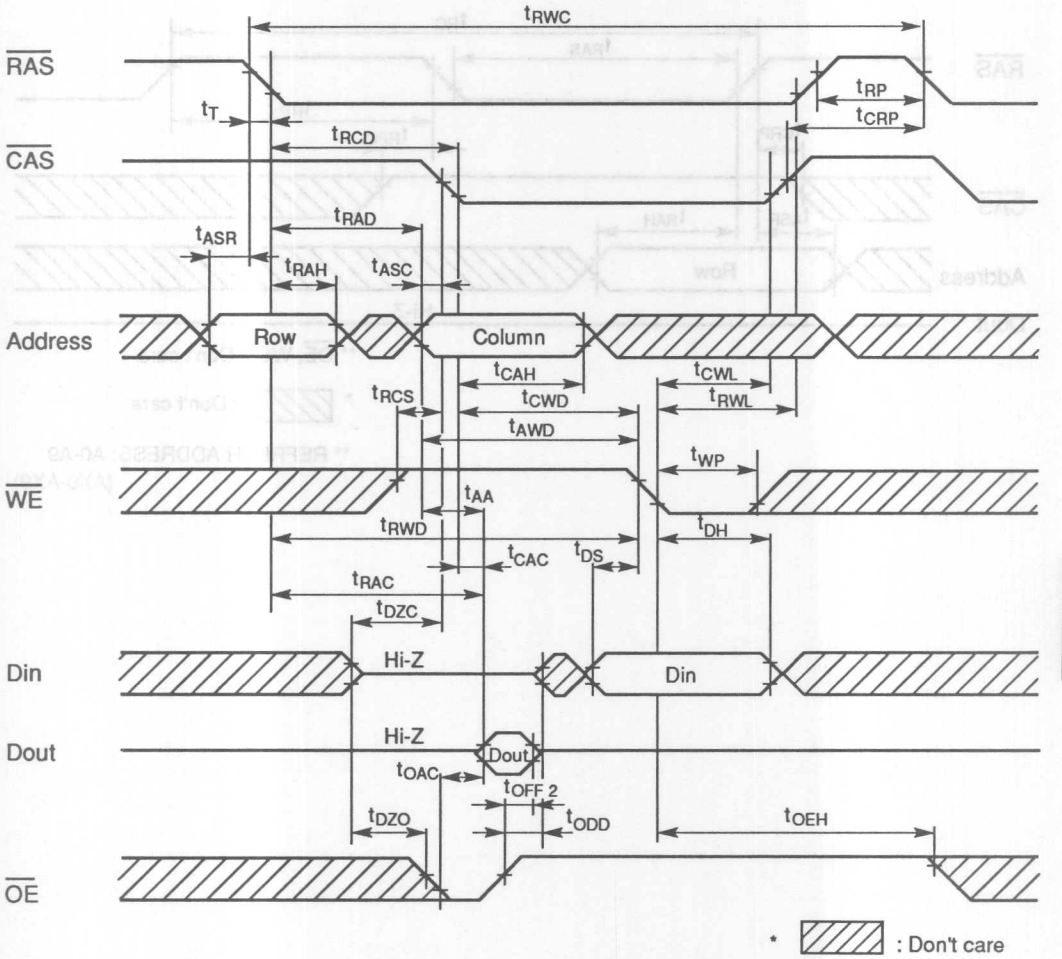
• **Delayed Write Cycle (3)**



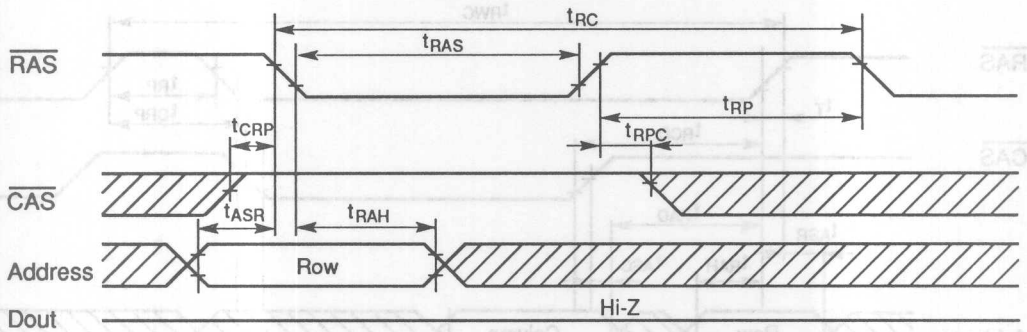
* ▨ : Don't care

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• **Read-Modify-Write Cycle (4)**



• **$\overline{RAS}$-Only Refresh Cycle (5)**

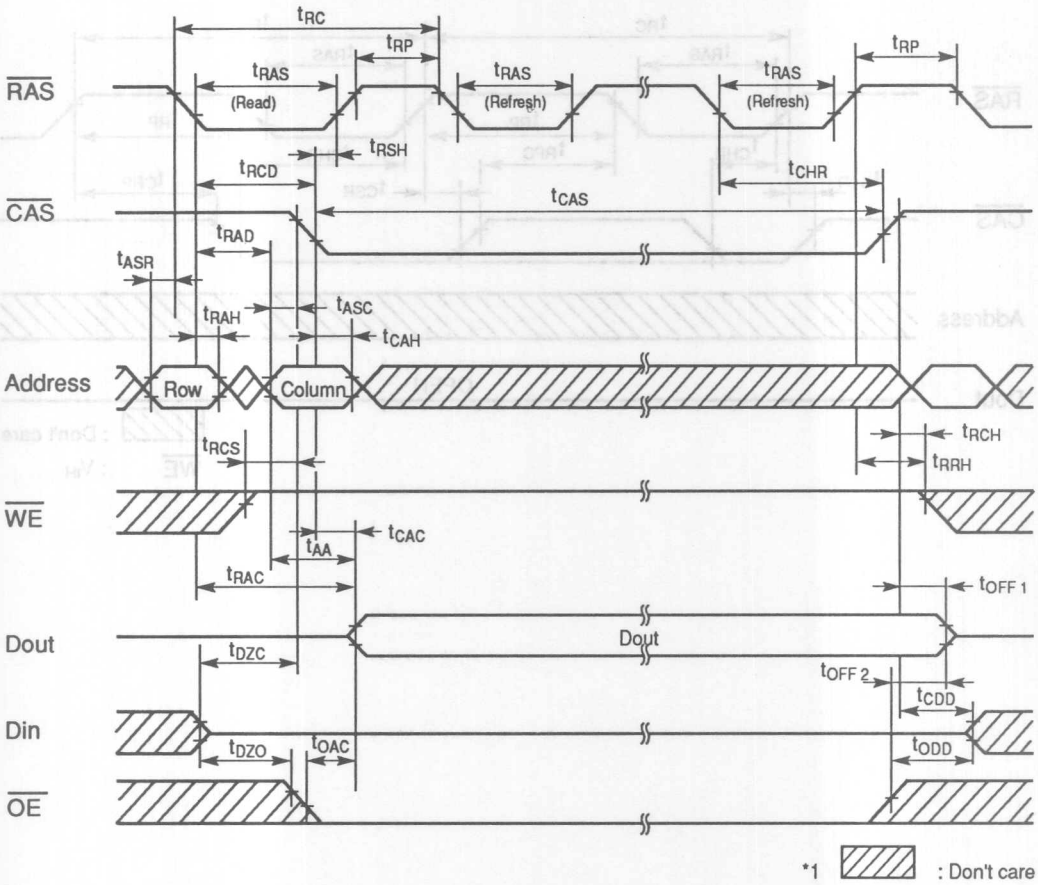


** $\overline{OE}$, $\overline{WE}$: Don't care

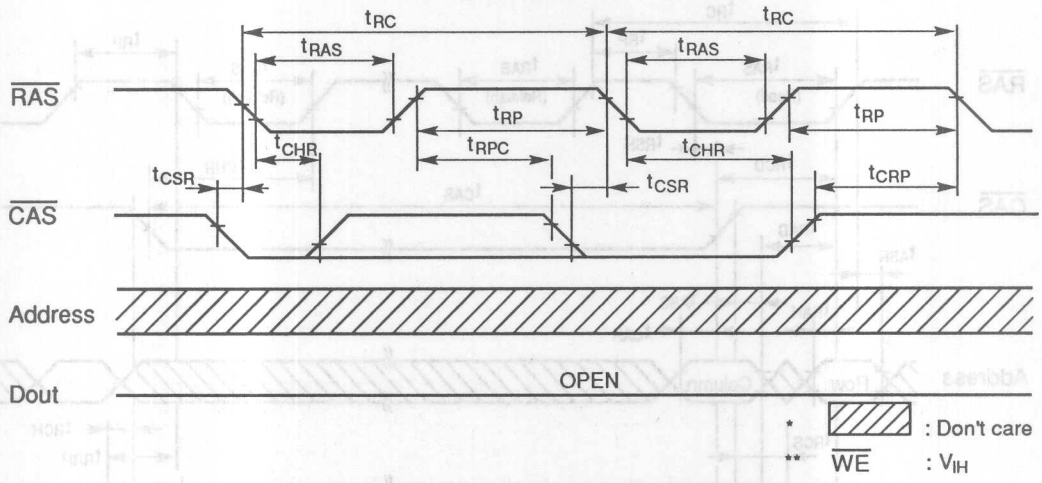
* ▨ : Don't care

** REFRESH ADDRESS: A0-A9
(AX0-AX9)

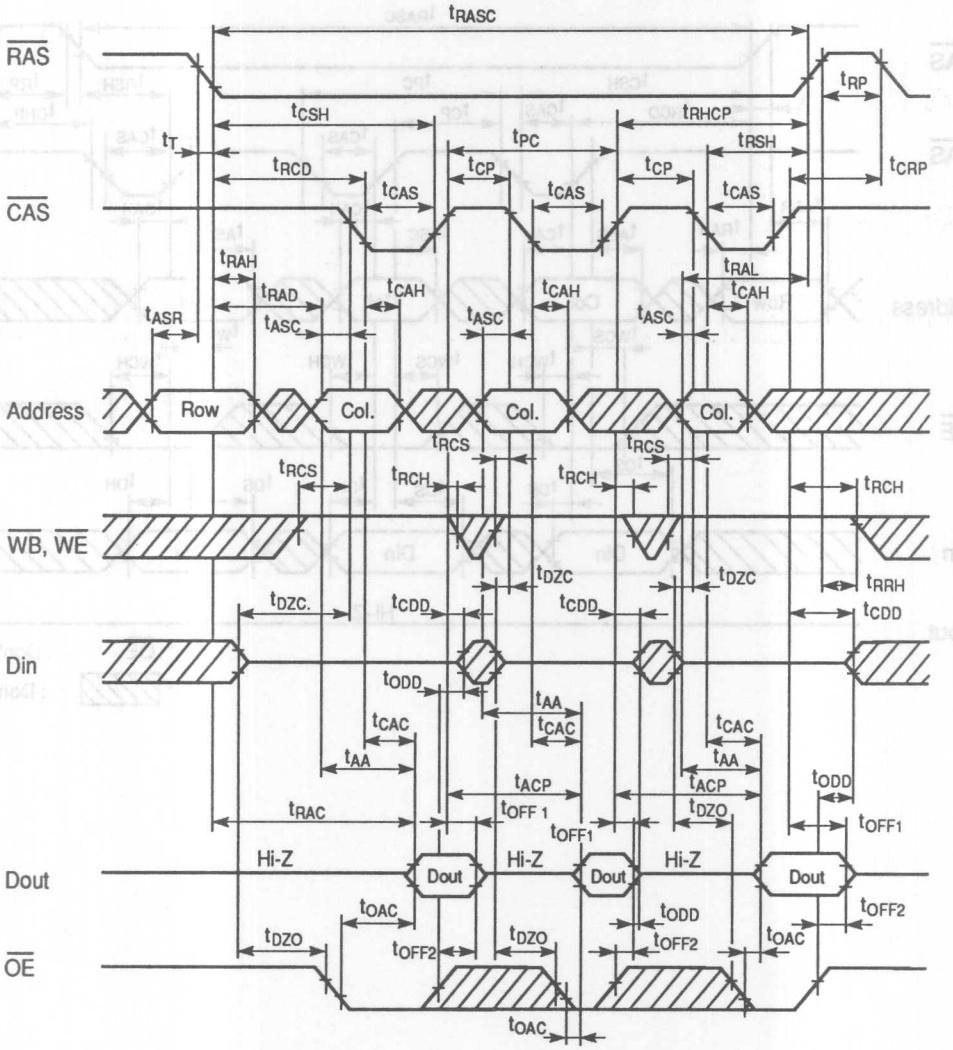
• **Hidden Refresh Cycle (6)**



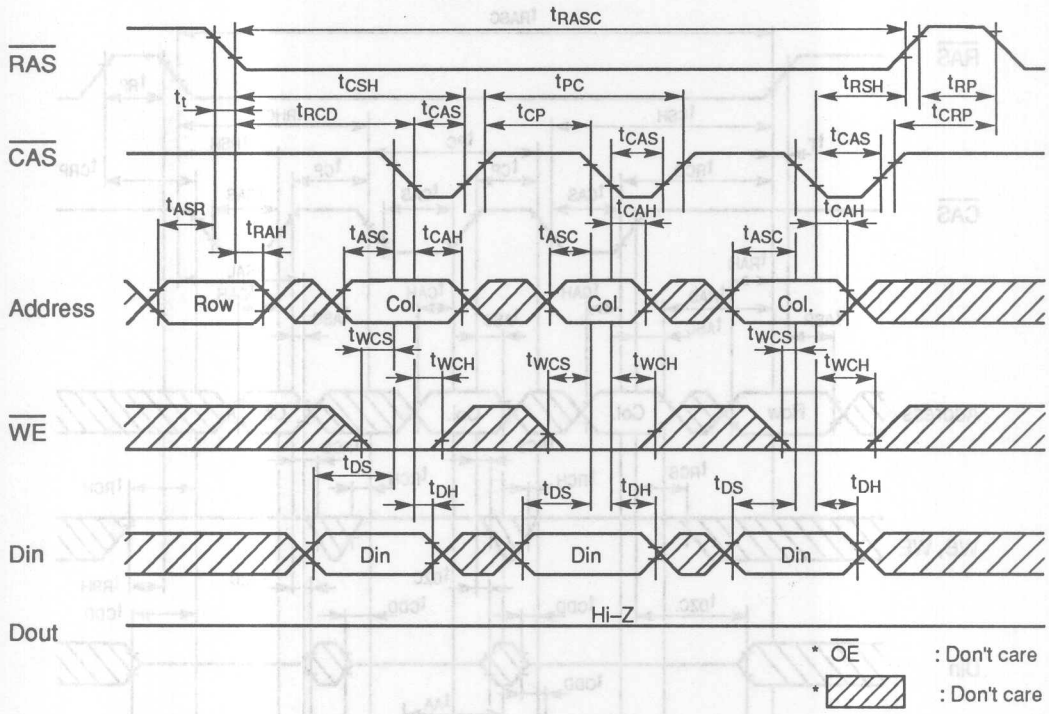
• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (7)



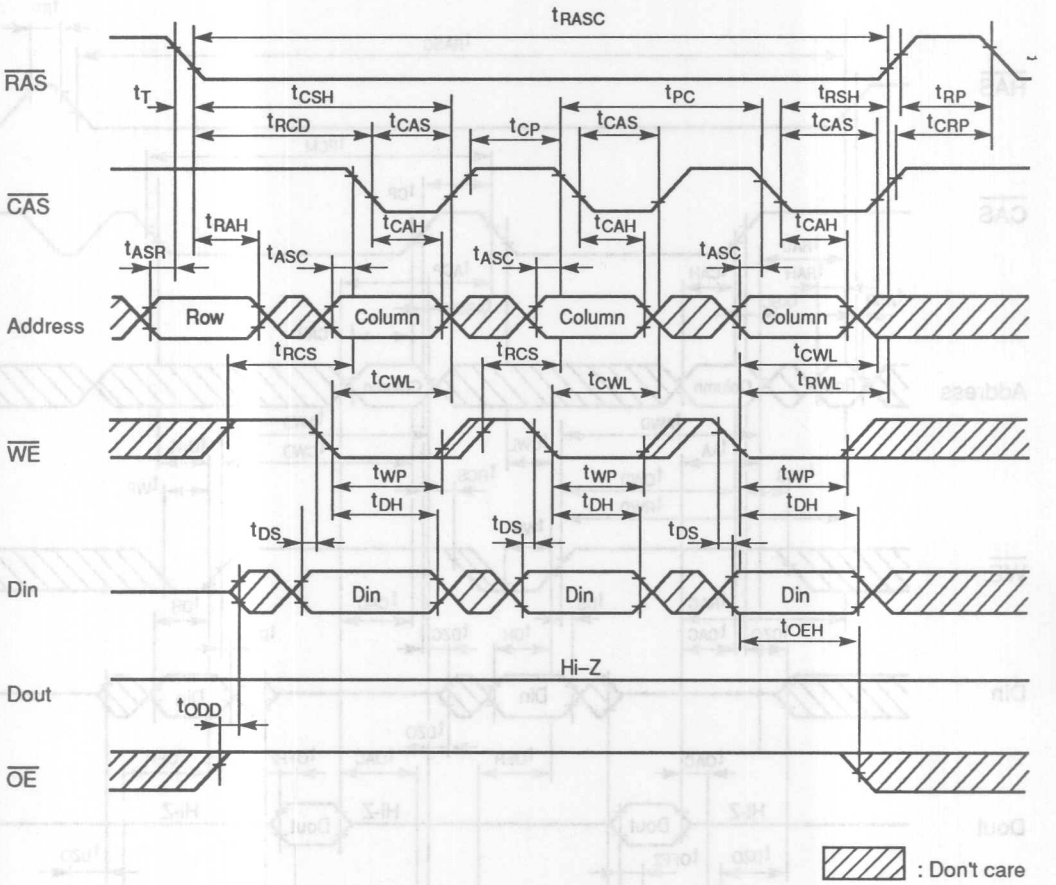
• **Fast Page Mode Read Cycle (8)**



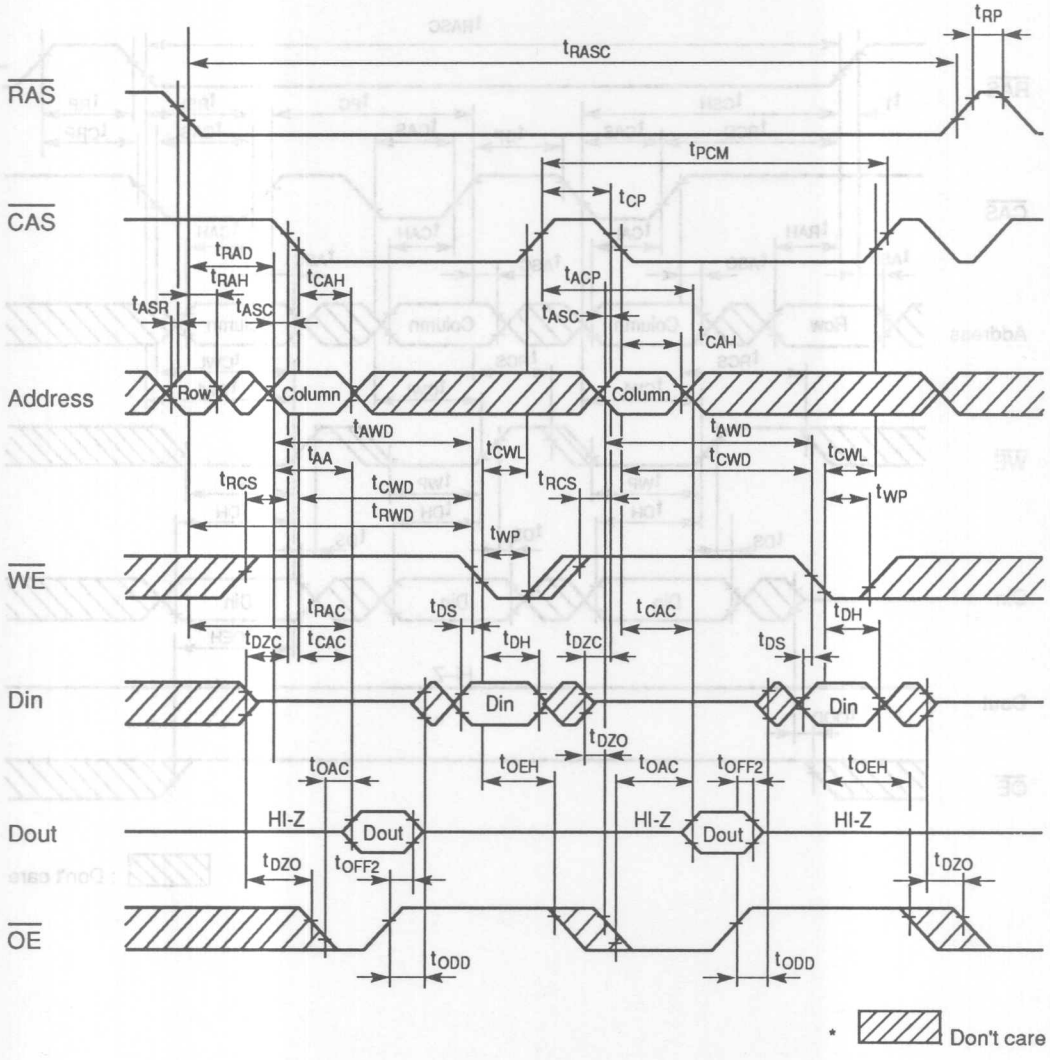
• **Fast Page Mode Early Write Cycle (9)**



• **Fast Page Delayed Write Cycle (10)**

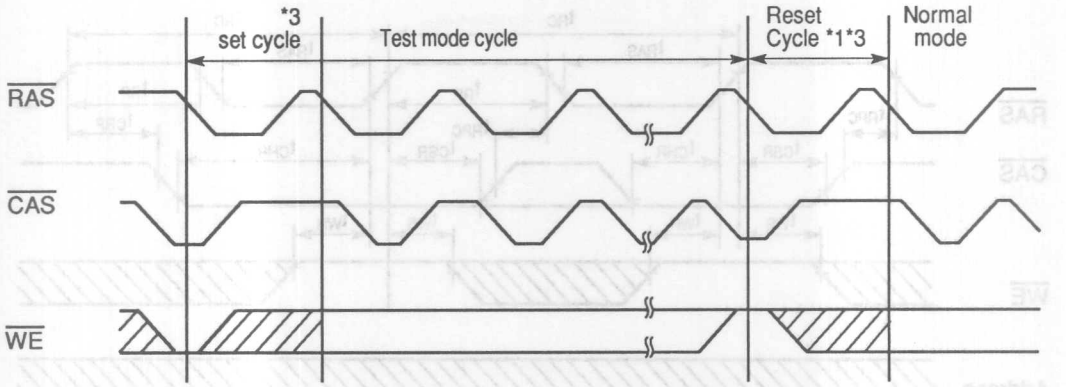


• **Fast Page Mode Read-Modify-Write Cycle (11)**



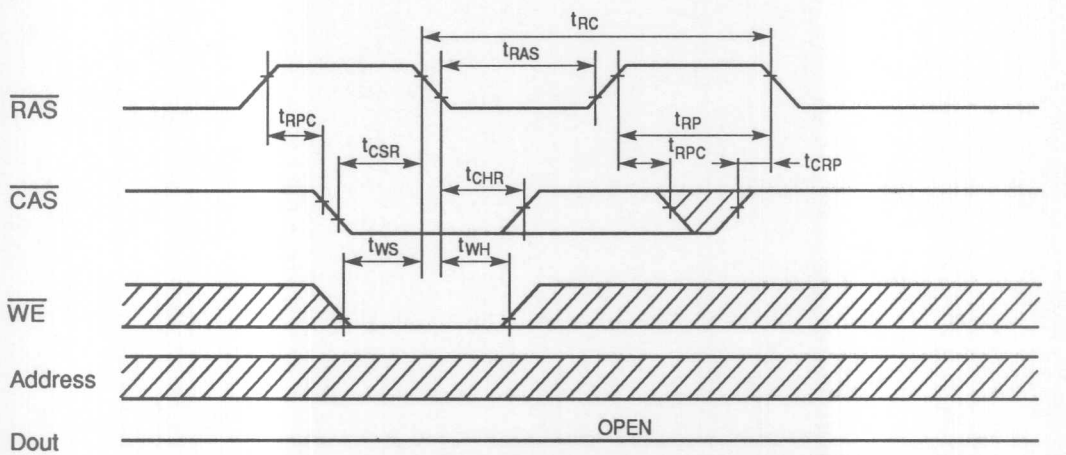
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• **Test Mode Cycle**



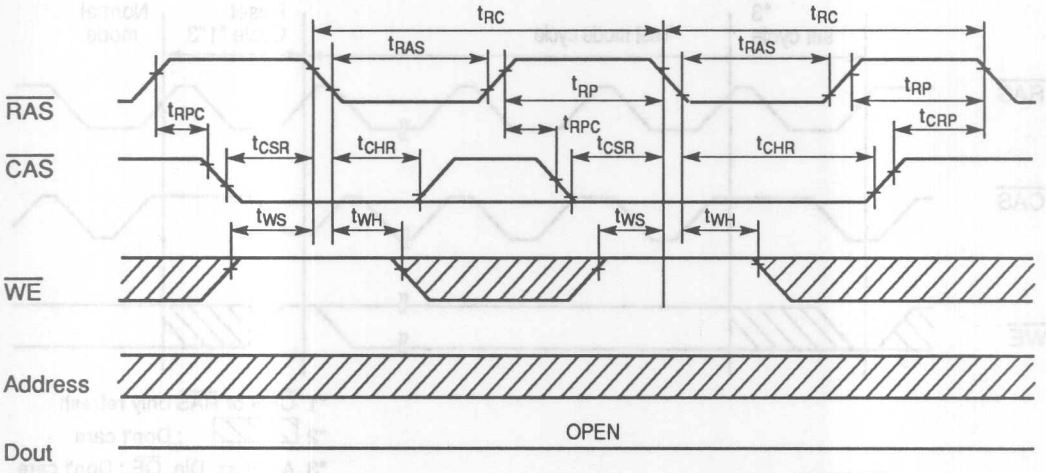
*1 $\overline{CBR}$ or $\overline{RAS}$ only refresh
*2 ▨ : Don't care
*3 Address, Din, $\overline{OE}$: Don't care

• **Test Mode Set Cycle (1)**



Note *1 ▨ : Don't care

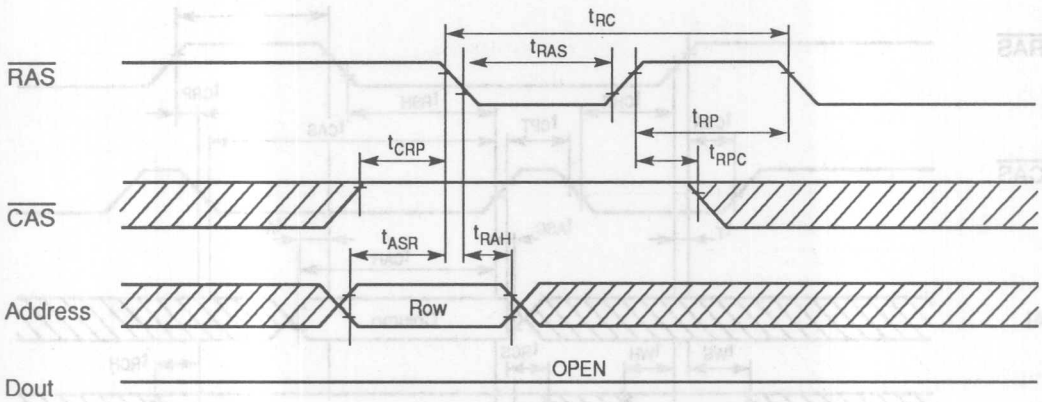
• **Test Mode Reset Cycle (2)**



Note *1 ▨ : Don't care

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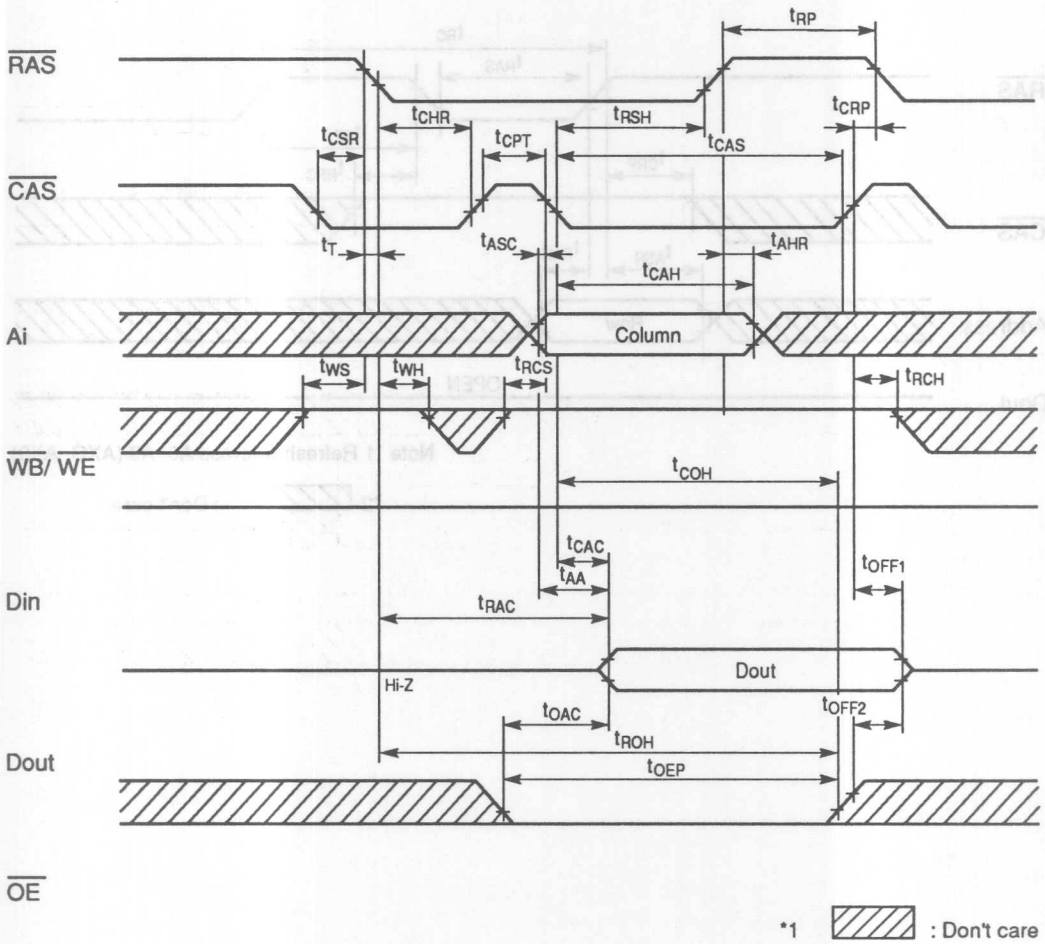
• **$\overline{RAS}$-Only Refresh Cycle**



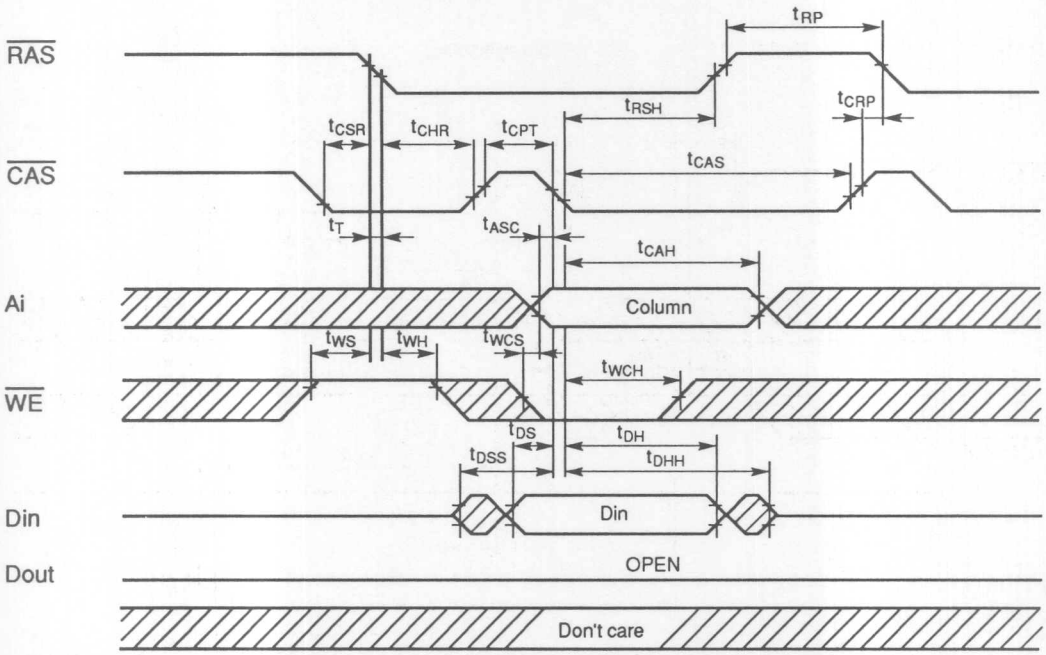
Note *1 Refresh Address A0~A9 (AX0~AX9)

*2 ▨ : Don't care

• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle, (READ)



• $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle, (WRITE)



*1 : Don't care

Section 6
MOS Dynamic RAM Module

6

HITACHI®

HB561003 Series

262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561003 is a 2.25M dynamic random-access memory module organized as 262,144 x 9 bits [bit nine (PD, PQ) is generally used for parity and is controlled by $\overline{PCAS}$] in a 30-pin single in-line package comprising nine HM50256CP, 262,144 x 1-bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on a substrate together with decoupling capacitors.

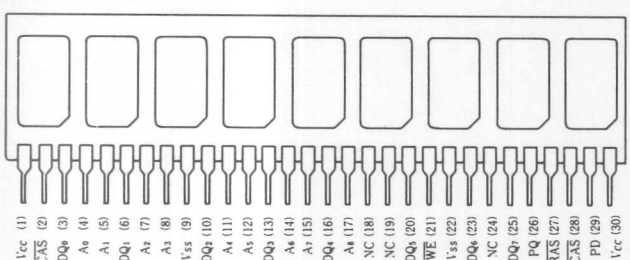
■FEATURES

- 262,144 words x 9 bits Organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561003 operates as nine HM50256CPs as shown in the functional block diagram.
- Low Power: Operating: 2,160mW typ. (t_{RC} = 260ns)
  Standby: 135mW typ.
- High speed:

	Access Time from $\overline{RAS}$ (max)	Access Time from $\overline{CAS}$ (max)	Read or Write Cycle (min)
HB561003AR/B-12	120ns	60ns	220ns
HB561003AR/B-15	150ns	75ns	260ns

- Page mode capability
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature: 0°C to +70°C
- HB561003AR is leaded type
- HB561003B is leadless type (socket type)

■PIN ARRANGEMENT



(Side View)

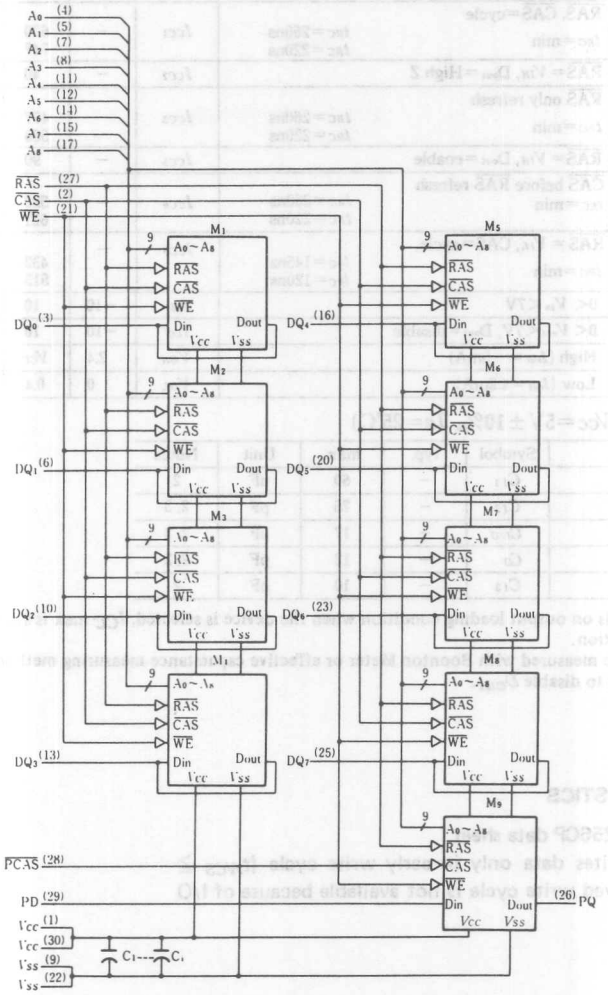
Notes:
1. HB561003B's pin arrangement is same as HD561003AR's.
2. Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
3. Separate $\overline{PCAS}$ control for one separate pair of Data-In and Data-Out lines.
4. The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

■ PIN DESCRIPTION

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobes
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobes
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

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■FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}: −1V to +7V
Operating temperature, T_a (Ambient): 0°C to +70°C
Storage temperature (Ambient): −55°C to +125°C
Power dissipation: 9W
Short circuit output current: 50mA

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Test Conditions		Symbol	min.	max.	Unit	Notes
Operating current	$\overline{RAS}$, $\overline{CAS}$=cycle, t_{RC}=min	t_{RC}=260ns	I_{CC1}	–	630	mA	1
		t_{RC}=220ns			747		
Standby current	$\overline{RAS}$=V_{IH}, D_{out}=High Z		I_{CC2}	–	40	mA	
Refresh current	$\overline{RAS}$ only refresh, t_{RC}=min	t_{RC}=260ns	I_{CC3}	–	477	mA	
		t_{RC}=220ns			558		
Standby current	$\overline{RAS}$=V_{IH}, D_{out}=enable		I_{CC5}	–	90	mA	1
Refresh current	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC}=min	t_{RC}=260ns	I_{CC6}	–	522	mA	
		t_{RC}=220ns			621		
Page made supply current	$\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycle, t_{PC}=min	t_{PC}=145ns	I_{CC7}	–	432	mA	
		t_{PC}=120ns			513		
Input leakage	0< V_{in} <7V		I_{LI}	−10	10	μA	
Output leakage	0< V_{out} <7V, D_{out}=disable		I_{LO}	−10	10	μA	
Output levels	High (I_{out}=−5mA)		V_{OH}	2.4	V_{CC}	V	
	Low (I_{out}=4.2mA)		V_{OL}	0	0.4	V	

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	–	60	pF	2
Clocks	C_{I2}	–	75	pF	2, 3
DQ	$C_{I/O}$	–	17	pF	2, 3
PQ	C_O	–	12	pF	2, 3
PD	C_{I3}	–	10	pF	2

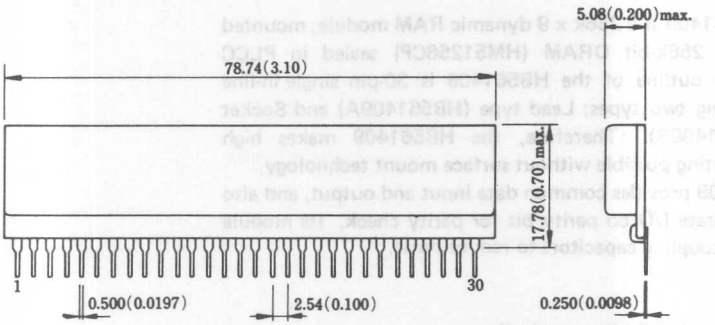
Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■AC CHARACTERISTICS

Refer to the HM50256CP data sheet.
The HB561003 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

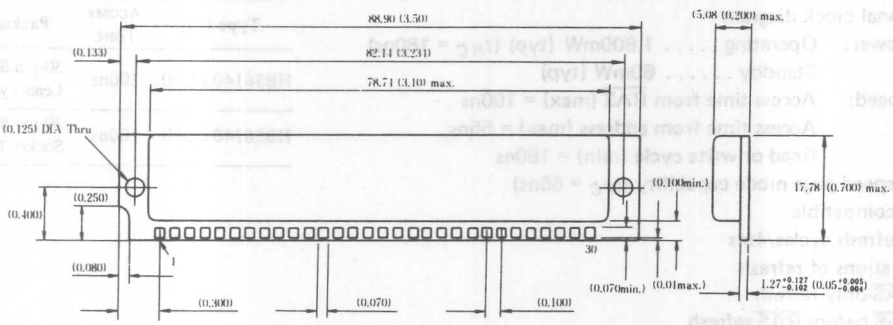
■PACKAGE OUTLINE

● HB561003AR Series



Unit : mm(inch)

● HB561003B Series



Unit : mm(inch)

HB561409 Series

262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561409 is a 256k x 9 dynamic RAM module, mounted 9 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB561409 is 30-pin single in-line package having two types; Lead type (HB561409A) and Socket type (HB561409B). Therefore, the HB561409 makes high density mounting possible without surface mount technology.
The HB561409 provides common data input and output, and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors to reduce noise.

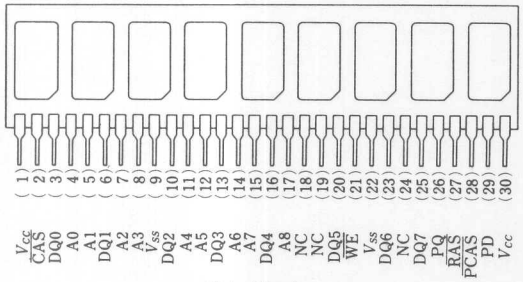
Features

- 262,144 words x 9 bits organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM51256CP)
- HB561409A/B operates as nine HM51256CPs as shown in the functional block diagram
- Low Power: Operating . . . . . 1,800mW (typ) (t_{RC} = 180ns)
  Standby . . . . . 60mW (typ)
- High speed: Access time from $\overline{RAS}$ (max) = 100ns
  Access time from address (max) = 55ns
  Read or write cycle (min) = 180ns
- High speed page mode capability (t_{PC} = 65ns)
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature . . . . . 0°C to +70°C.

Ordering Information

Type No.	Access Time	Package
HB561409A-10	100ns	30-pin SIP Lead Type
HB561409B-10	100ns	30-pin SIMM Socket Type

Pin Arrangement



(Side View)

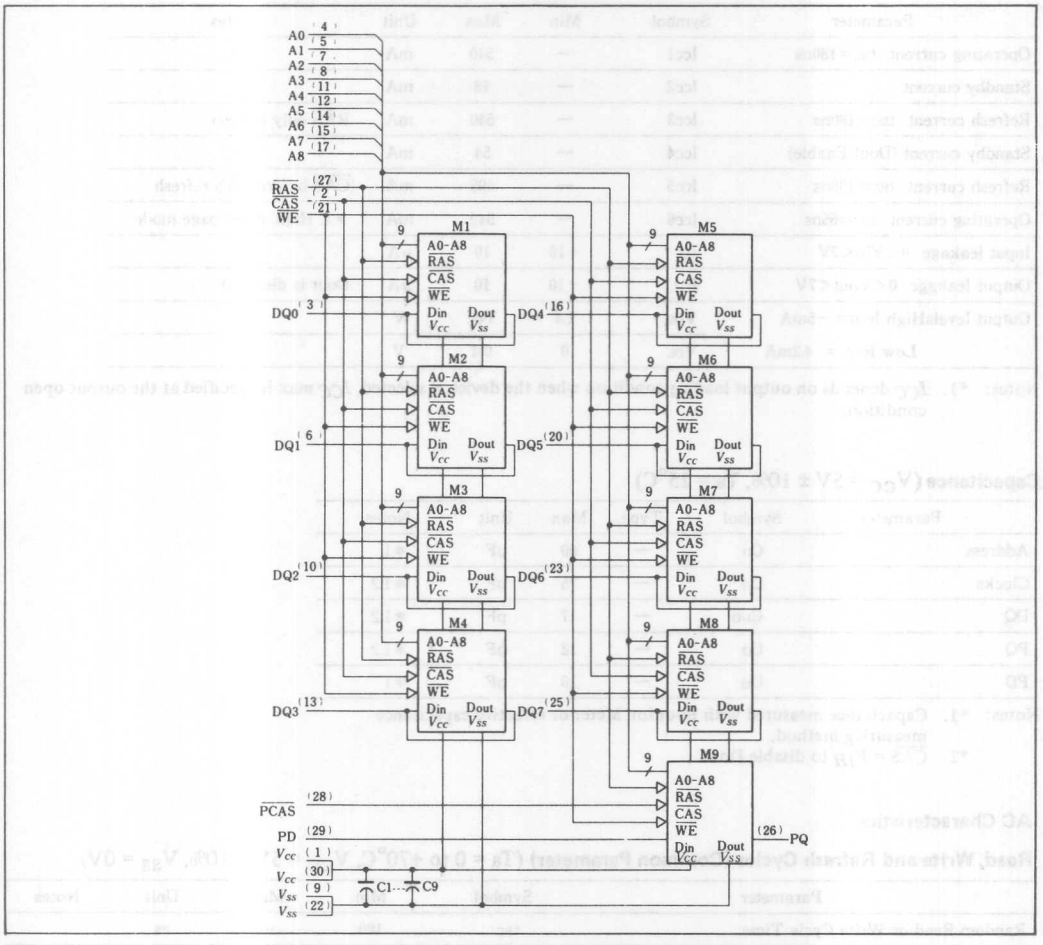
Notes: 1. HB561409B's pin arrangement is same as HB561409A's.
2. Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
3. Separate $\overline{PCAS}$ control for one separate pair of Data-In and Data-Outlines.
4. The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

Pin Description

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobe
Vcc	+5V Supply
Vss	Ground
$\overline{WE}$	Write Enable

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Functional Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 9W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current t_{RC}=180ns	Icc1	—	540	mA	*1
Standby current	Icc2	—	18	mA	
Refresh current t_{RC}=180ns	Icc3	—	540	mA	$\overline{RAS}$ only refresh
Standby current (Dout Enable)	Icc4	—	54	mA	*1
Refresh current t_{RC}=180ns	Icc5	—	495	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh
Operating current t_{PC}=65ns	Icc6	—	540	mA	*1, High speed page mode
Input leakage 0<Vin<7V	I_{LI}	−10	10	μA	
Output leakage 0<Vout<7V	I_{LO}	−10	10	μA	Dout is disabled
Output levelsHigh Iout=−5mA	V_{OH}	2.4	Vcc	V	
Low Iout = 4.2mA	V_{OL}	0	0.4	V	

Notes: *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Type	Max	Unit	Notes
Address	C_{I1}	—	60	pF	*1
Clocks	C_{I2}	—	75	pF	*1,2
DQ	$C_{I/O}$	—	17	pF	*1,2
PQ	C_O	—	12	pF	*1,2
PD	C_{I3}	—	10	pF	*1

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

Read, Write and Refresh Cycles (Common Parameter) (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	75	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	80	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	ns	*8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	45	ns	*9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	ns	*7
Refresh Period	t_{REF}	—	4	ms	

• Read Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Access Time from $\overline{RAS}$	t_{RAS}	—	100	ns	*2, *3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	ns	*3, *4
Access Time from Address	t_{AA}	—	55	ns	*3, *5
Read Command Set-up Time	t_{RCS}	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	30	ns	*6

• Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Write Command Set-up Time	t_{WCS}	0	—	ns	*10
Write Command Hold Time	t_{WCH}	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	85	—	ns	
Write Command Pulse Width	t_{WP}	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	ns	*11
Data-in Hold Time	t_{DH}	25	—	ns	*11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	80	—	ns	

• Refresh Cycle

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	ns	

• High Speed Page Mode Cycle

Parameter	Symbol	Min	Max	Unit	Notes
High Speed Page Mode Cycle Time	t_{PC}	65	—	ns	*12
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	75	75000	ns	*13
$\overline{CAS}$ Precharge Time	t_{CP}	20	—	ns	
Write Invalid Time	t_{WI}	15	—	ns	
Access Time from Column Precharge Time	t_{CAP}	—	60	ns	*14

Notes) *1. AC measurements assume t_T = 5ns.
*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max.)
*6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.
*7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

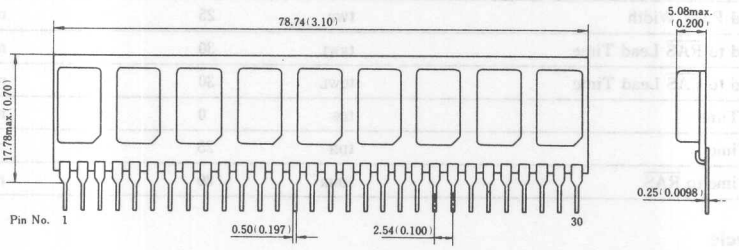
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. Only early write cycle to prevent contention on Data in and out ($t_{WCS} \geqq 0$).
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle.
12. Assumes that $t_{ASC} = t_{CP}$-5ns.
13. t_{RAPC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
15. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
16. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using an internal refresh counter.

Timing Waveforms

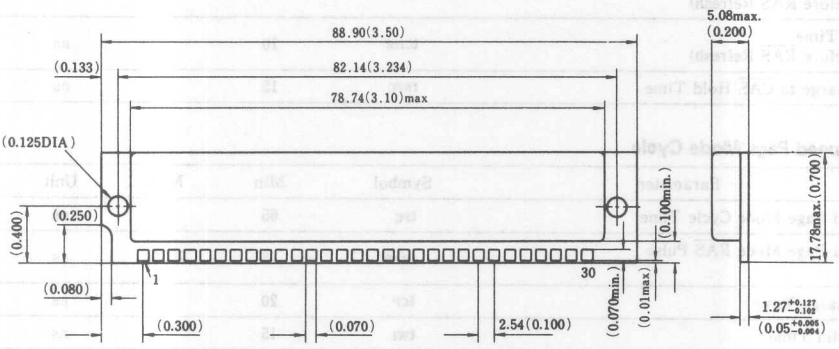
Refer to the HM51256CP data sheet.

Package Outline, Unit; mm (inch)

HB561409A



HB561409B



HB561008 Series

262,144-word x 8-bit Dynamic Random Access Memory Module

The HB561008AR/B is a 2M dynamic random-access memory module organized as 262,144 x 8 bits in a 30-pin single in-line package comprising eight HM50256CP, 262,144 x 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together with decoupling capacitors.

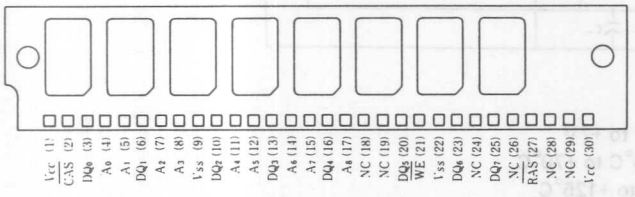
■ FEATURES

- 262,144 words x 8-bits Organization
- Industry standard 30-Pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes eight 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561008AR/B operates as eight HM50256CPs as shown in the functional block diagram.
- Lower Power; Operating: 1,920mW typ. (t_{RC} = 260ns)
  Standby: 120mW typ.
- High speed:

	Access Time from $\overline{RAS}$ (max)	Access Time from $\overline{CAS}$ (max)	Read or Write Cycle (min)
HB561008AR/B-12	120ns	60ns	220ns
HB561008AR/B-15	150ns	75ns	260ns

- Page mode capability
- TTL compatible
- 256 refresh cycles: (4ms)
- 3 variations of refresh
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- Operating Ambient Air Temperature: 0 to +70°C
- HB561008AR ..... Leaded type
- HB561008B .... Leadless type (socket type)

■PIN ARRANGEMENT



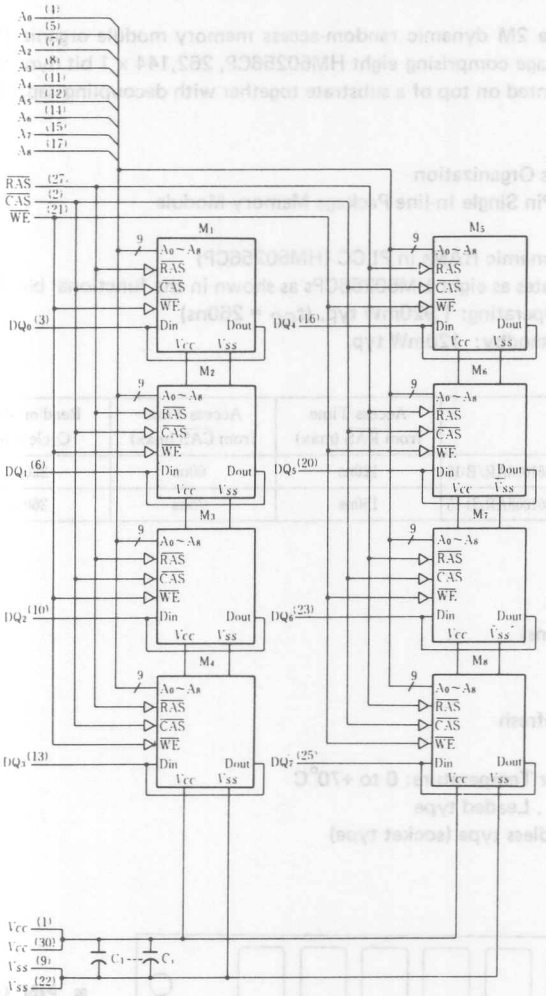
(Side View)

Notes: 1. HB561008AR's pin arrangement is same as HB561008B's.
2. Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on Data-in and Data-out.

■ PIN DESCRIPTION

A0-A8	Address Inputs
$\overline{CAS}$	Column Address Strobes
DQ0-DQ7	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row Address Strobes
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

Voltage on any pin relative to V_{SS}: −1V to +7V
Operating temperature, T_a (Ambient): 0°C to +70°C
Storage temperature (Ambient): −55°C to +125°C
Power dissipation: 8W
Short circuit output current: 50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V +10%, V_{SS}=0V)

Parameter	Test Conditions	Symbol	min.	max.	Unit	Notes
Operating current	$\overline{RAS}$, $\overline{CAS}$=cycle t_{RC}=min t_{RC}=260ns t_{RC}=220ns	I_{CC1}	—	560 660	mA	1
Standby current	$\overline{RAS}$= V_{IH}, D_{out}=High Z	I_{CC2}	—	36	mA	
Refresh current	$\overline{RAS}$ only refresh t_{RC}=min t_{RC}=260ns t_{RC}=220ns	I_{CC3}	—	425 495	mA	
Standby current	$\overline{RAS}$= V_{IH}, D_{out}=enable	I_{CC5}	—	80	mA	1
Refresh current	$\overline{CAS}$ before $\overline{RAS}$ refresh t_{RC}=min t_{RC}=260ns t_{RC}=220ns	I_{CC6}	—	465 550	mA	
Page mode supply current	$\overline{RAS}$= V_{IL}, $\overline{CAS}$=cycle, t_{PC}=min t_{PC}=145ns t_{PC}=120ns	I_{CC7}	—	385 455	mA	
Input leakage	0< V_{in} <7V	I_{LI}	−10	10	μA	
Output leakage	0< V_{out} <7V, D_{out}=disable	I_{LO}	−10	10	μA	
Output levels	High (I_{out} = −5mA)	V_{OH}	2.4	V_{CC}	V	
	Low (I_{out} =4.2mA)	V_{OL}	0	0.4	V	

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	—	55	pF	2
Clocks	C_{I2}	--	70	pF	2, 3
DQ	$C_{I/O}$	--	17	pF	2, 3

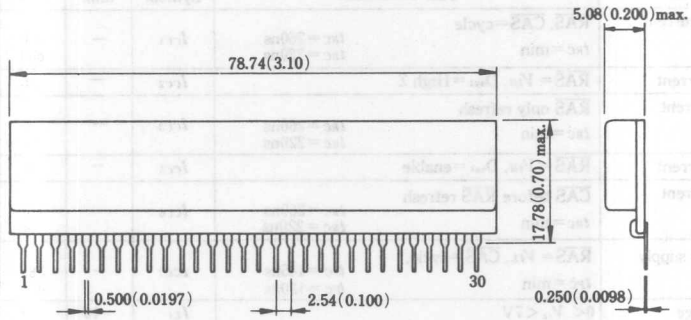
Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS

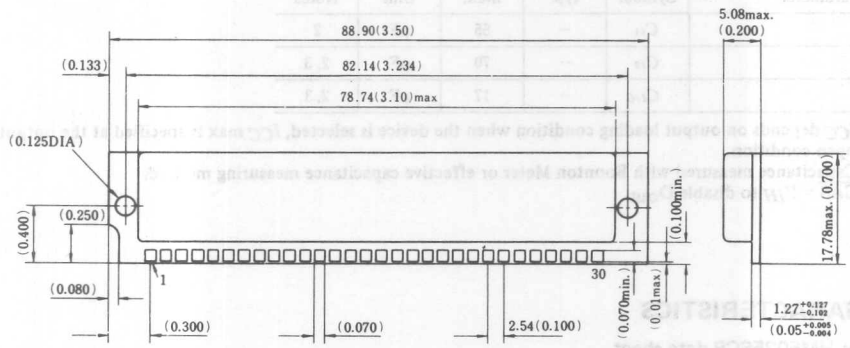
Refer to the HM50256CP data sheet.
The HB561008 writes data only in early write cycle ($t_{WCS} \geqq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

■PACKAGE OUTLINE; Unit: mm (inch)

● HB561008AR Series



● HB561008B Series



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HB56D25608A/B-6H/7H/8A/10A/12A

262,144-Word × 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A25608 is a 256K × 8 dynamic RAM module, mounted two 1-Mbit DRAM (HM514256A) sealed in SOJ package. An outline of the HB56A25609 is 30-pin single in-line package having Lead types (HB56A25608A), Socket type (HB56A25608B). Therefore, the HB56A25608 makes high density mounting possible without surface mount technology. The HB56A25608 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

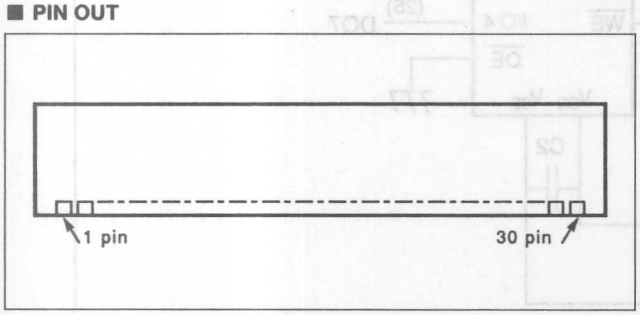
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . .60/70/80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .990/880/726/605/517/mW (max.)
  - Standby Mode. . . . . .22mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25608A-6H	60ns	30 pin SIP Lead Type
HB56D25608A-7H	70ns	
HB56D25608A-8A	80ns	
HB56D25608A-10A	100ns	
HB56D25608A-12A	120ns	
HB56D25608B-6H	60ns	30 pin SIP Socket Type
HB56D25608B-7H	70ns	
HB56D25608B-8A	80ns	
HB56D25608B-10A	100ns	
HB56D25608B-12A	120ns	

■ PIN OUT

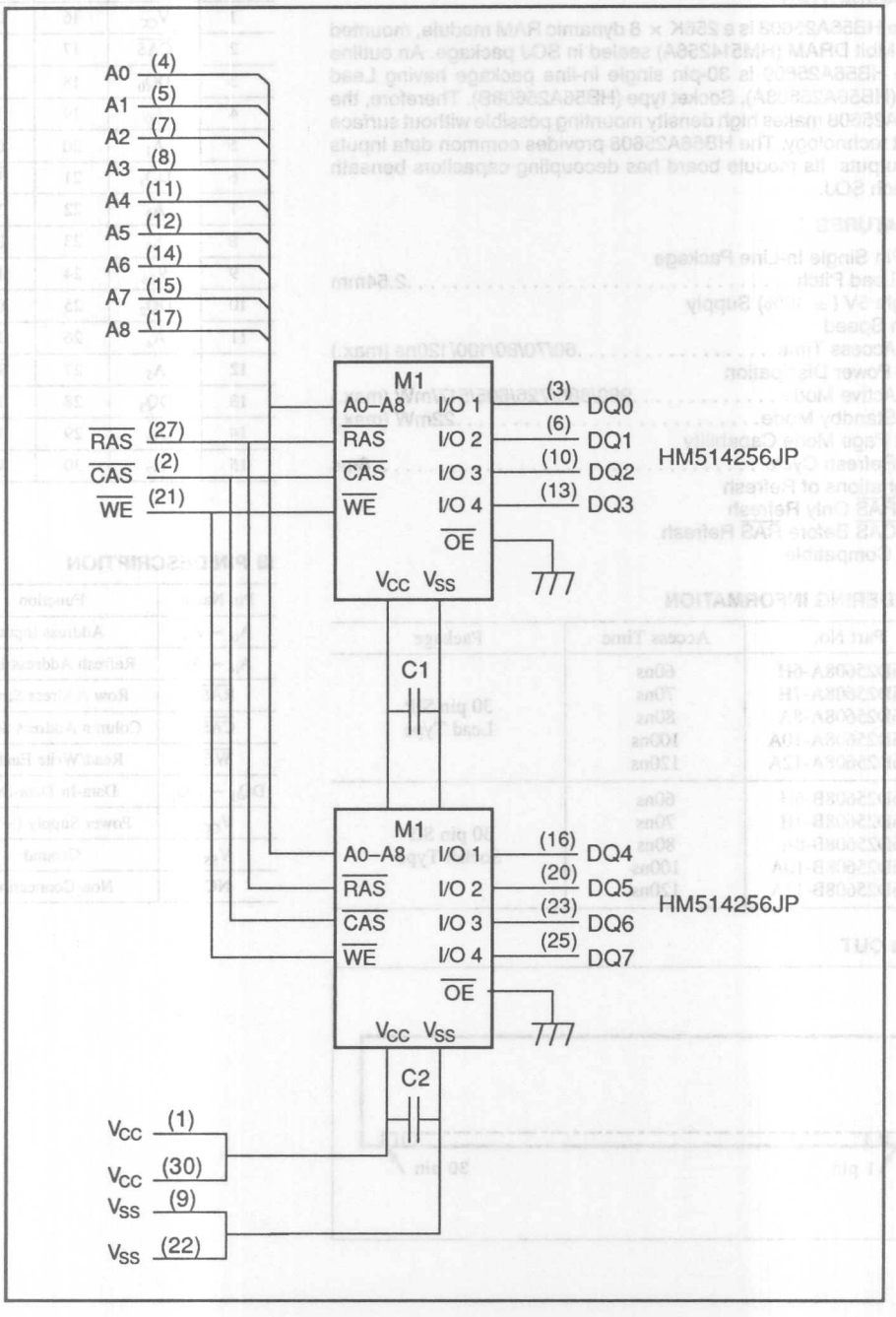


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	NC
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

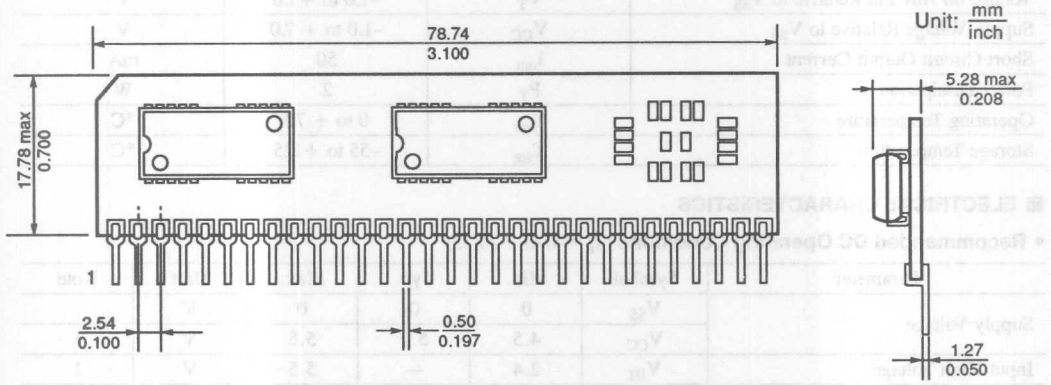
Pin Name	Function
A_0 ~ A_8	Address Input
A_0 ~ A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0 ~ DQ_7	Data-In/Data-Out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

■ BLOCK DIAGRAM

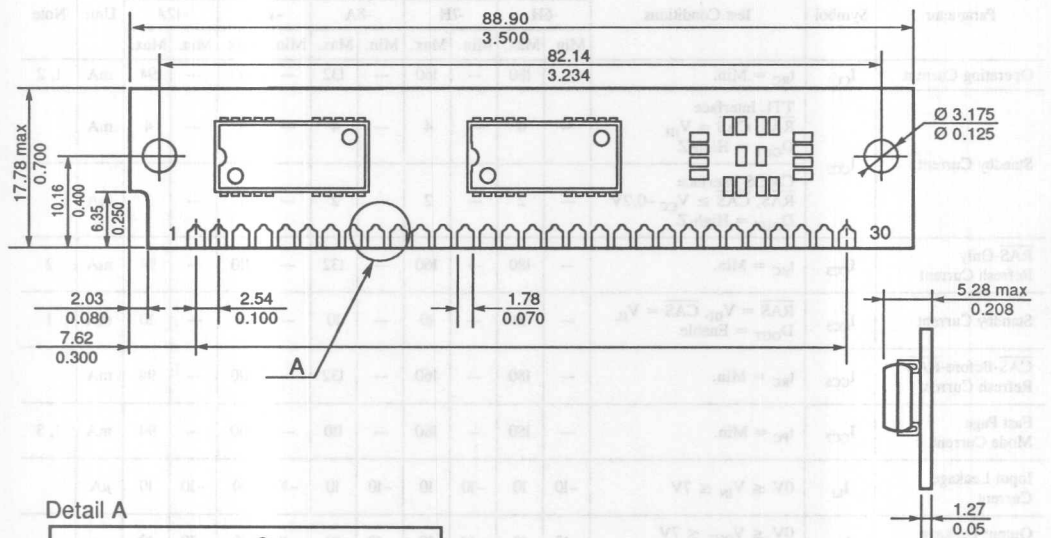


■ PHYSICAL OUTLINE

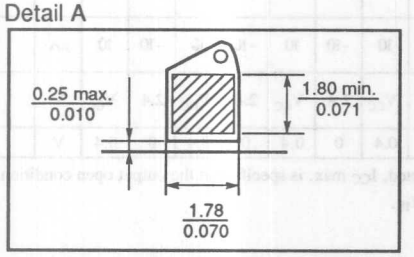
• HB56D25608A Series



• HB56D25608B Series



Detail A



NOTE: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	2	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56D25608A/B										Unit	Note
			-6H		-7H		-8A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	180	—	160	—	132	—	110	—	94	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	—	4	—	4	—	4	—	4	—	4	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	2	—	2	—	2	—	2	—	2	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	180	—	160	—	132	—	110	—	94	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	10	—	10	—	10	—	10	—	10	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	180	—	160	—	132	—	110	—	94	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	180	—	160	—	110	—	110	—	94	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	25	pF	1
Input Capacitance (Clock)	C_{I2}	—	30	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O1}$	—	17	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (1), (12)

• Read, Write and Refresh Cycle (Common Parameter)

Parameter	Symbol	HB56D25608A/B										Unit	Note
		-6H		-7H		-8A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	125	—	140	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	55	—	60	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ns	15

• Read Cycle

Parameter	Symbol	HB56D25608A/B										Unit	Note
		-6H		-7H		-8A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

• Write Cycle

Parameter	Symbol	HB56D25608A/B										Unit	Note
		-6H		-7H		-8A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

• Refresh Cycle

Parameter	Symbol	HB56D25608A/B										Unit	Note
		-6H		-7H		-8A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

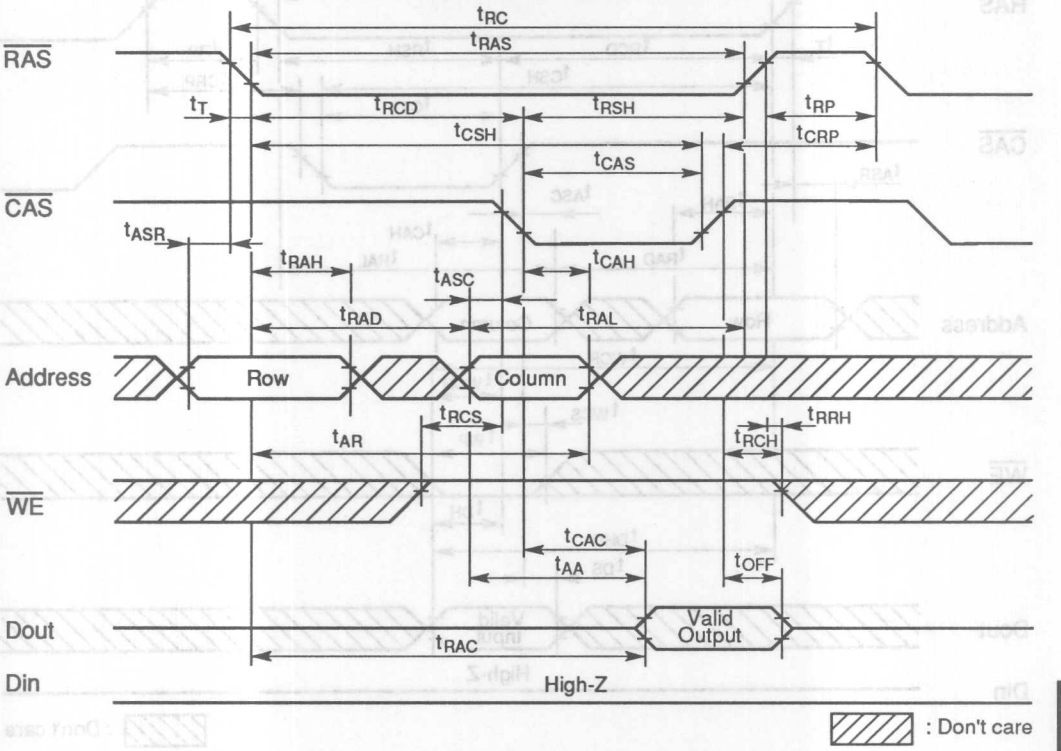
Parameter	Symbol	HB56D25608A/B										Unit	Note
		-6H		-7H		-8A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	60	100000	70	100000	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

NOTES:

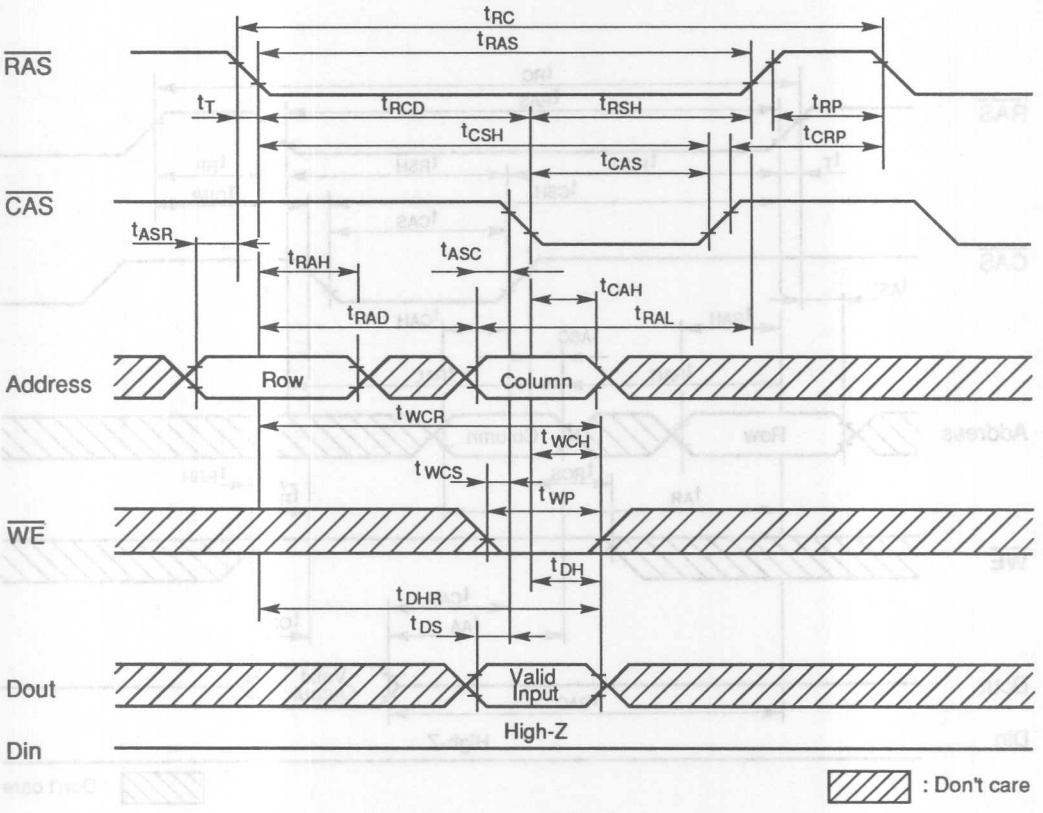
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min.))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 512 refresh cycles.

■ TIMING WAVEFORMS

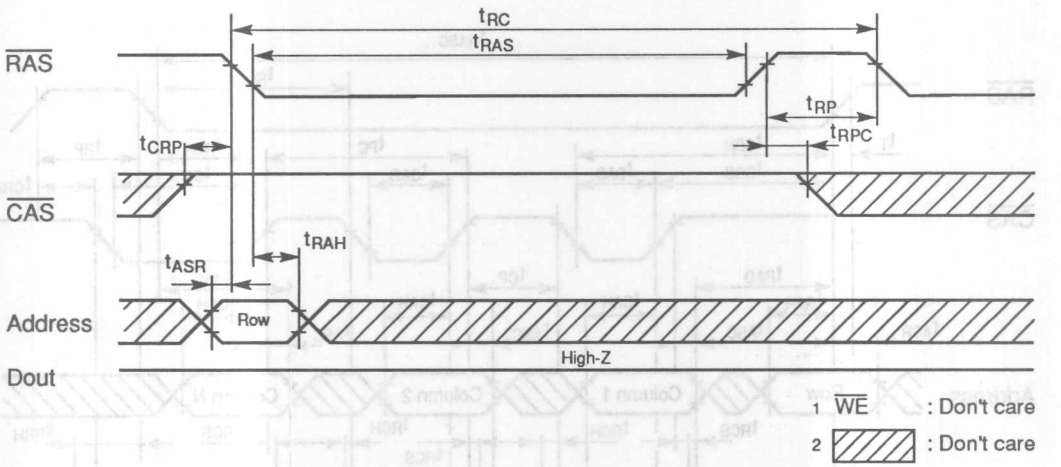
• **Read Cycle**



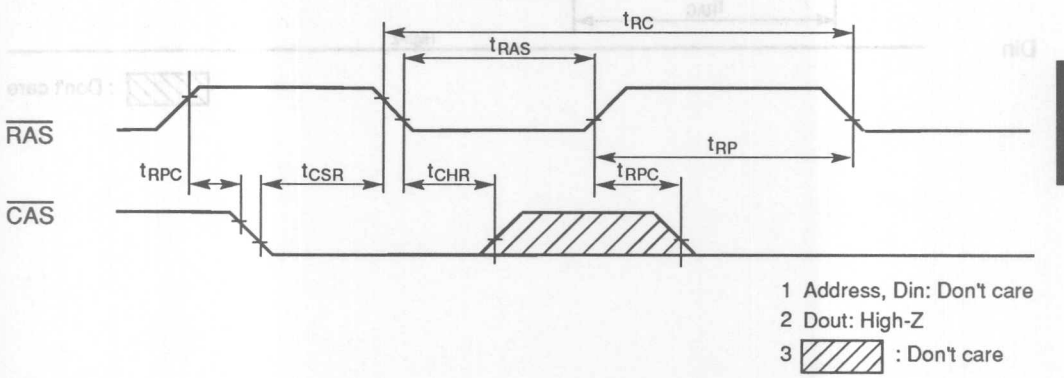
• **Early Write Cycle**



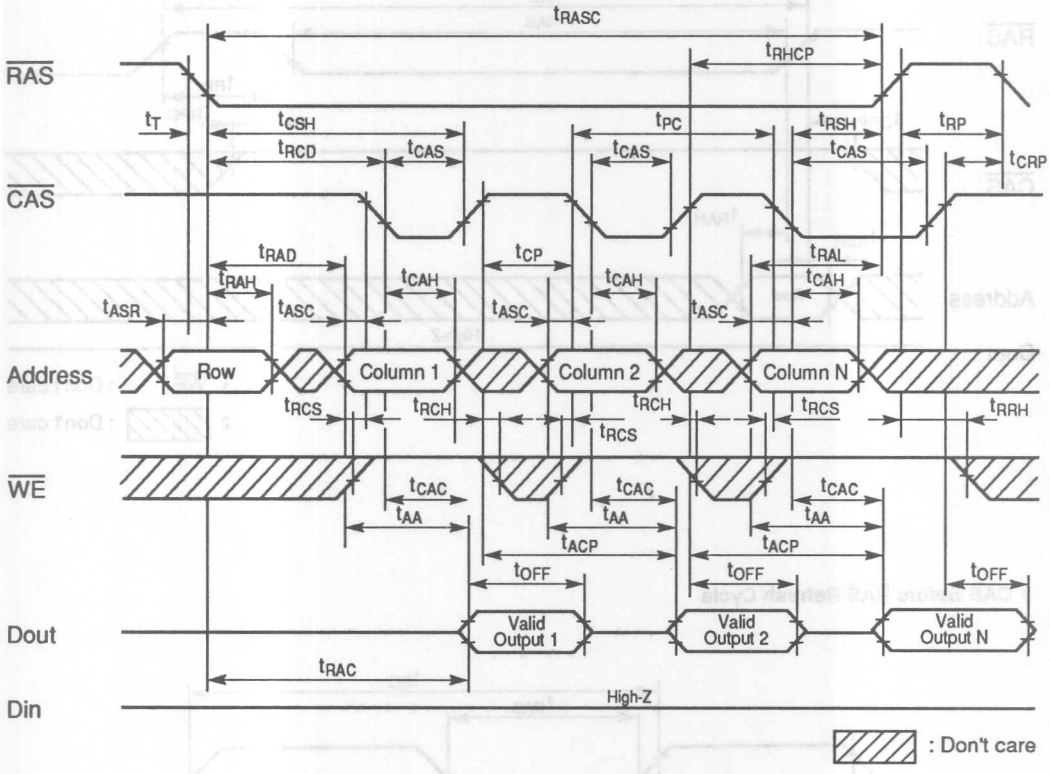
• **$\overline{RAS}$ Only Refresh Cycle**



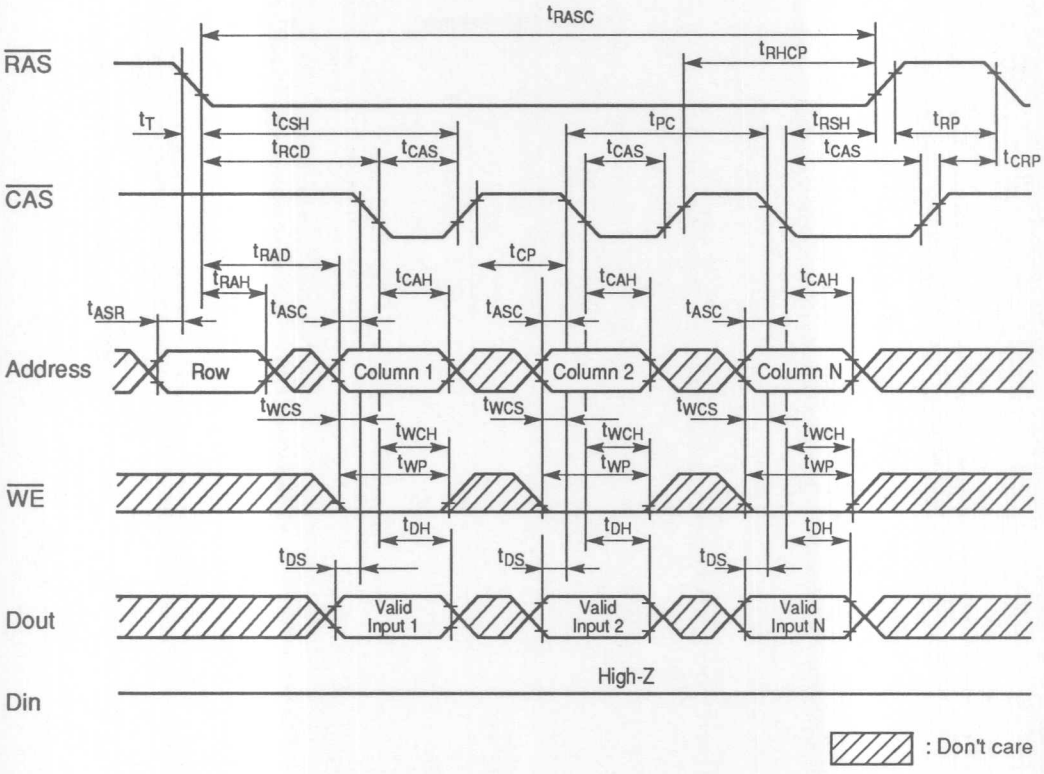
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D25609A/B-85A/10A/12A

262,144-Word × 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A25609 is a 256K × 9 dynamic RAM module, mounted two 1-Mbit DRAM (HM514256A) sealed in SOJ package and 256Kbit DRAM (HM51256) sealed in PLCC package. An outline of the HB56A25609 is 30-pin single in-line package having Lead types (HB56A25609A), Socket type (HB56A25609B). Therefore, the HB56A25609 makes high density mounting possible without surface mount technology. The HB56A25609 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ and PLCC.

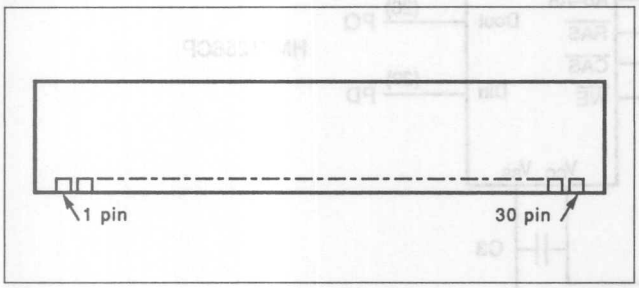
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time. . . . . 85/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 1.11/0.94/0.79mW (max.)
  - Standby Mode. . . . . 33mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25609A-85A	85ns	30 pin SIP Lead Type
HB56D25609A-10A	100ns	
HB56D25609A-12A	120ns	
HB56D25609B-85A	85ns	30 pin SIP Socket Type
HB56D25609B-10A	100ns	
HB56D25609B-12A	120ns	

■ PIN OUT

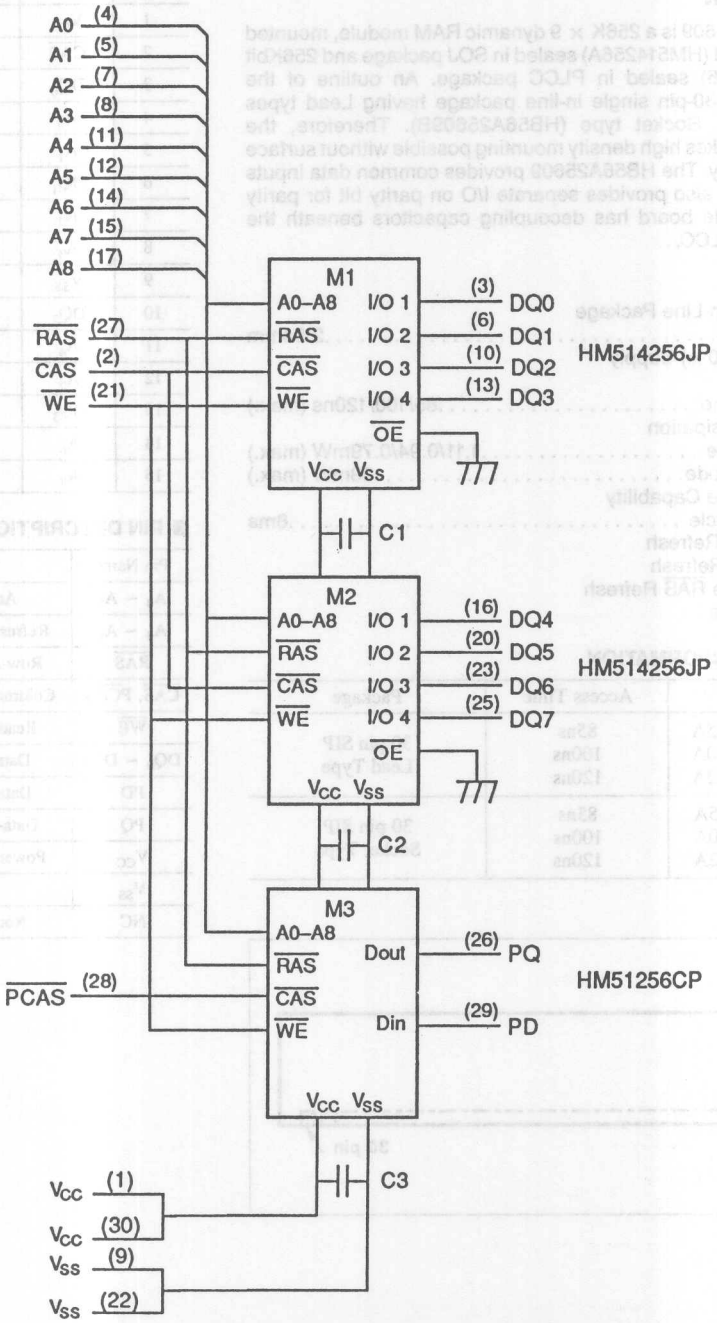


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	NC
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_8	Address Input
A_0 ~ A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0 ~ DQ_7	Data-In/Data-Out
PD	Data-In for Parity
PQ	Data-Out for Parity
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

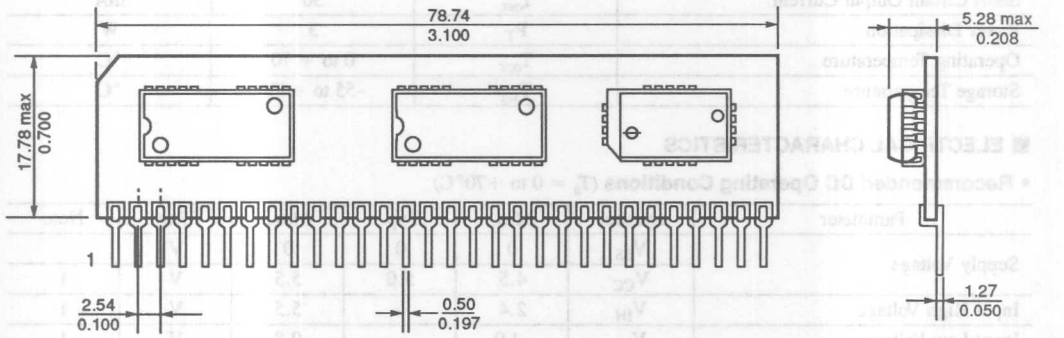
■ BLOCK DIAGRAM



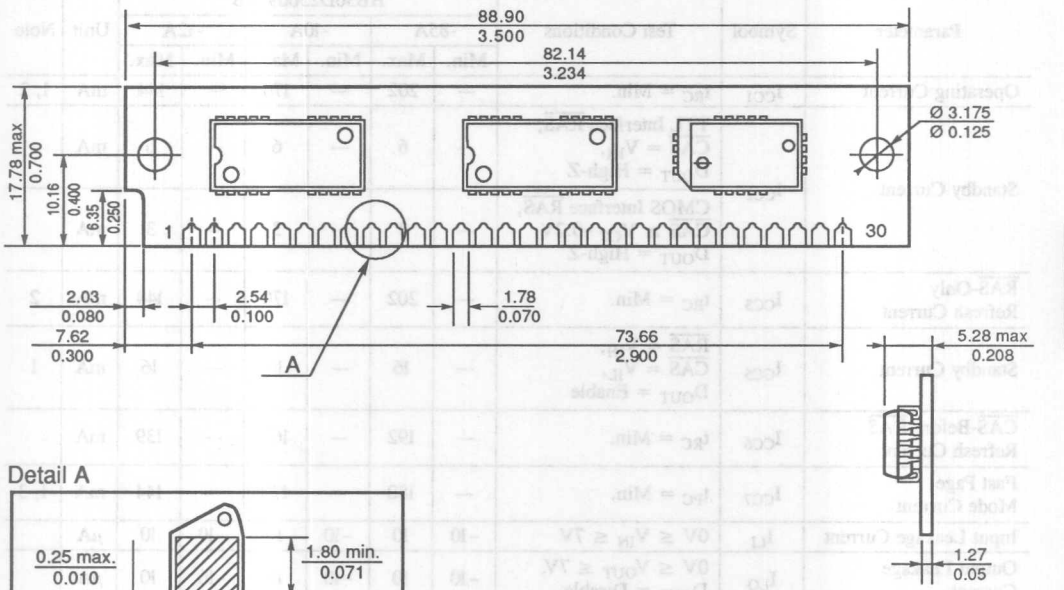
■ PHYSICAL OUTLINE

• HB56D25609A Series

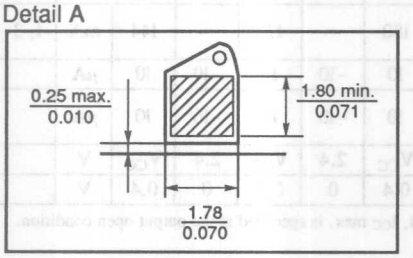
Unit: mm / inch



• HB56D25609B Series



Detail A



NOTE: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	3	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56D25609A/B						Unit	Note
			-85A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	202	—	170	—	144	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	6	—	6	—	6	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	3	—	3	—	3	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	202	—	170	—	144	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	16	—	16	—	16	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	192	—	165	—	139	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	180	—	170	—	144	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	30	pF	1
Input Capacitance (Clock)	C_{I2}	—	36	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1, 2
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (1), (12)

• Read, Write and Refresh Cycle (Common Parameter)

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

• Read Cycle

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	20	—	20	—	25	—	ns	11
Data-In Hold Time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

• Refresh Cycle

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

• Fast Page Mode Cycle

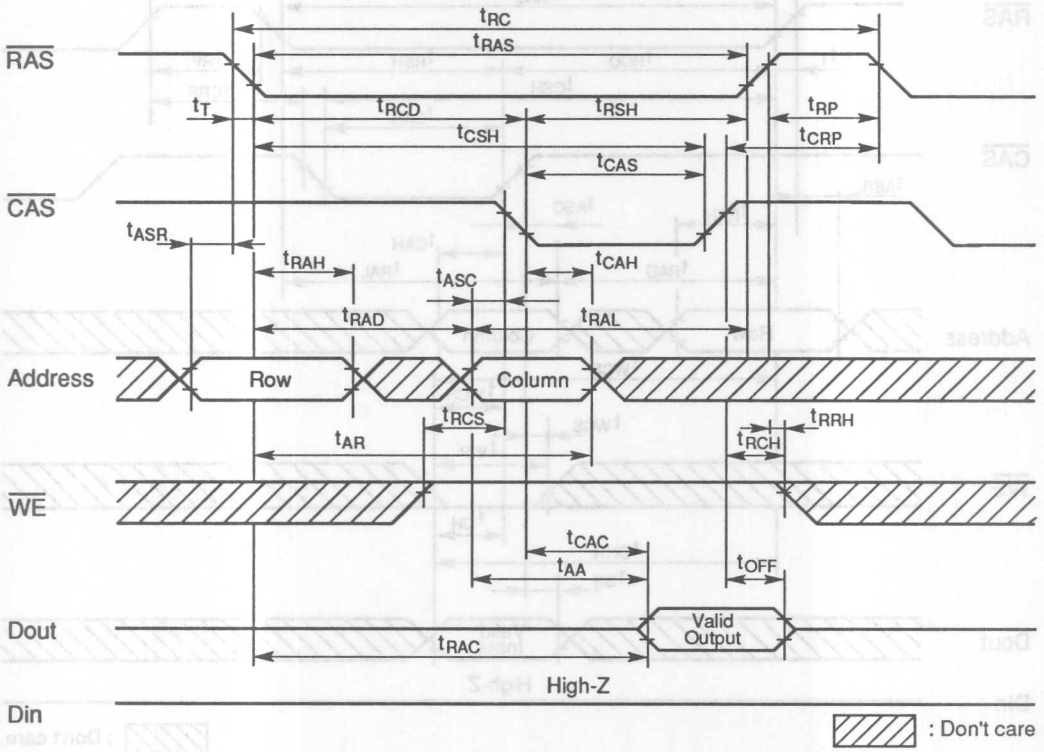
Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

NOTES:

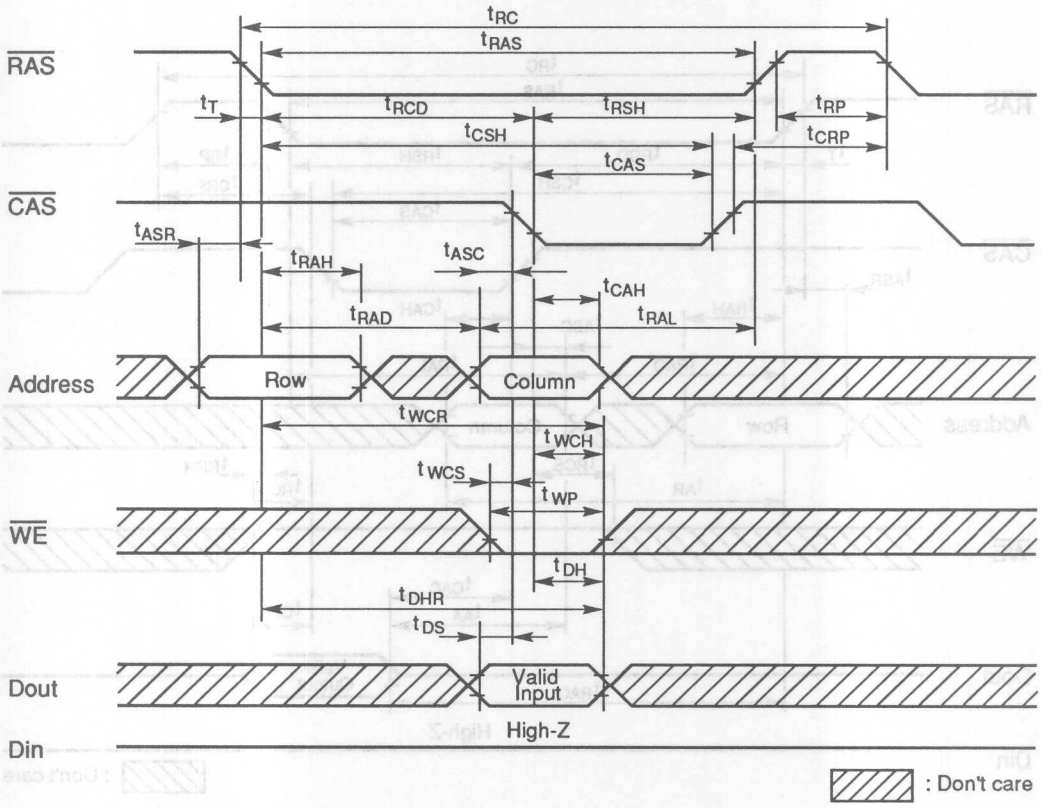
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$(min.))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 512 refresh cycles.

■ TIMING WAVEFORMS

• **Read Cycle**

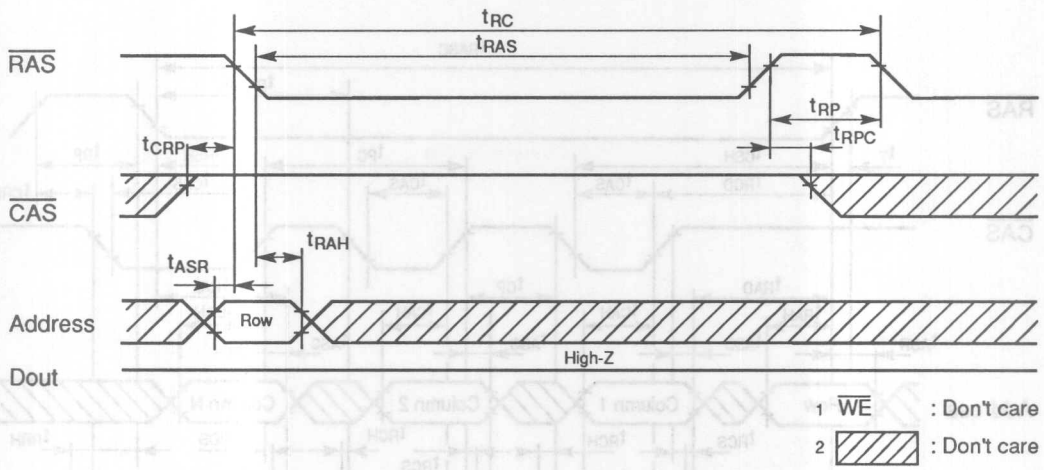


• **Early Write Cycle**

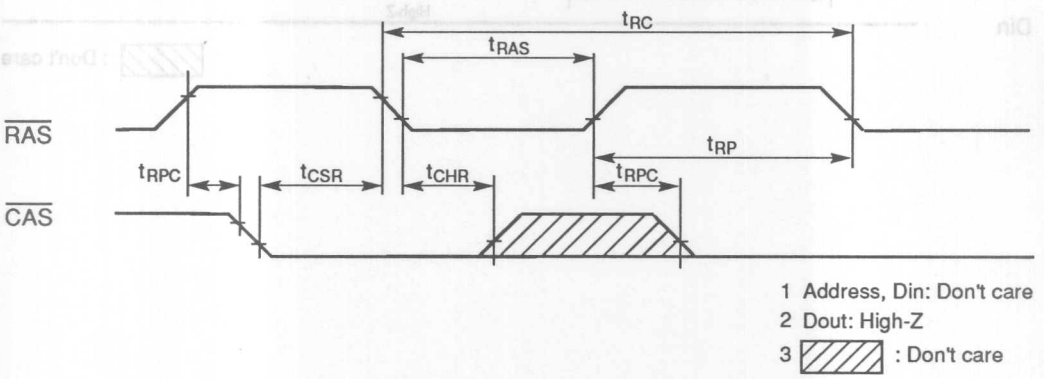


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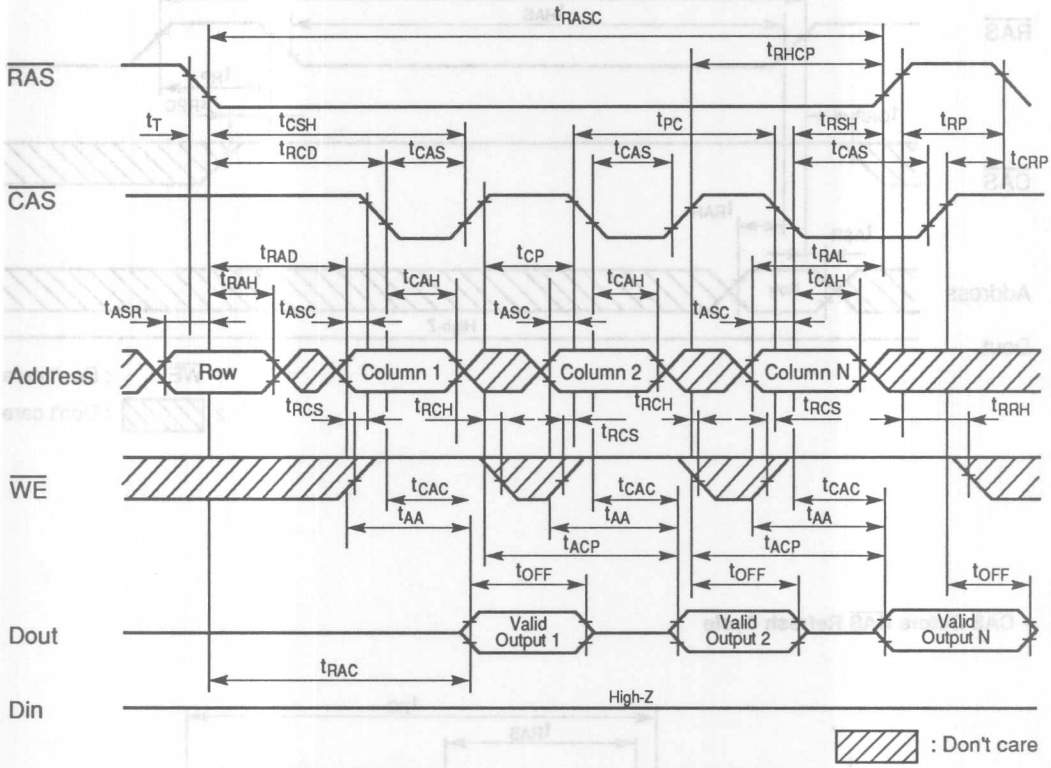
• **$\overline{RAS}$ Only Refresh Cycle**



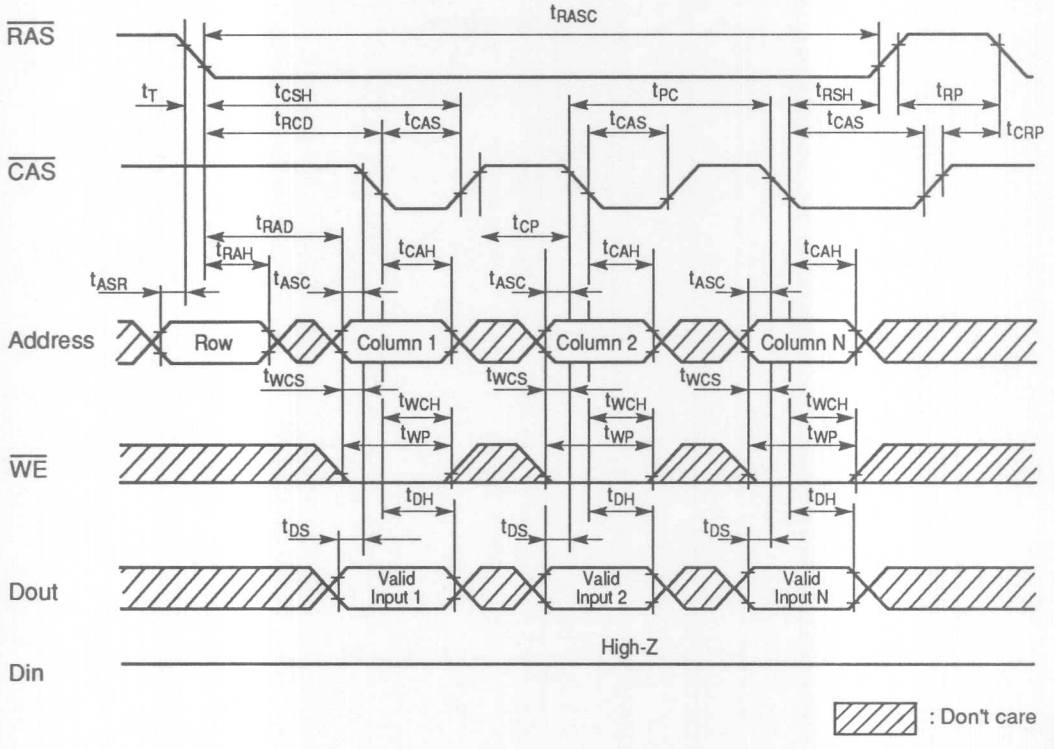
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D25636B-85/10/12

262,144-Word × 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D25636B is a 256K × 36 dynamic RAM module, mounted 8 pieces of 1Mbit DRAM (HM514256JP) sealed in SOJ package and 4 pieces of 256Kbit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D25636B is 72-pin single in-line package. Therefore, the HB56D25636B makes high density mounting possible without surface mount technology. The HB56D25636B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and PLCC.

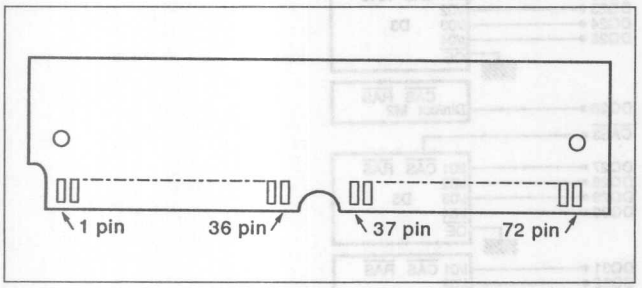
■ FEATURES

- 72-Pin Single In-Line Package
  - Lead Pitch 1.27mm
- Single 5V (± 5%) Supply
- High Speed
  - Access Time. . . . . 85/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 4.24/3.57/3.02mW (max.)
  - Standby Mode . . . . . 126mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{\text{RAS}}$ Only Refresh
  - $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

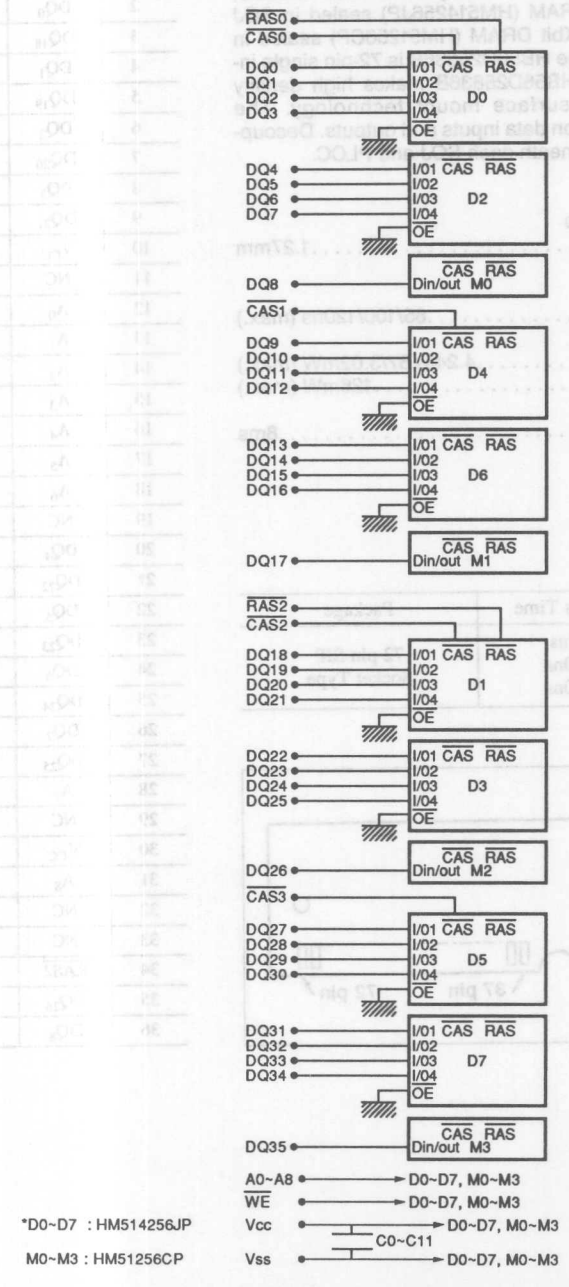
Part No.	Access Time	Package
HB56D25636B-85	85ns	72 pin SIP Socket Type
HB56D25636B-10	100ns	
HB56D25636B-12	120ns	

■ PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS0}$
5	DQ_{19}	41	$\overline{CAS2}$
6	DQ_2	42	$\overline{CAS3}$
7	DQ_{20}	43	$\overline{CAS1}$
8	DQ_3	44	$\overline{RAS0}$
9	DQ_{21}	45	NC
10	V_{CC}	46	NC
11	NC	47	$\overline{WE}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	NC	68	PD_2
33	NC	69	PD_3
34	$\overline{RAS2}$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}

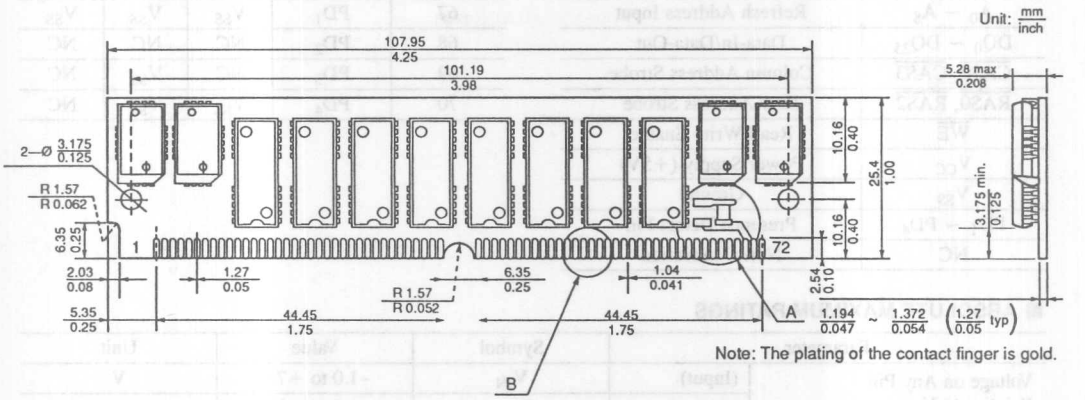
■ BLOCK DIAGRAM



*D0~D7 : HM514256JP

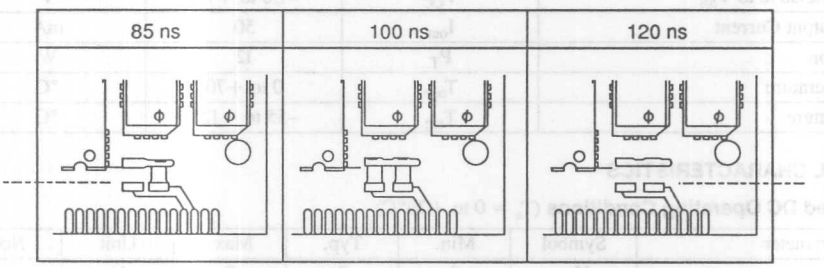
M0~M3 : HM51256CP

■ PHYSICAL OUTLINE

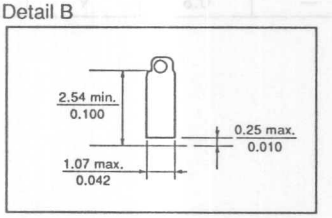


Note: The plating of the contact finger is gold.

Detail A



Detail B



■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_8$	Address Input
$A_0 \sim A_8$	Refresh Address Input
$DQ_0 \sim DQ_{35}$	Data-In/Data-Out
$\overline{CAS0}$, $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
$PD_1 \sim PD_4$	Presence Detect Pin
NC	Non-Connection

■ PRESENCE DETECT PIN ARRANGEMENT

Pin No.	Pin Name	HB56D25636B		
		85ns	100ns	120ns
67	PD_1	V_{SS}	V_{SS}	V_{SS}
68	PD_2	NC	NC	NC
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{IN}	−1.0 to +7.0	V
	(Output)	V_{OUT}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **Recommended DC Operating Conditions** (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56D25636B						Unit	Note
			-85		-10		-12			
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	808	—	680	—	576	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	24	—	24	—	24	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} -0.2V D_{OUT} = High-Z	—	12	—	12	—	12	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	808	—	680	—	576	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	64	—	64	—	64	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	768	—	660	—	556	mA	
Page Mode Current	I_{CC7}	t_{PC} = Min.	—	764	—	680	—	576	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = -5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output Capacitance (DQ_0-DQ_7, DQ_9-DQ_{16}, DQ_{18}-DQ_{25}, DQ_{27}-DQ_{34})	$C_{I/O1}$	—	17	pF	1, 2
Output Capacitance (DQ_8, DQ_{17}, DQ_{26}, DQ_{35})	$C_{I/O2}$	—	22	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) [1], [12]

• Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

• Read Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Refresh Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

• Write Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	20	—	20	—	25	—	ns	11
Data-In Hold Time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

• Fast Page Mode Cycle

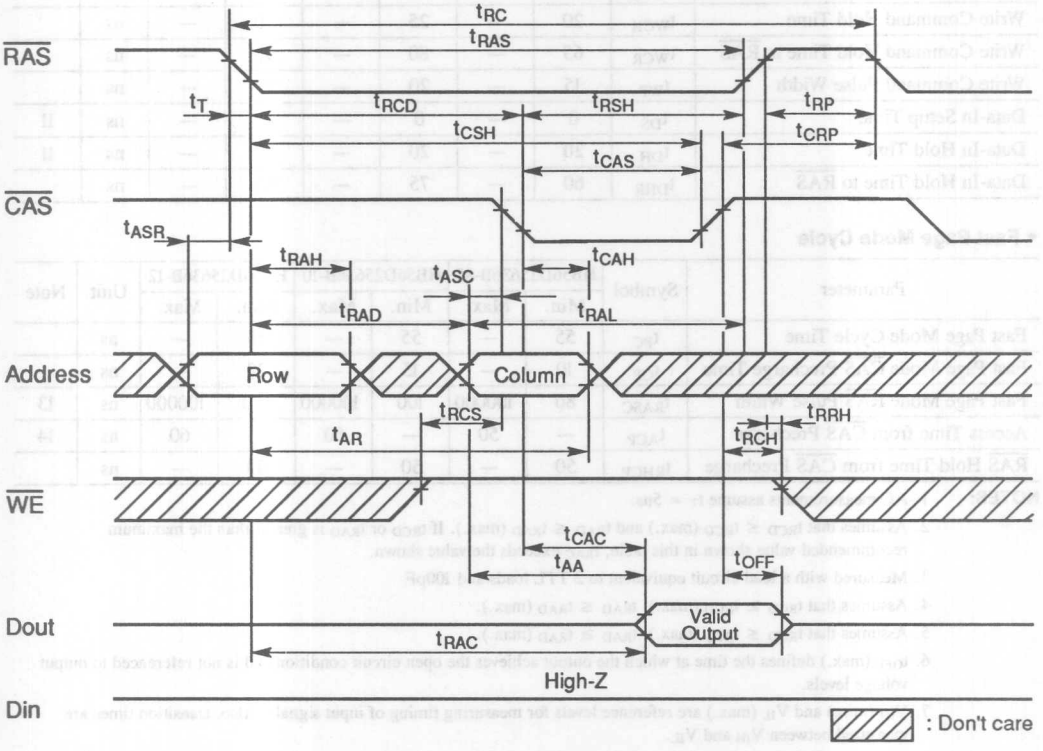
Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

NOTES:

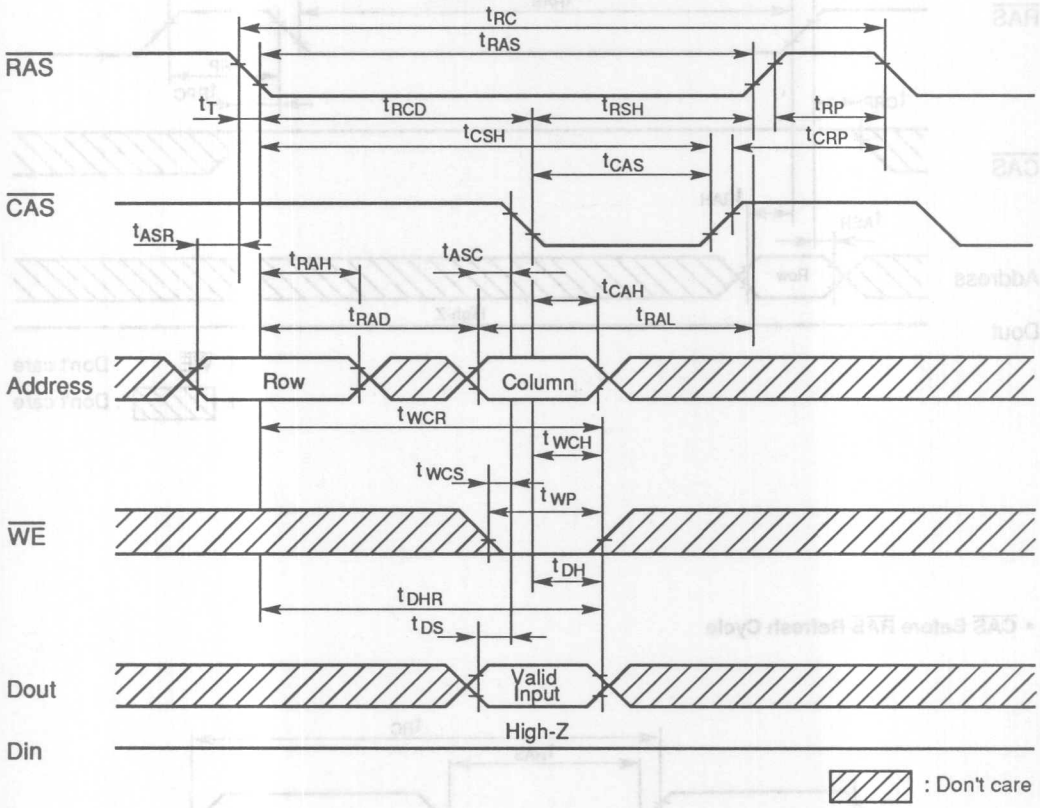
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min.)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 512 refresh cycles.

■ TIMING WAVEFORMS

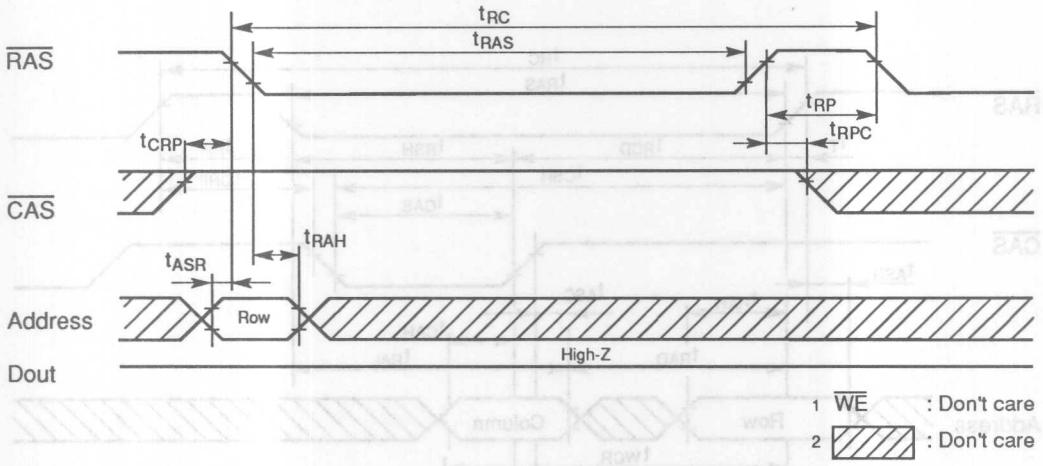
• **Read Cycle**



• **Early Write Cycle**

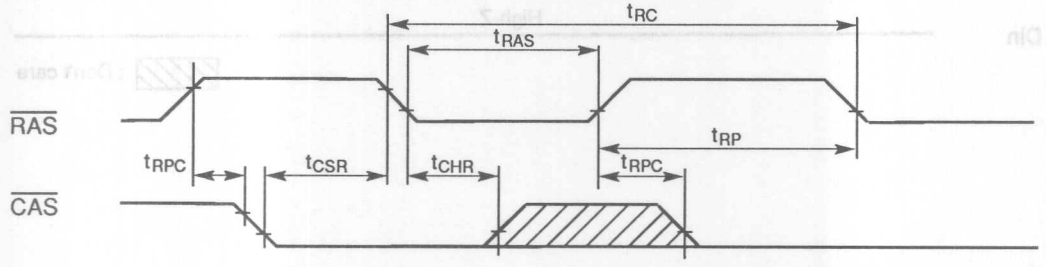


• $\overline{RAS}$ Only Refresh Cycle



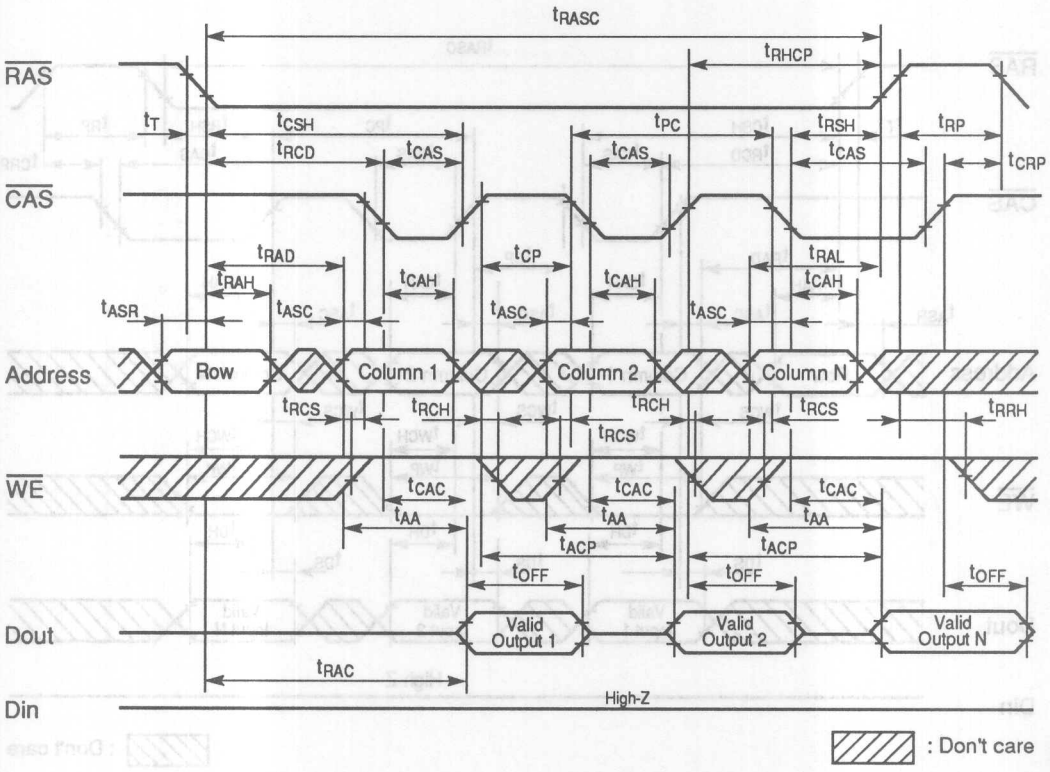
1 $\overline{WE}$: Don't care
2 ▨ : Don't care

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

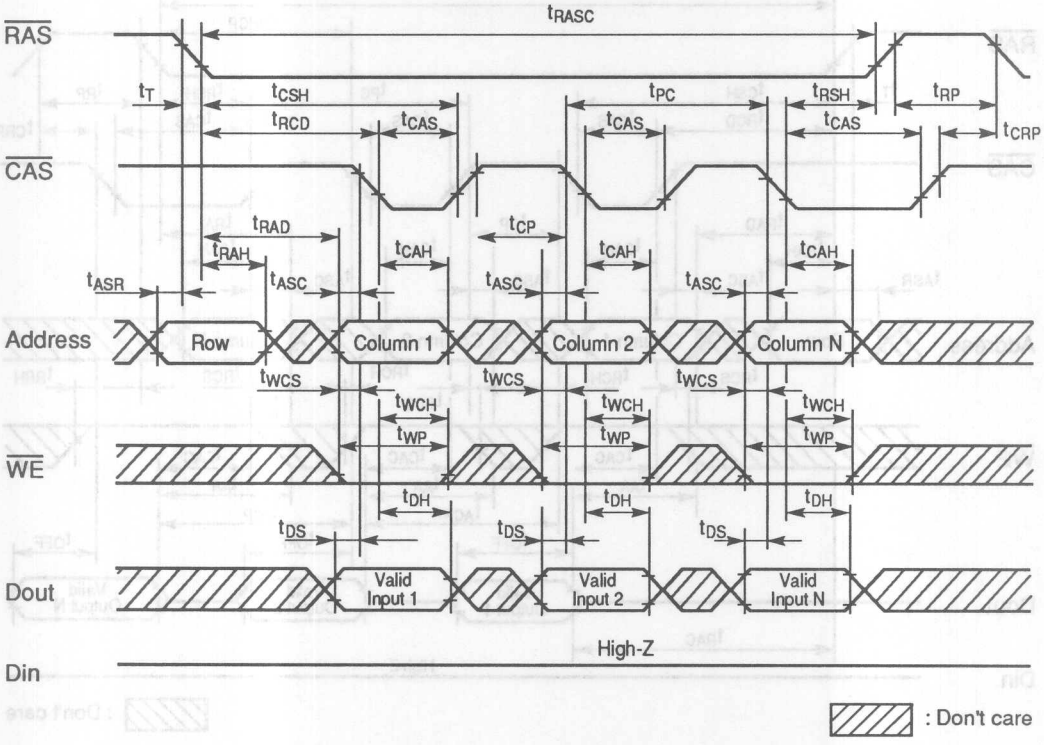


1 Address, Din: Don't care
2 Dout: High-Z
3 ▨ : Don't care

• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D51236B-85/10/12

524,288-Word × 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D51236B is a 512K × 36 dynamic RAM module, mounted 16 pieces of 1Mbit DRAM (HM514256JP) sealed in SOJ package and 8 pieces of 256Kbit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D51236B is 72-pin single in-line package. Therefore, the HB56D51236B makes high density mounting possible without surface mount technology. The HB56D51236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and PLCC but only on the one side of its module board.

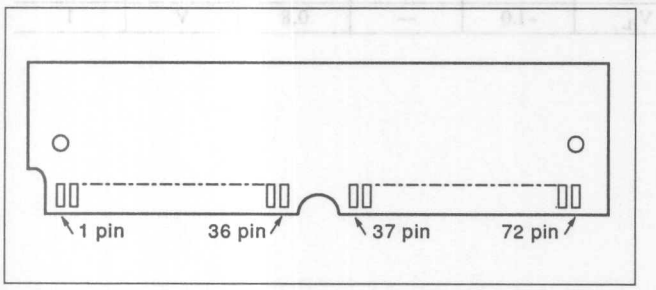
■ FEATURES

- 72-Pin Single In-Line Package
  - Lead Pitch 1.27mm
- Single 5V (± 5%) Supply
- High Speed
  - Access Time. . . . . .85/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .4.58/3.91/3.36W (max.)
  - Standby Mode. . . . . .252mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{\text{RAS}}$ Only Refresh
  - $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D51236B-85	85ns	72 pin SIP Socket Type
HB56D51236B-10	100ns	
HB56D51236B-12	120ns	

■ PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{\text{CAS0}}$
5	DQ_{19}	41	$\overline{\text{CAS2}}$
6	DQ_2	42	$\overline{\text{CAS3}}$
7	DQ_{20}	43	$\overline{\text{CAS1}}$
8	DQ_3	44	$\overline{\text{RAS0}}$
9	DQ_{21}	45	$\overline{\text{RAS1}}$
10	V_{CC}	46	NC
11	NC	47	$\overline{\text{WE}}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	NC	68	PD_2
33	$\overline{\text{RAS3}}$	69	PD_3
34	$\overline{\text{RAS2}}$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_8$	Address Input
$A_0 \sim A_8$	Refresh Address Input
$DQ_0 \sim DQ_{35}$	Data-In/Data-Out
$\overline{CAS0} \sim \overline{CAS3}$	Column Address Strobe
$\overline{RAS0} \sim \overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
$PD_1 \sim PD_4$	Presence Detect Pin
NC	Non-Connection

■ PRESENCE DETECT PIN ARRENGE

Pin No.	Pin Name	HB56D51236B		
		85ns	100ns	120ns
67	PD_1	NC	NC	NC
68	PD_2	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{IN}	−1.0 to +7.0	V
	(Output)	V_{OUT}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

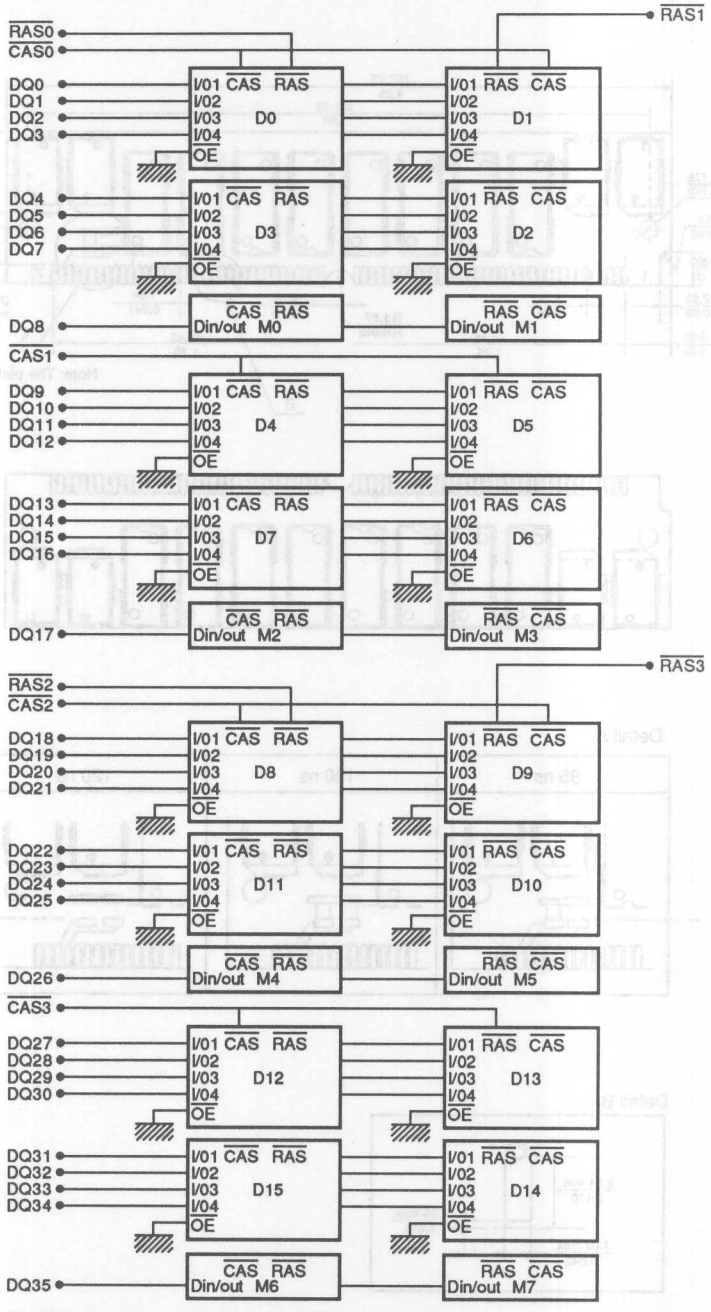
■ ELECTRICAL CHARACTERISTICS

• **Recommended DC Operating Conditions** (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

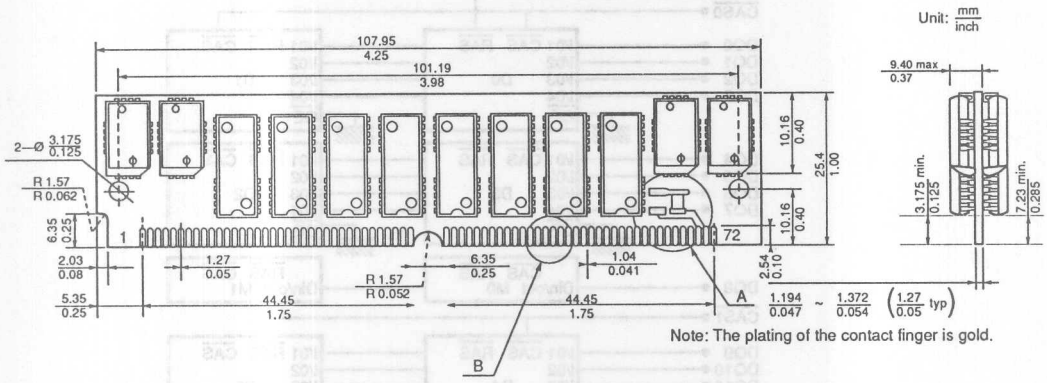
■ BLOCK DIAGRAM



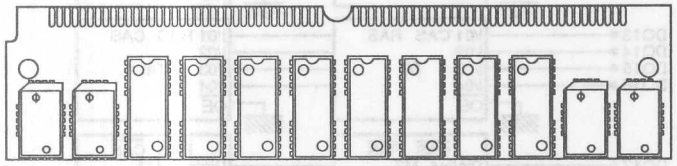
*D0~D15 : HM514256JP

M0~M7 : HM51256CP

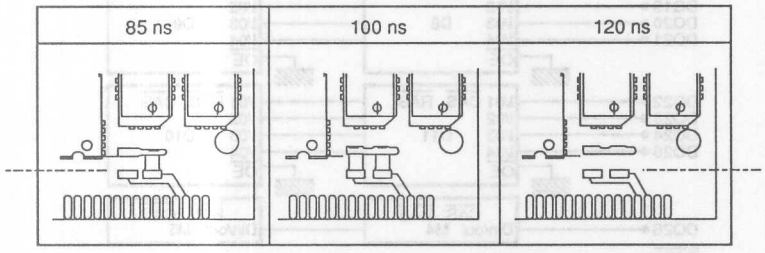
■ PHYSICAL OUTLINE



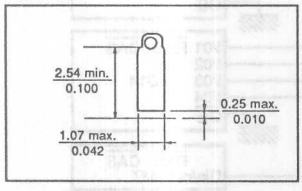
Note: The plating of the contact finger is gold.



Detail A



Detail B



■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56D51236B						Unit	Note
			-85		-10		-12			
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	872	—	744	—	640	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	48	—	48	—	48	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} -0.2V D_{OUT} = High-Z	—	24	—	24	—	24	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	872	—	744	—	640	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	128	—	128	—	128	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	832	—	724	—	620	mA	
Page Mode Current	I_{CC7}	t_{PC} = Min.	—	828	—	744	—	640	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = -5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output Capacitance (DQ_0–DQ_7, DQ_9–DQ_{16}, DQ_{18}–DQ_{25}, DQ_{27}–DQ_{34})	$C_{I/O1}$	—	29	pF	1, 2
Output Capacitance (DQ_8, DQ_{17}, DQ_{26}, DQ_{35})	$C_{I/O2}$	—	39	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) [1], [12]

• Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

• Read Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	20	—	20	—	25	—	ns	11
Data-In Hold Time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

• Refresh Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

• Fast Page Mode Cycle

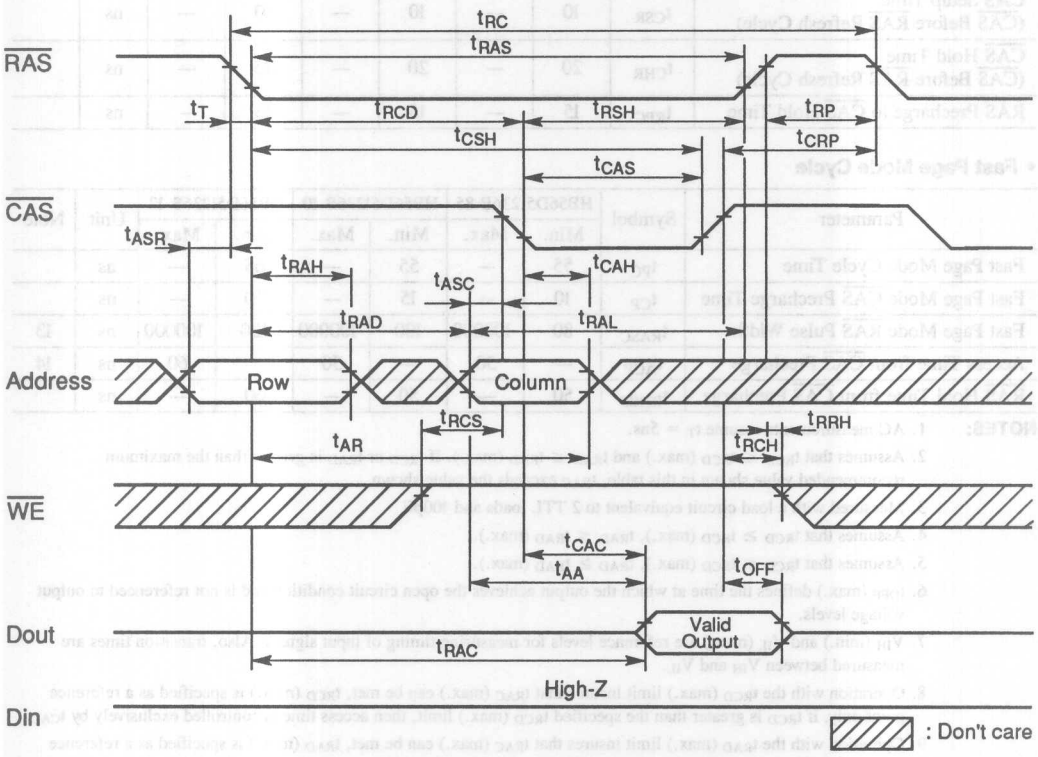
Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

NOTES:

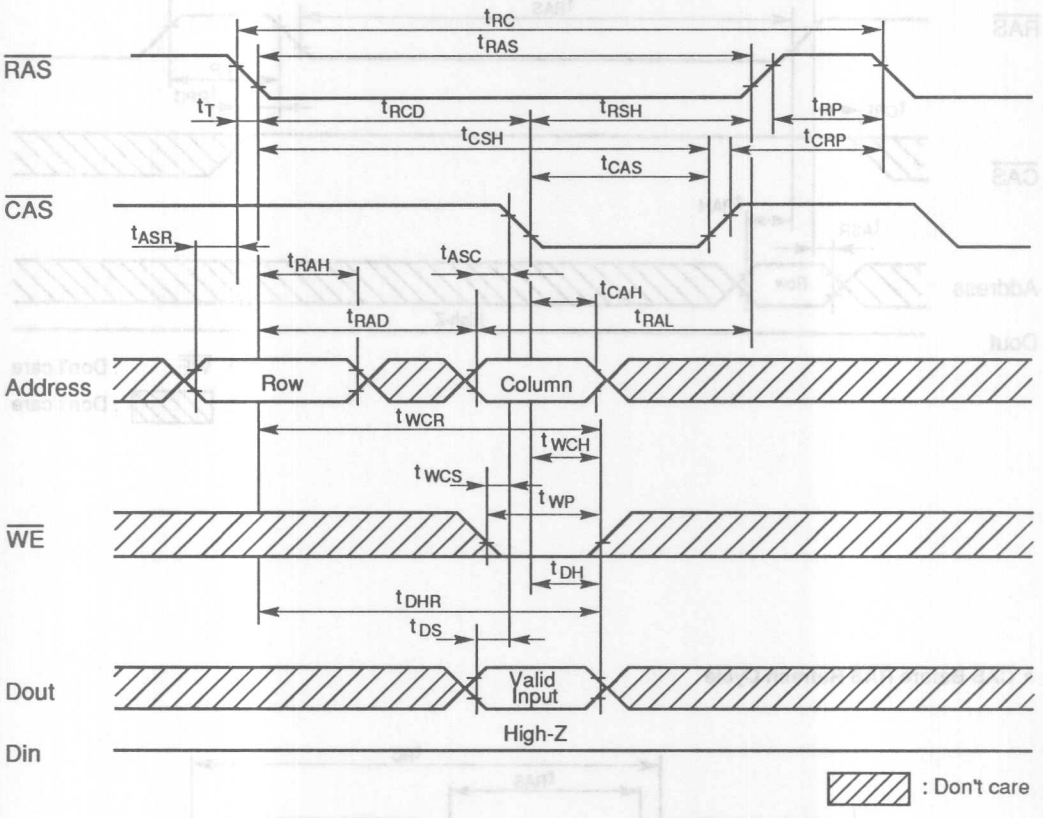
1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min.)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 512 refresh cycles.

■ TIMING WAVEFORMS

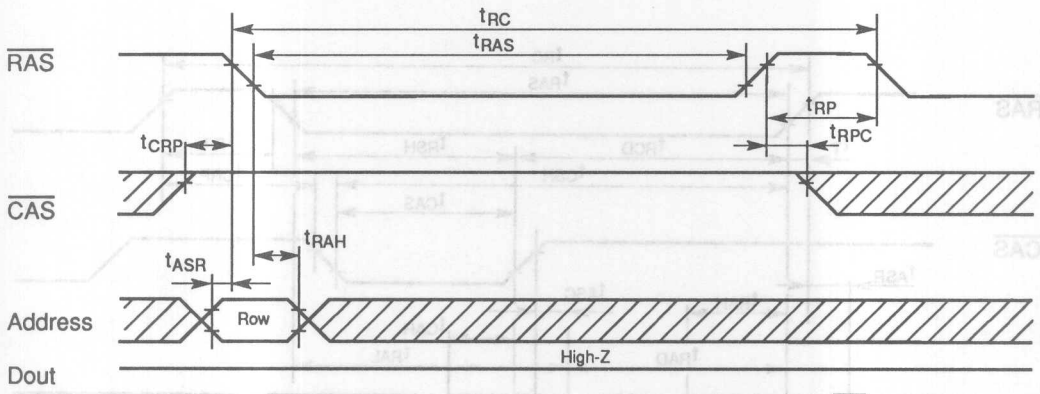
• Read Cycle



• **Early Write Cycle**

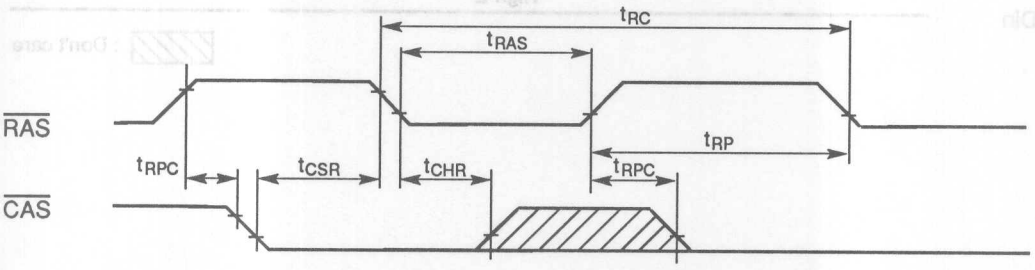


• $\overline{RAS}$ Only Refresh Cycle



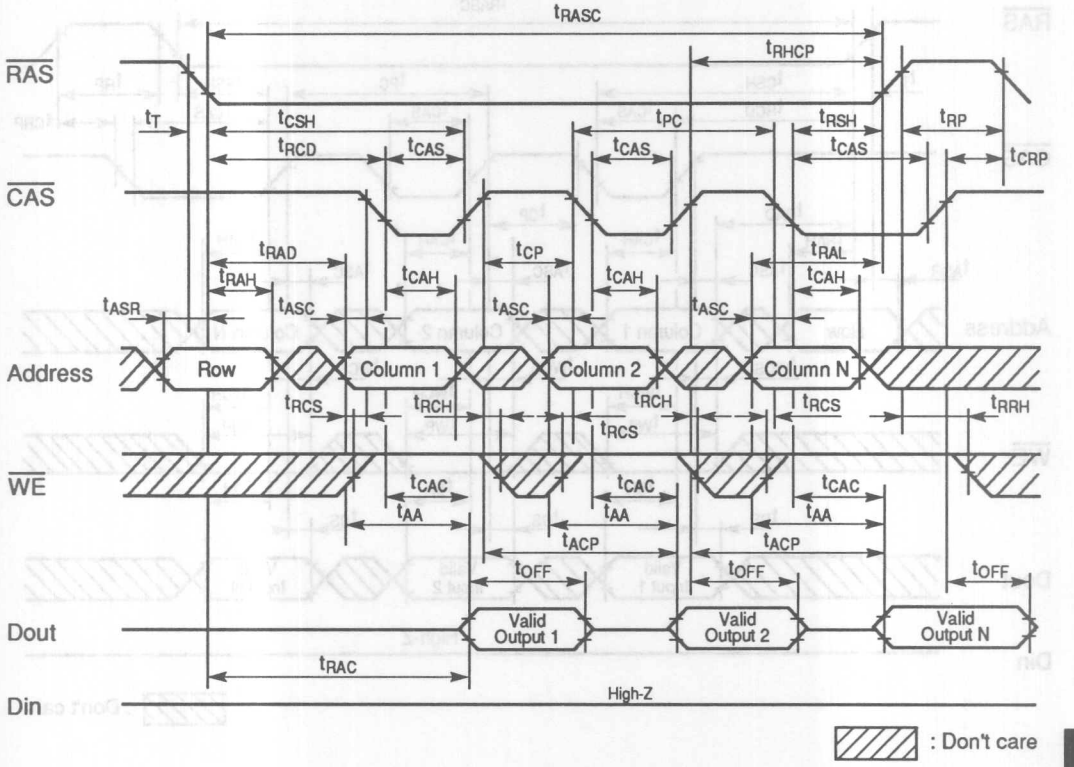
1 $\overline{WE}$: Don't care
2 ▨ : Don't care

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

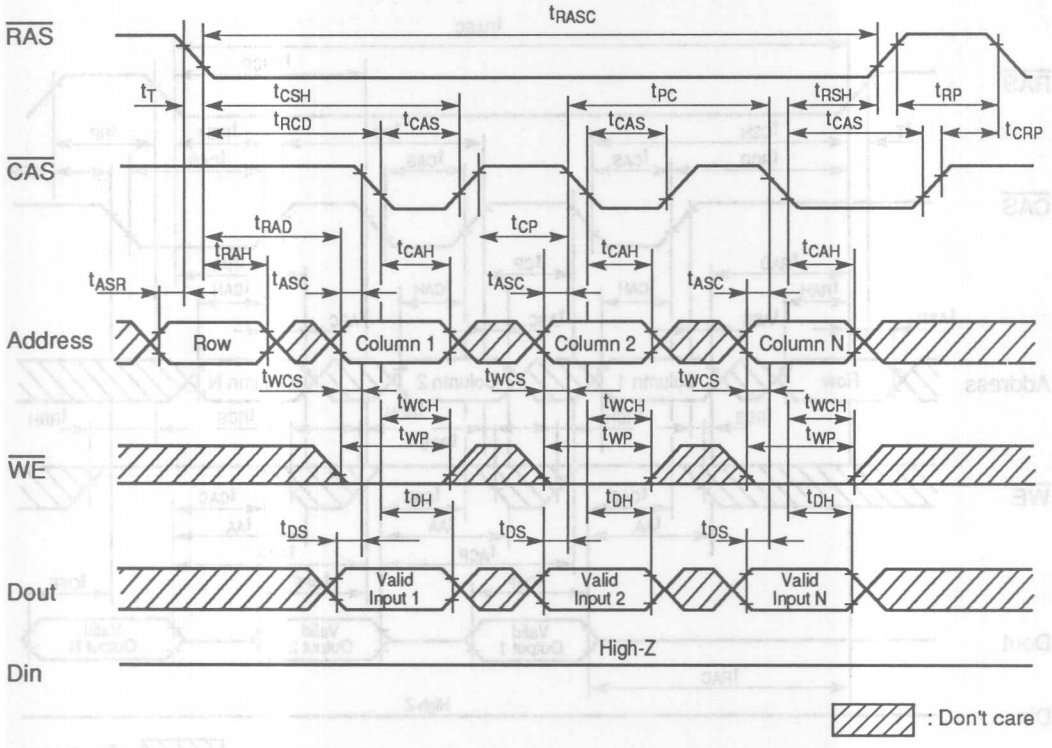


1 Address, Din: Don't care
2 Dout: High-Z
3 ▨ : Don't care

• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56A48A/AT/B-8/10/12
8-Bit DRAM

4,194,304-Word × 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A48 is a 4M × 8 dynamic RAM module, mounted eight 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A48 is 30-pin single in-line package having Lead types (HB56A48A, HB56A48AT), Socket type (HB56A48B). Therefore, the HB56A48 makes high density mounting possible without surface mount technology. The HB56A48 provides common data inputs and outputs. Its module board has decoupling capacitors beneath each SOJ.

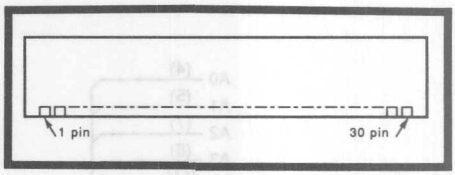
■ FEATURES

- 30-pin single in-line package
  —Lead pitch 2.54mm
- Single 5V (± 10%) supply
- High Speed
  Access time . . . . . 80ns/100ns/120ns (max.)
- Low power dissipation
  —Active mode . . . . . 3.96W/3.52W/3.08W (max.)
  —Standby mode . . . . . 88mW (max.)
- Fast page mode capability
- 1,024 refresh cycle/16ms
- 3 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
  —Hidden refresh
- TTL compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Socket Type
80ns	HB56A48A-8	HB56A48AT-8	HB56A48B-8
100ns	HB56A48A-10	HB56A48AT-10	HB56A48B-10
120ns	HB56A48A-12	HB56A48AT-12	HB56A48B-12

■ PIN OUT

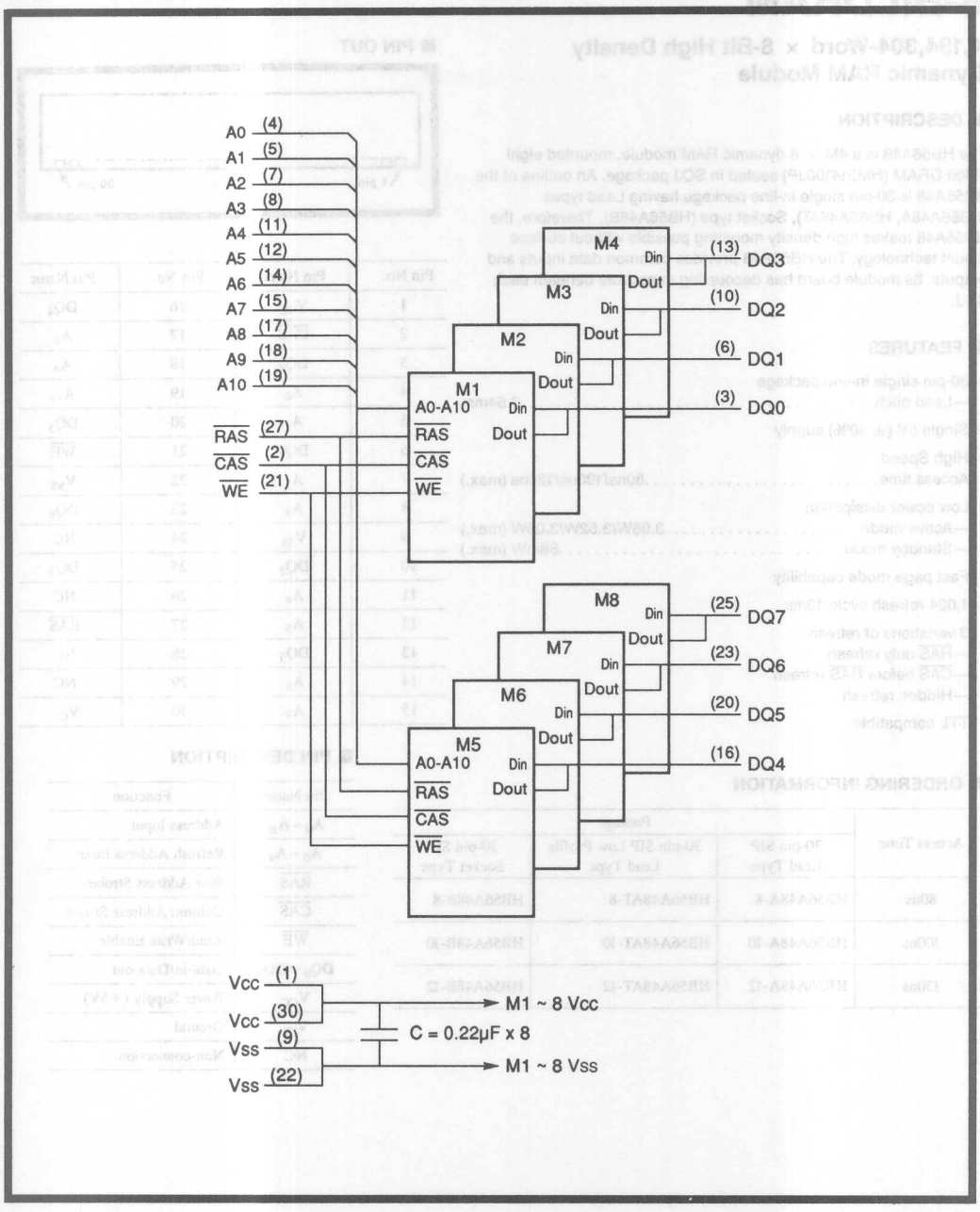


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	A_{10}
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_{10}$	Address Input
$A_0 \sim A_9$	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$DQ_0 \sim DQ_7$	Data-in/Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

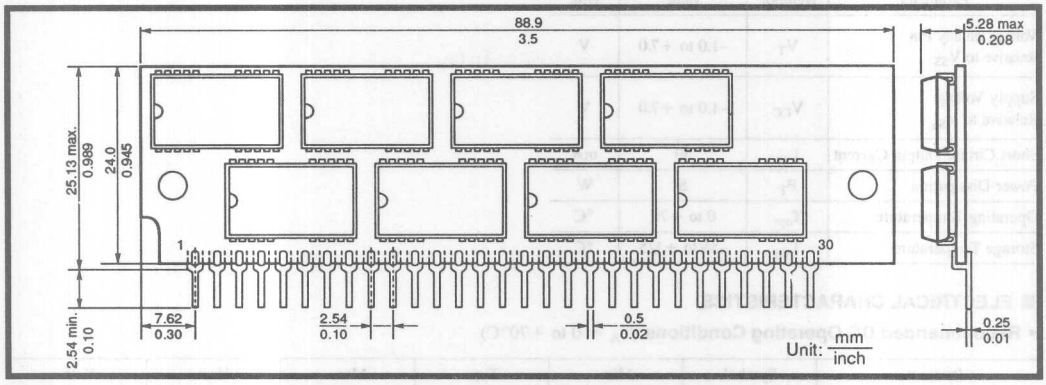
■ BLOCK DIAGRAM



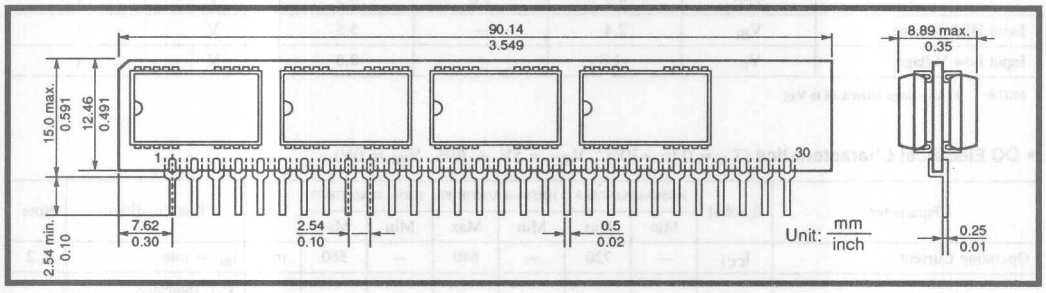
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■ PHYSICAL OUTLINE

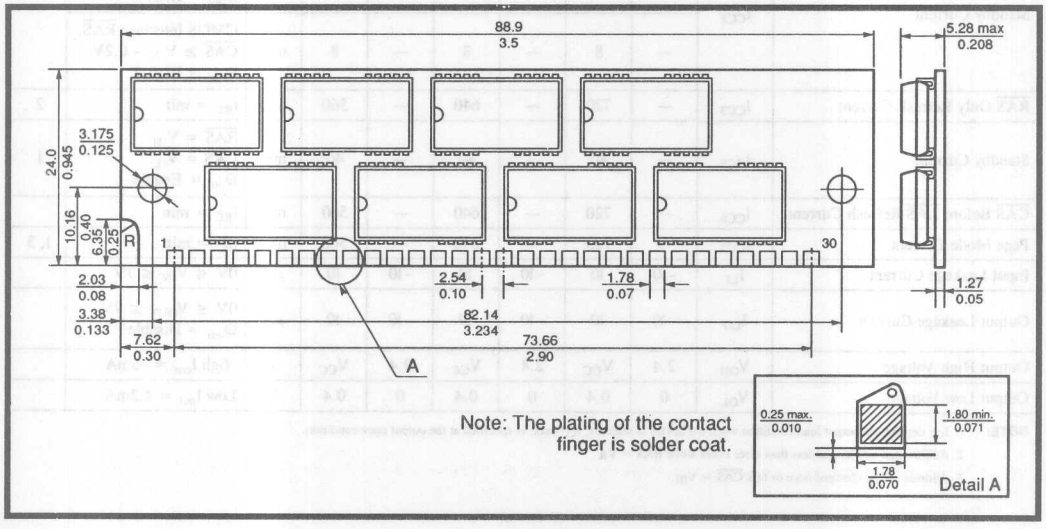
• HB56A48A Series



• HB56A48AT Series



• HB56A48B Series



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	720	—	640	—	560	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	720	—	640	—	560	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	720	—	640	—	560	mA	t_{RC} = min	
Page Mode Current	I_{CC7}	—	720	—	640	—	560	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	65	pF	1
Input Capacitance (Clock)	C_{I2}	—	81	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	30	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) [1, 12, 15]

• Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ns	17

• Read Cycle

Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

• Refresh Cycle

Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14, 16
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

• Test Mode Cycle

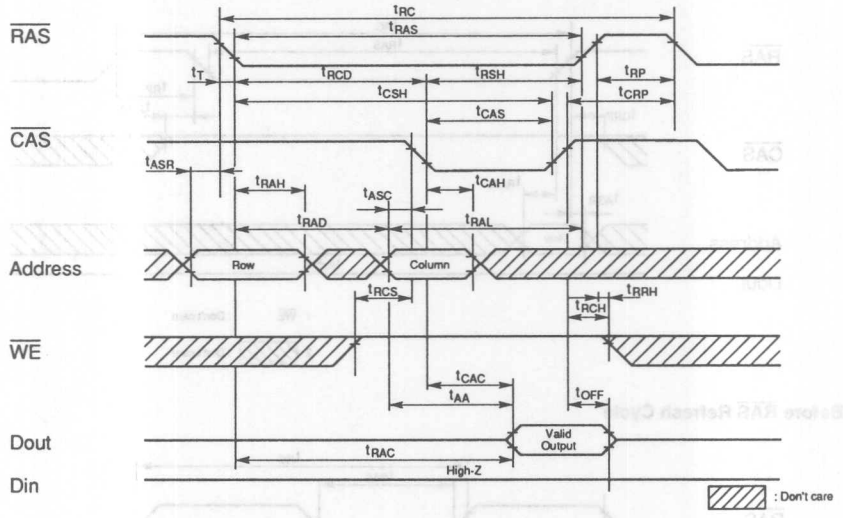
Parameter	Symbol	HB56A48A/AT/B-8		HB56A48A/AT/B-10		HB56A48A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode $\overline{WE}$ Set-up Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

NOTES:

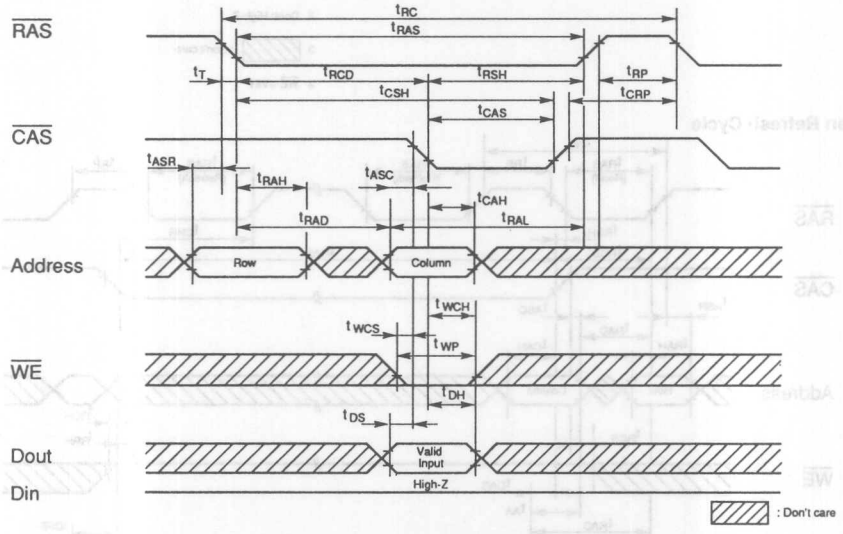
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} defines is 1,024 refresh cycles.

■ TIMING WAVEFORM

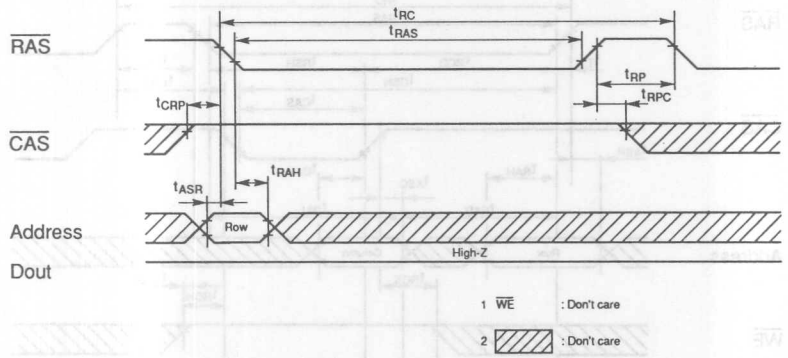
• Read Cycle



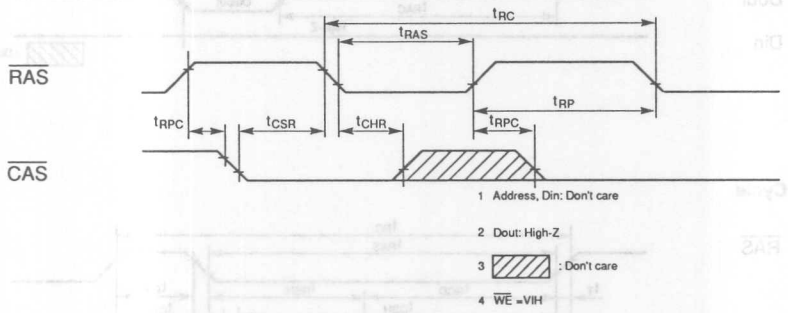
• Early Write Cycle



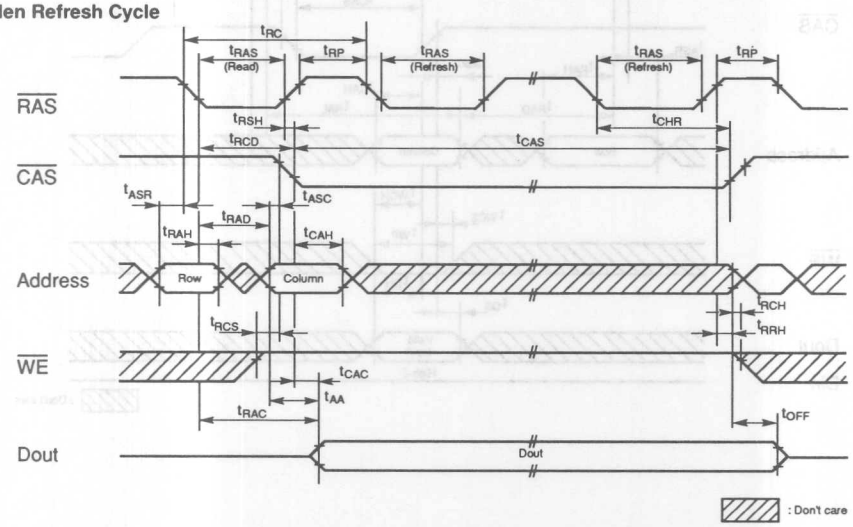
- **$\overline{RAS}$ Only Refresh Cycle**



- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**

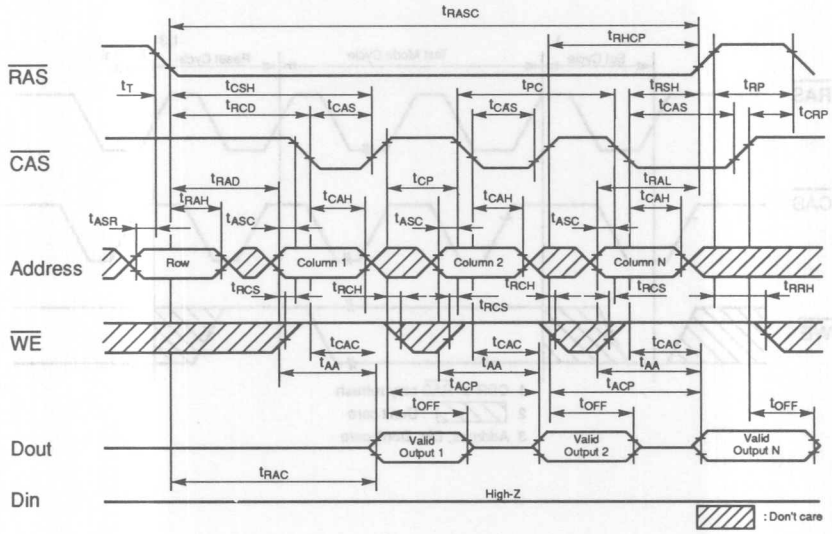


- **Hidden Refresh Cycle**

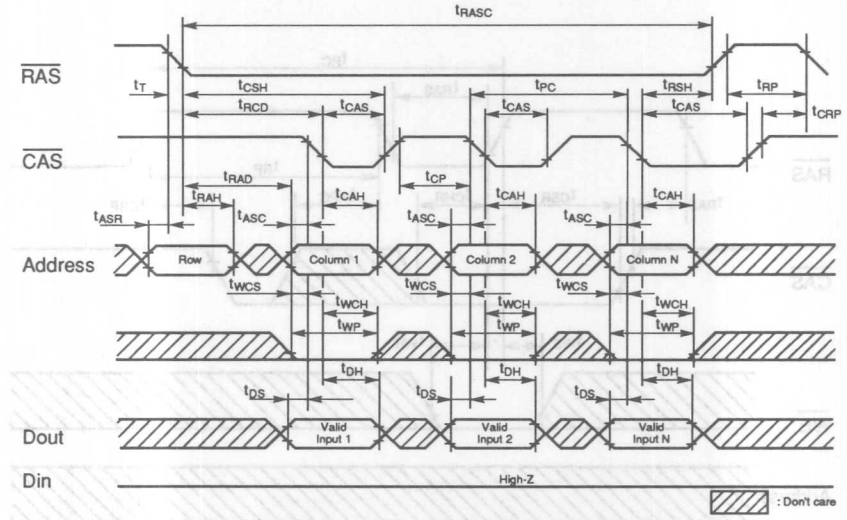


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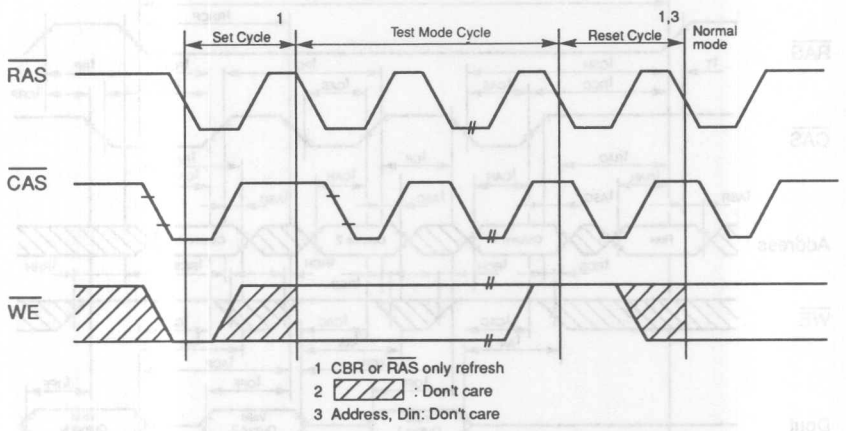
• **Fast Page Mode Read Cycle**



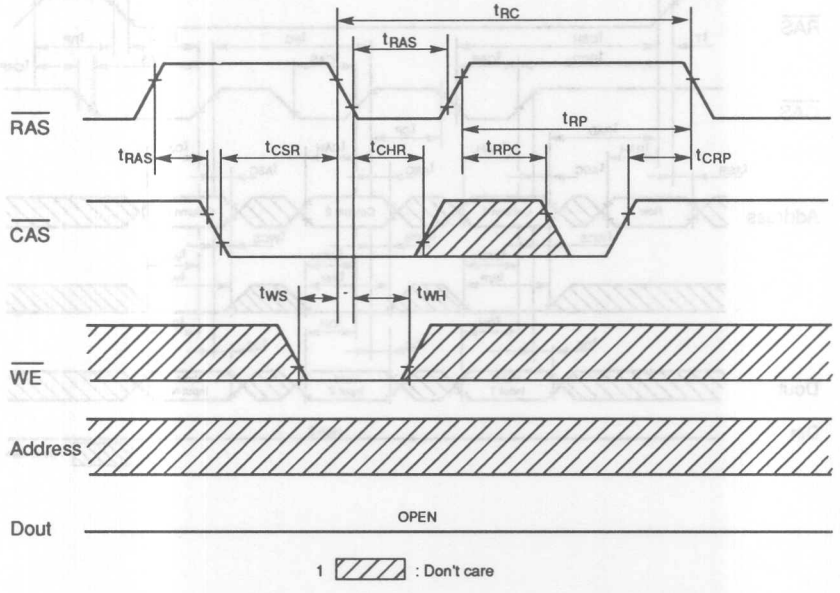
• **Fast Page Mode Early Write Cycle**



• **Test Mode Cycle**

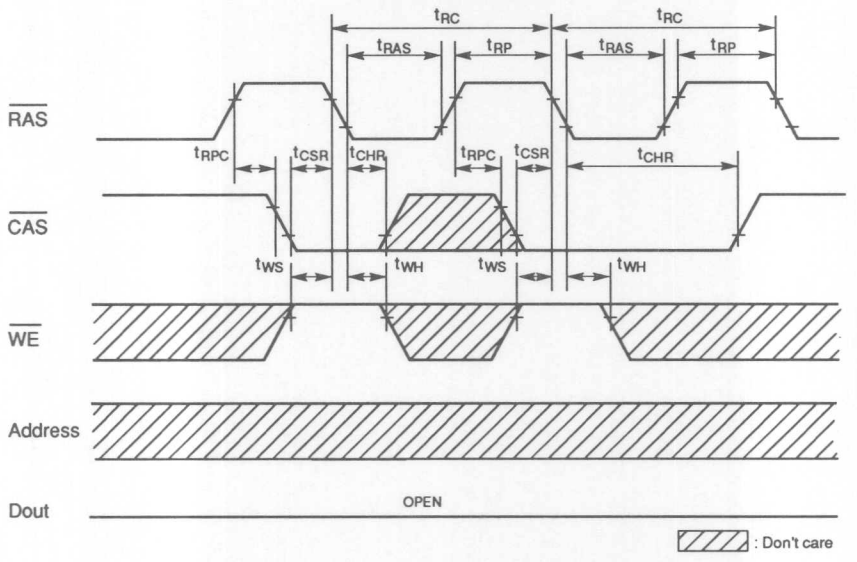


• **Test Mode Set Cycle**

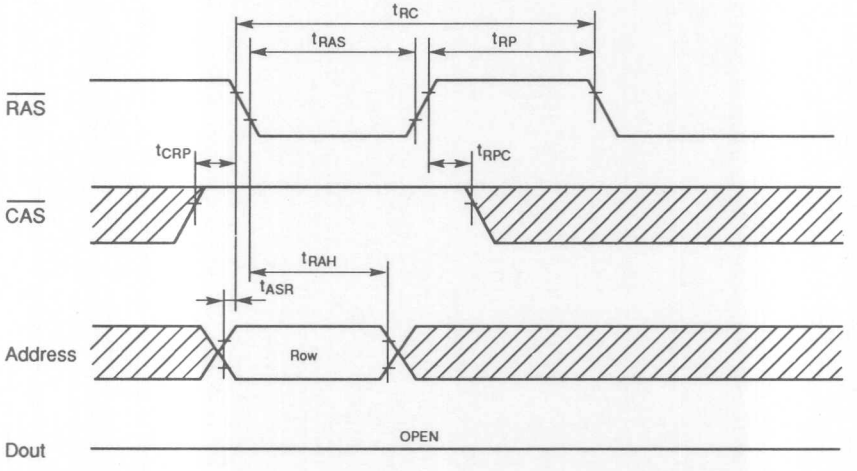


■ TEST MODE RESET CYCLE

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• $\overline{RAS}$ Only Refresh Cycle



HB56A49A/AT/B-8/10/12
9-Bit DRAM

4,194,304-Word × 9 Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A49 is a 4M × 9 dynamic RAM module, mounted nine 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A49 is 30-pin single in-line package having Lead types (HB56A49A, HB56A49AT), Socket type (HB56A49B). Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

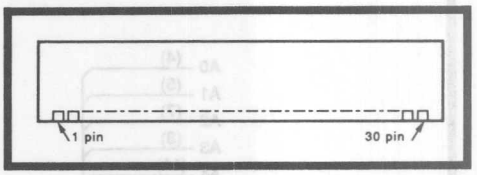
■ FEATURES

- 30-pin single in-line package
  —Lead pitch 2.54mm
- Single 5V (± 10%) supply
- High Speed
  Access time . . . . . 80ns/100ns/120ns (max.)
- Low power dissipation
  —Active mode . . . . . 4455mW/3960mW/3465mW (max.)
  —Standby mode . . . . . 99mW (max.)
- Fast page mode capability
- 1,024 refresh cycle/16ms
- 3 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
  —Hidden refresh
- TTL compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Socket Type
80ns	HB56A49A-8	HB56A49AT-8	HB56A49B-8
100ns	HB56A49A-10	HB56A49AT-10	HB56A49B-10
120ns	HB56A49A-12	HB56A49AT-12	HB56A49B-12

■ PIN OUT

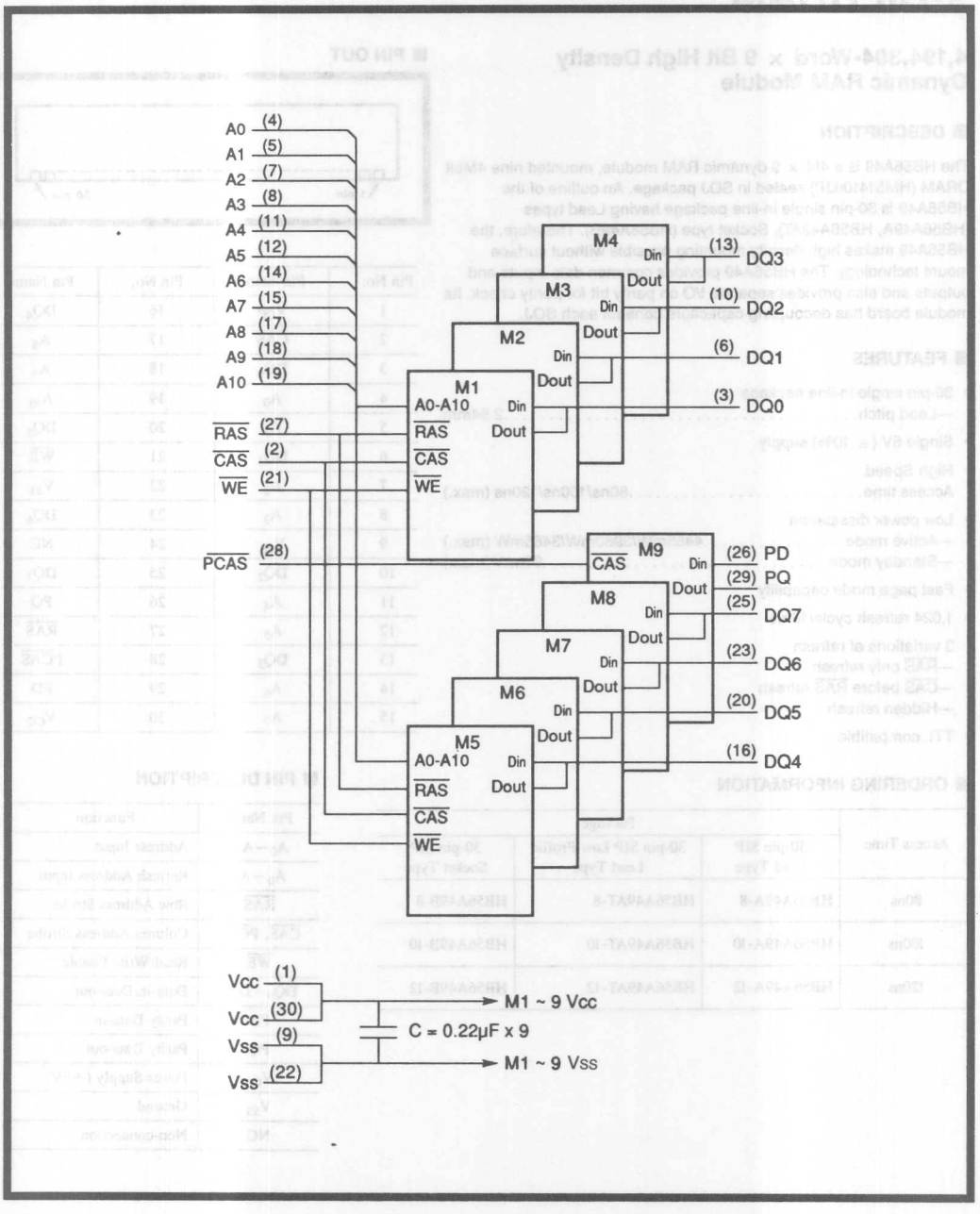


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	A_{10}
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_{10}$	Address Input
$A_0 \sim A_9$	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$DQ_0 \sim DQ_7$	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

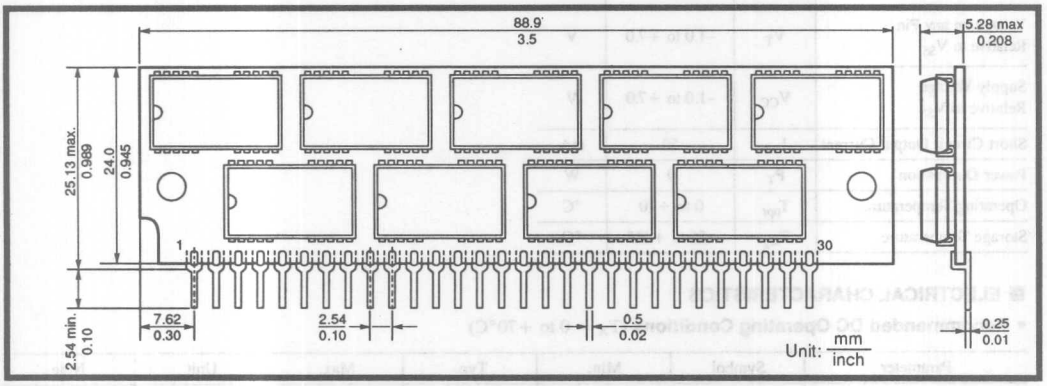
■ BLOCK DIAGRAM



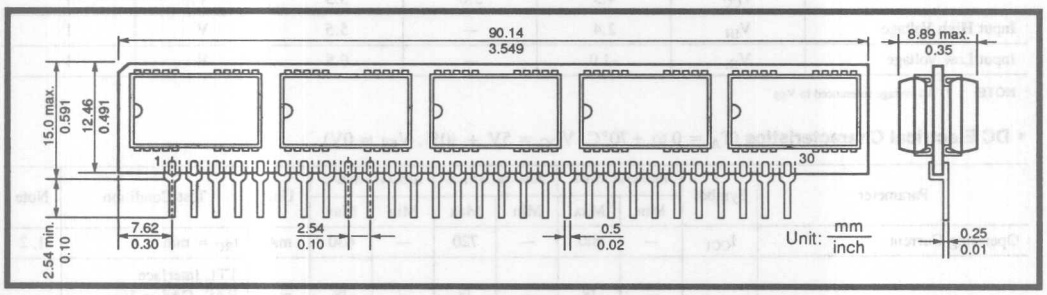
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■ PHYSICAL OUTLINE

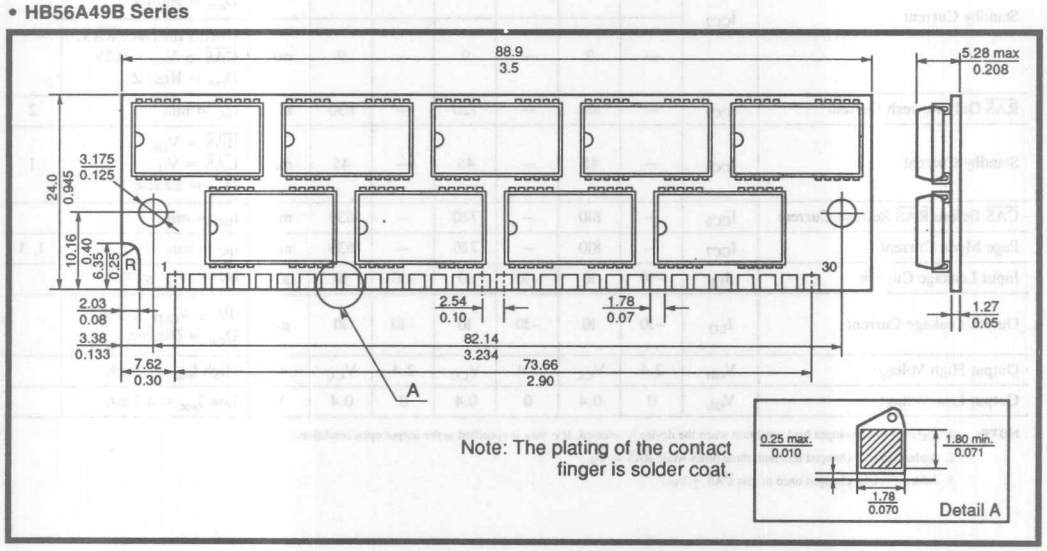
• HB56A49A Series



• HB56A49AT Series



• HB56A49B Series



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	9	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	810	—	720	—	630	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	18	—	18	—	18	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	9	—	9	—	9	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	810	—	720	—	630	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	810	—	720	—	630	mA	t_{RC} = min	
Page Mode Current	I_{CC7}	—	810	—	720	—	630	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	70	pF	1
Input Capacitance (Clock)	C_{I2}	—	88	pF	1
Input/Output Capacitance (DQ_0-DQ_7)	$C_{I/O}$	—	30	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	20	pF	1
Output Capacitance (PQ)	C_O	—	20	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) [1, 12, 15]

• Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ns	17

• Read Cycle

Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

• Refresh Cycle

Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode CAS Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time From CAS Precharge	t_{ACP}	—	50	—	50	—	60	ns	14, 16
RAS Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

• Test Mode Cycle

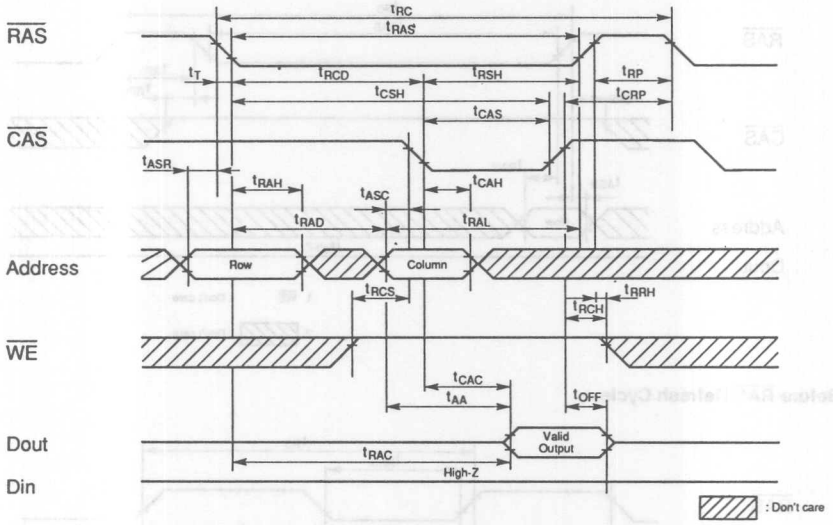
Parameter	Symbol	HB56A49A/AT/B-8		HB56A49A/AT/B-10		HB56A49A/AT/B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Test Mode WE Set-up Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode WE Hold Time	t_{WH}	20	—	20	—	20	—	ns	

NOTES:

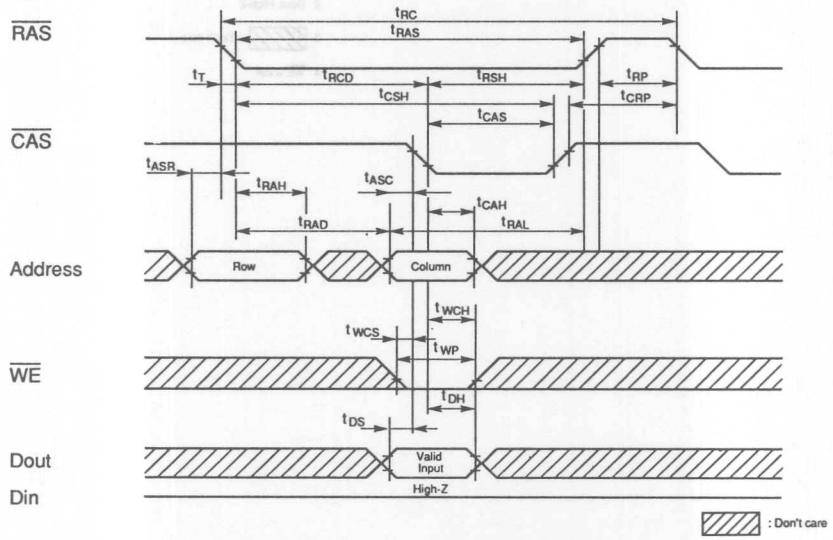
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of eight test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} defines is 1,024 refresh cycles.

■ TIMING WAVEFORM

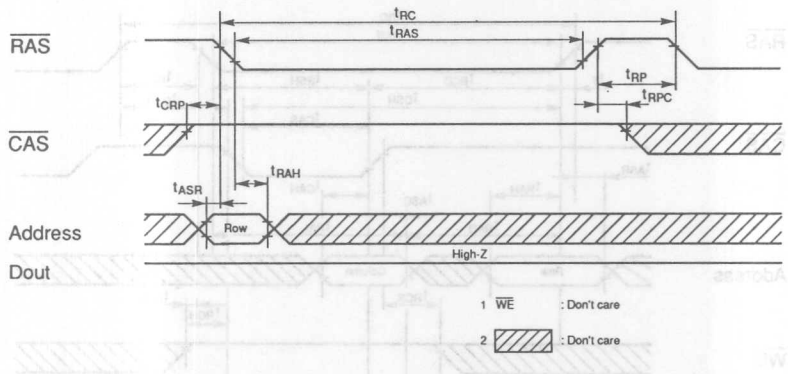
• Read Cycle



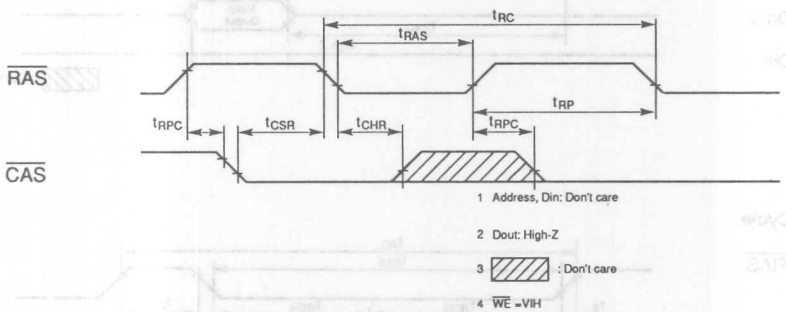
• Early Write Cycle



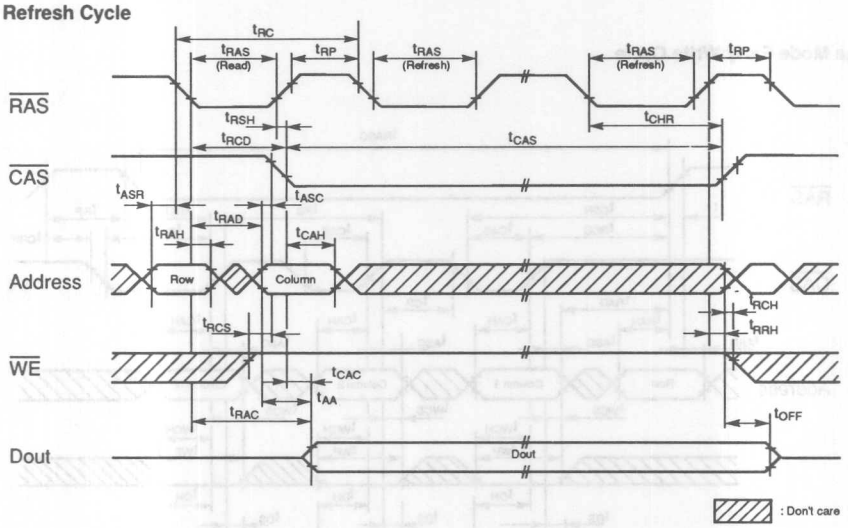
• **$\overline{RAS}$ Only Refresh Cycle**



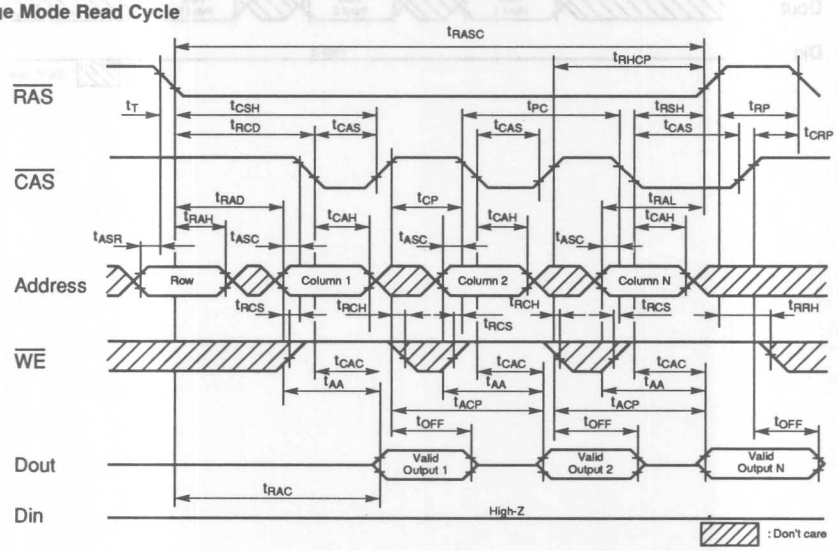
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



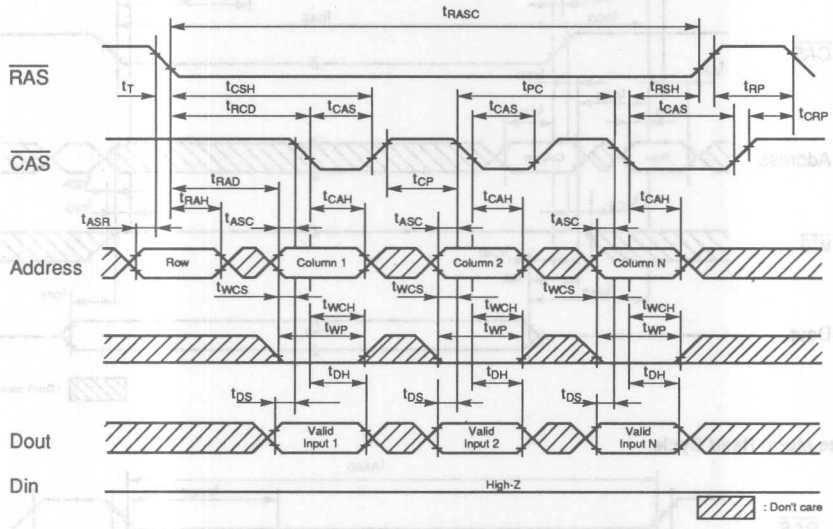
• **Hidden Refresh Cycle**



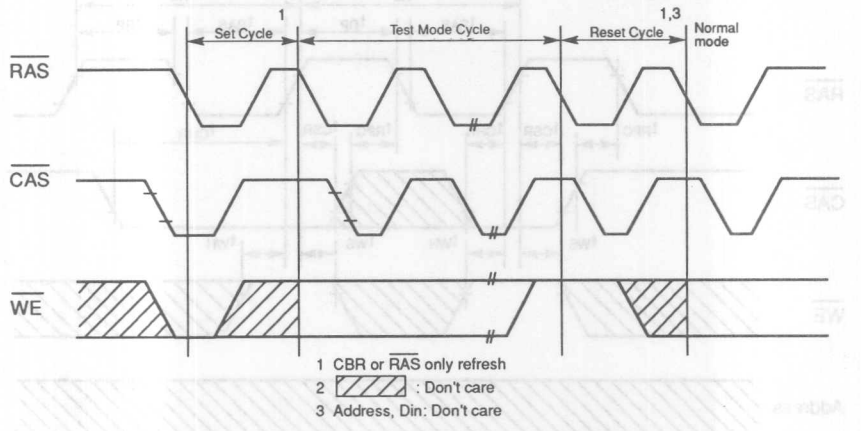
• **Fast Page Mode Read Cycle**



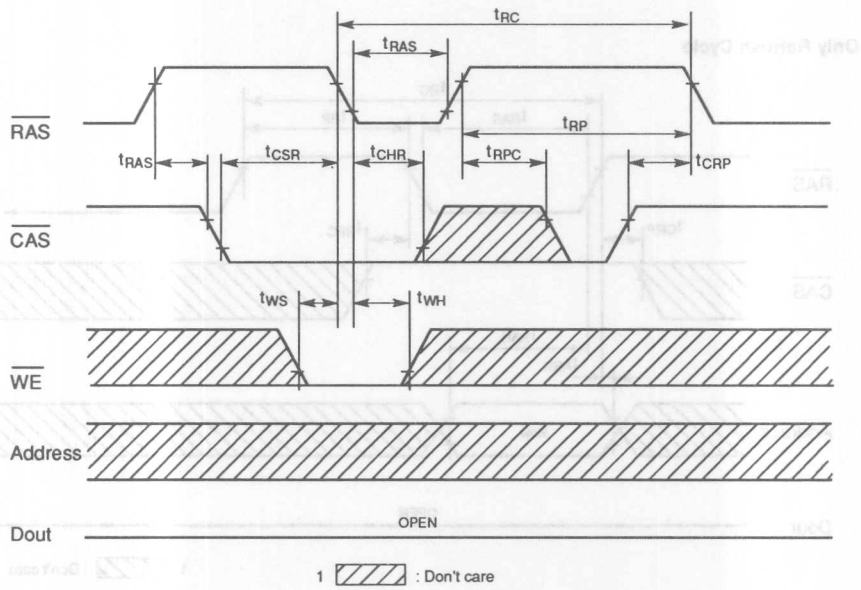
• **Fast Page Mode Early Write Cycle**



• **Test Mode Cycle**

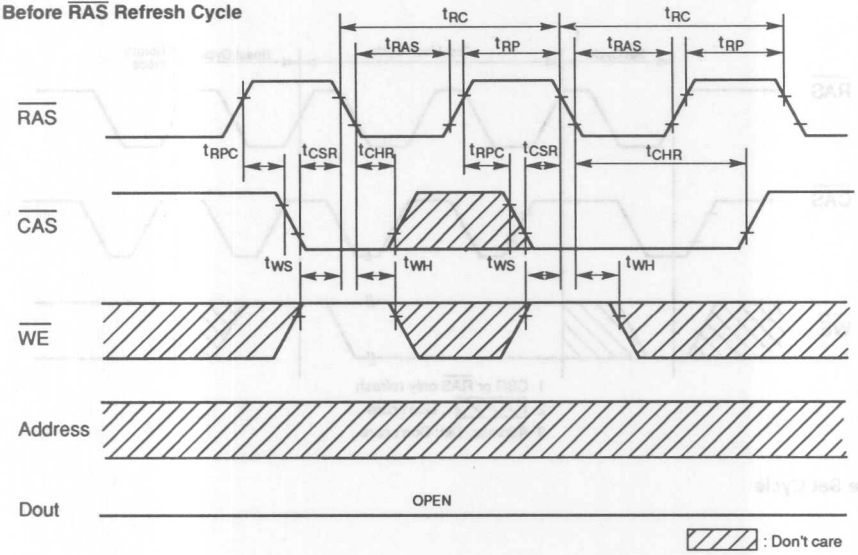


• **Test Mode Set Cycle**

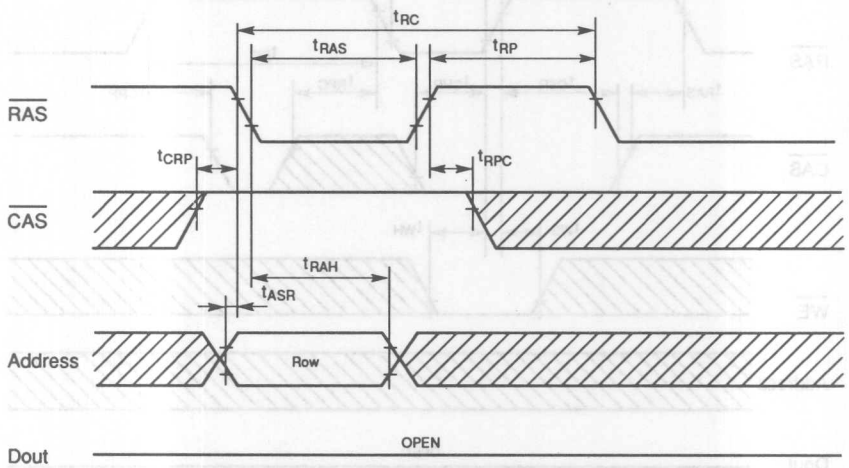


■ TEST MODE RESET CYCLE

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• $\overline{RAS}$ Only Refresh Cycle



HB56D136B-8/10/12
36-Bit DRAM

1,048,576-Word × 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D136B is a 1M × 36 dynamic RAM module, mounted 8 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package and 4 pieces of 1Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56D136B is 72-pin single in-line package. Therefore, the HB56D136B makes high density mounting possible without surface mount technology. The HB56D136B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

■ FEATURES

- 72-pin single in-line package
  —Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High Speed
  Access time . . . . . 80ns/100ns/120ns (max.)
- Low power dissipation
  —Active mode . . . . . 5.25W/4.62W/3.99W (max.)
  —Standby mode . . . . . 126mW (max.)
- Fast page mode capability
- 1,024 refresh cycle/16ms
- 2 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
- TTL compatible

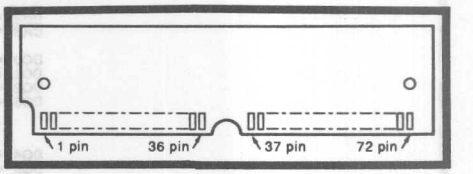
■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D136B-8	80ns	72-pin SIP Socket Type
HB56D136B-10	100ns	
HB56D136B-12	120ns	

■ PRESENCE DETECT PIN OUT

Pin No.	Pin Name	HB56D136B		
		80ns	100ns	120ns
67	PD_1	V_{SS}	V_{SS}	V_{SS}
68	PD_2	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ PIN OUT

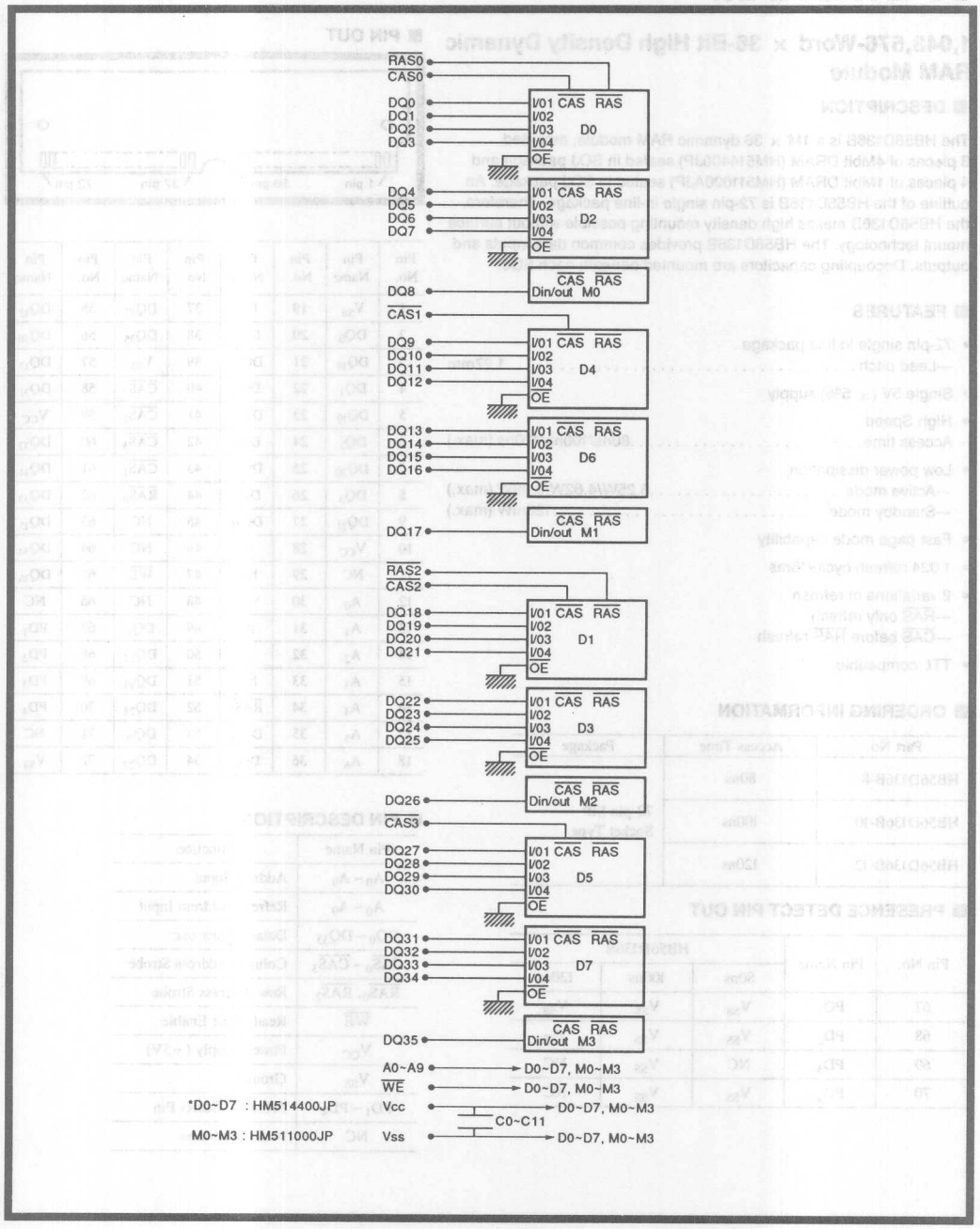


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS_2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS_3}$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS_1}$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	NC	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD_1
14	A_2	32	A_9	50	DQ_{27}	68	PD_2
15	A_3	33	NC	51	DQ_{10}	69	PD_3
16	A_4	34	$\overline{RAS_2}$	52	DQ_{28}	70	PD_4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

■ PIN DESCRIPTION

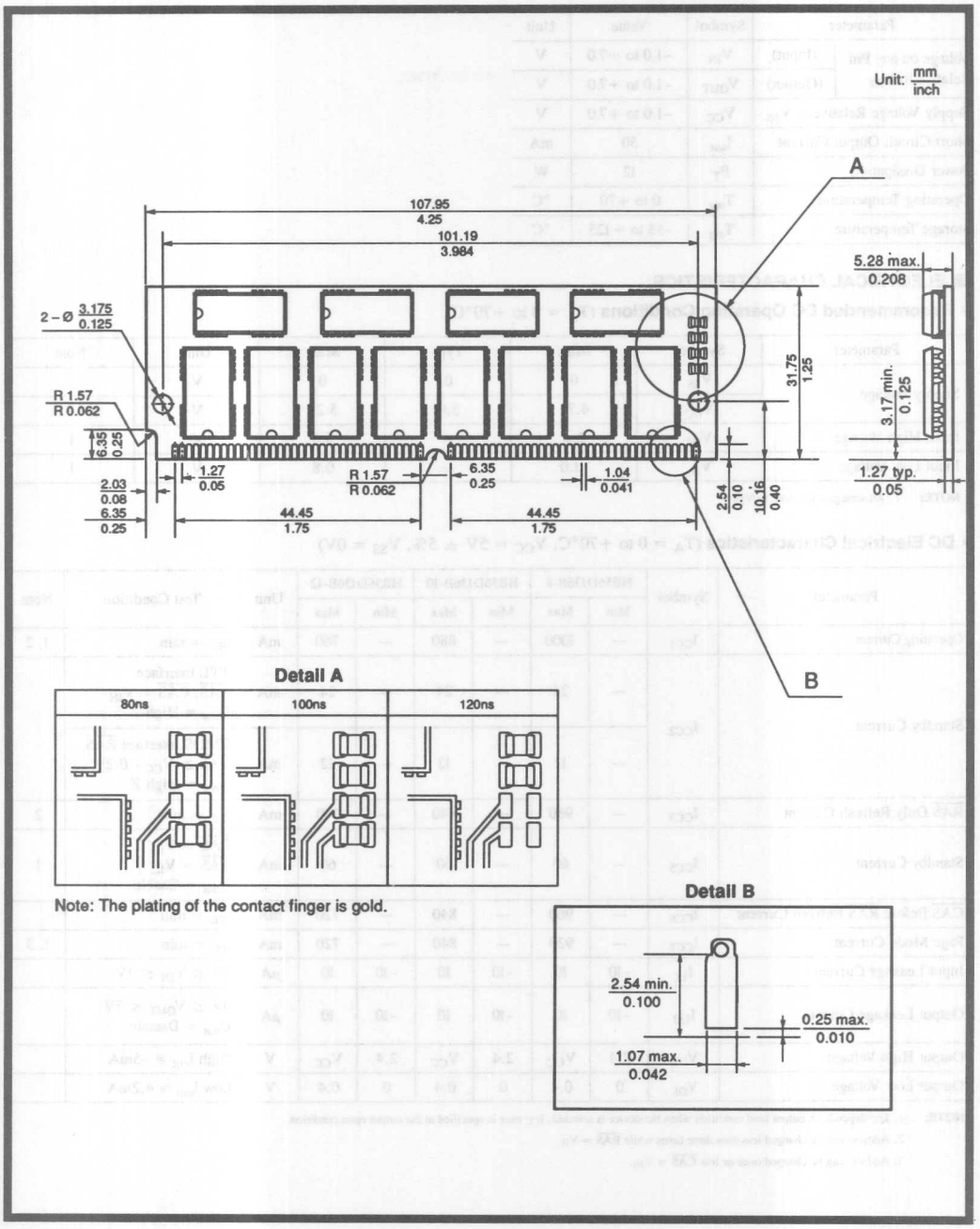
Pin Name	Function
$A_0 \sim A_9$	Address Input
$A_0 \sim A_9$	Refresh Address Input
$DQ_0 \sim DQ_{35}$	Data-in/Data-out
$\overline{CAS_0} \sim \overline{CAS_3}$	Column Address Strobe
$\overline{RAS_0}$, $\overline{RAS_2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
$PD_1 \sim PD_4$	Presence Detect Pin
NC	Non-connection

■ BLOCK DIAGRAM



HITACHI
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■ PHYSICAL OUTLINE



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	(Input)	V_{IN}	−1.0 to +7.0	V
	(Output)	V_{OUT}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1000	—	880	—	760	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	24	—	24	—	24	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	12	—	12	—	12	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	960	—	840	—	740	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	60	—	60	—	60	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	960	—	840	—	720	mA	t_{RC} = min	
Page Mode Current	I_{CC7}	—	920	—	840	—	720	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ± 5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output Capacitance (DQ_0–DQ_7, DQ_9–DQ_{16}, DQ_{18}–DQ_{25}, DQ_{27}–DQ_{34})	$C_{I/O1}$	—	17	pF	1, 2
Output Capacitance (DQ_8, DQ_{17}, DQ_{26}, DQ_{35})	$C_{I/O2}$	—	22	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• **AC Characteristics** (T_A = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) [1, 12]

• **Read, Write and Refresh Cycle (Common Parameters)**

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ns	15

• Read Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11

• Refresh Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

• Fast Page Mode Cycle

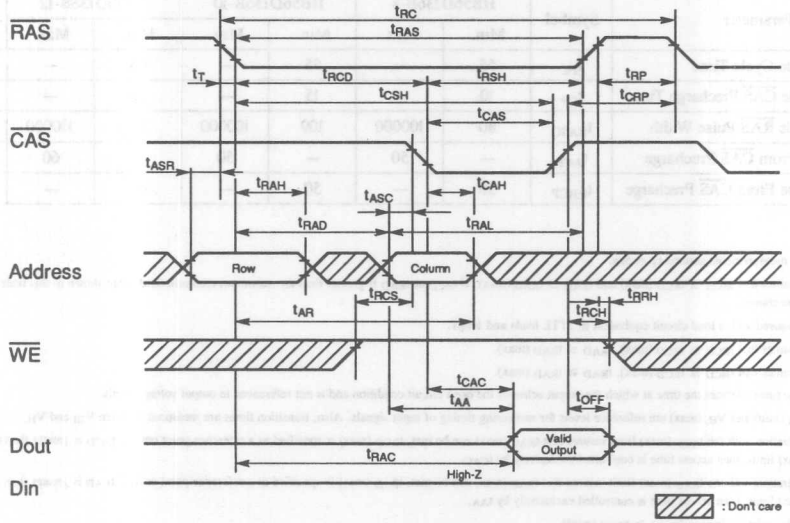
Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

NOTES:

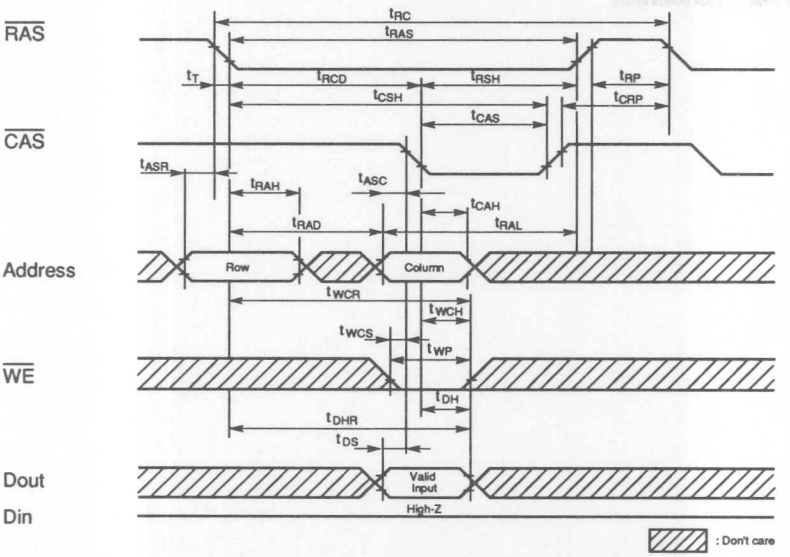
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}
15. t_{REF} defines is 1,024 refresh cycles.

■ TIMING WAVEFORM

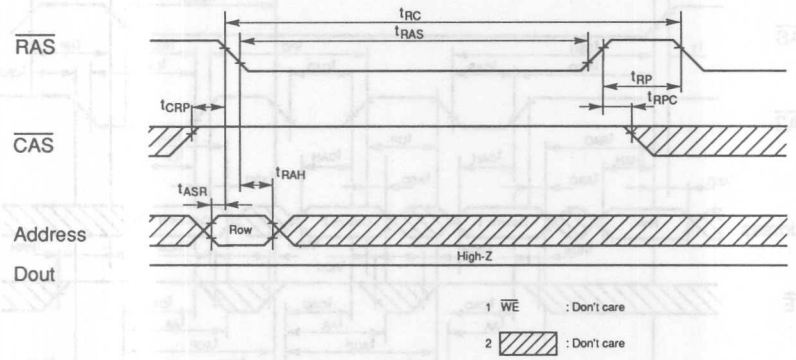
• Read Cycle



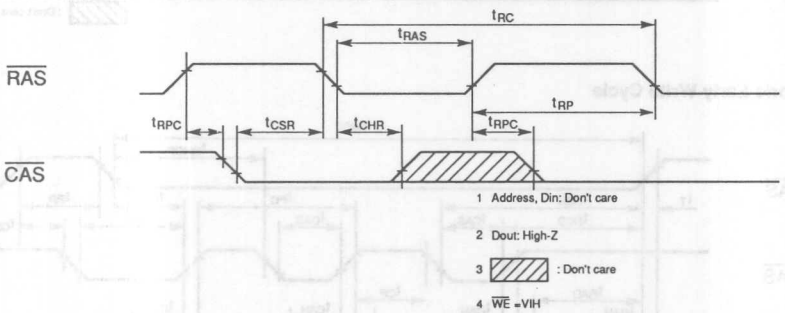
• Early Write Cycle



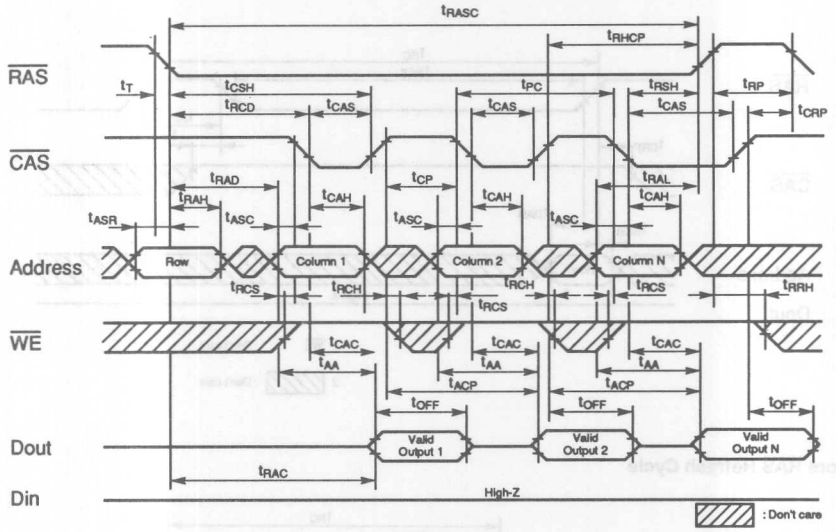
• **$\overline{RAS}$ Only Refresh Cycle**



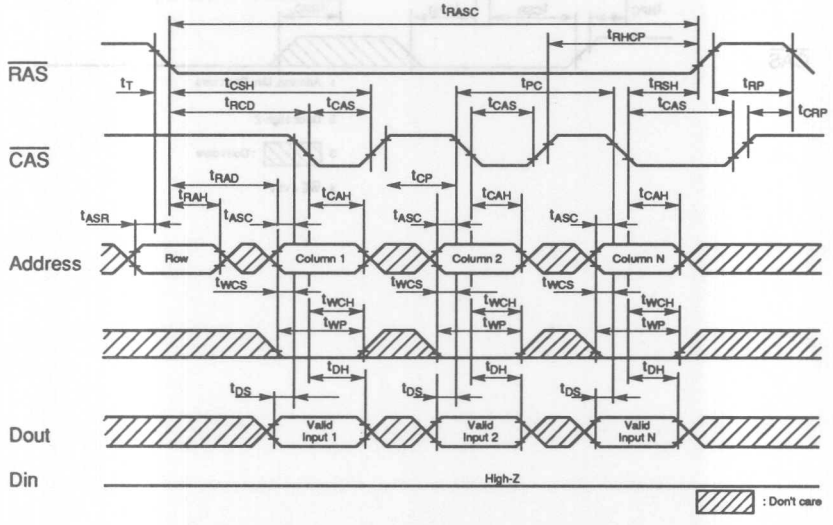
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D236B-8/10/12

2,097,152-Word × 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D236B is a 2M × 36 dynamic RAM module, mounted 16 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package and 8 pieces of 1Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56D236B is 72-pin single in-line package. Therefore, the HB56D236B makes high density mounting possible without surface mount technology. The HB56D236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the side of its module board.

■ FEATURES

- 72-pin single in-line package
  —Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High Speed
  —Access time . . . . . .80ns/100ns/120ns (max.)
- Low power dissipation
  —Active mode. . . . . .5.57W/4.94W/4.31W (max.)
  —Standby mode . . . . . .252mW (max.)
- Fast page mode capability
- 1,024 refresh cycle/16ms
- 2 variations of refresh
  —$\overline{RAS}$ only refresh
  —$\overline{CAS}$ before $\overline{RAS}$ refresh
- TTL compatible

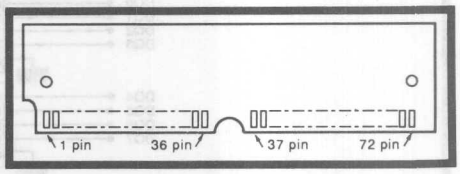
■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D236B-8	80ns	72-pin SIP Socket Type
HB56D236B-10	100ns	
HB56D236B-12	120ns	

■ PRESENCE DETECT PIN OUT

Pin No.	Pin Name	HB56D236B		
		80ns	100ns	120ns
67	PD_1	NC	NC	NC
68	PD_2	NC	NC	NC
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ PIN OUT

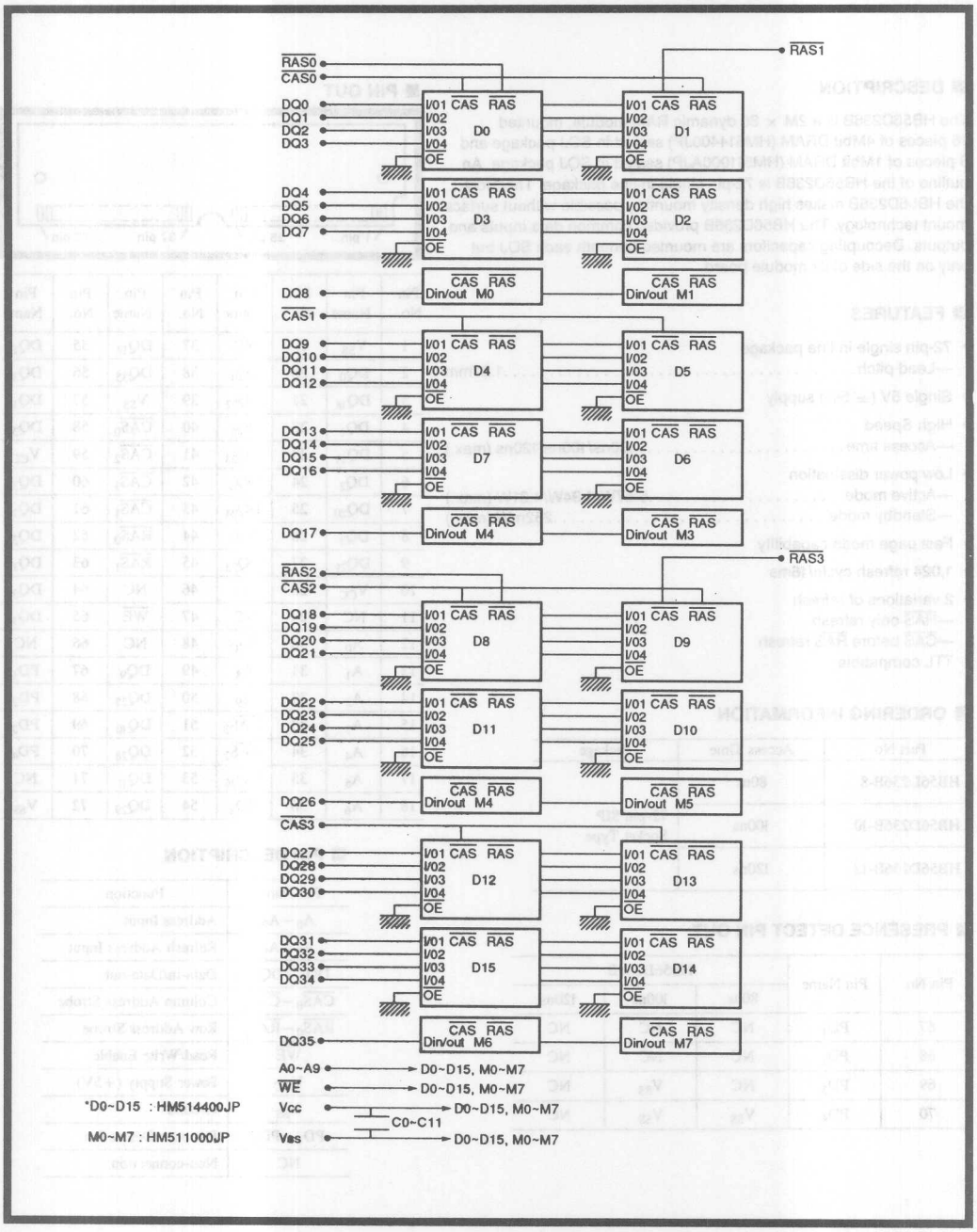


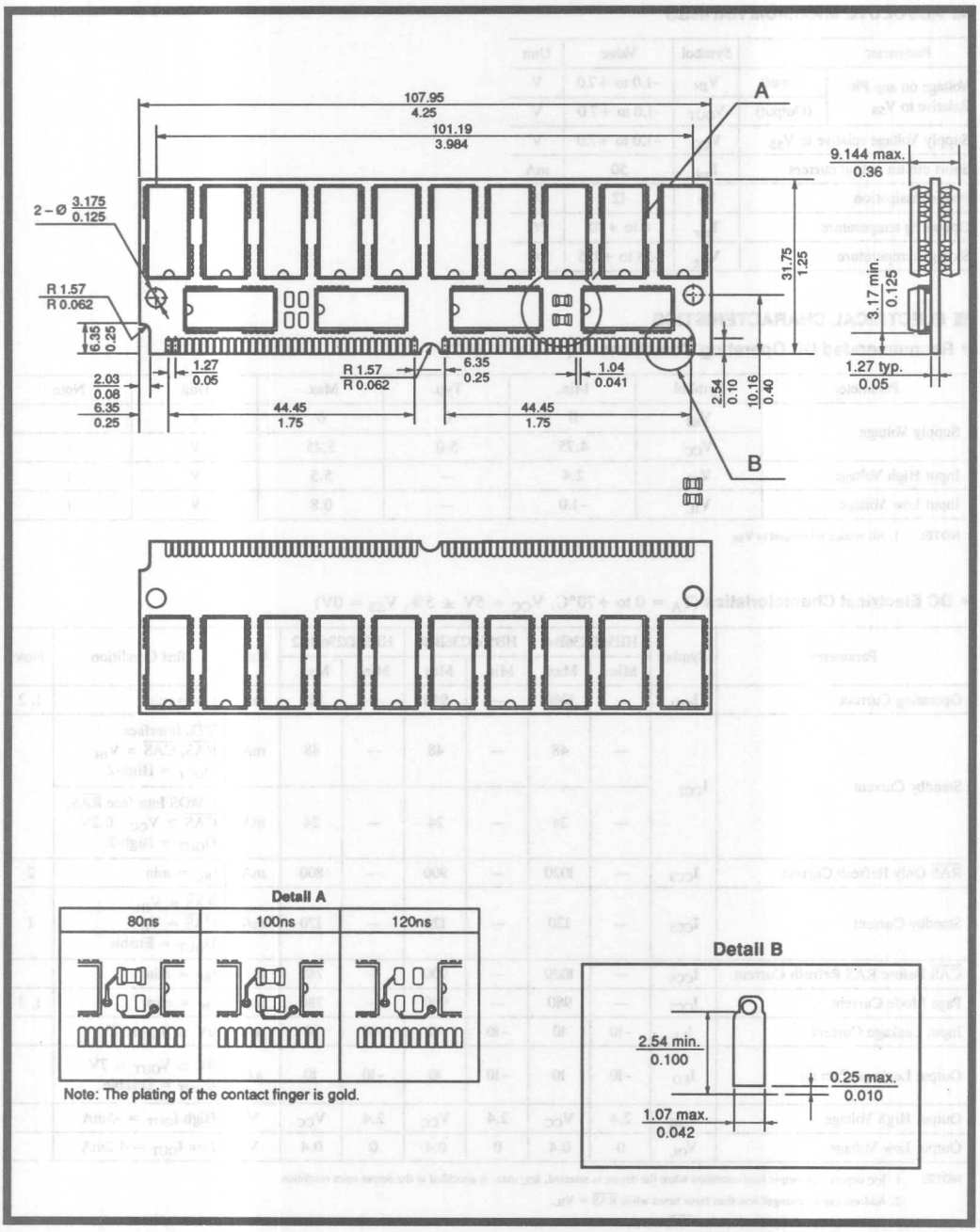
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS}_0$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS}_2$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS}_3$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS}_1$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS}_0$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	$\overline{RAS}_1$	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD_1
14	A_2	32	A_9	50	DQ_{27}	68	PD_2
15	A_3	33	$\overline{RAS}_3$	51	DQ_{10}	69	PD_3
16	A_4	34	$\overline{RAS}_2$	52	DQ_{28}	70	PD_4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_9$	Address Input
$A_0 \sim A_9$	Refresh Address Input
$DQ_0 \sim DQ_{35}$	Data-in/Data-out
$\overline{CAS}_0 \sim \overline{CAS}_3$	Column Address Strobe
$\overline{RAS}_0 \sim \overline{RAS}_3$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
$PD_1 \sim PD_4$	Presence Detect Pin
NC	Non-connection

■ BLOCK DIAGRAM




107.95
4.25
101.19
3.984
A
B
9.144 max.
0.36
2 – Ø 3.175
0.125
R 1.57
R 0.062
6.35
0.25
31.75
1.25
3.17 min.
0.125
1.27 typ.
0.05
2.03
0.08
1.27
0.05
R 1.57
R 0.062
6.35
0.25
1.04
0.041
2.54
0.10
10.16
0.40
44.45
1.75
44.45
1.75
Detail A
80ns
100ns
120ns
Note: The plating of the contact finger is gold.
Detail B
2.54 min.
0.100
0.25 max.
0.010
1.07 max.
0.042

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	(Input)	V_{IN}	-1.0 to +7.0	V
	(Output)	V_{OUT}	-1.0 to +7.0	V
Supply Voltage relative to V_{SS}		V_{CC}	-1.0 to +7.0	V
Short circuit output current		I_{out}	50	mA
Power dissipation		P_T	12	W
Operating temperature		T_{opr}	0 to +70	°C
Storage temperature		V_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Test Condition	Note
		Min.	Max.	Min.	Max.	Min.	Max.			
Operating Current	I_{CC1}	—	1060	—	940	—	820	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	48	—	48	—	48	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	
		—	24	—	24	—	24	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} - 0.2V D_{OUT} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1020	—	900	—	800	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	120	—	120	—	120	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1020	—	900	—	780	mA	t_{RC} = min	
Page Mode Current	I_{CC7}	—	980	—	900	—	780	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	-10	10	-10	10	-10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	-10	10	-10	10	-10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{OUT} = -5mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{OUT} = 4.2mA	

NOTE: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ± 5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output Capacitance (DQ_{0-7}, DQ_{9-16}, DQ_{18-25}, DQ_{27-34})	$C_{I/O1}$	—	29	pF	1, 2
Output ($DQ_{8,17,26,35}$)	$C_{I/O2}$	—	39	pF	1, 2

NOTE: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

• AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) [1, 12]

• Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-8-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
RAS Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ns	15

• Read Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11

• Refresh Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

• Fast Page Mode Cycle

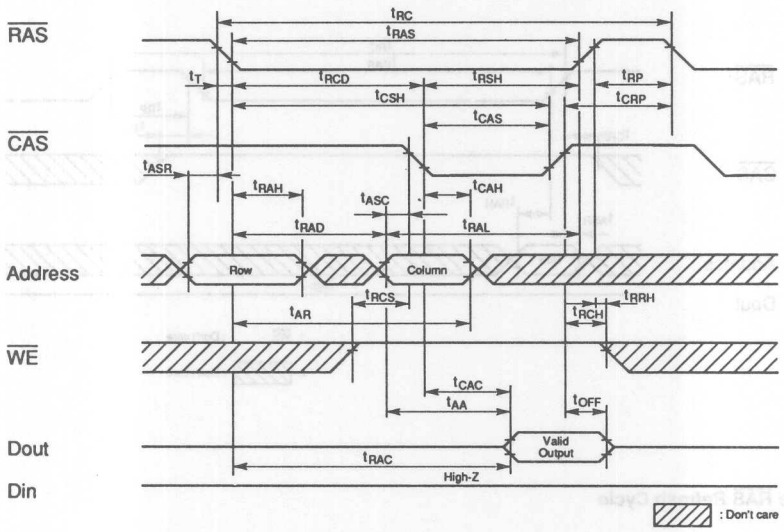
Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

NOTES:

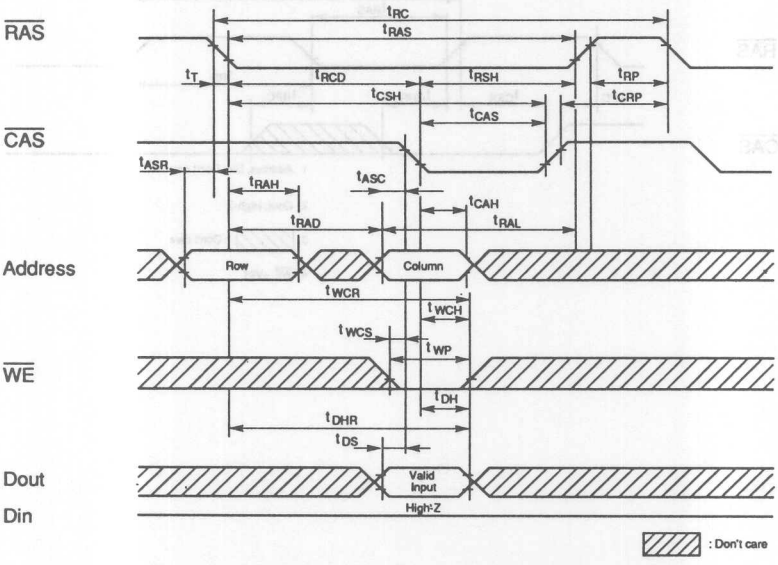
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 1,024 refresh cycles.

■ TIMING WAVEFORM

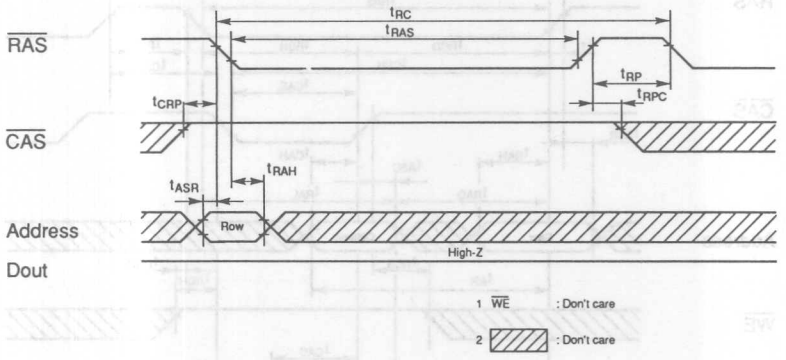
• Read Cycle



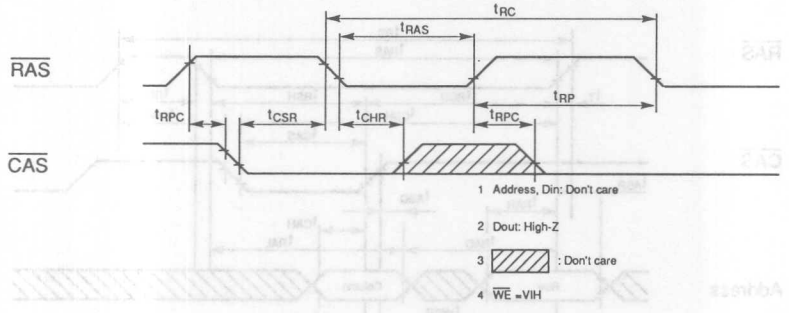
• Early Write Cycle



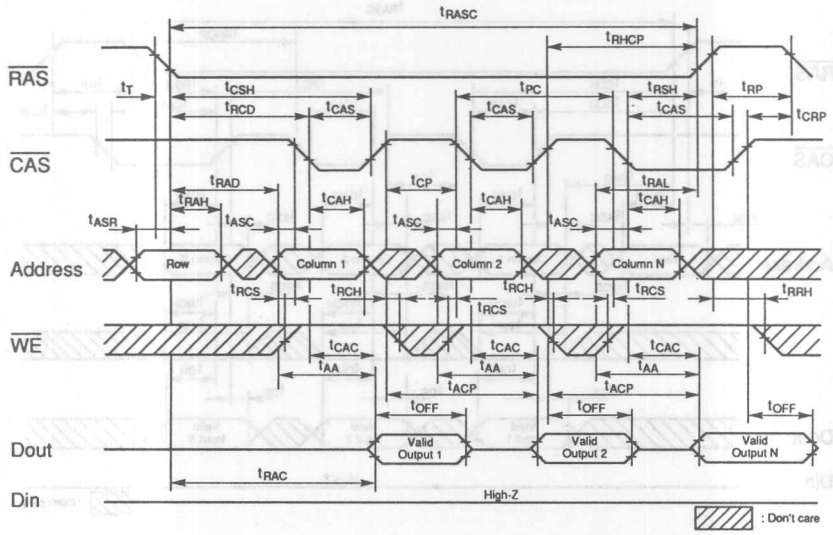
• **$\overline{RAS}$ Only Refresh Cycle**



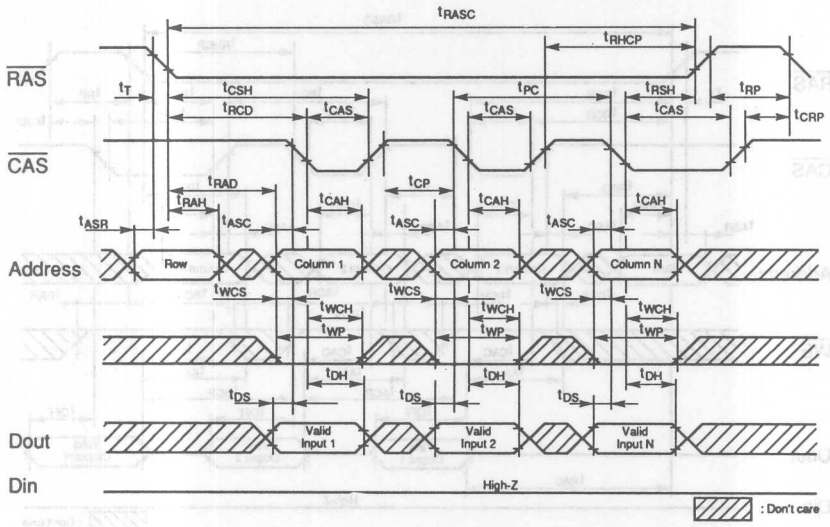
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



Section 7
MOS Mask ROM

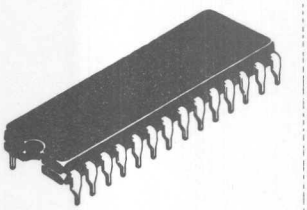
HITACHI®

HN623257P, HN623257F

32768-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN623257P/F is a 256-kbit CMOS mask-programmable ROM organized as 32768 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

HN623257P



(DP-28)

HN623257F

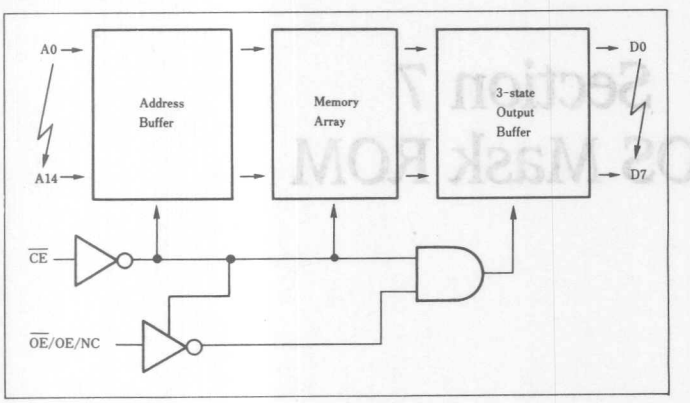


(FP-28DA)

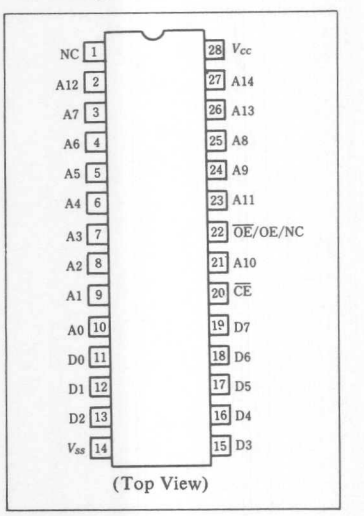
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Address Access Time: 150ns (Max.)
- Low Power Consumption: 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide Data Organization

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage *1	Vcc	−0.3 to +7.0	V
All Input or Output Voltage *1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	−20 to +75	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions (V_{SS} = 0V, Ta = –20 to +75°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = –20 to +75°C)

Parameter		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	45	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geq V_{CC}-0.2V$
Input Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	Vin=0 to 5.5V
Output Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH}=–205μA
		V_{OL}	—	0.4	V	I_{OL}=3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Parameter	Symbol	min	max	Unit
Input Capacitance	Cin	—	10	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = –20 to +75°C)

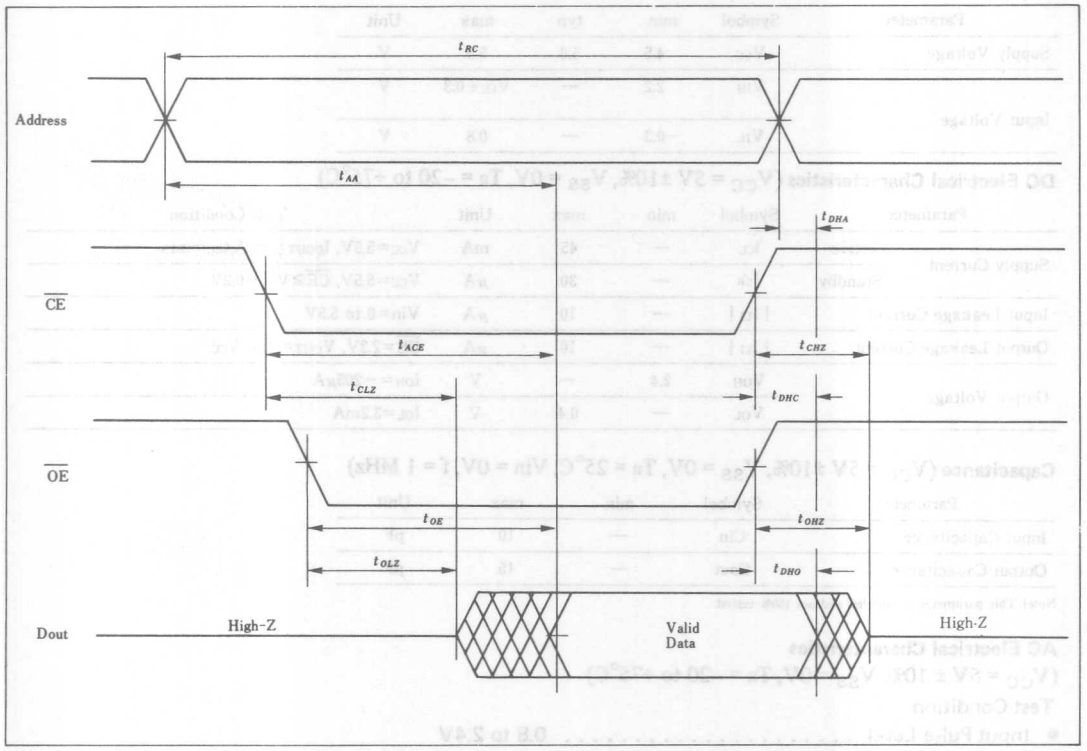
Test Condition

- Input Pulse Level . . . . . 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load . . . . . 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	150	—	ns
Address Access Time	t_{AA}	—	150	ns
$\overline{CE}$ Access Time	t_{ACE}	—	150	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
$\overline{CE}$ to Output in High Z*1	t_{CHZ}	—	70	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{OE}$ to Output in High Z*1	t_{OHZ}	—	70	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns

Note) *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram



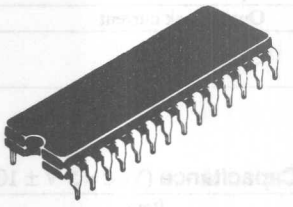
Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA}, t_{DHC} or t_{DHO}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA}, t_{ACE} or t_{OE}, whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ}, whichever occurs last.

HN623258P, HN623258F

32768-Word × 8-Bit CMOS Mask Programmable ROM

HN623258P/F is a 256-Kbit CMOS mask-programable ROM organized as 32768-word x 8-bit. It can be operated with a battery because of low power consumption.

HN623258P



(DP-28)

HN623258F

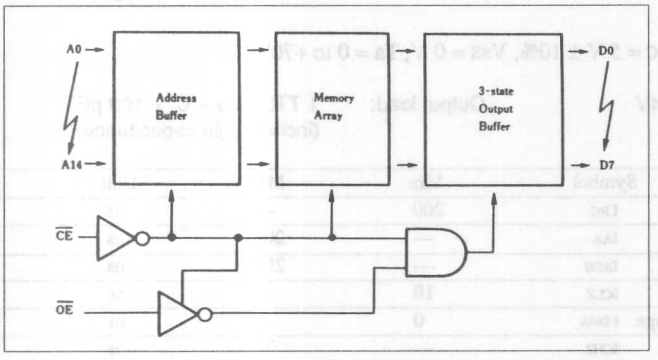


(FP-28DA)

Features

- Low power: Active 100 mW (typ), Standby 5 µW (typ)
- Addres access time: 200 ns (max)
- Single 5 V
- TTL compatible
- Wired OR is permitted for the output in three states

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	–0.3 to +7.0	V
Terminal voltage*1	VT	–0.3 to Vcc +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

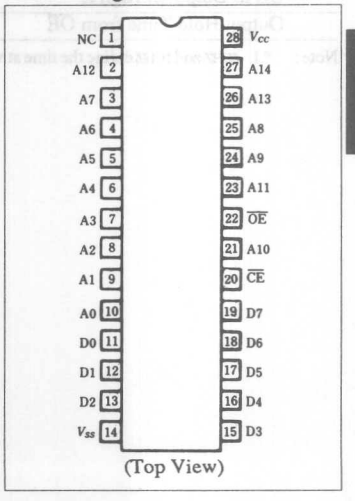
Note: *1. With respect to Vss.

Recommended Operating Conditions

(Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	VIH	2.2	—	Vcc + 0.3	V
	VIL	–0.3	—	0.8	V

Pin Arrangement



(Top View)

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	45	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\|I_{LI}\|$	—	10	µA	V_{IN} = 0 to 5.5 V
Output leak current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacity	Cin	—	10	pF
Output capacity	Cout	—	15	pF

Note: This parameter is samples and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

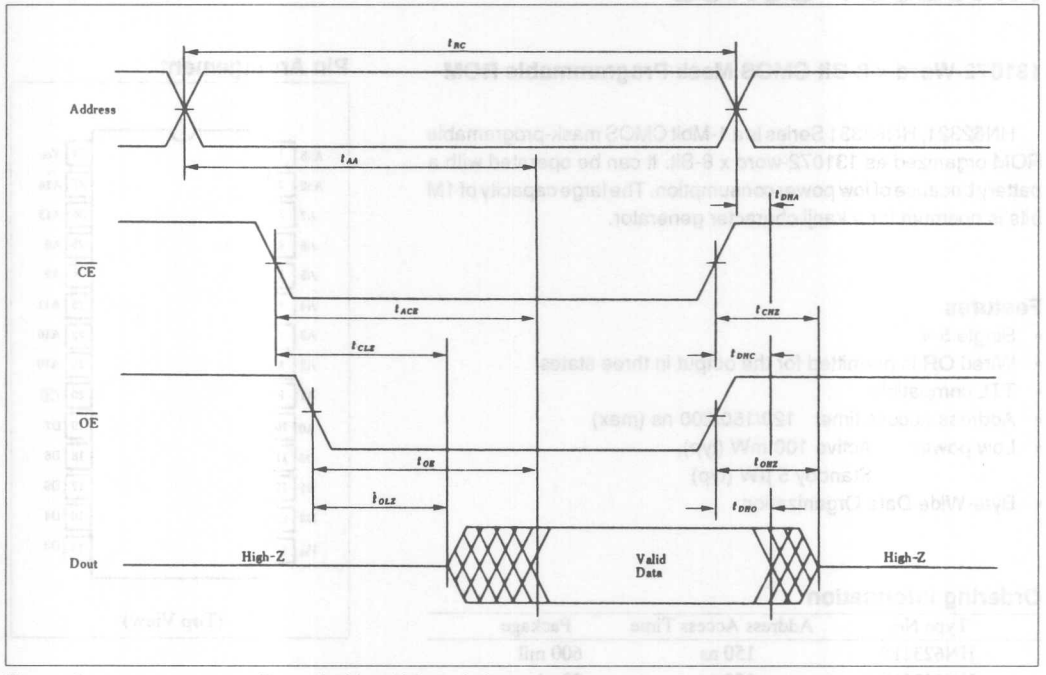
Test Condition

Input pulse level: 0.8 to 2.4V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	Min	Max	Unit
Cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
Output Holt Time from Address Change	t_{DHA}	0	—	ns
$\overline{CE}$ to Output in High Z*1	t_{CHZ}	—	70	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{OE}$ to Output in High Z*1	t_{OHZ}	—	70	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



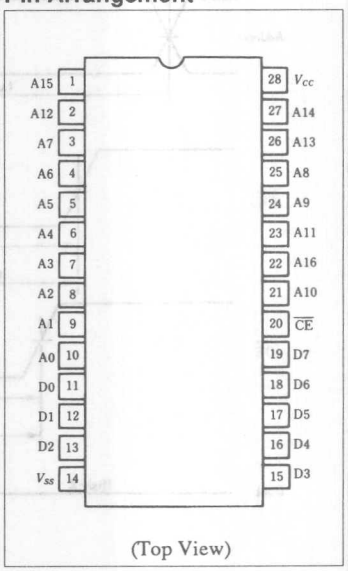
Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

HN62321 Series
HN62331 Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

HN62321, HN62331 Series is a 1-Mbit CMOS mask-programable ROM organized as 131072-word x 8-Bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

Pin Arrangement



(Top View)

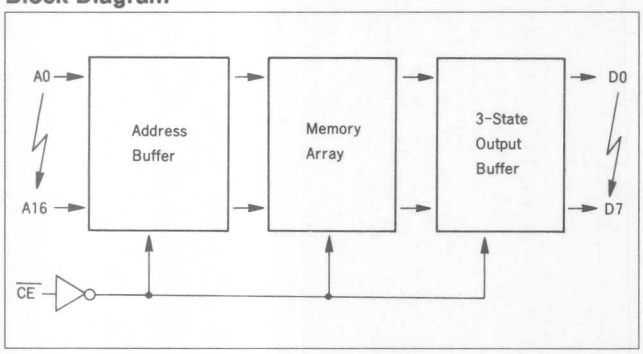
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/150/200 ns (max)
- Low power: Active 100 mW (typ),
  Standby 5 μW (typ)
- Byte-Wide Data Organization

Ordering Information

Type No.	Address Access Time	Package
HN62321P	150 ns	600 mil
HN62321BP	200 ns	28-pin
HN62331P	120 ns	plastic DIP
HN62321F	150 ns	
HN62321BF	200 ns	28-pin
HN62331F	120 ns	plastic SOP

Block Diagram



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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

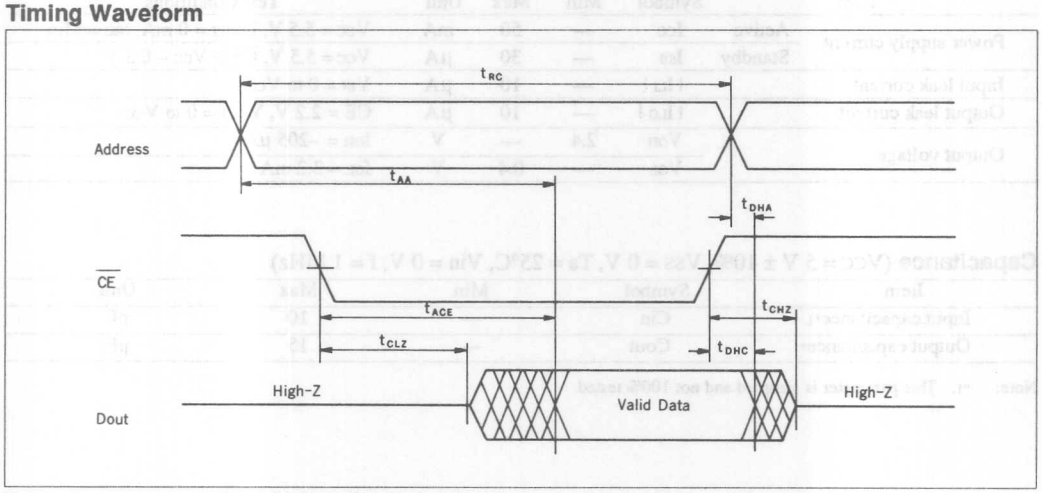
Test Conditions

Input pulse level:	0.8 to 2.4 V	Output load:	1 TTL gate + C_L = 100 pF
I/O timing reference level:	1.5 V		(including jig capacitance)
Input rise/fall time:	10 ns		

Item	Symbol	HN62331		HN62321		HN62321B		Unit
		Min	Max	Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	150	—	200	—	ns
Address access time	t_{AA}	—	120	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	60	—	70	—	100	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	10	—	10	—	ns

Note: *1 t_{CHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. t_{DHA}, t_{DHC}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}; Determined by whichever is slower.

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HN62331AP/F

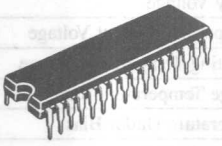
131,072 × 8-Bit CMOS MASK Programmable Read Only Memory

■ DESCRIPTION

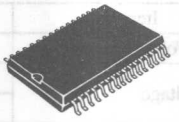
The HN62331A is a 1-Mbit CMOS mask-programmable ROM organized as 131,072-words × 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62331A, which provides large capacity of 1M bits, is ideally suited for kanji character generators.

■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .120ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide Data Organization
- Pin Compatible with JEDEC



(DP-32)

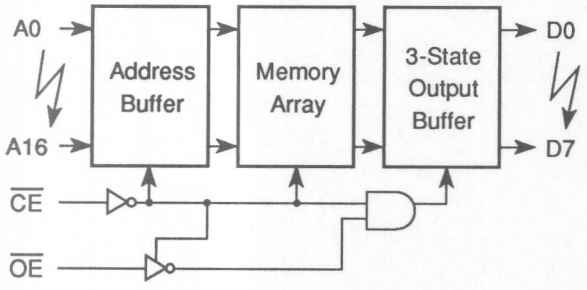


(FP-32D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62331AP	120ns	600 mil 32 pin Plastic DIP
HN62331AF	120ns	32 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−3.0 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.45	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.4V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	10	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

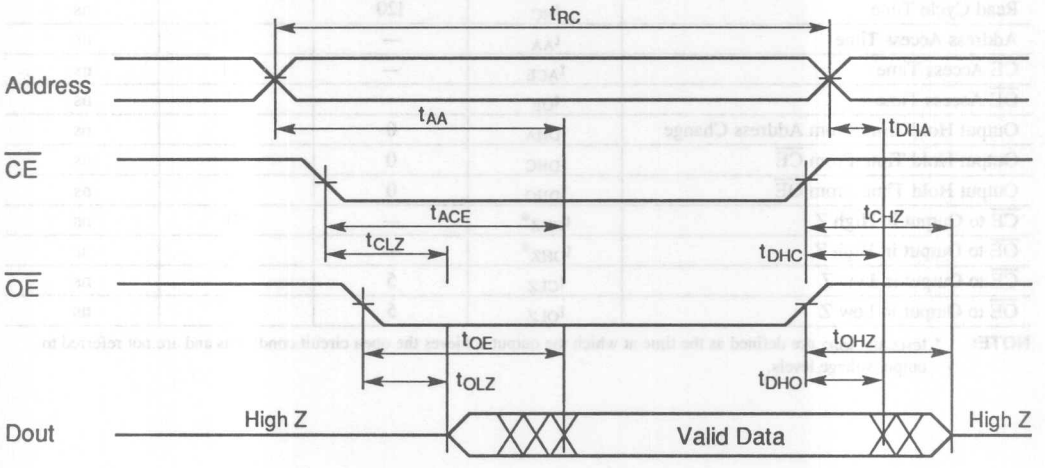
■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	120	—	ns
Address Access Time	t_{AA}	—	120	ns
$\overline{CE}$ Access Time	t_{ACE}	—	120	ns
$\overline{OE}$ Access Time	t_{OE}	—	60	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	60	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	60	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	—	ns

NOTE: * t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

- **Test Conditions**
  - Input Pulse Level: 0.45 ~ 2.4V
  - Input and Output Timing Reference Level: 1.5V
  - Input Rise and Fall Time: 10ns
  - Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

■ TIMING WAVEFORM



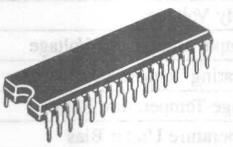
NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

HN62331P/F

131,072 × 8-Bit CMOS MASK Programmable Read Only Memory

■ DESCRIPTION

The HN62331 is a 1-Mbit CMOS mask-programmable ROM organized as 131,072-words × 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62331, which provides large capacity of 1M bits, is ideally suited for kanji character generators.



(DP-32)



(FP-32D)

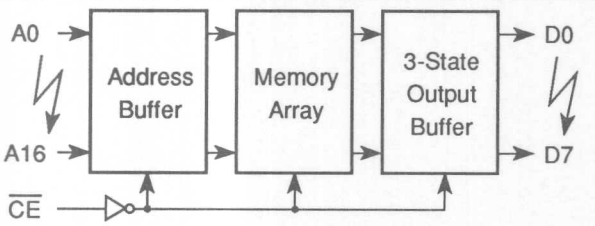
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .120ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide Data Organization
- Pin Compatible with JEDEC

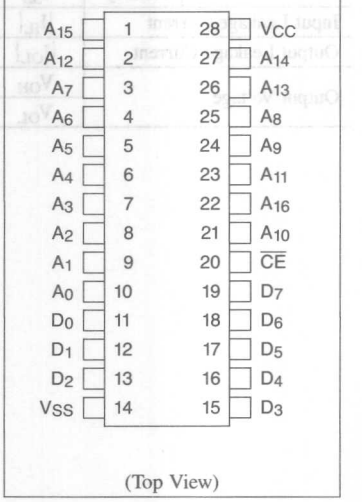
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62331P	120ns	600 mil 32 pin Plastic DIP
HN62331F	120ns	32 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−3.0 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.45	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.4V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

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■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	10	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

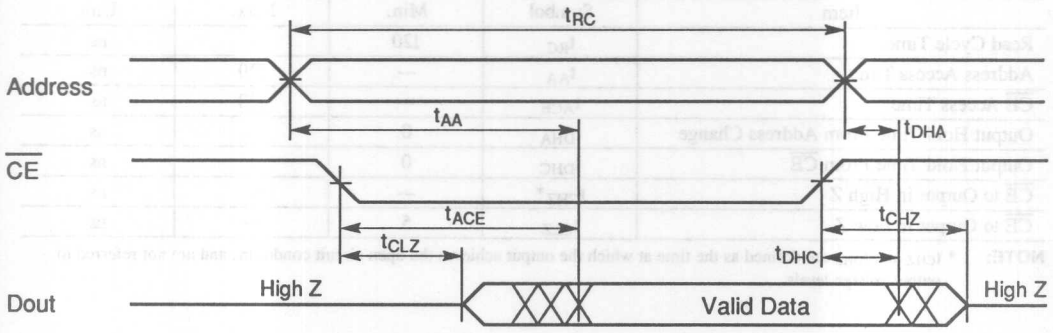
■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	120	—	ns
Address Access Time	t_{AA}	—	120	ns
$\overline{CE}$ Access Time	t_{ACE}	—	120	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	60	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	ns

NOTE: * t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

- **Test Conditions**
  - Input Pulse Level: 0.45 ~ 2.4V
  - Input and Output Timing Reference Level: 1.5V
  - Input Rise and Fall Time: 10ns
  - Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

■ TIMING WAVEFORM



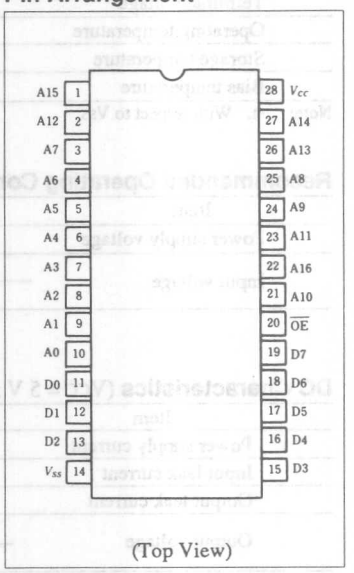
NOTES: 1. t_{DHA}, t_{DHC}; determined by faster.
2. t_{AA}, t_{ACE}; determined by slower.

HN62321E Series
HN62331E Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

HN62321E, HN62331E Series is a 1-Mbit CMOS mask-programable ROM organized as 131072-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

Pin Arrangement



(Top View)

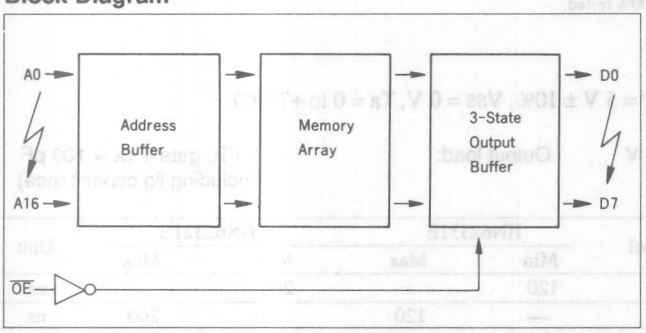
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/200 ns (max)
- OE access time: 60/100ns (max)
- Low power: 100 mW (typ)
- Byte-Wide Data Organization

Ordering Information

Type No.	Address Access Time	Package
HN62321EP	200 ns	600 mil 28-pin
HN62331EP	120 ns	plastic DIP
HN62321EF	200 ns	28-pin
HN62331EF	120 ns	plastic SOP

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Max	Unit	Test Conditions
Power supply current	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
Input leak current	$\|I_{LI}\|$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current	$\|I_{LO}\|$	—	10	µA	$\overline{OE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –205 µA
	V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

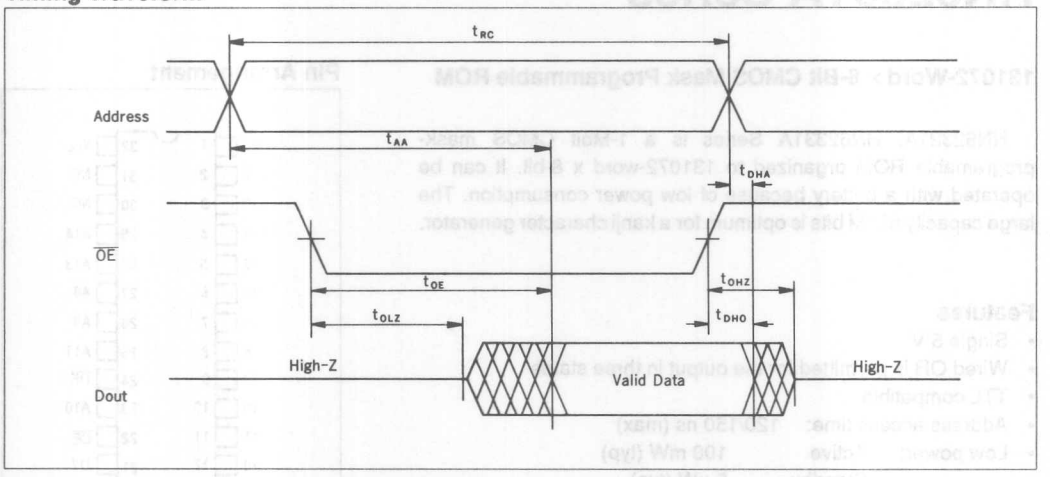
Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	HN62331E		HN62321E		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	200	—	ns
Address access time	t_{AA}	—	120	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	100	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	60	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	—	10	—	ns

Note: *1 t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Timing Waveform



Notes: 1. t_{DHA}, t_{DHO}; Determined by whichever is faster.
2. t_{AA}, t_{OE}; Determined by whichever is slower.

HN62321A Series
HN62331A Series

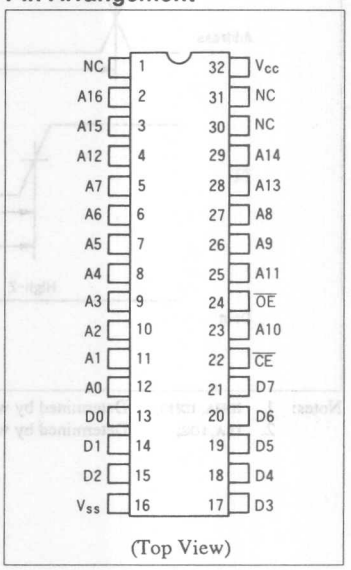
131072-Word × 8-Bit CMOS Mask Programmable ROM

HN62321A, HN62331A Series is a 1-Mbit CMOS mask-programable ROM organized to 131072-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/150 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide Data Organization, JEDEC pin arrangement

Pin Arrangement

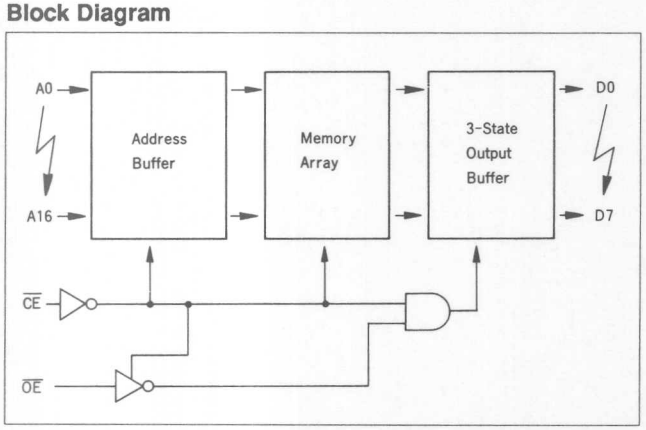


(Top View)

Ordering Information

Type No.	Address Access Time	Package
HN62321AP	150 ns	600 mil 32-pin
HN62331AP	120 ns	plastic DIP
HN62321AF	150 ns	32-pin
HN62331AF	120 ns	plastic SOP

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

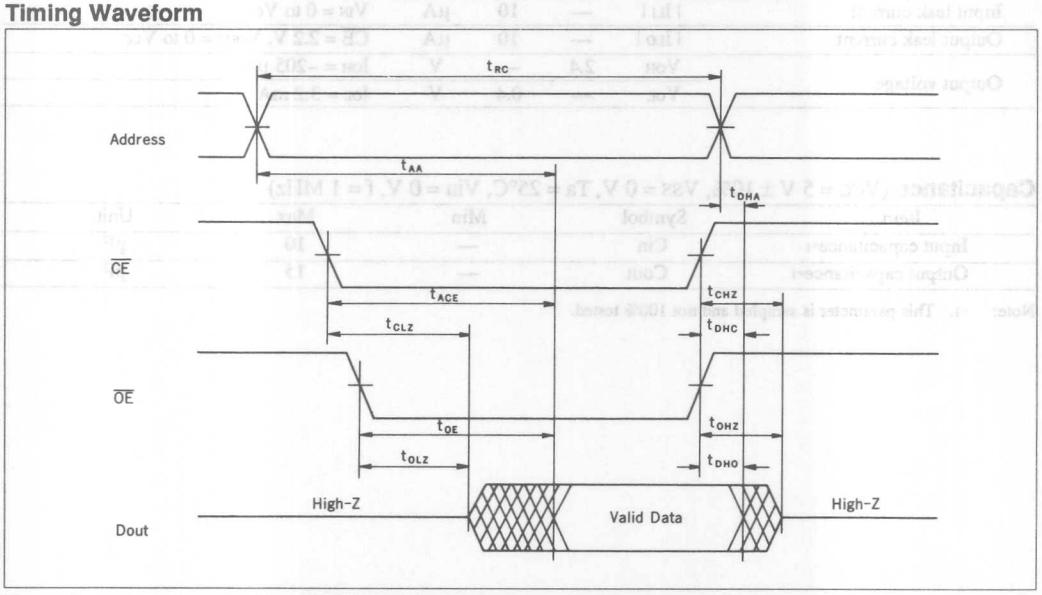
Test Conditions

Input pulse level:	0.8 to 2.4 V	Output load:	1 TTL gate + C_L = 100 pF
I/O timing reference level:	1.5 V		(including jig capacitance)
Input rise/fall time:	10 ns		

Item	Symbol	HN62331A		HN62321A		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	150	—	ns
Address access time	t_{AA}	—	120	—	150	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Input in High Z	t_{CHZ}*1	—	60	—	70	ns
$\overline{OE}$ to Input in High Z	t_{OHZ}*1	—	60	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	–	10	–	ns

Note: *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by whichever is slower.
3. t_{CLZ}, t_{OLZ}; Determined by whichever is slower.

HN62412 Series
HN62422 Series

131072-Word × 16-Bit/262144-Word × 8-Bit CMOS Mask Programmable ROM

HN62412, HN62422 Series is a 2-Mbit CMOS mask-programable ROM organized either as 131072-word x 16-bit or as 262144-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 2M bits is optimum for a kanji character generator.

Features

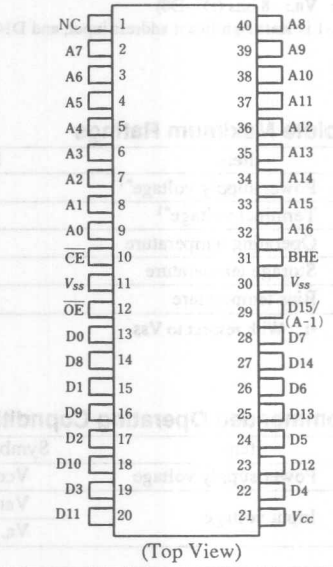
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62412P	200 ns	600 mil 40-pin
HN62422P	150 ns	plastic DIP
HN62412FP	200 ns	44-pin
HN62422FP	150 ns	plastic QFP

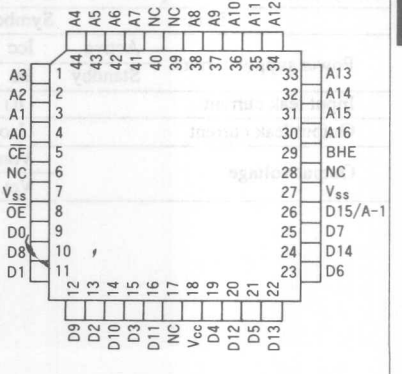
Pin Arrangement

HN62412P, HN62422P



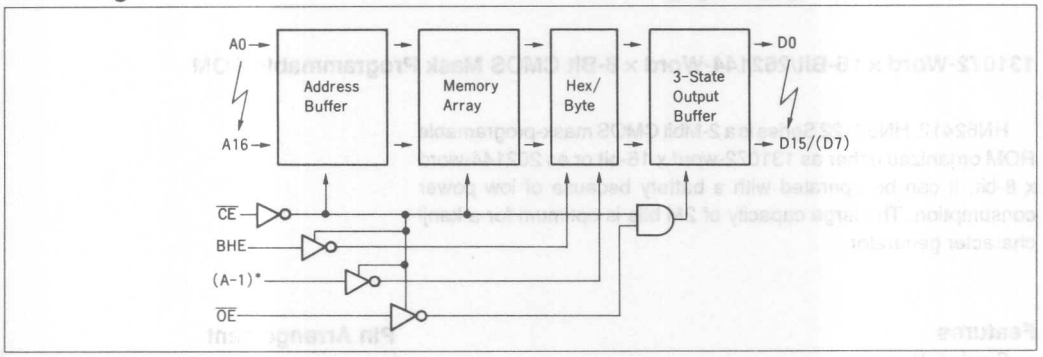
(Top View)

HN62412FP, HN62422FP



(Top View)

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1 A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to Vcc + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to Vss

Recommended Operating Copnditions (Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	Vcc + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	Icc	—	50	mA	Vcc = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	Vcc = 5.5 V, $\overline{CE}$ ≥ Vcc – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to Vcc
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to Vcc
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

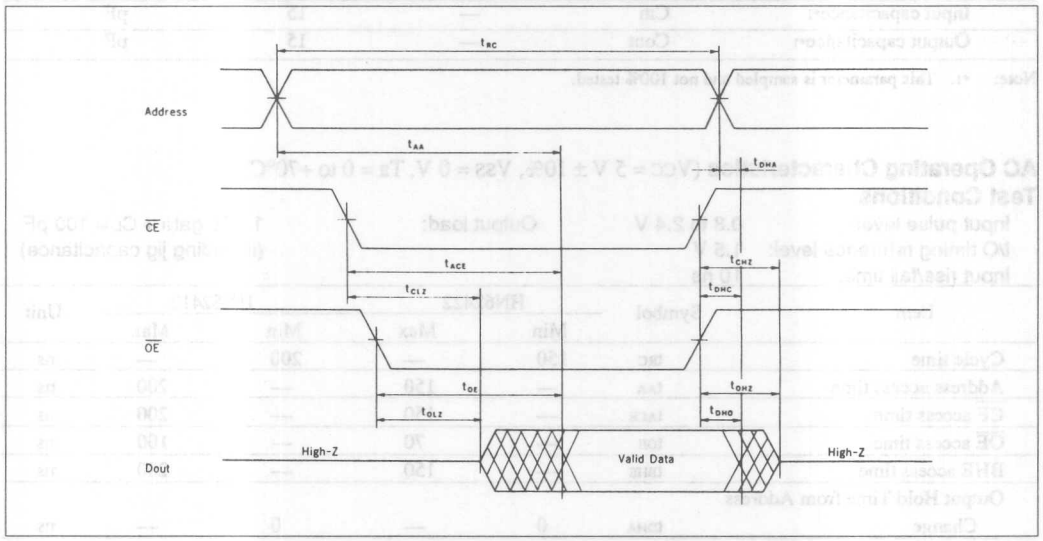
Test Conditions

Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	HN62422		HN62412		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
$\overline{BHE}$ access time	t_{BHE}	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	—	10	—	ns

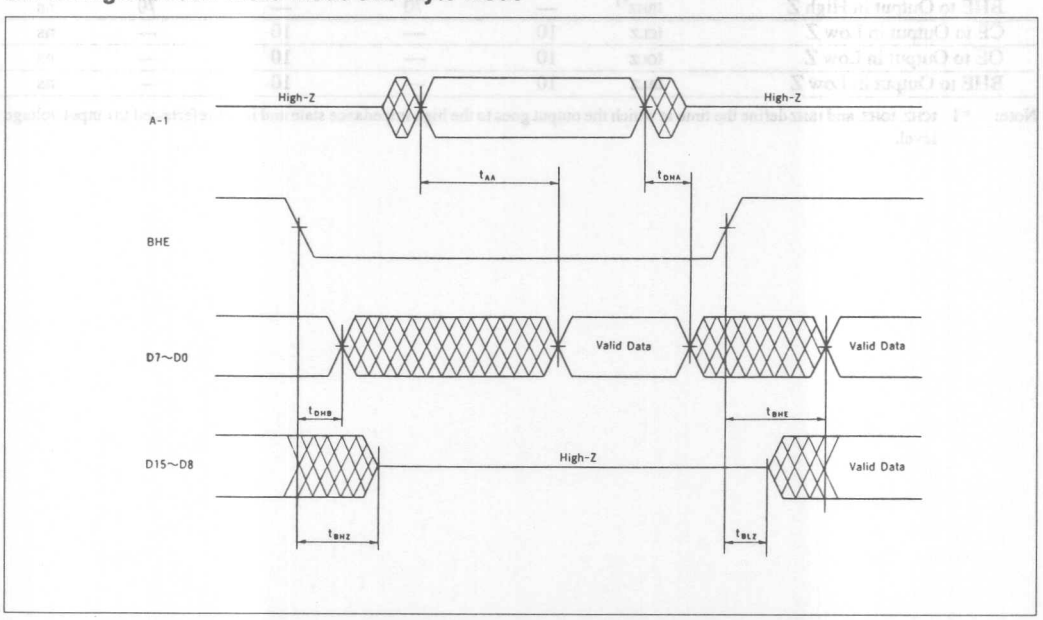
Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

Timing Waveform
Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. CE, OE are of selected status. A16–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, CE and OE are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62404 Series
HN62424 Series

262144-Word × 16-Bit/524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62404, HN62424 Series is a 4-Mbit CMOS mask-programable ROM organized either as 262144-word x 16-bit or as 524288-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

Features

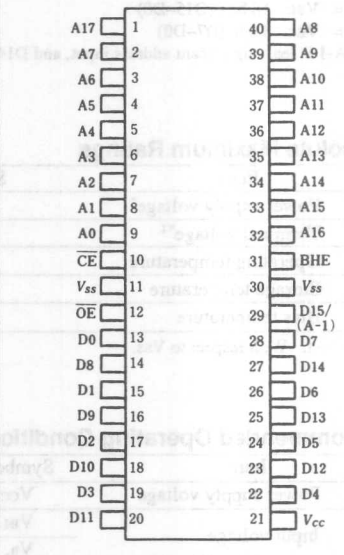
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access ccess time: 150/200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide or Word-Wide Data Organization(switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62404P	200 ns	600 mil 40-pin
HN62424P	150 ns	plastic DIP
HN62404FP	200 ns	44-pin
HN62424FP	150 ns	plastic QFP

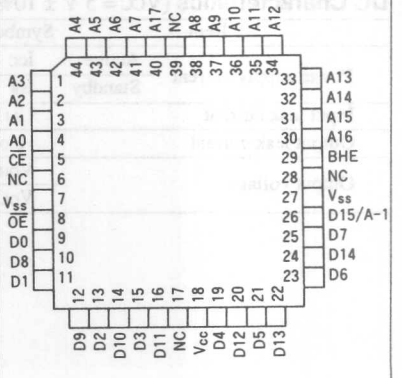
Pin Arrangement

HN62404, HN62424P



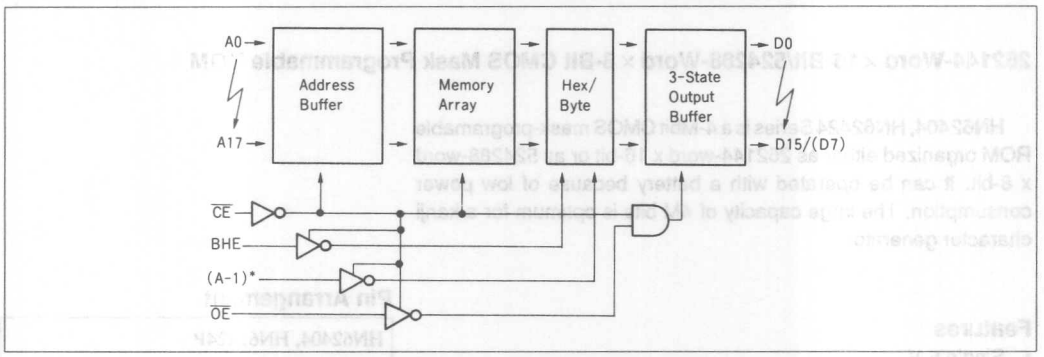
(Top View)

HN62404FP, HN62424FP



(Top View)

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

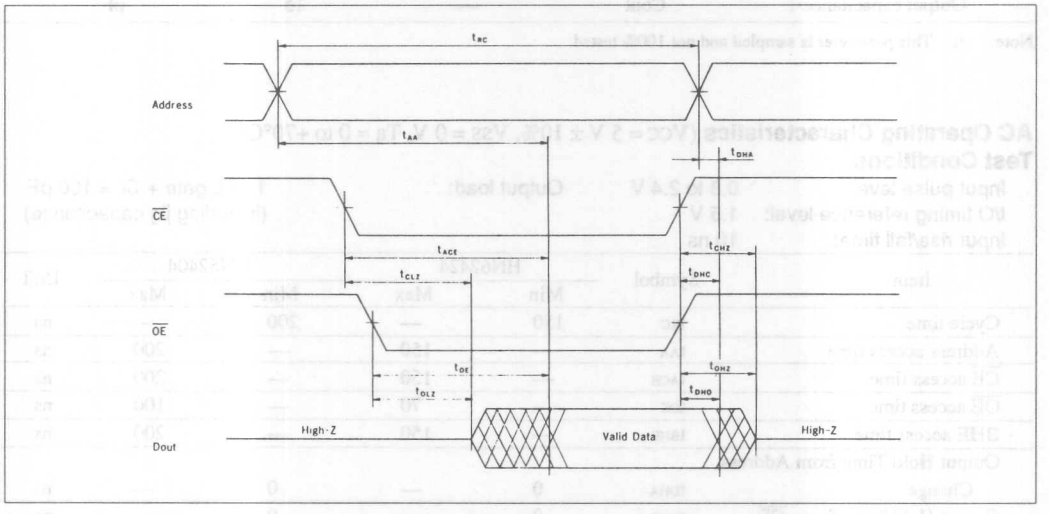
Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	HN62424		HN62404		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
$\overline{BHE}$ access time	t_{BHE}	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	—	10	—	ns

Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

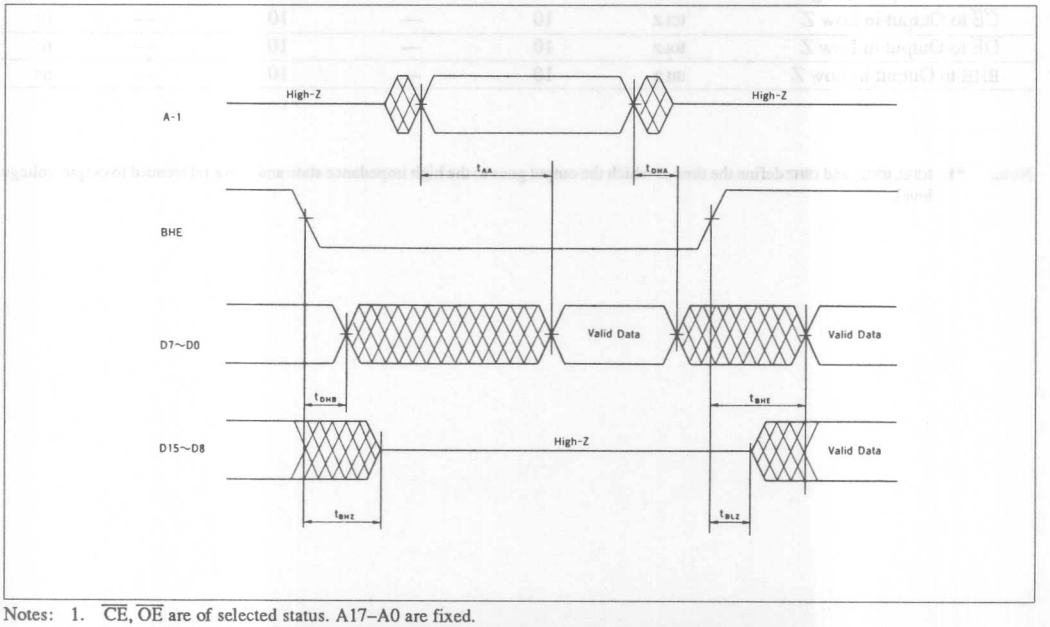
Timing Waveform

Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by whichever is slower.
3. t_{CLZ}, t_{OLZ}; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A17–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, CE and OE are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62304B Series
HN62324B Series

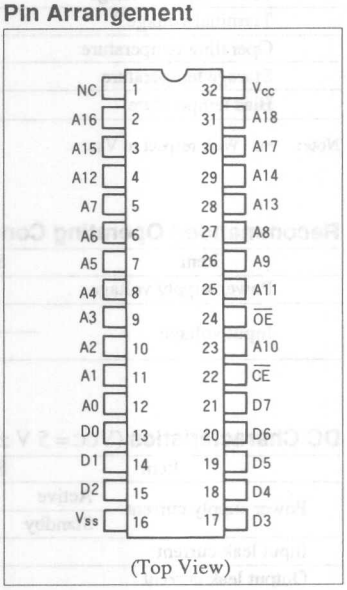
524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62304B, HN62324B Series is a 4-Mbit CMOS mask-programable ROM organized as 524288-word x 8-bits. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max.)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide Data Organization

Pin Arrangement

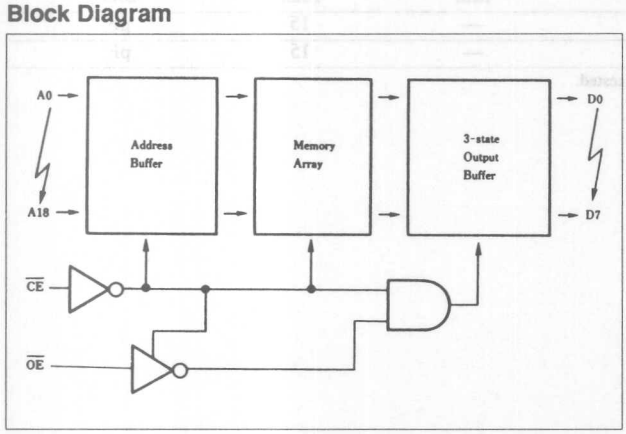


(Top View)

Ordering Information

Type No.	Address Access Time	Package
HN62304BP	200 ns	600 mil 32-pin
HN62324BP	150 ns	plastic DIP
HN62304BF	200 ns	32-pin
HN62324BF	150 ns	plastic SOP

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

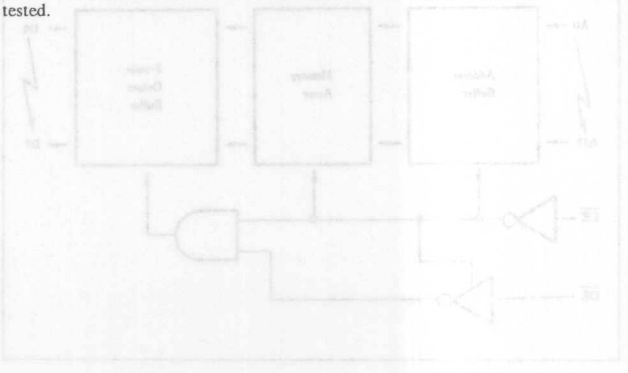
DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.



AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

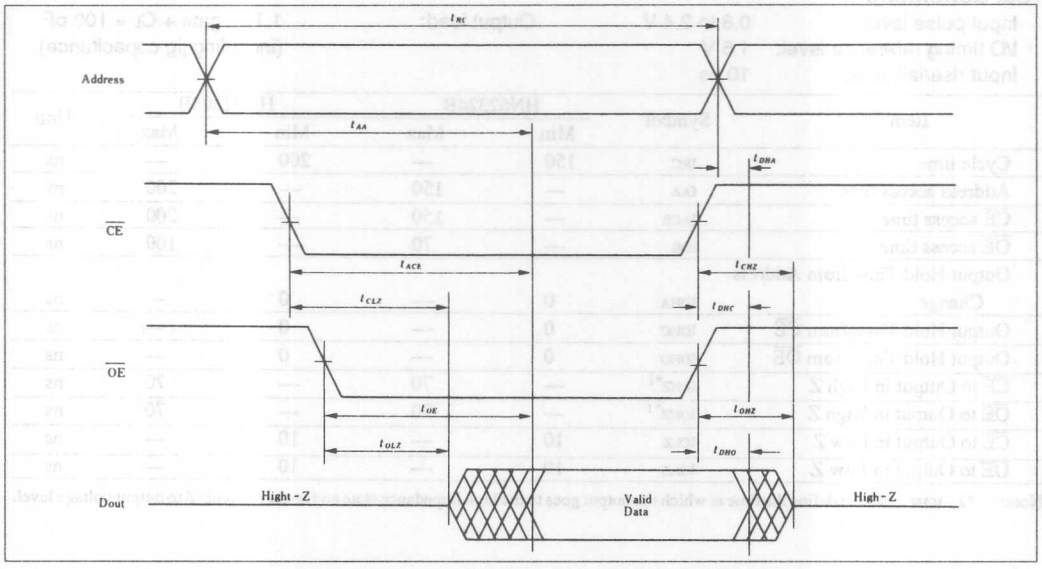
Test Conditions

Input pulse level:	0.8 to 2.4 V	Output load:	1 TTL gate + C_L = 100 pF
I/O timing reference level:	1.5 V		(including jig capacitance)
Input rise/fall time:	10 ns		

Item	Symbol	HN62324B		HN62304B		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

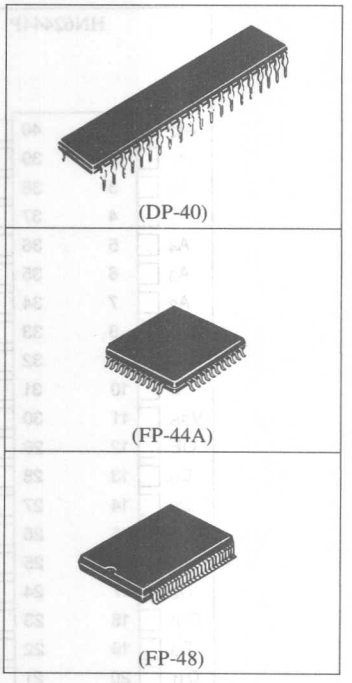
Timing Waveform



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

HN62444 Series — Preliminary

262,144 × 16-Bit/524,288 × 8-Bit CMOS MASK Programmable Read Only Memory



■ DESCRIPTION

The HN62444 is a 4-Mbit CMOS mask-programmable ROM organized either as 262,144 words by 16 bits or as 524,288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62444, which provides large capacity of 4M bits, is ideally suited for kanji character generators.

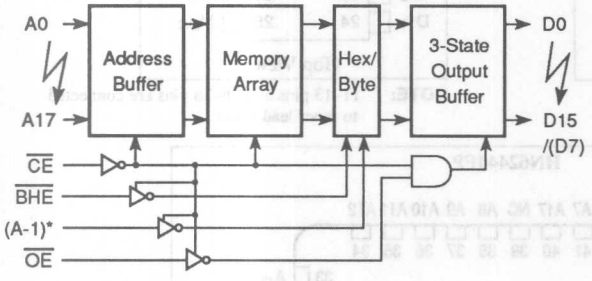
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .100ns (max.)
- Low Power Consumption . . . . . .150mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide or Word-wide Data Organization with BHE

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62444P	100ns	600 mil 40 pin Plastic DIP
HN62444FP	100ns	44 pin Plastic QFP
HN62444F	100ns	48 pin Plastic SOP

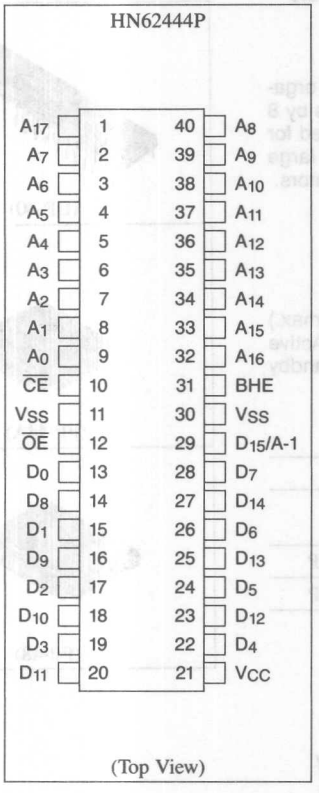
■ BLOCK DIAGRAM



BHE = V_{IH}; 16-bit (D_{15} ~ D_0)
BHE = V_{IL}; 8-bit (D_7 ~ D_0)
* A-1 is least significant address. When BHE is "low", D_{14} ~ D_8 goes the high impedance state.

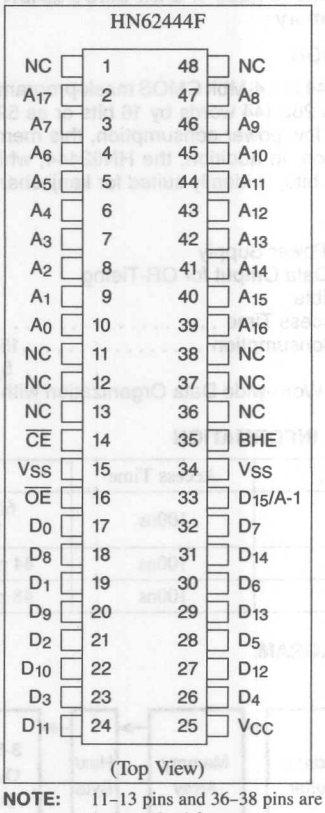
■ PIN ARRANGEMENT

HN62444P



(Top View)

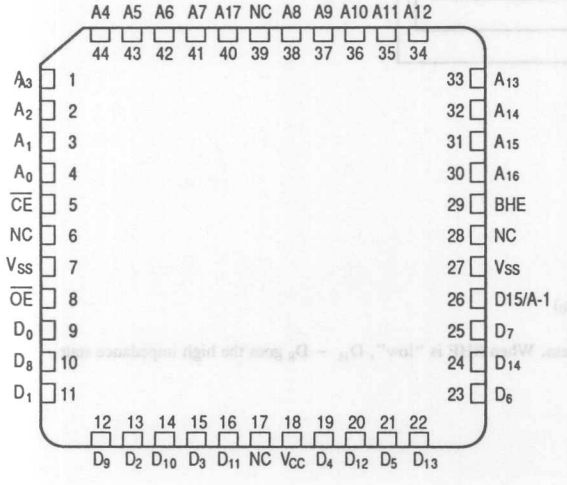
HN62444F



(Top View)

NOTE: 11–13 pins and 36–38 pins are connected to inner lead frame.

HN62444FP



(Top View)

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−0.3 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.45	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	70	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.4V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100	—	ns
Address Access Time	t_{AA}	—	100	ns
$\overline{CE}$ Access Time	t_{ACE}	—	100	ns
$\overline{OE}$ Access Time	t_{OE}	—	50	ns
BHE Access Time	t_{BHE}	—	100	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	ns
Output Hold Time From BHE	t_{DHB}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	40	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	40	ns
BHE to Output in High Z	t_{BHZ}*	—	40	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	—	ns
BHE to Output in Low Z	t_{BLZ}	5	—	ns

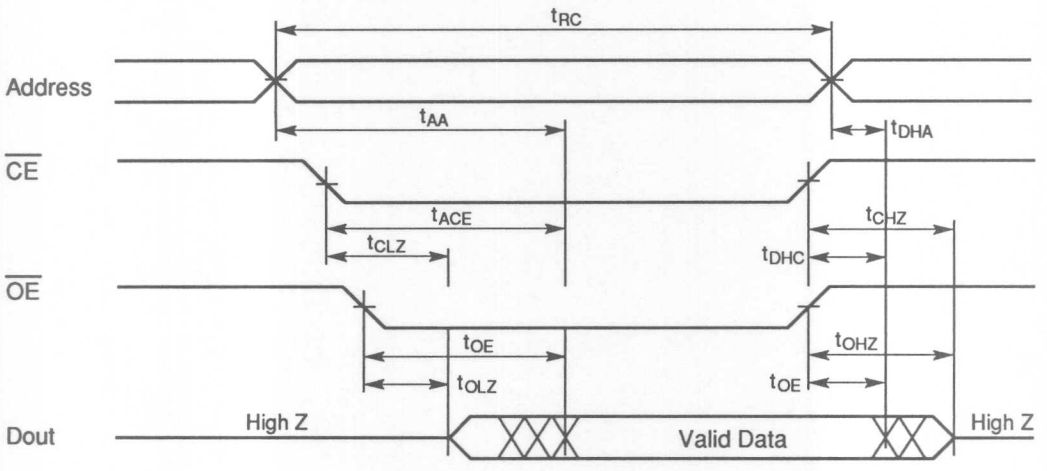
NOTE: * t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

• Test Conditions

- Input Pulse Level: 0.45 ~ 2.4V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Time: 10ns
- Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

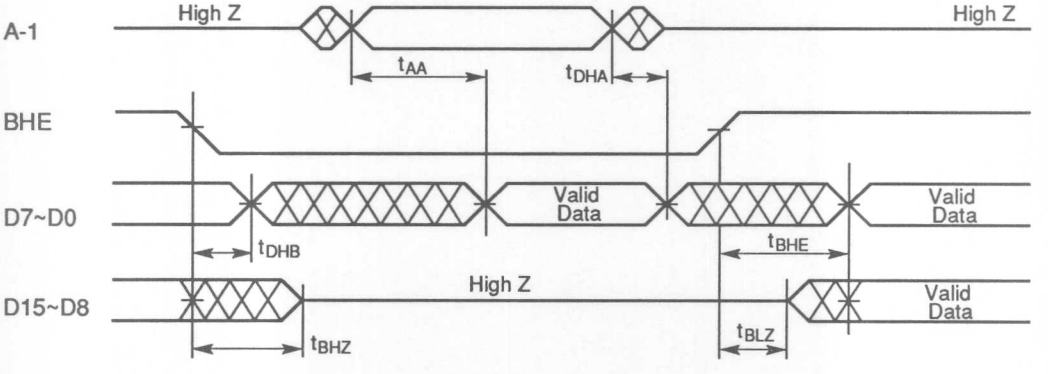
■ TIMING WAVEFORM

• Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}') (1)



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

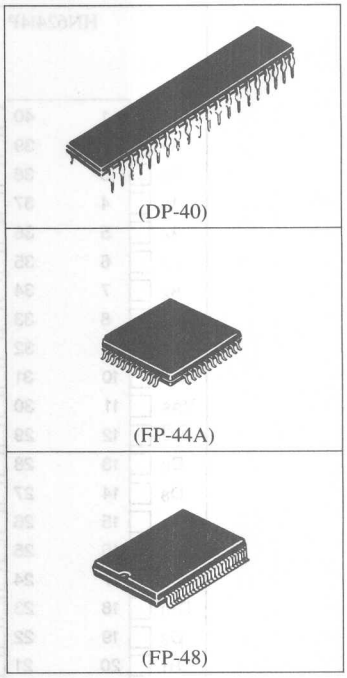
• Word Mode, Byte Mode Switch (2)



NOTES:
1. $\overline{CE}$ and $\overline{OE}$ are enable $A_{17} \sim A_0$ are valid.
2. D_{15}/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not apply to them.

HN62414 Series — Preliminary

262,144 × 16-Bit/524,288 × 8-Bit CMOS MASK Programmable Read Only Memory



■ DESCRIPTION

The HN62414 is a 4-Mbit CMOS mask-programmable ROM organized either as 262,414 words by 16 bits or as 524,288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62414, which provides large capacity of 4M bits, is ideally suited for kanji character generators.

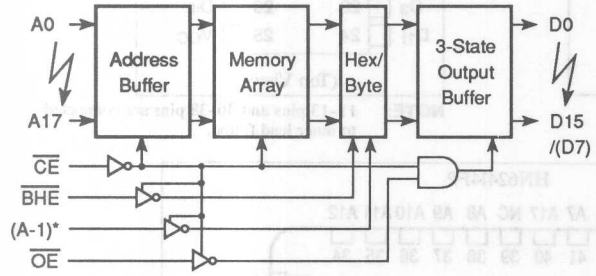
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .170/200ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide or Word-wide Data Organization with BHE

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62414P-17/20	170/200ns	600 mil 40 pin Plastic DIP
HN62414FP-17/20	170/200ns	44 pin Plastic QFP
HN62414F-17/20	170/200ns	48 pin Plastic SOP

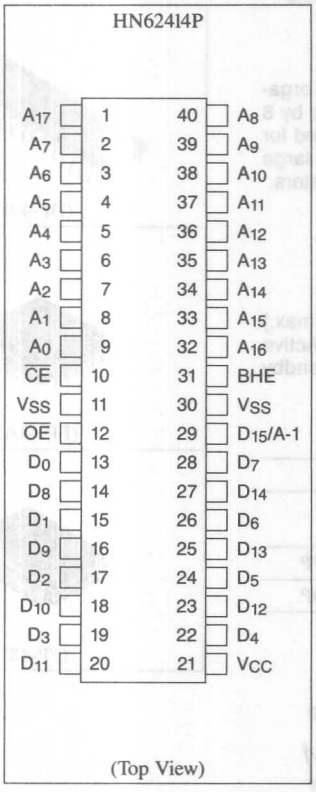
■ BLOCK DIAGRAM



BHE = V_{IH}; 16-bit (D_{15} ~ D_0)
BHE = V_{IL}; 8-bit (D_7 ~ D_0)
* A-1 is least significant address. When BHE is "low", D_{14} ~ D_8 goes the high impedance state.

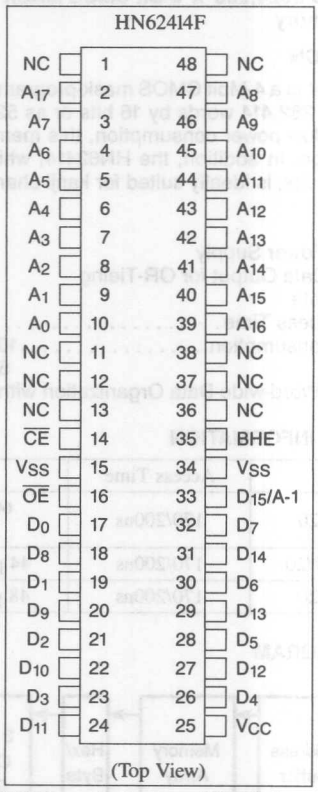
■ PIN ARRANGEMENT

HN62414P



(Top View)

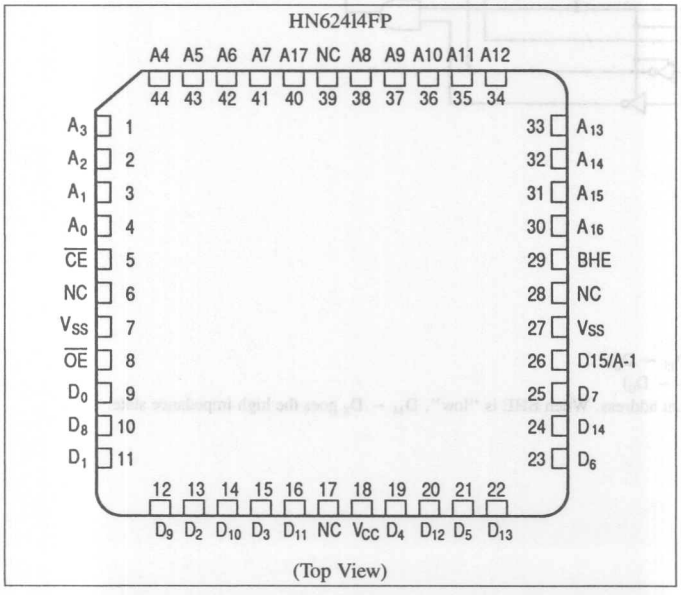
HN62414F



(Top View)

NOTE: 11–13 pins and 36–38 pins are connected to inner lead frame.

HN62414FP



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−0.3 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.2V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	HN62414-17		HN62414-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	170	—	200	—	ns
Address Access Time	t_{AA}	—	170	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	170	—	200	ns
$\overline{OE}$ Access Time	t_{OE}	—	70	—	100	ns
BHE Access Time	t_{BHE}	—	170	—	200	ns
Output Hold Time From Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output Hold Time From BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	70	—	70	ns
BHE to Output in High Z	t_{BHZ}*	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns
BHE to Output in Low Z	t_{BLZ}	10	—	10	—	ns

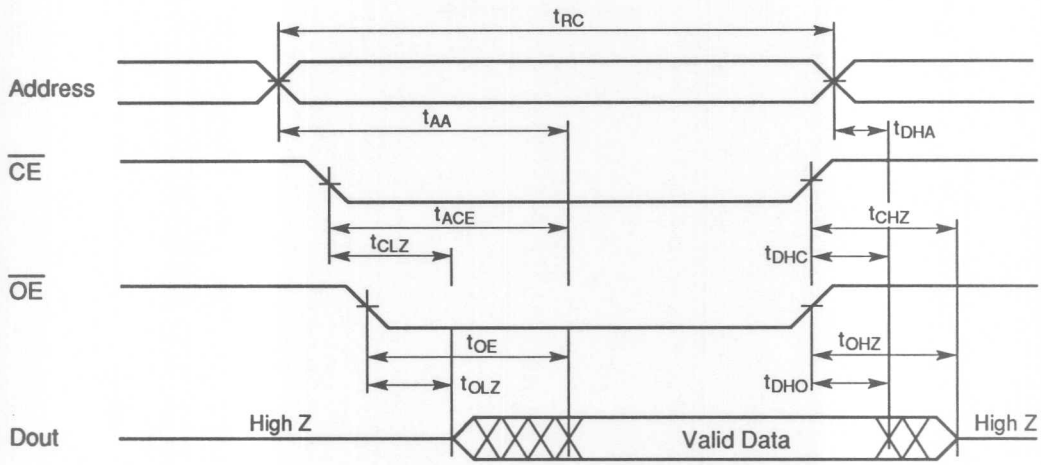
NOTE: * t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

• Test Conditions

- Input Pulse Level: 0.8 ~ 2.4V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Time: 10ns
- Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

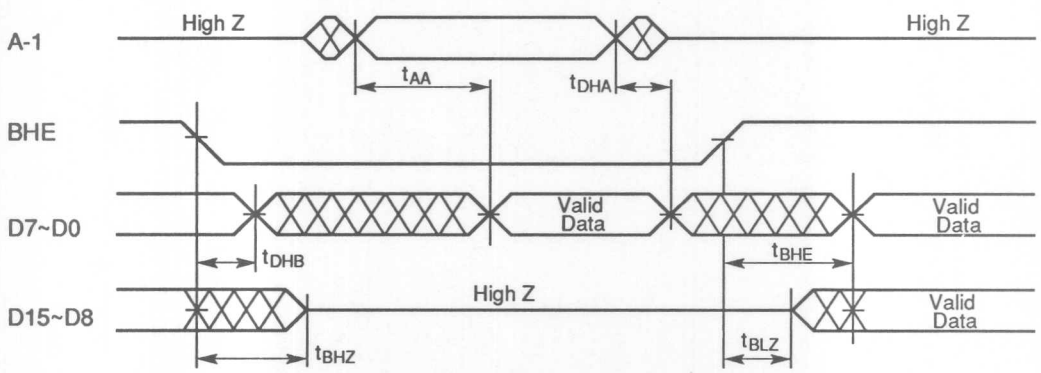
■ TIMING WAVEFORM

• Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}') (1)



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

• Word Mode, Byte Mode Switch (2)



NOTES:
1. $\overline{CE}$ and $\overline{OE}$ are enable $A_{17} \sim A_0$ are valid.
2. D_{15}/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not apply to them.

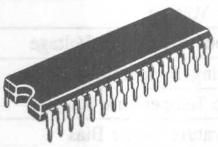
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HN62314B Series — Preliminary

524,288 × 8-Bit CMOS MASK Programmable Read Only Memory

■ DESCRIPTION

The HN62314B is a 4-Mbit CMOS mask-programmable ROM organized as 524,288-words × 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62314B, which provides large capacity of 4M bits, is ideally suited for kanji character generators.



(DP-32)



(FP-32D)

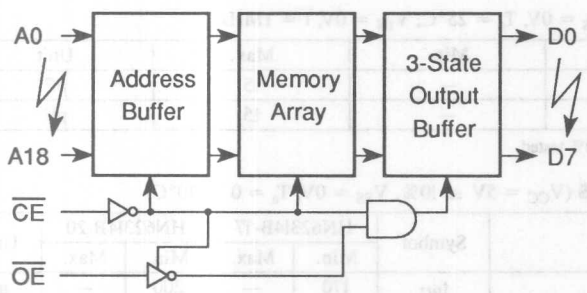
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .200ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide Data Organization
- Pin Compatible with JEDEC

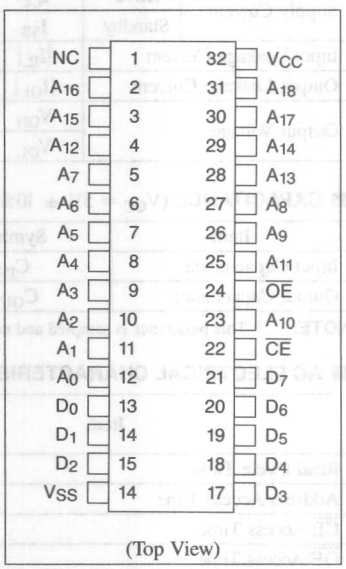
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62314BP-17/20	170/200ns	600 mil 32 pin Plastic DIP
HN62314BF-17/20	170/200ns	32 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−3.0 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.2V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

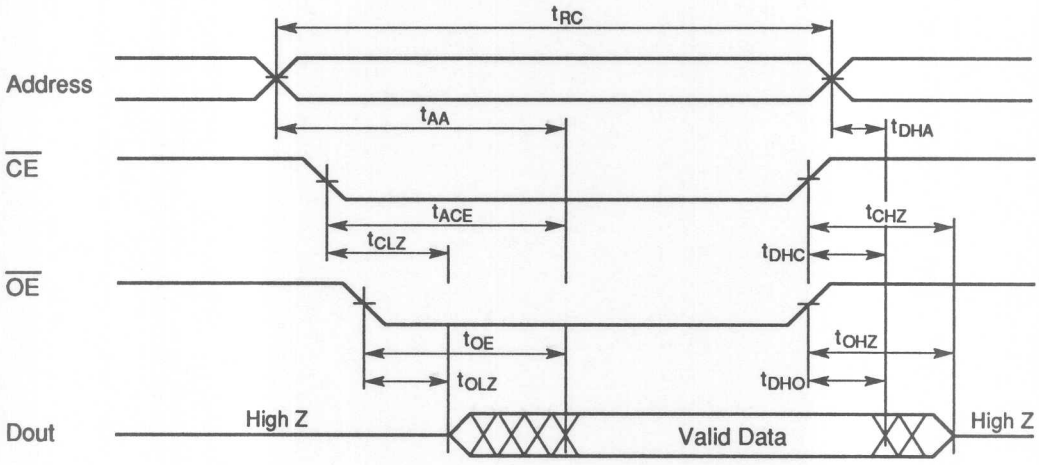
■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	HN62314B-17		HN62314B-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	170	—	200	—	ns
Address Access Time	t_{AA}	—	170	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	170	—	200	ns
$\overline{OE}$ Access Time	t_{OE}	—	70	—	100	ns
Output Hold Time From Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns

NOTE: * t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

- **Test Conditions**
  - Input Pulse Level: 0.8 ~ 2.4V
  - Input and Output Timing Reference Level: 1.5V
  - Input Rise and Fall Time: 10ns
  - Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

■ TIMING WAVEFORM



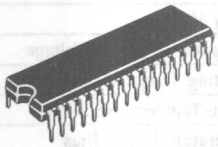
NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

HN62344B Series — Preliminary

524,288 × 8-Bit CMOS MASK Programmable Read Only Memory

■ DESCRIPTION

The HN62344B is a 4-Mbit CMOS mask-programmable ROM organized as 524,288-words × 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62344B, which provides large capacity of 4M bits, is ideally suited for kanji character generators.



(DP-32)



(FP-32D)

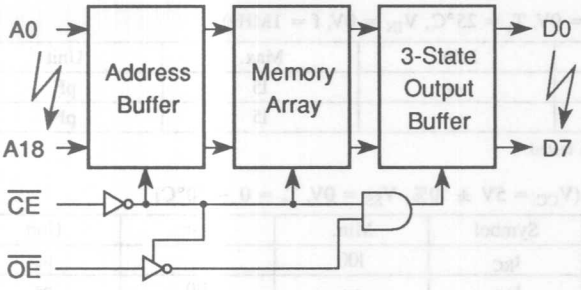
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .100ns (max.)
- Low Power Consumption . . . . . .150mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide Data Organization
- Pin Compatible with JEDEC

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62344BP	100ns	600 mil 32 pin Plastic DIP
HN62344BF	100ns	32 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−3.0 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.45	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	70	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.4V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

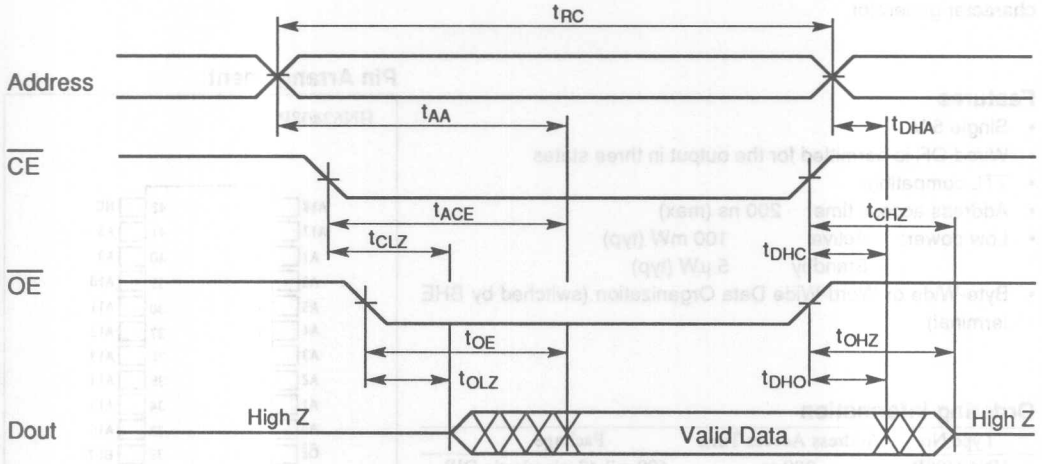
■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100	—	ns
Address Access Time	t_{AA}	—	110	ns
$\overline{CE}$ Access Time	t_{ACE}	—	100	ns
$\overline{OE}$ Access Time	t_{OE}	—	50	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	40	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	40	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	—	ns

NOTE: * t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

- **Test Conditions**
  - Input Pulse Level: 0.45 ~ 2.4V
  - Input and Output Timing Reference Level: 1.5V
  - Input Rise and Fall Time: 10ns
  - Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

■ TIMING WAVEFORM



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

HN62408 Series — Preliminary

524288-Word × 16-Bit/1048576-Word × 8-Bit CMOS Mask Programmable ROM

HN62408 Series is a 8-Mbit CMOS mask-programable ROM organized either as 524288-word x 16-Bit or as 1048576-Wod x 8-Bit. It can be operated with a battery because of low power consumption. The large capacity of 8M bits is optimum for a kanji character generator.

Features

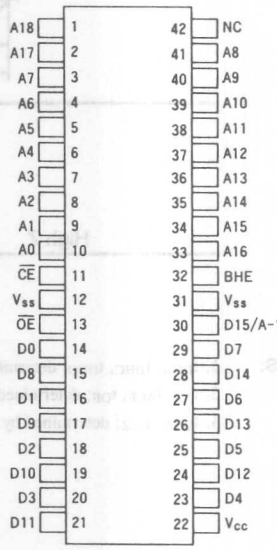
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62408P	200 ns	600 mil 42-pin plastic DIP
HN62408FP	200 ns	44-pin plastic QFP

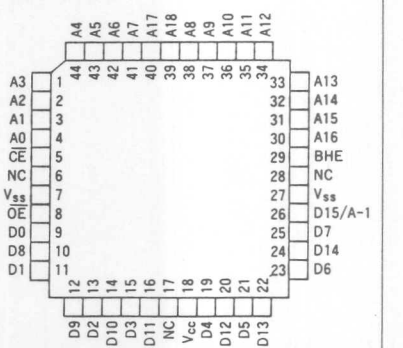
Pin Arrangement

HN62408P



(Top View)

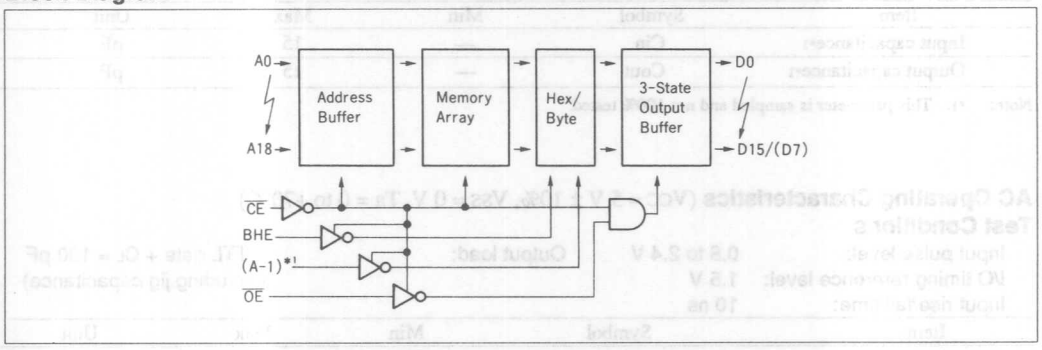
HN62408FP



(Top View)

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sale Dept. regarding specifications.

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Rrecommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

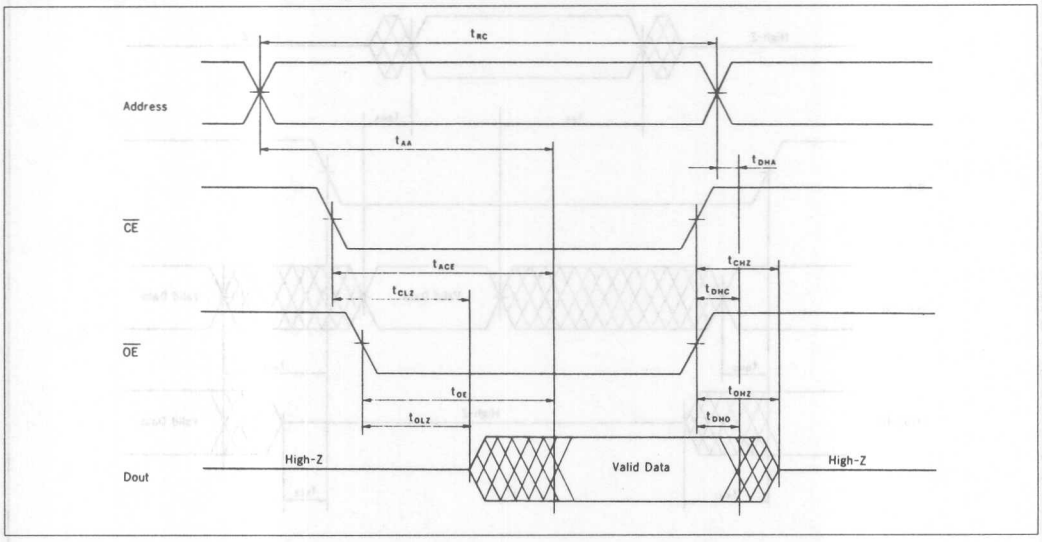
Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	Min	Max	Unit
Cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
BHE access time	t_{BHE}	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns
Output Hold Time from BHE	t_{DHB}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
BHE to Output in Low Z	t_{BLZ}	10	—	ns

Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

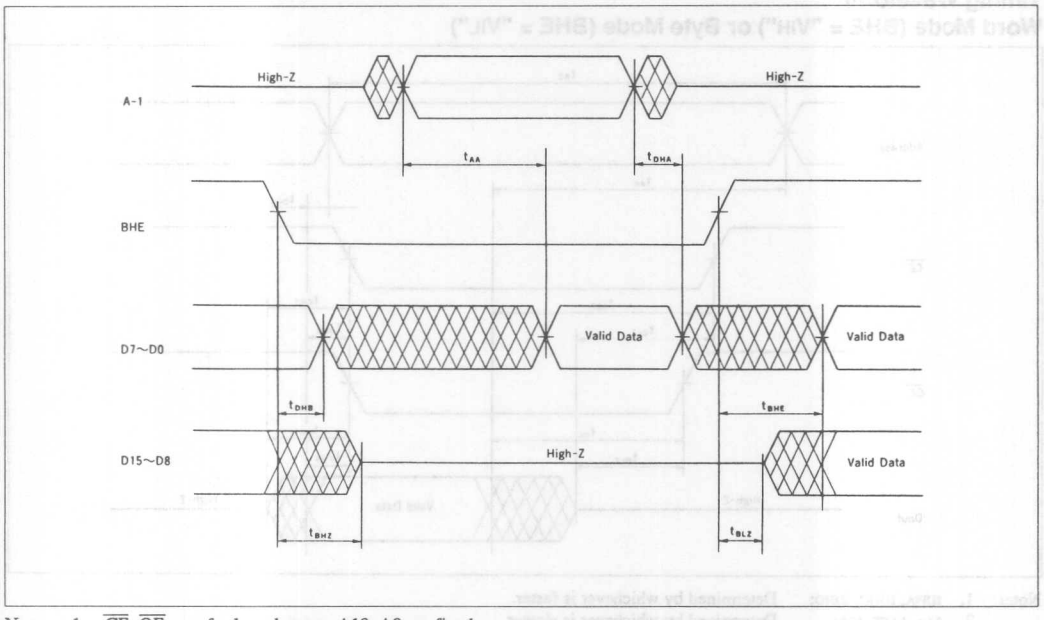
Timing Waveform

Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



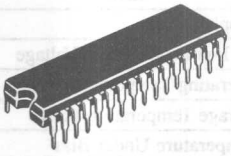
Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = V_{IH}, CE and OE are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62308B Series

1048576 × 8-Bit CMOS MASK Programmable Read Only Memory

■ DESCRIPTION

The HN62308B is a 8-Mbit CMOS mask-programmable ROM organized as 1048576-words × 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62308B, which provides large capacity of 8M bits, is ideally suited for kanji character generators.



(DP-32)



(FP-32D)

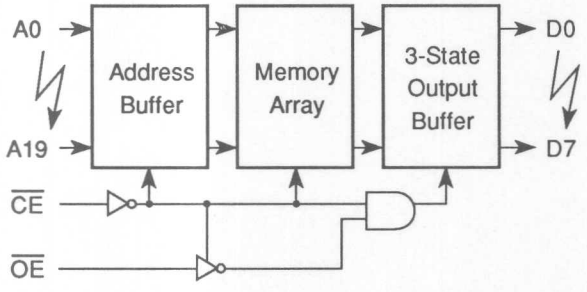
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .200ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide Data Organization
- Pin Compatible with JEDEC

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62308BP	200ns	600 mil 32 pin Plastic DIP
HN62308BF	200ns	32 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−3.0 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.2V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

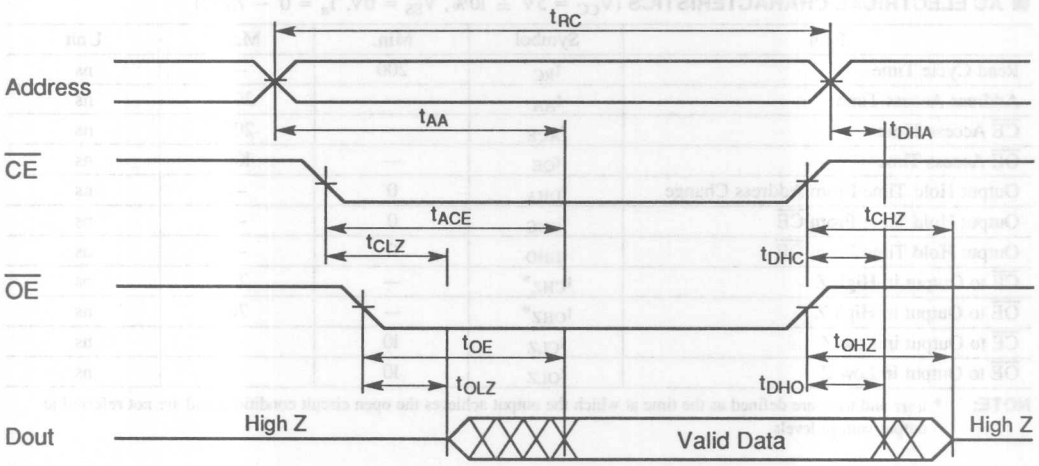
■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	200	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns

NOTE: * t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

- **Test Conditions**
  - Input Pulse Level: 0.8 ~ 2.4V
  - Input and Output Timing Reference Level: 1.5V
  - Input Rise and Fall Time: 10ns
  - Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

■ TIMING WAVEFORM

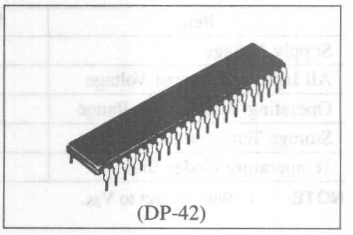


NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HN66403P Series

524,288 × 16-Bit/1,048,576 × 8-Bit CMOS MASK Programmable Read Only Memory



(DP-42)

■ DESCRIPTION

The HN66403P is an 8-Mbit CMOS mask-programmable ROM module consisted of 2 pieces of HN62404 products and HD74HC00 equivalent product. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN66403P, which provides large capacity of 8M bits, is ideally suited for kanji character generators.

■ FEATURES

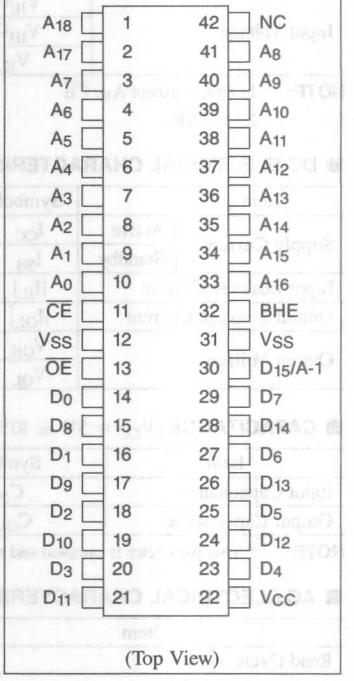
- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .250ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide or Word-wide Data Organization with BHE
- Pin Compatible with HN62408P

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN66403P	250ns	600 mil 42 pin Plastic DIP

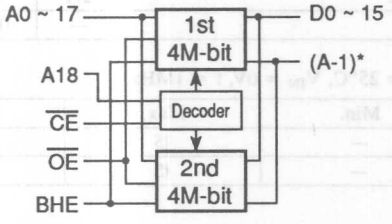
■ PIN ARRANGEMENT

HN66403P



(Top View)

■ BLOCK DIAGRAM



BHE = V_{IH}; 16-bit (D_{15} ~ D_0)
BHE = V_{IL}; 8-bit (D_7 ~ D_0)
* A-1 is least significant address. When BHE is "low", D_{14} ~ D_8 goes the high impedance state.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−0.3 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}(1)	2.2	—	V_{CC} + 0.3	V
	V_{IH}(2)	V_{CC} × 0.7	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

NOTE: 1. Others except A_{18}, $\overline{CE}$
2. A_{18}, $\overline{CE}$

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE}$ ≥ V_{CC} − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = V_{CC} × 0.7, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

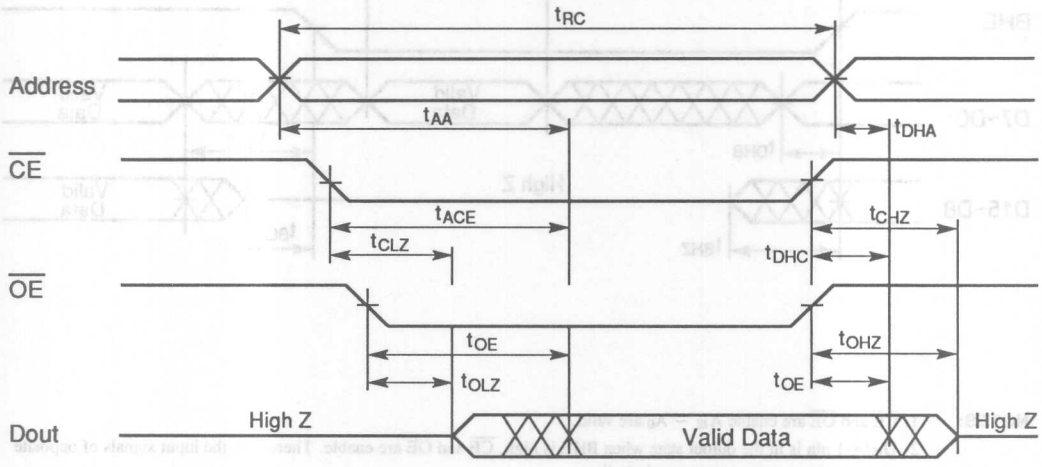
Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
$\overline{CE}$ Access Time	t_{ACE}	—	250	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
BHE Access Time	t_{BHE}	—	250	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	ns
Output Hold Time From BHE	t_{DHB}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	120	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	70	ns
BHE to Output in High Z	t_{BHZ}*	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
BHE to Output in Low Z	t_{BLZ}	10	—	ns

NOTE: * t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

- **Test Conditions**
  - Input Pulse Level: 0.8 ~ 2.4V
    Other except pin A_{18}, $\overline{CE}$
  - Input and Output Timing Reference Level: 1.5V
  - Input Rise and Fall Time: 10ns
  - Output Load: 1 TTL gate + CL = 100pF
    (including scope and jig capacitance)

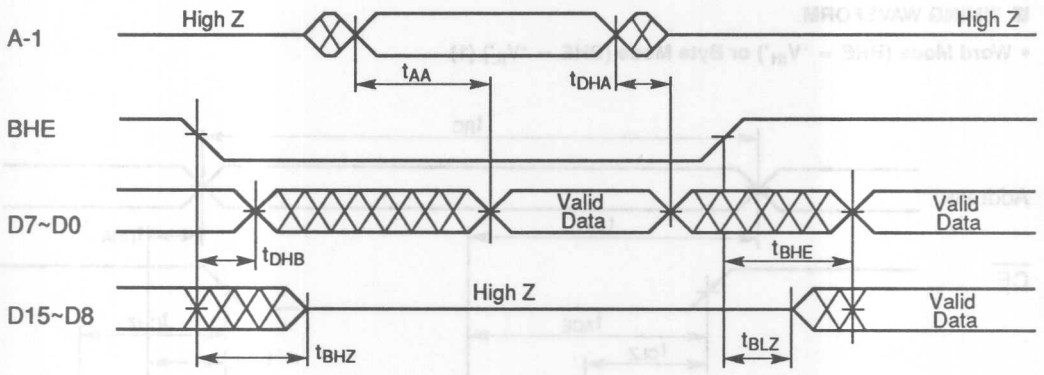
■ TIMING WAVEFORM

- **Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}') (1)**



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

• **Word Mode, Byte Mode Switch (2)**

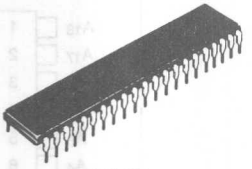


NOTES: 1. $\overline{CE}$ and $\overline{OE}$ are enable $A_{18} \sim A_0$ are valid.

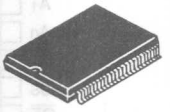
2. D_{15}/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not apply to them.

HN624016 Series

1,048,576 × 16-Bit/2,097,152 × 8-Bit CMOS MASK Programmable Read Only Memory



(DP-42)



(FP-48)

■ DESCRIPTION

The HN624016 is a 16-Mbit CMOS mask-programmable ROM organized either as 1048576 words by 16 bits or as 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN624016, which provides large capacity of 16M bits, is ideally suited for kanji character generators.

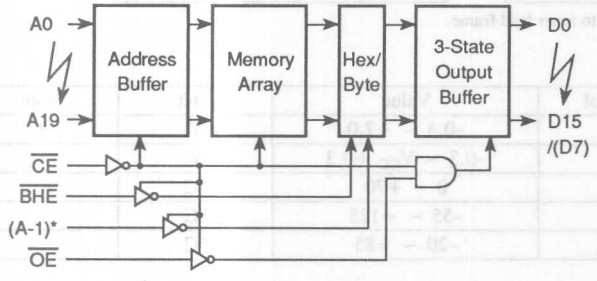
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . .200ns (max.)
- Low Power Consumption . . . . . .100mW (typ.) Active
  5μW (typ.) Standby
- Byte-wide or Word-wide Data Organization with BHE

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624016P	200ns	600 mil 42 pin Plastic DIP
HN624016F	200ns	48 pin Plastic SOP

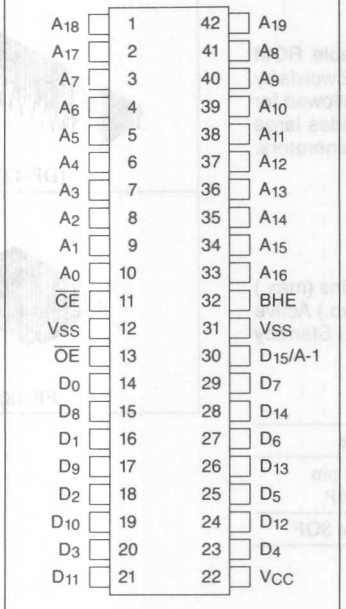
■ BLOCK DIAGRAM



BHE = V_{IH}; 16-bit (D_{15} ~ D_0)
BHE = V_{IL}; 8-bit (D_7 ~ D_0)
* A-1 is least significant address. When BHE is "low", D_{14} ~ D_8 goes the high impedance state.

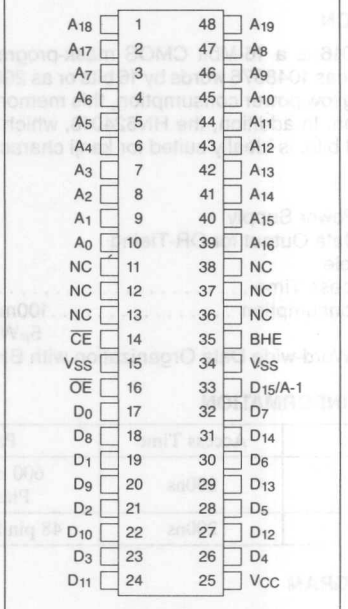
■ PIN ARRANGEMENT

HN624016P



(Top View)

HN624016F



(Top View)

NOTE: 12–13 pin and 36–37 pin are connected to inner lead frame.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	−0.3 ~ V_{CC} +0.3	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	−55 ~ +125	°C	
Temperature Under Bias	T_{bias}	−20 ~ +85	°C	

NOTE: 1. With respect to V_{SS}.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item		Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I_{CC}	V_{CC} = 5.5V, ID_{OUT} = 0mA, t_{RC} = Min.	—	50	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC}$ − 0.2V	—	30	μA
Input Leakage Current		$\|I_{IL}\|$	V_{IN} = 0 ~ V_{CC}	—	10	μA
Output Leakage Current		$\|I_{OL}\|$	$\overline{CE}$ = 2.2V, V_{OUT} = 0 ~ V_{CC}	—	10	μA
Output Voltage		V_{OH}	I_{OH} = −205μA	2.4	—	V
		V_{OL}	I_{OL} = 1.6mA	—	0.4	V

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	15	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 ~ 70°C)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	200	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
BHE Access Time	t_{BHE}	—	200	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time From $\overline{OE}$	t_{DHO}	0	—	ns
Output Hold Time From BHE	t_{DHB}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*	—	70	ns
BHE to Output in High Z	t_{BHZ}*	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
BHE to Output in Low Z	t_{BLZ}	10	—	ns

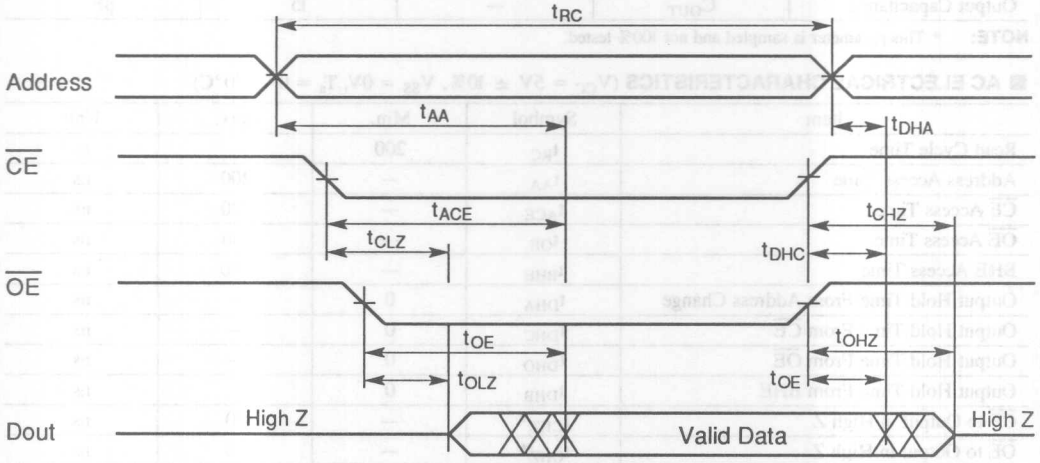
NOTE: * t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

• Test Conditions

- Input Pulse Level: 0.8 ~ 2.4V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Time: 10ns
- Output Load: 1 TTL gate + CL = 100pF (including scope and jig capacitance)

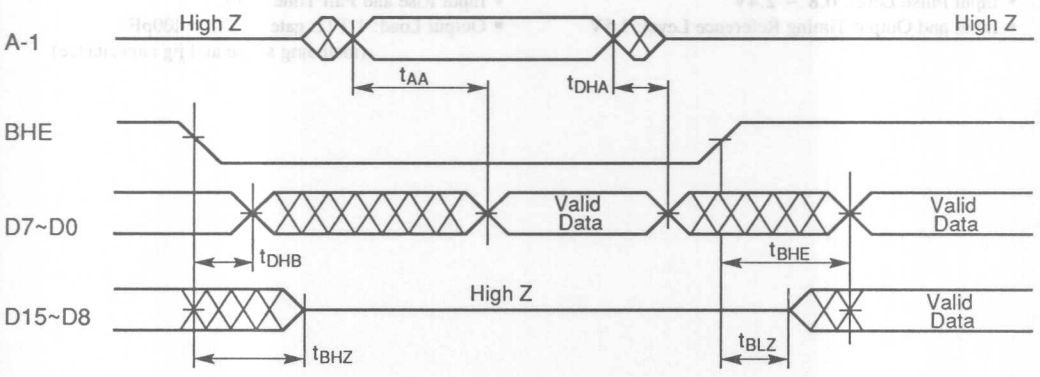
■ TIMING WAVEFORM

• Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}') (1)



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

• Word Mode, Byte Mode Switch (2)



NOTES:
1. $\overline{CE}$ and $\overline{OE}$ are enable $A_{19} \sim A_0$ are valid.
2. D_{15}/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not apply to them.

Section 8
MOS PROM

8

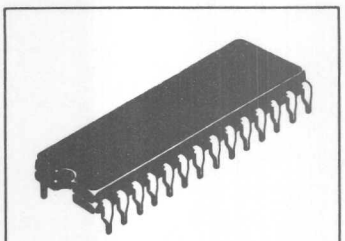
HITACHI®

HN58064 Series

8192-word x 8-bit Electrically Erasable and Programmable ROM.

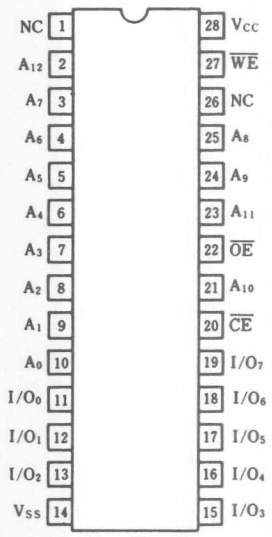
■ FEATURES

- Single 5V Supply
- Address, Data, $\overline{CE}$, $\overline{OE}$ Latches
- Byte Erase / Byte Write Time. . . . . 10 ms typ.
- Chip Erase Time . . . . . 20 ms typ.
- Fast Access Time. . . . . 250/300ns max.
- Low Power Dissipation. . . . . 300mW typ. (Active)
  . . . . . 125mW typ. (Standby)
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles



(DP-28)

■ PIN ARRANGEMENT



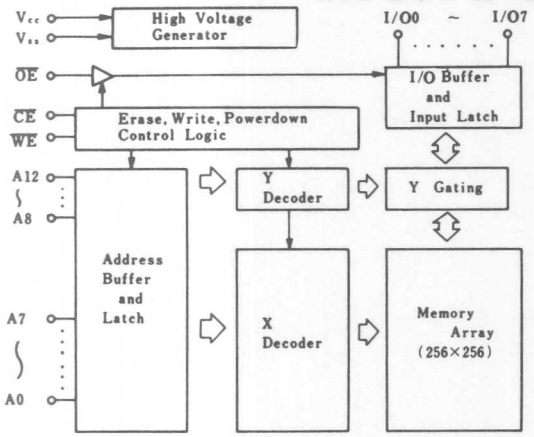
(Top View)

A0 – A12	Address Input
I/O0 – I/O7	Data in / Data out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
Vcc	Power (+5V)
Vss	GND
NC	No Connect

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58064P-25	250ns	600 mil 28 pin Plastic DIP
HN58064P-30	300ns	

■ BLOCK DIAGRAM



■ MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Standby	V_{IH}	X	X	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	Din = V_{IH}
Byte Write	V_{IL}	V_{IH}	V_{IL}	Din
Chip Erase	V_{IL}	V_{IL}	V_{IL}	Din = V_{IH}
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IH} or V_{IL}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	−0.6 to +7.0	V
Input Voltage*1	V_{in}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Note: *1. With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.1	–	0.8	V
	V_{IH}	2.0	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{in} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V, V_{out} = 5.5/0.4V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	25	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	60	100	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V

■ CAPACITANCE (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	12	pF

■ AC TEST CONDITIONS

Input Pulse Levels:	0.4V to 2.4V
Input Rise and Fall Time:	≦ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	0.8V and 2.0V

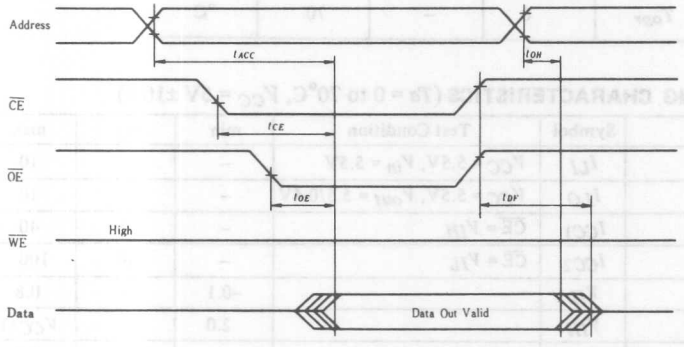
■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• READ OPERATION

Parameter	Symbol	Test Condition	HN58064-25		HN58064-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	100	–	150	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	0	–	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	0	90	0	130	ns

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

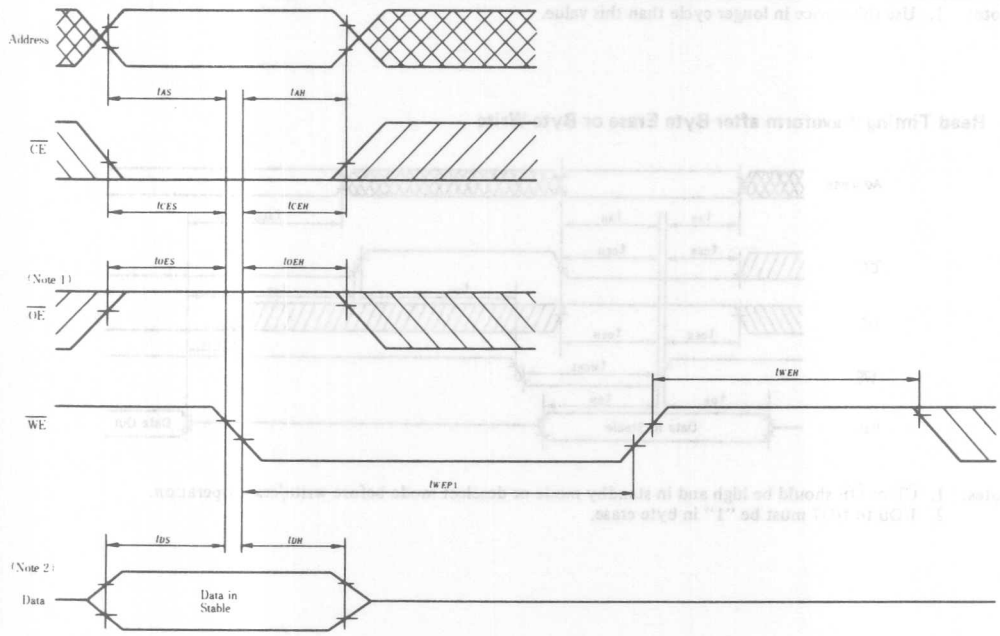
• WAVE FORM ..... READ CYCLE



• BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		0	–	–	ns
Address Hold Time	t_{AH}		100	–	–	ns
$\overline{CE}$ Setup Time	t_{CES}		0	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		100	–	–	ns
$\overline{OE}$ Setup Time	t_{OES}		0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		100	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP1}		8	10	15	ms
$\overline{WE}$ High Time	t_{WEH}		1000	–	–	ns
Data Setup Time	t_{DS}		0	–	–	ns
Data Hold Time	t_{DH}		100	–	–	ns

• WAVE FORM ..... ERASE AND WRITE CYCLE



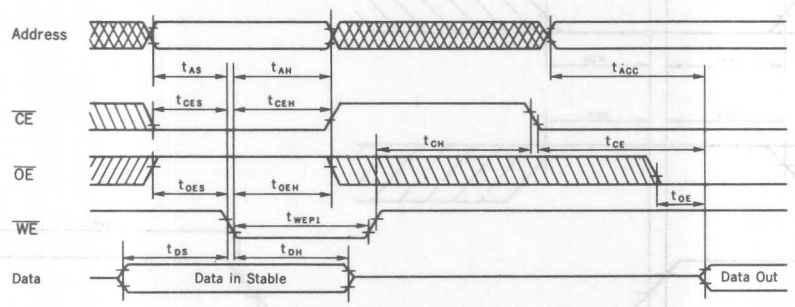
Notes: 1. $\overline{CE}$ or $\overline{OE}$ should be "1" and in Standby Mode or Deselect Mode before Write/Erase operation.
2. I/O0 to I/O7 must be "1" in Byte Erase.

• Read Cycle after Byte Erase or Byte Write

Parameter	Symbol	HN58064-25			HN58064-30			Unit
		min*1	typ	max	min*1	typ	max	
Address setup time	t_{AS}	0	–	–	0	–	–	ns
Address hold time	t_{AH}	100	–	–	100	–	–	ns
$\overline{CE}$ setup time	t_{CES}	0	–	–	0	–	–	ns
$\overline{CE}$ hold time	t_{CEH}	100	–	–	100	–	–	ns
$\overline{OE}$ setup time	t_{DES}	0	–	–	0	–	–	ns
$\overline{OE}$ hold time	t_{DEH}	100	–	–	100	–	–	ns
$\overline{WE}$ pulse width	t_{WEPI}	10	12	15	10	12	15	ms
$\overline{CE}$ high time	t_{CH}	10	–	–	10	–	–	μs
Data setup time	t_{DS}	0	–	–	0	–	–	ns
Data hold time	t_{DH}	100	–	–	100	–	–	ns
Address to output delay time	t_{ACC}	250	–	–	300	–	–	ns
$\overline{CE}$ to output delay time	t_{CE}	250	–	–	300	–	–	ns
$\overline{OE}$ to output delay time	t_{OE}	100	–	–	150	–	–	ns

Note: 1. Use this device in longer cycle than this value.

• Read Timing Waveform after Byte Erase or Byte Write



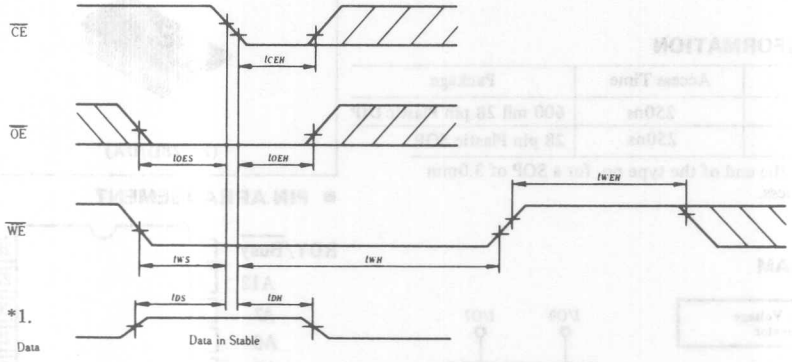
Notes: 1. $\overline{CE}$ or $\overline{OE}$ should be high and in standby mode or deselect mode before write/erase operation.
2. I/O0 to I/O7 must be "1" in byte erase.

HITACHI
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• CHIP ERASE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{CE}$ Hold Time	t_{CEH}		100	–	–	ns
$\overline{OE}$ Setup Time	t_{OES}		0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		100	–	–	ns
$\overline{WE}$ Setup Time	t_{WS}		0	–	–	ns
$\overline{WE}$ Pulse Width	t_{WH}		15	20	25	ms
$\overline{WE}$ High Time	t_{WEH}		1000	–	–	ns
Data Setup Time	t_{DS}		0	–	–	ns
Data Hold Time	t_{DH}		100	–	–	ns

• WAVE FORM ..... CHIP ERASE



Notes: 1. I/O0 ~ 7 must be "1" in Chip Erase Operation.
2. Don't Care about Address.

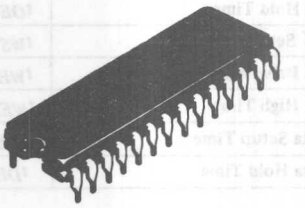
HN58C65 Series

8192-word x 8-bit Electrically Erasable and Programmable CMOS ROM

■ FEATURES

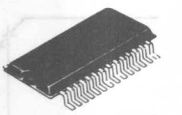
- Single 5V Supply
- On Chip Latches; Address, Data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic Byte Write . . . . . 10ms max.
- Automatic Page Write
  (32byte) . . . . . 10ms max.
- Fast Access Time . . . . . 250ns max.
- Low Power Dissipation . . . 20mW/MHz typ. (Active)
  . . . 2mW typ. (Standby)
- $\overline{DATA}$ Polling and Ready/$\overline{Busy}$
- Data Protection Circuity on Power On/Power Off
- Conforms to JEDEC Byte-Wide Standard
- Reliable CMOS with MNOS Cell Technology
- 10^5 Erase/Write Cycles in page mode and 10 year Data Retention

HN58C65P Series



(DP-28)

HN58C65FP Series



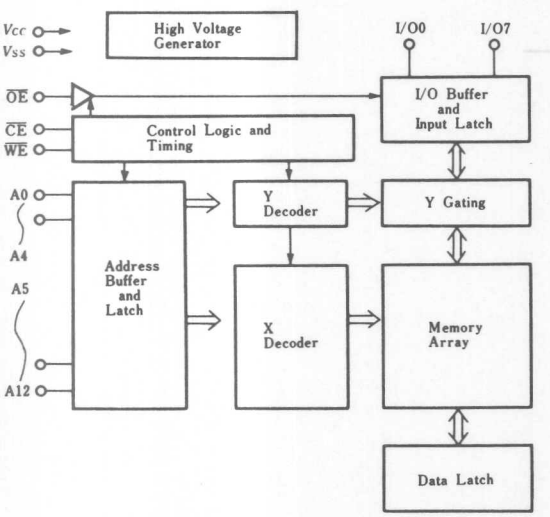
(FP-28D/DA)

■ ORDERING INFORMATION

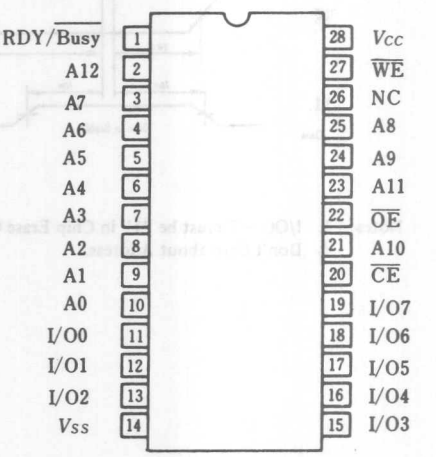
Type No.	Access Time	Package
HN58C65P-25	250ns	600 mil 28 pin Plastic DIP
HN58C65FP-25	250ns	28 pin Plastic SOP

Note) T is added to the end of the type no. for a SOP of 3.0mm (max.) thickness.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

A0 – A12	Address Input
I/O1 – I/O7	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

■ MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{Busy}$ (1)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	V_{IH}	High Z	Dout
Standby	V_{IH}	×	×	High Z	High Z
Write	V_{IL}	V_{IH}	V_{IL}	High Z→ V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Write Inhibit	×	×	V_{IH}	High Z	–
Write Inhibit	×	V_{IL}	×	High Z	–
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data Out (I/O7)

Note: X: V_{IL} or V_{IH}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	–0.6 to +7.0	V
Input Voltage*1	V_{in}	–0.5*2 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Notes: *1. With respect to V_{SS}.
*2. –3.0V for pulse width ≦ 50ns.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	–0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V V_{out} = 5.5/0.4V	–	–	2	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
V_{CC} Current (Active)	I_{CC2}	Iout=0mA, duty=100%, cycle 1μs	–	–	8	mA
		Iout=0mA, duty=100%, Min. Cycle	–	–	25	mA
Input Low Voltage	V_{IL}		–0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400μA	2.4	–	–	V

Note: *1. –1.0V for pulse width ≦ 50ns

■ CAPACITANCE (T_a=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	12	pF

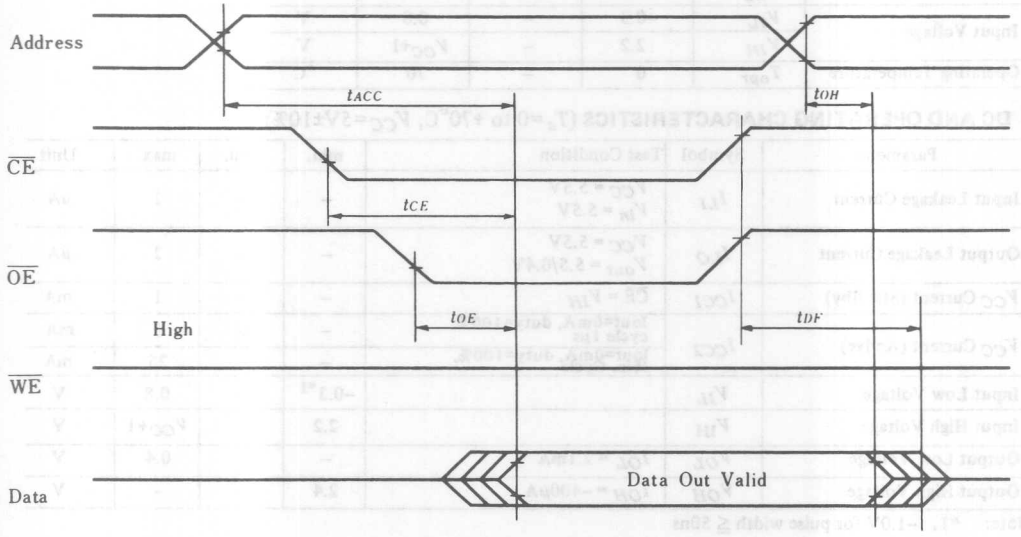
■ AC CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

• AC Test Conditions

Input Pulse Levels: 0.40V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Output Load: 1TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2V
Outputs; 0.8V and 2V

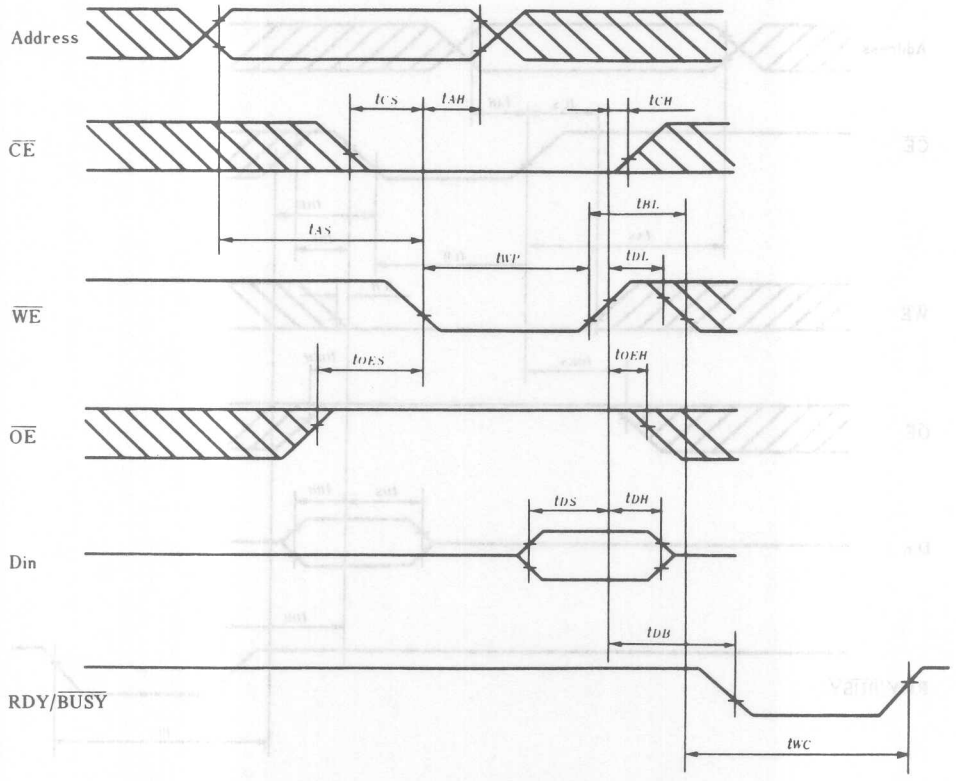
• Read Operation

Parameter	Symbol	Test Condition	HN58C65-25		Unit
			min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	10	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	90	ns



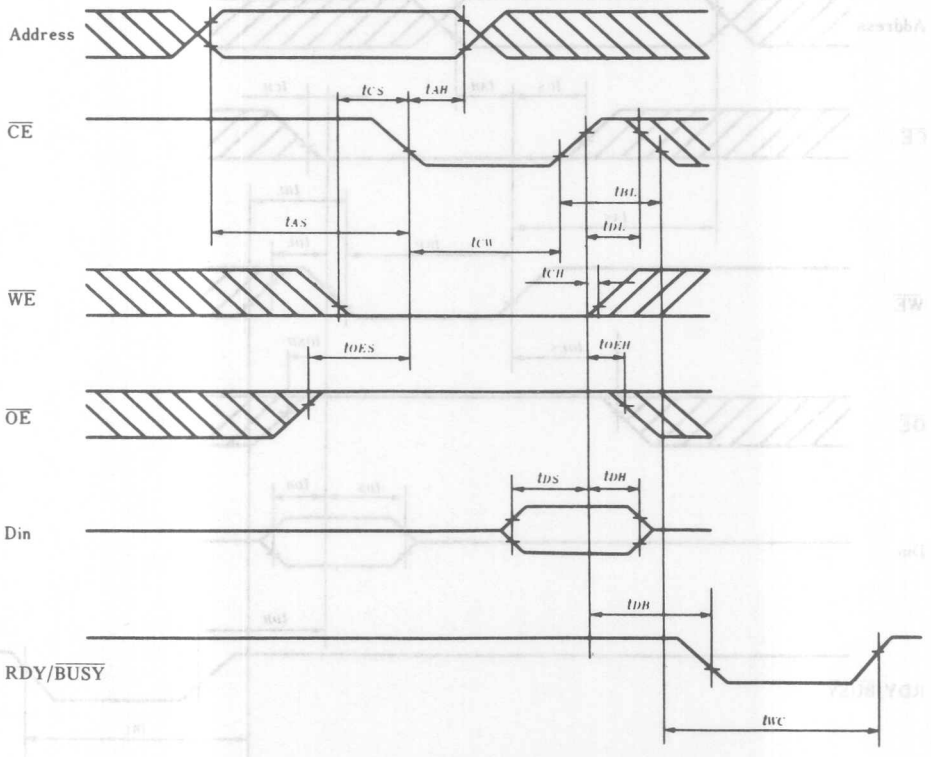
• Byte Erase and Byte Write Operation ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs



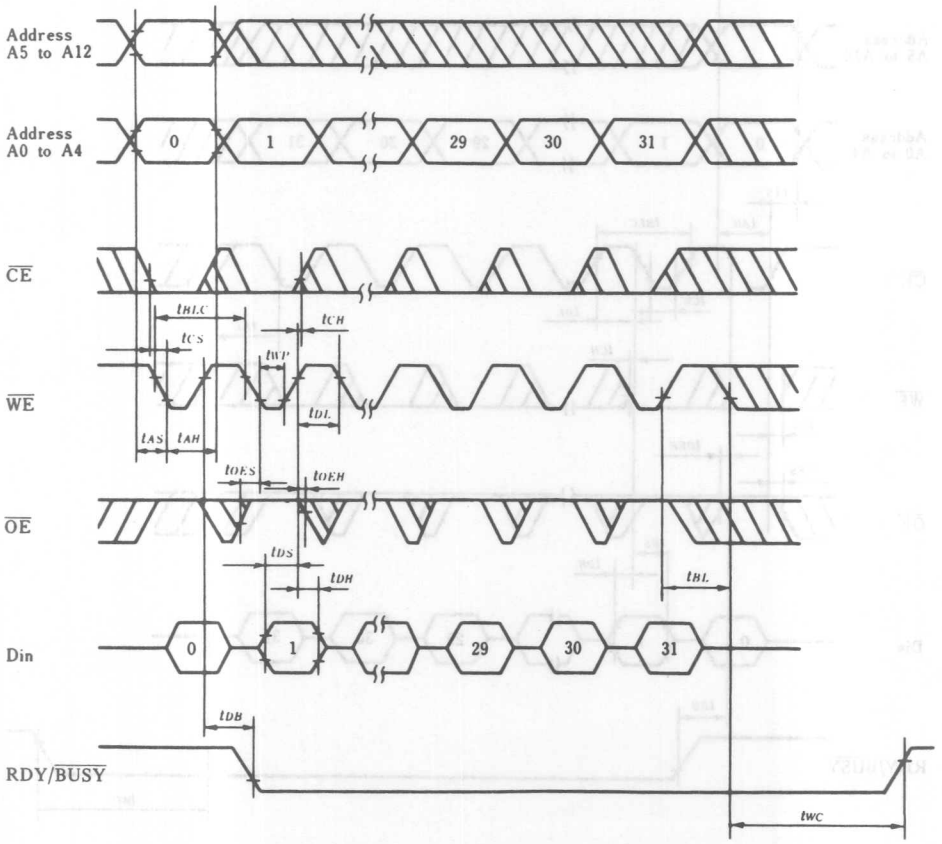
• Byte Erase and Byte Write Operation ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs



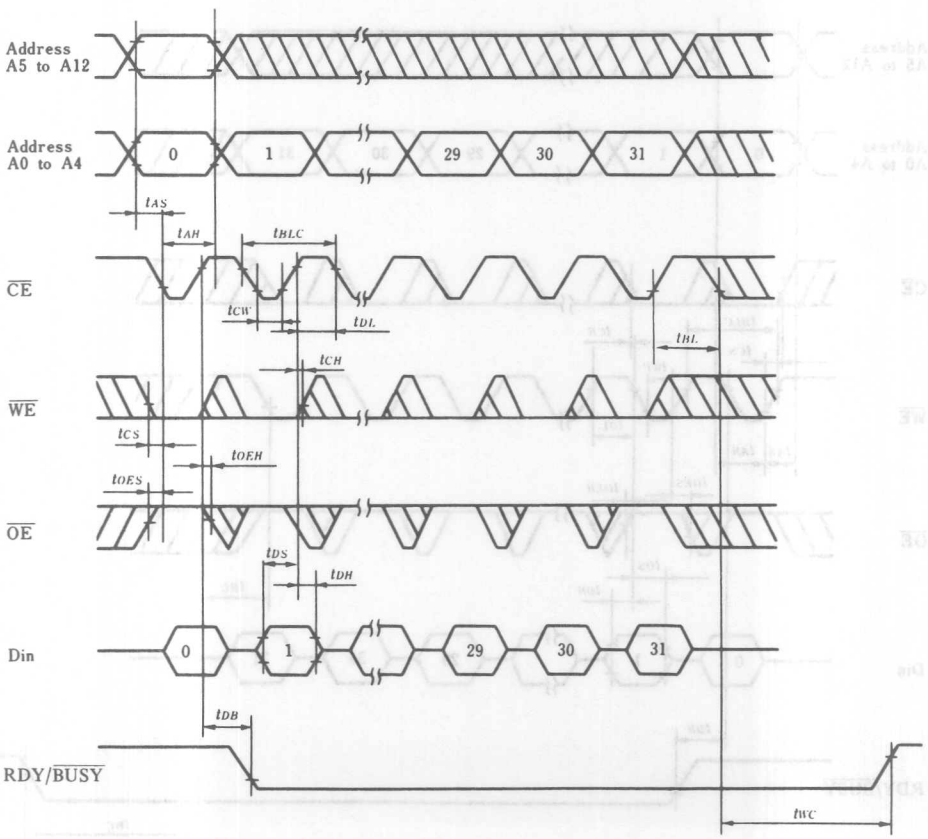
• Page Erase and Page Write Operation ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs
Byte Load Cycle	t_{BLC}	0.3	–	30	μs



• Page Erase and Page Write Operation ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs
Byte Load Cycle	t_{BLC}	0.3	–	30	μs



- **Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30μs of the preceding rising edge of the $\overline{WE}$.

- **$\overline{DATA}$ Polling**

$\overline{Data}$ polling allows comparison operation to determine the status of the EEPROM. During a write cycle, an attempted read of the last byte written in the EEPROM results in the complement data of that byte at I/O7.

- **RDY/$\overline{Busy}$ Signal**

RDY/$\overline{Busy}$ signal can be also used to determine the status of the EEPROM. The RDY/$\overline{Busy}$ signal has high impedance, except in a write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

- **$\overline{WE}$, $\overline{CE}$ Pin Operation**

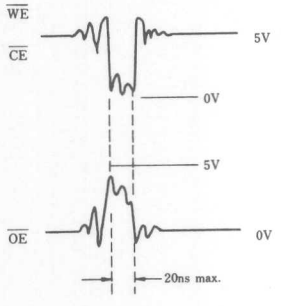
During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$ and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

- **Data Protection**

To protect the data during operation and power on/off, the HN58C65 has the internal functions described below.

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.
To prevent this phenomenon, the HN58C65 has a noise cancellation function that cuts the noise if its width is 20ns or less in program mode. Be careful not to allow noise of a width of more than 20ns on the control pins.



2. Data Protection at V_{CC} On/Off

2-1 Prevention of unintentional programming at V_{CC} on/off.

When V_{CC} is turned on or off, the noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

In addition, when V_{CC} is turned on or off, the input level of on control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	X	X
$\overline{OE}$	X	V_{SS}	X
$\overline{WE}$	X	X	V_{CC}

X: Don't care.

HN58C66 Series

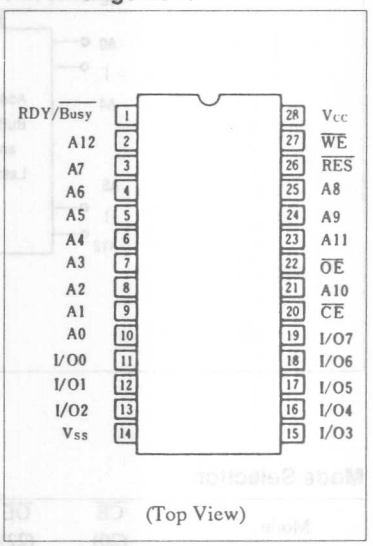
8192-Word × 8-Bit CMOS Electrically Erasable and Programmable ROM

The Hitachi HN58C66 is a 64k CMOS EEPROM (electrically erasable and programmable ROM), featuring data protection by program reset. It realizes low power consumption (60 mW typ) and a high level of reliability (10^5 erase/write cycles and 10 year data retention), employing MNOS memory technology and CMOS process and circuitry technology. No external circuit for data protection is required since a program reset function is added, so its system design is easy. It is suitable for IC cards and memory cards.

Features

- Single 5 V supply
- On chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (32 bytes): 10 ms max
- High speed: Access time 250 ns max
- Low power dissipation
  - Active mode: 20 mW/MHz typ
  - Standby mode: 2 mW typ
- $\overline{Data}$ polling and RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode) and 10 year data retention
- Program reset by $\overline{RES}$

Pin Arrangement



(Top View)

Ordering Information

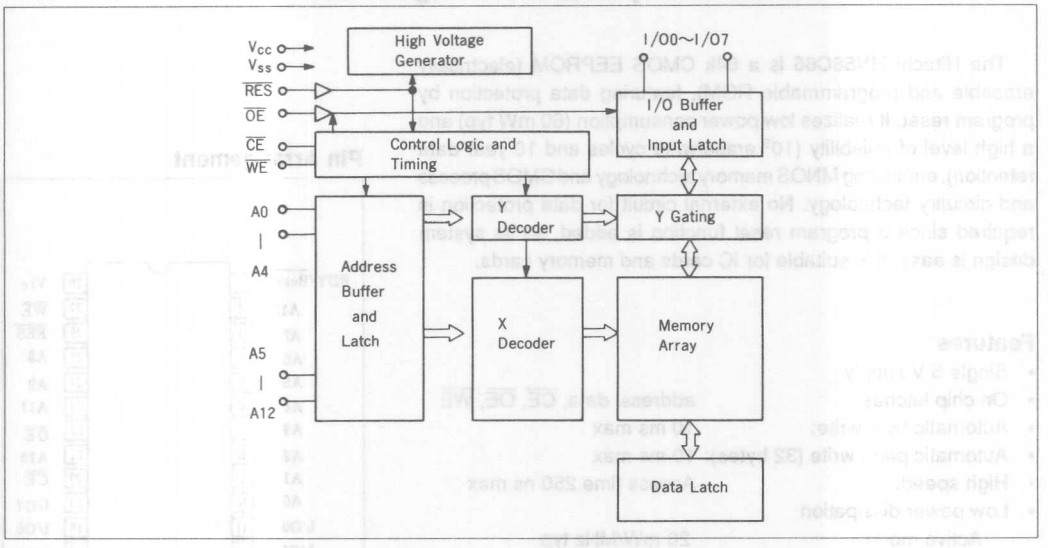
Type No.	Access Time	Package
HN58C66P-25	250 ns	600-mil 28-pin plastic DIP (DP-28)
HN58C66FP-25	250 ns	28-pin plastic SOP*1 (FP-28D/DA)

Note: T is added to the end of the type no. for an SOP of 3.00 mm (max) thickness.

Pin Description

Pin Name	Function
A0–A12	Address
I/O0–I/O7	Input/Output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
Vcc	Power supply (+5 V)
Vss	Ground
RDY/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Program reset

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{Busy}$ (1)	$\overline{RES}$ (26)	I/O (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	V_H*1	Dout
Standby	V_{IH}	×	×	High-Z	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z→V_{OL}	V_H	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write inhibit	×	×	V_{IH}	High-Z	×	—
	×	V_{IL}	×	High-Z	×	—
Data polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	V_H	Data out (I/O7)
Program reset	×	×	×	High-Z	V_{IL}	High-Z

Notes: *1. Refer to the recommended DC operating condition.
*2. × = Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage*1	Vcc	–0.6 to +7.0	V
Input voltage*1	Vin	–0.5*2 to +7.0	V
Operating temperature range*3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: *1. Relative to Vss
*2. Vin min = –3.0 V for pulse width ≤ 50 ns
*3. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 1	V
	V_H	V_{CC}–0.5	—	V_{CC} + 1	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10 %)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2 *1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC2}	—	—	8	mA	Iout = 0 mA, duty = 100% cycle = 1µs
		—	—	25	mA	Iout = 0 mA, duty = 100% maximum cycle
Input low voltage	V_{IL}	–0.3 *2	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 1	V	
	V_H	V_{CC} – 0.5	—	V_{CC} + 1	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes : *1. I_{LI} on $\overline{RES}$ = 100 µA max.
*2. V_{IL} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

AC Characteristics (Ta = 0 to + 70°C, V_{CC} = 5 V ± 10%)

Test Conditions

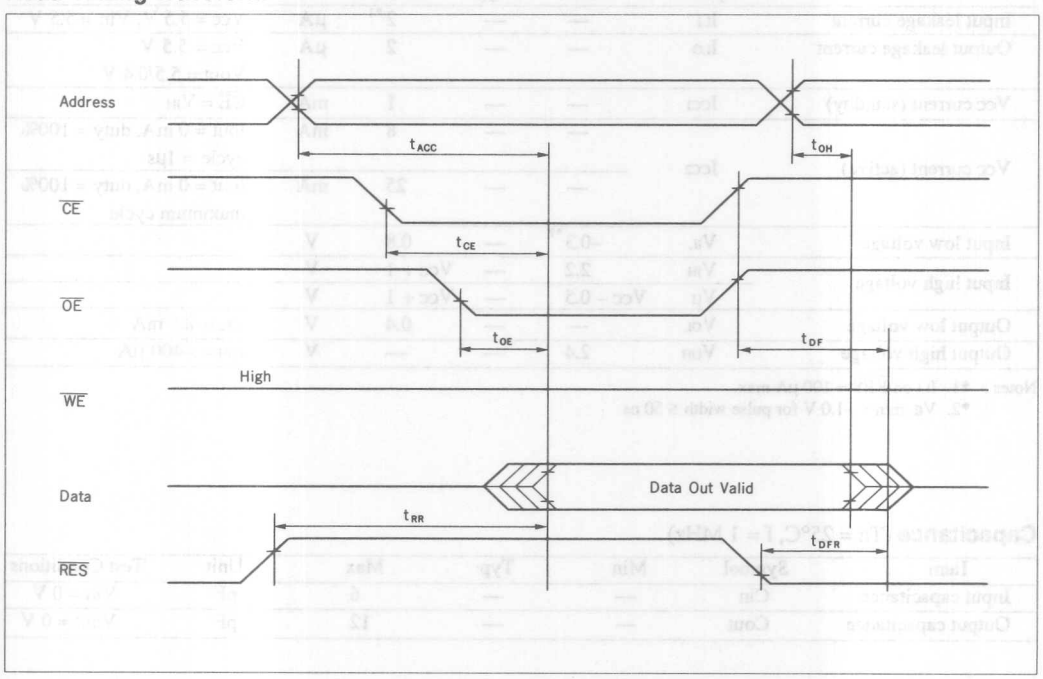
Input pulse levels: 0.4 V to 2.4 V
Input rise and fall time: ≤ 20 ns

Output load: 1TTL Gate + 100 pF
Reference levels for measuring timing:
Inputs; 0.8 V and 2.0 V
Outputs; 0.8 V and 2.0 V

Read Cycle

Item	Symbol	Min	Max	Unit	Test Conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t_{OE}	10	100	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{OE}$ high to output float	t_{DF}	0	90	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
	t_{DFR}	—	350	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{RES}$ to output delay	t_{RR}	—	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

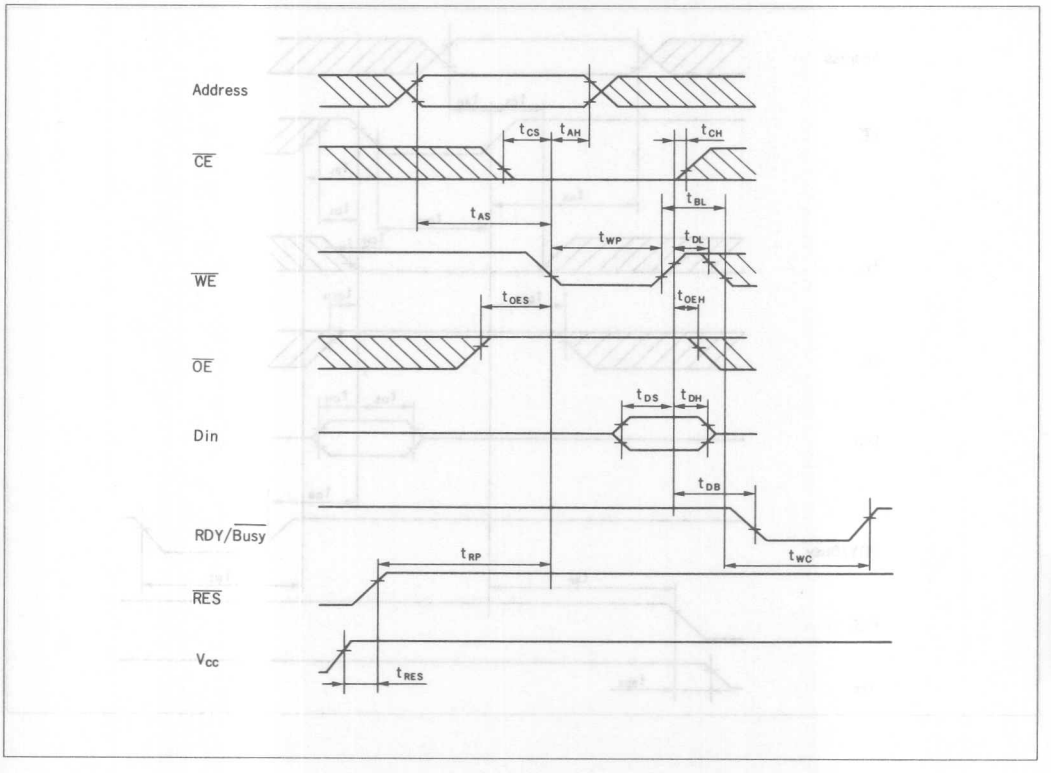
Read Timing Waveform



Byte Erase and Byte Write Cycle ($\overline{WE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{WP}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Data latch time	t_{DL}	100	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

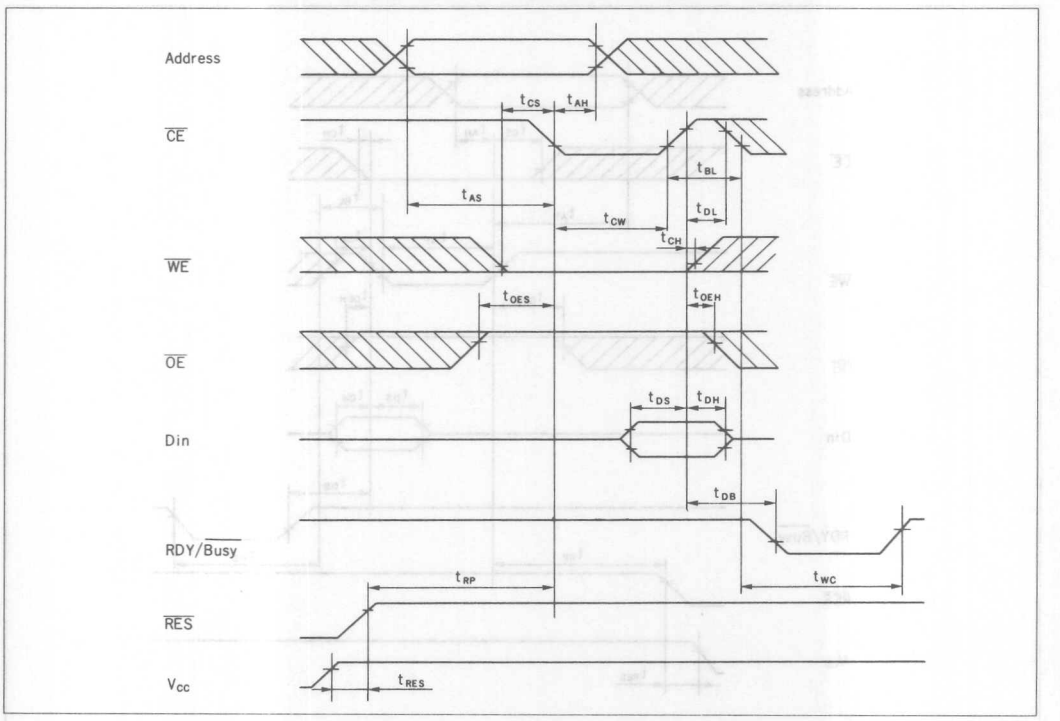
Byte Erase and Byte Write Timing Waveform (1) ($\overline{WE}$ controlled)



Byte Erase and Byte Write Cycle ($\overline{CE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{CW}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Data latch time	t_{DL}	100	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

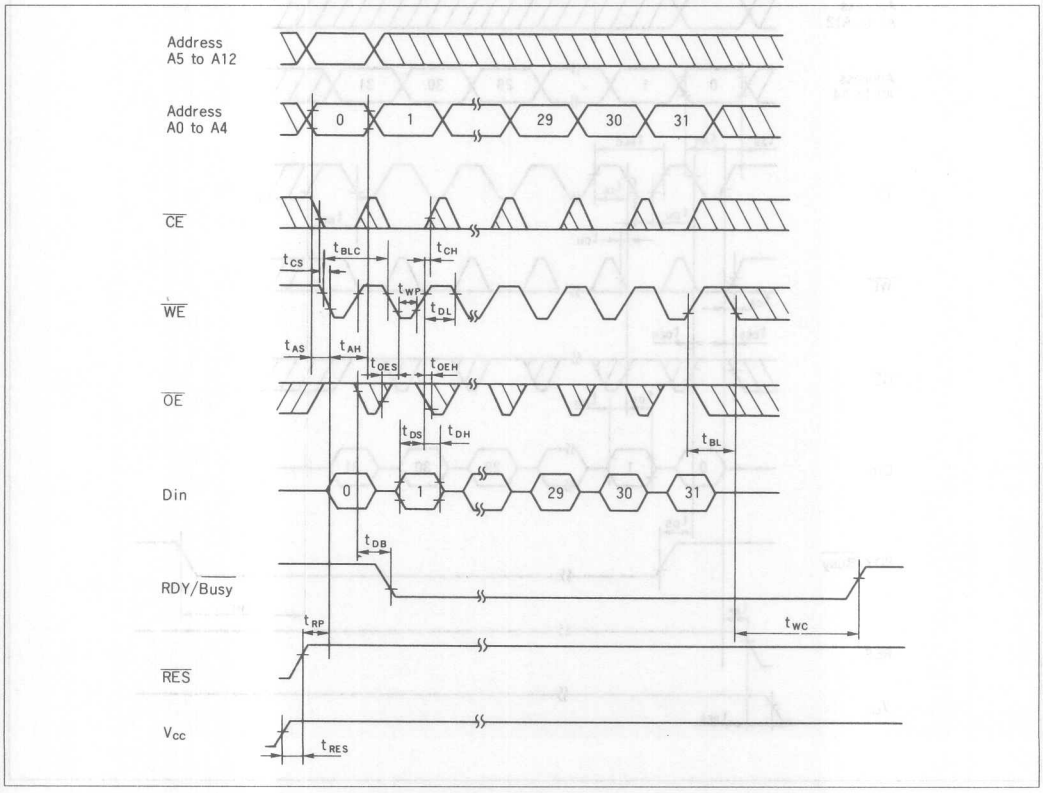
Byte Erase and Byte Write Timing Waveform (2) ($\overline{CE}$ controlled)



Page Erase and Page Write Cycle ($\overline{WE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{CW}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Data latch time	t_{DL}	100	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Byte load cycle	t_{BLC}	0.3	—	30	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

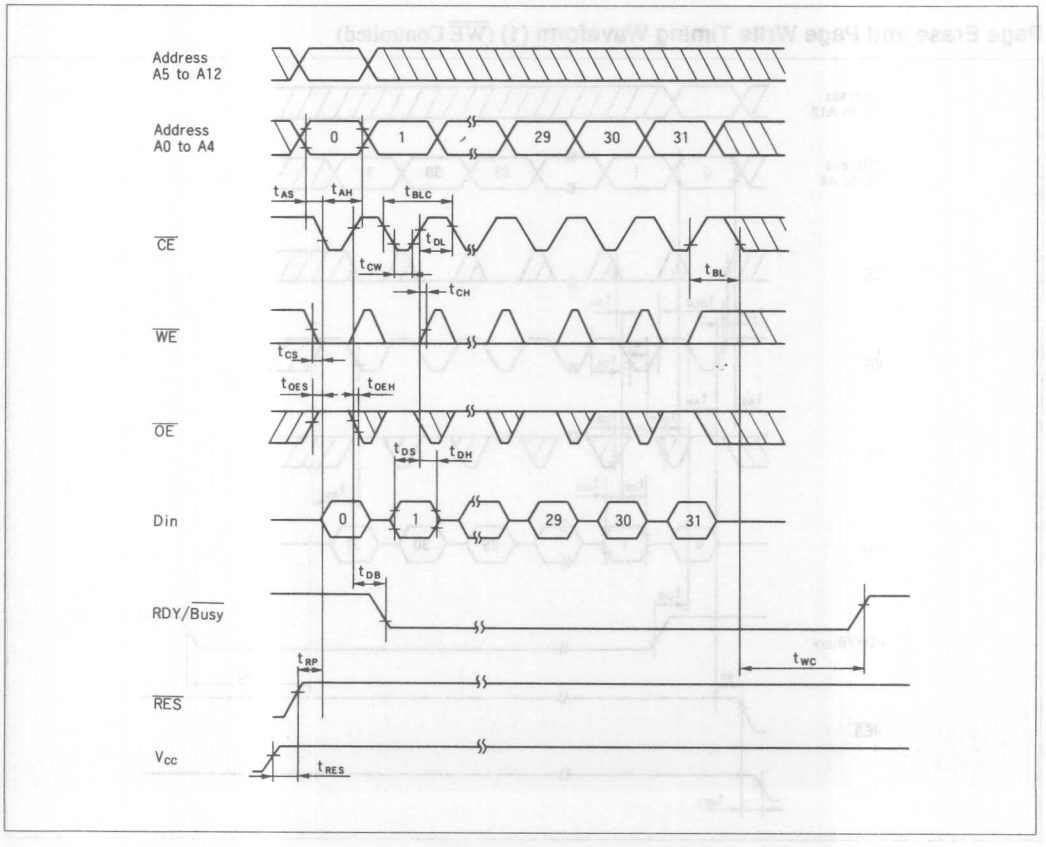
Page Erase and Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Erase and Page Write Cycle ($\overline{CE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{CW}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Data latch time	t_{DL}	100	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Byte load cycle	t_{BLC}	0.3	—	30	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

Page Erase and Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Functional Description

*** Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times per page. Therefore, page write allows the data to be written 10^5 times in 32-byte units, 2 x 10^5 times in 16-byte units, or 4 x 10^5 times in 8-byte units.

*** $\overline{\text{Data}}$ Polling**

$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

*** RDY/$\overline{\text{Busy}}$ Signal**

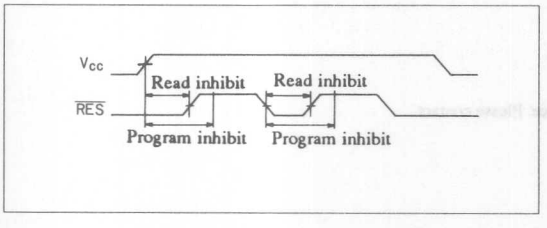
RDY/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

*** $\overline{WE}$, $\overline{CE}$ Pin Operation**

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

*** $\overline{RES}$ Signal**

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



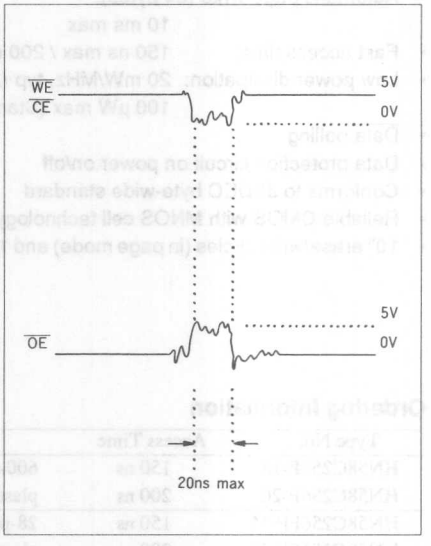
*** Data Protection**

Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.

To prevent this phenomenon, the HN58C66 has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



HN58C256 Series — Under Development

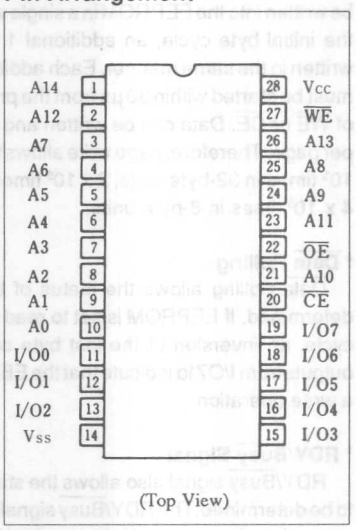
32768-Word × 8-Bit Electrically Erasable and Programmable CMOS ROM

The Hitachi HN58C256 is an electrically erasable and programmable ROM organized as 32768-word x 8-bit. It realizes high speed, low power consumption, and a high reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page reprogramming function to make its erase and write operations faster.

Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 150 ns max / 200 ns max
- Low power dissipation: 20 mW/MHz, typ (Active)
  100 µW max (Standby)
- $\overline{Data}$ polling
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode) and 10 year data retention

Pin Arrangement



(Top View)

Ordering Information

Type No.	Access Time	Package
HN58C256P-15	150 ns	600-mil 28-pin
HN58C256P-20	200 ns	plastic DIP (DP-28)
HN58C256FP-15	150 ns	28-pin
HN58C256FP-20	200 ns	plastic SOP*1 (FP-28D/DA)

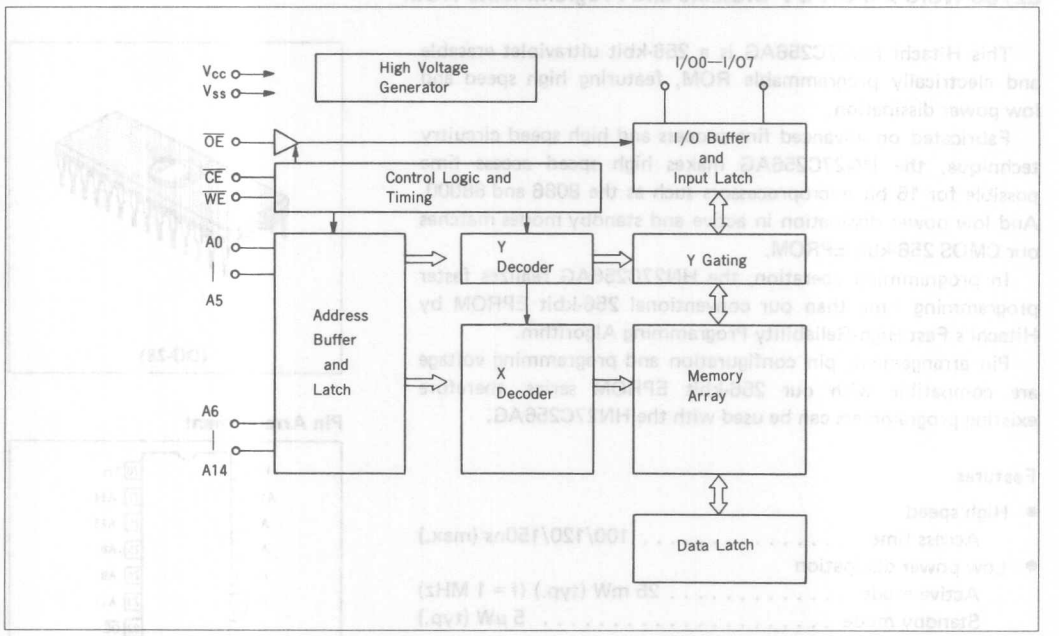
Notes: *1. T is added to the end of the type no. for an SOP of 3.00 mm (max) thickness.
Die shipment is also available. Because the die has a $\overline{RES}$ pad, it can perform a reset function (refer to HN58C66 data sheet).

Pin Description

Pin Name	Function
A0–A14	Address
I/O0–I/O7	Input/Output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



HN27C256AG Series — Preliminary

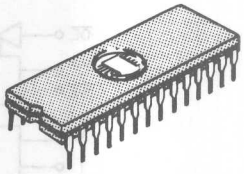
32768-Word x 8-Bit UV Erasable and Programmable ROM

This Hitachi HN27C256AG is a 256-kbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation.

Fabricated on advanced fine process and high speed circuitry technique, the HN27C256AG makes high speed access time possible for 16 bit microprocessors such as the 8086 and 68000. And low power dissipation in active and standby modes matches our CMOS 256-kbit EPROM.

In programming operation, the HN27C256AG realizes faster programming time than our conventional 256-kbit EPROM by Hitachi's Fast High-Reliability Programming Algorithm.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256AG.



(DG-28)

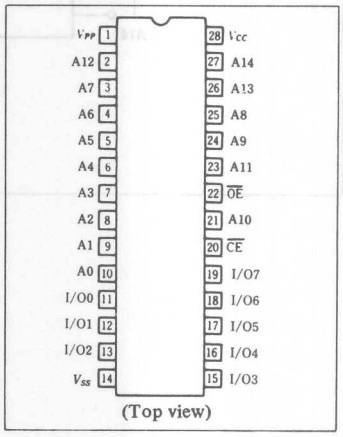
Features

- High speed
  - Access time . . . . . 100/120/150ns (max.)
- Low power dissipation
  - Active mode . . . . . 25 mW (typ.) (f = 1 MHz)
  - Standby mode . . . . . 5 μW (typ.)
- High reliability and fast programming
  - Programming voltage: +12.5V DC
  - Fast High-Reliability Programming Algorithm available
- Device identifier mode
  - Manufacturer code and device code

Ordering Information

Type No.	Access Time	Package
HN27C256AG-10	100 ns	600-mil 28-pin cerdip
HN27C256AG-12	120 ns	
HN27C256AG-15	150 ns	

Pin Arrangement



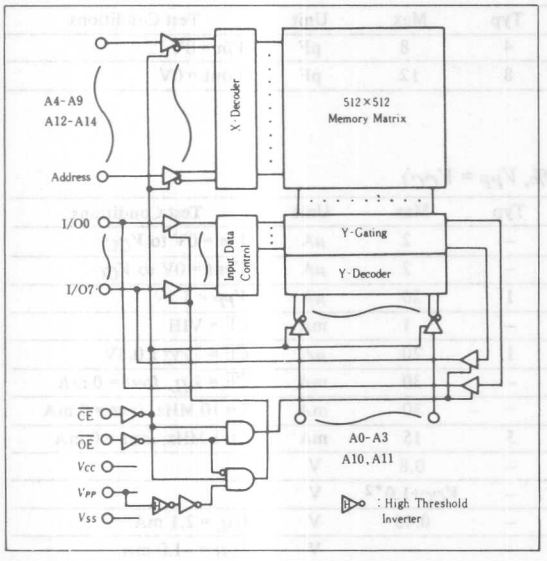
(Top view)

Pin Description

Pin Name	Function
A0 – A14	Address
I/O0–IO7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Note) The specifications of this device are subject to change without notice. Please contact Hitachi's Sales Dept. regarding specifications.

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	×	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	×	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din
Program verify	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Dout
Optional verify	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	Dout
Program inhibit	V_{IH}	V_{IH}	×	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes: 1. × = Don't care.
2. V_H = 12.0V ± 0.5V.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output Voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0V for pulse width ≦ 50ns.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	*Cin*	–	4	8	pF	*Vin* = 0V
Output capacitance	*Cout*	–	8	12	pF	Vout = 0V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ±10%, $V_{PP} = V_{CC}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	*Vin* = 0V to V_{CC}
Output leakage current	I_{LO}	–	–	2	μA	*Vout* = 0V to V_{CC}
V_{PP} current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
Standby V_{CC} current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = VIH
Operating	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ± 0.3V
	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, *Iout* = 0 mA
Operating V_{CC} current	I_{CC2}	–	–	30	mA	f = 10 MHz, *Iout* = 0 mA
	I_{CC3}	–	5	15	mA	f = 1 MHz, *Iout* = 0 mA
Input low voltage*3	V_{IL}	−0.3*1	–	0.8	V	
Input high voltage*3	V_{IH}	2.2	–	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	–	–	V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC}−0.7	–	–	V	I_{OH} = −100 μA

Notes: *1. V_{IL} min = −1.0V for pulse width ≦ 50ns.
*2. V_{IH} max = V_{CC} + 1.5V for pulse width ≦ 20ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
*3. Only defined for DC and long cycle function test. V_{IL} max = 0.45V, V_{IH} min = 2.4V for AC function test.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = −5V ±10%, $V_{PP} = V_{CC}$)

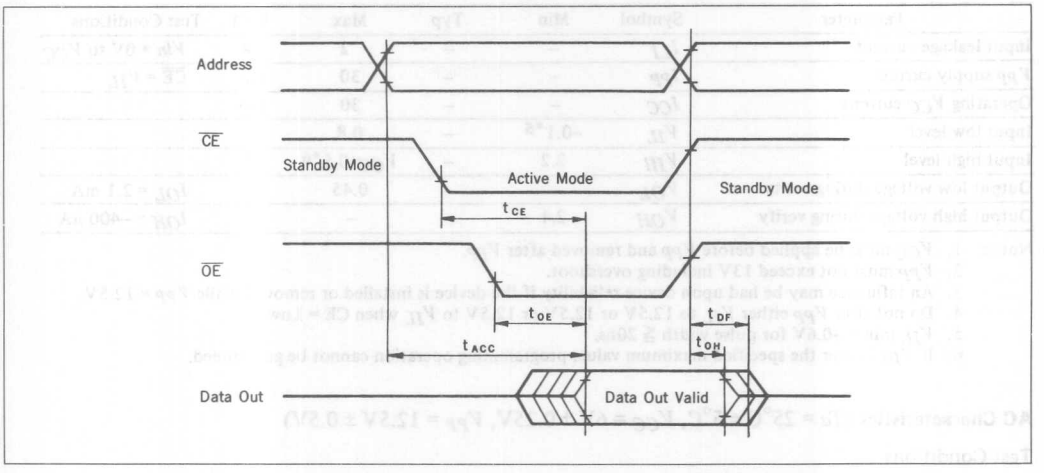
Test condition

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 10ns
- Output load: 1 TTL Gate + 100pF
- Reference lvels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	HN27C256AG-10		HN27C256AG-12		HN27C256AG-15		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	100	–	120	–	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	100	–	120	–	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	–	60	–	60	–	70	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	–	5	–	5	–	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

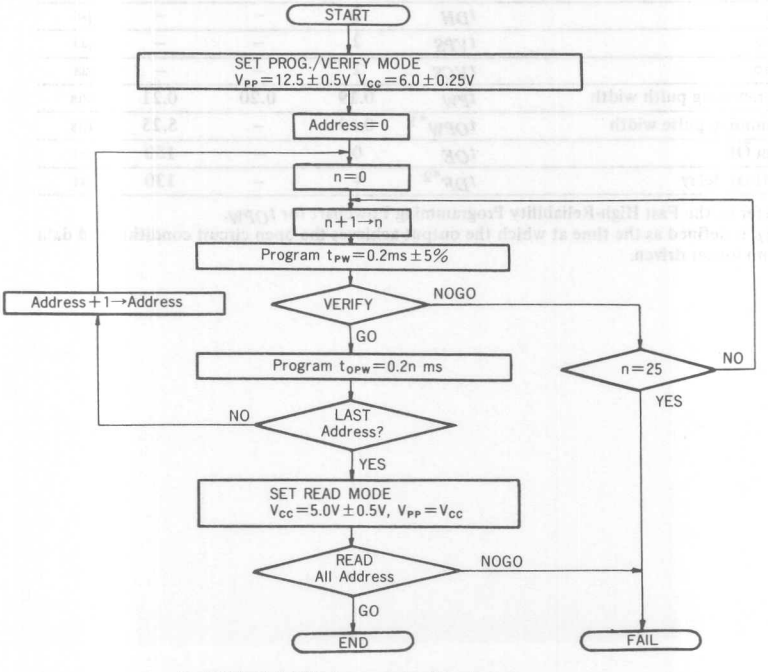
Read Timing Waveform



Programming Operation

Fast High-Reliability Programming

This device can be programmed by the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retention. The theoretical programming time (except blank checking and verifying time) is one-tenth of conventional high performance programming algorithms. Regarding the model and software version of the programmers available with this algorithm, please contact program manufacturer.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	−0.1*5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
Output low voltage during verity	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = −400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V or 12.5V to V_{IL} when CE = Low.
5. V_{IL} min = −0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

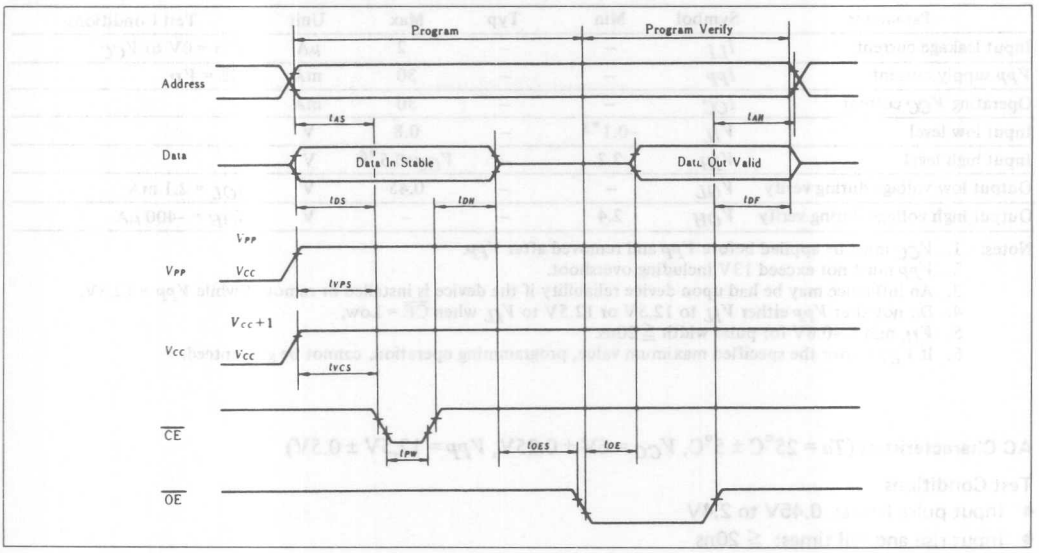
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	μs
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs
Data setup time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
V_{PP} setup time	t_{VPS}	2	–	–	μs
V_{CC} setup time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.19	0.20	0.21	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	0.19	–	5.25	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

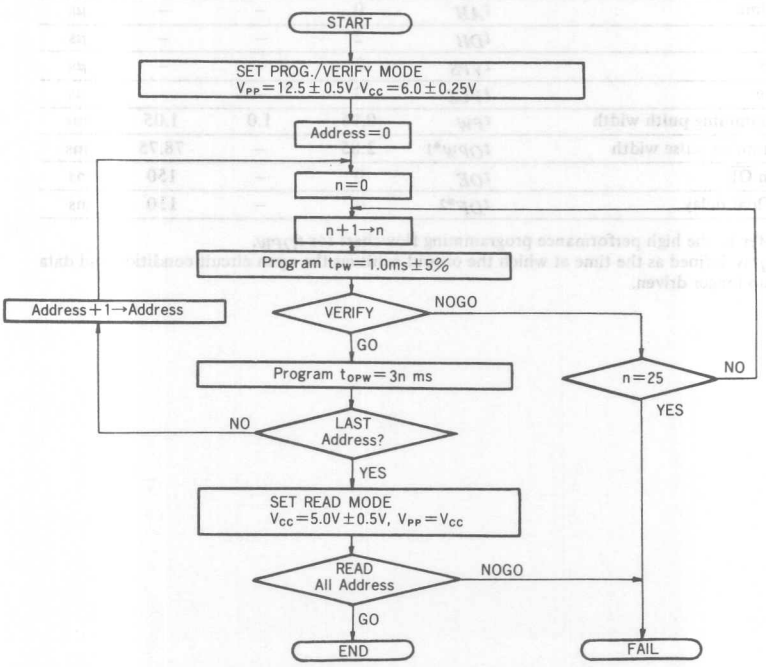
Notes: 1. Refer to the Fast High-Reliability Programming Fowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	–0.1*5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = –400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation. cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

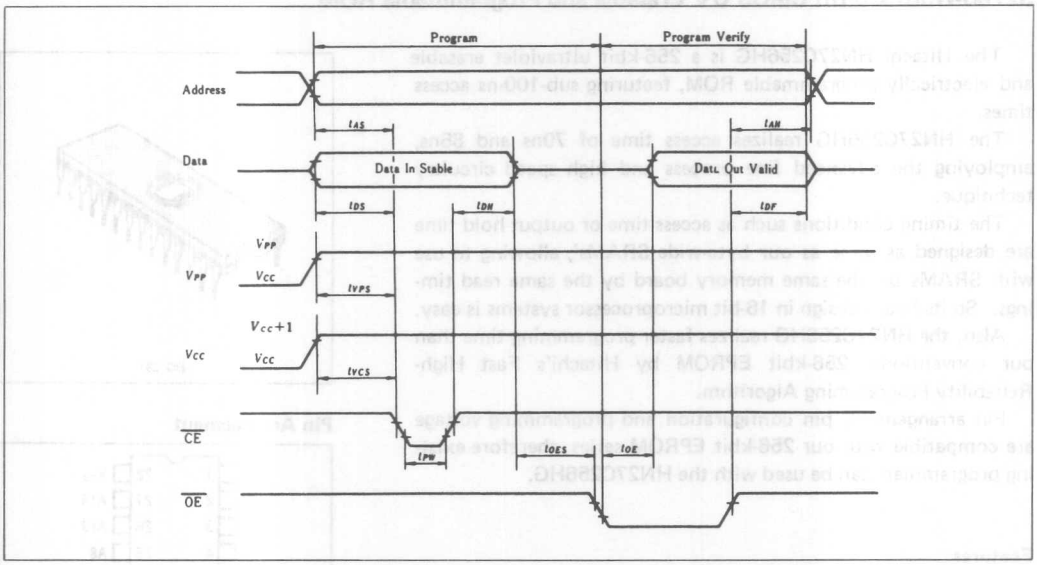
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	μs
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs
Data setup time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
V_{PP} setup time	t_{VPS}	2	–	–	μs
V_{CC} setup time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

Notes: 1. Refer to the high performance programming flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Erase

Erasure of HN27C256AG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W•sec/cm^2.

Mode Description

Device Identifier Mode

Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

HN27C256AG Series Identifier Code

Identifier	A0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0V ± 0.5V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

HN27C256HG Series

32768-Word x 8-Bit CMOS UV Erasable and Programmable ROM

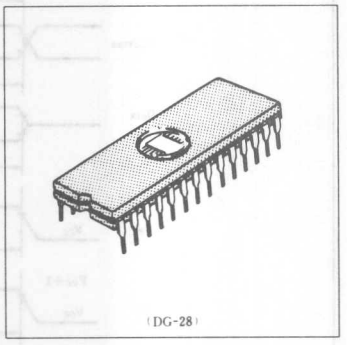
The Hitachi HN27C256HG is a 256-kbit ultraviolet erasable and electrically programmable ROM, featuring sub-100-ns access times.

The HN27C256HG realizes access time of 70ns and 85ns, employing the advanced fine process and high speed circuitry technique.

The timing conditions such as access time or output hold time are designed as same as our byte-wide SRAMs', allowing to use with SRAMs on the same memory board by the same read timings. So its board design in 16-bit microprocessor systems is easy.

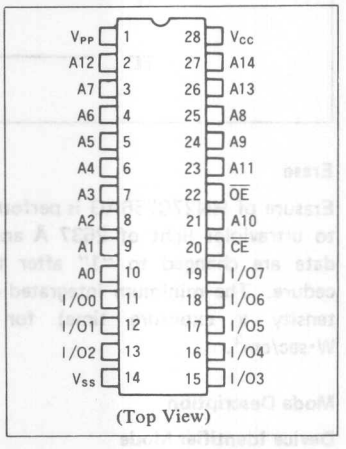
Also, the HN27C256HG realizes faster programming time than our conventional 256-kbit EPROM by Hitachi's Fast High-Reliability Programming Algorithm.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256HG.



(DG-28)

Pin Arrangement



(Top View)

Features

- High speed . . . . . Access time 70/85ns (max.)
- Low power dissipation
  - Active mode . . . . . 30 mW (typ.) (f = 1 MHz)
- High reliability and fast programming
  - Programming voltage: +12.5V DC
  - Fast High-Reliability Programming Algorithm available
- Device identifier mode
  - Manufacturer code and device code

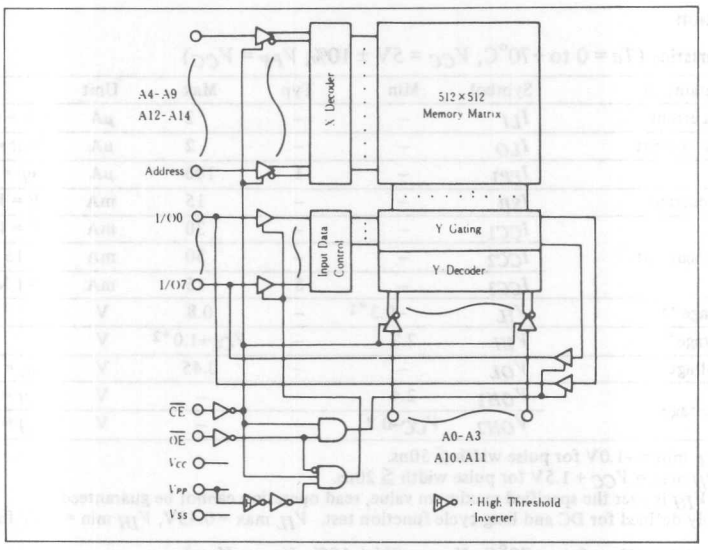
Ordering Information

Type No.	Access Time	Package
HN27C256HG-70	70 ns	600-mil 28-pin cerdip
HN27C256HG-85	85 ns	

Pin Description

Pin Name	Function
A0 – A14	Address
I/O0–IO7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	x	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	x	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	x	V_{PP}	V_{CC}	Din
Program verify	V_{IH}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Optional verify	V_{IL}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Program inhibit	V_{IH}	V_{IH}	x	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes: 1. x = Don't care
2. V_H = 12.0V ± 0.5V.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0V for pulse width ≦ 50ns.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	4	8	pF	Vin = 0V
Output capacitance	Cout	–	8	12	pF	Vout = 0V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
Output leakage current	I_{LO}	–	–	2	μA	$Vout$ = 0V to V_{CC}
V_{PP} current	I_{PP1}	–	1	100	μA	V_{PP} = 5.5V
Standby V_{CC} current	I_{SB}	–	–	15	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, $Iout$ = 0 mA
	I_{CC2}	–	–	50	mA	f = 15 MHz, $Iout$ = 0mA
	I_{CC3}	–	5	15	mA	f = 1 MHz, $Iout$ = 0 mA
Input low voltage*3	V_{IL}	–0.3*1	–	0.8	V	
Input high voltage*3	V_{IH}	2.2	–	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	–	–	V	I_{OH} = –1.0 mA
	V_{OH2}	V_{CC}–0.7	–	–	V	I_{OH} = –100 μA

Notes: 1. V_{IL} min = –1.0V for pulse width ≦ 50ns.
2. V_{IH} max = V_{CC} + 1.5V for pulse width ≦ 20ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.45V, V_{IH} min = 2.4V for AC function test.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{PP} = V_{CC})

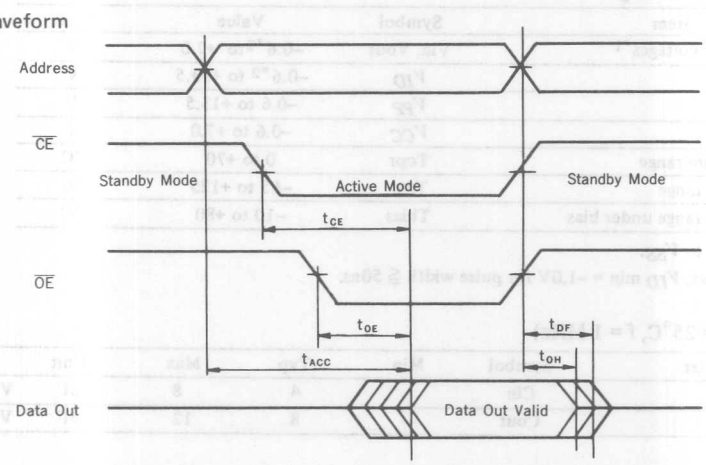
Test conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 10ns
- Output load: 1 TTL Gate + 100 pF
- Reference levels for measuring timing: Input; 1.5V
  Outputs; 1.5V

Parameter	Symbol	HN27C256 HG-70		HN27C256 HG-85		Unit	Test Conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	70	–	85	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	70	–	85	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	–	40	–	45	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	30	0	30	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	–	5	–	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

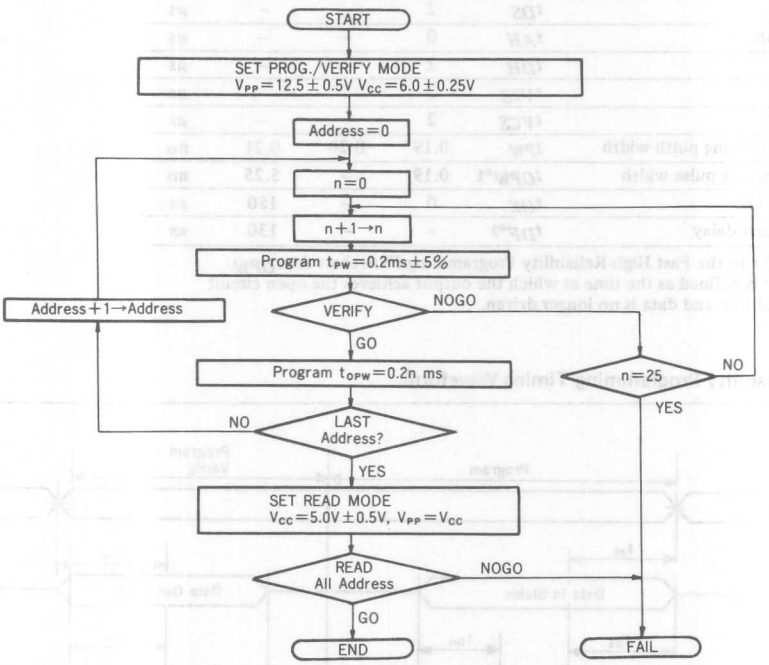
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Programming Operation

This device can be programmed by the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retention. The theoretical programming time (except blank checking and verifying time) is one-tenth of conventional high performance programming algorithms. Regarding the model and software version of the programmers available with this algorithm, please contact program manufacturer.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	−0.1 *5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = −400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = −0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Test Conditions

Input pulse levels: 0.45V to 2.4V

Input rise and fall times: ≦ 20ns

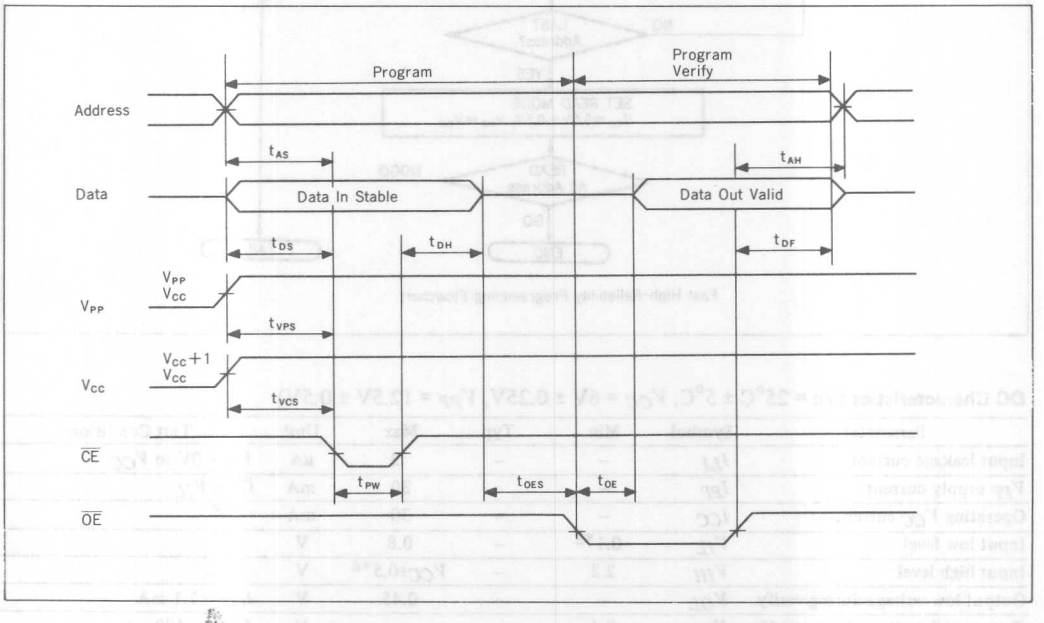
Reference levels for measuring timing: Inputs; 0.8V and 2.0V

Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	µs
$\overline{OE}$ setup time	t_{OES}	2	–	–	µs
Data setup time	t_{DS}	2	–	–	µs
Address hold time	t_{AH}	0	–	–	µs
Data hold time	t_{DH}	2	–	–	µs
V_{PP} setup time	t_{VPS}	2	–	–	µs
V_{CC} setup time	t_{VCS}	2	–	–	µs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.19	0.20	0.21	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	0.19	–	5.25	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

Notes: 1. Refer to the Fast High-Reliability Programming Flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

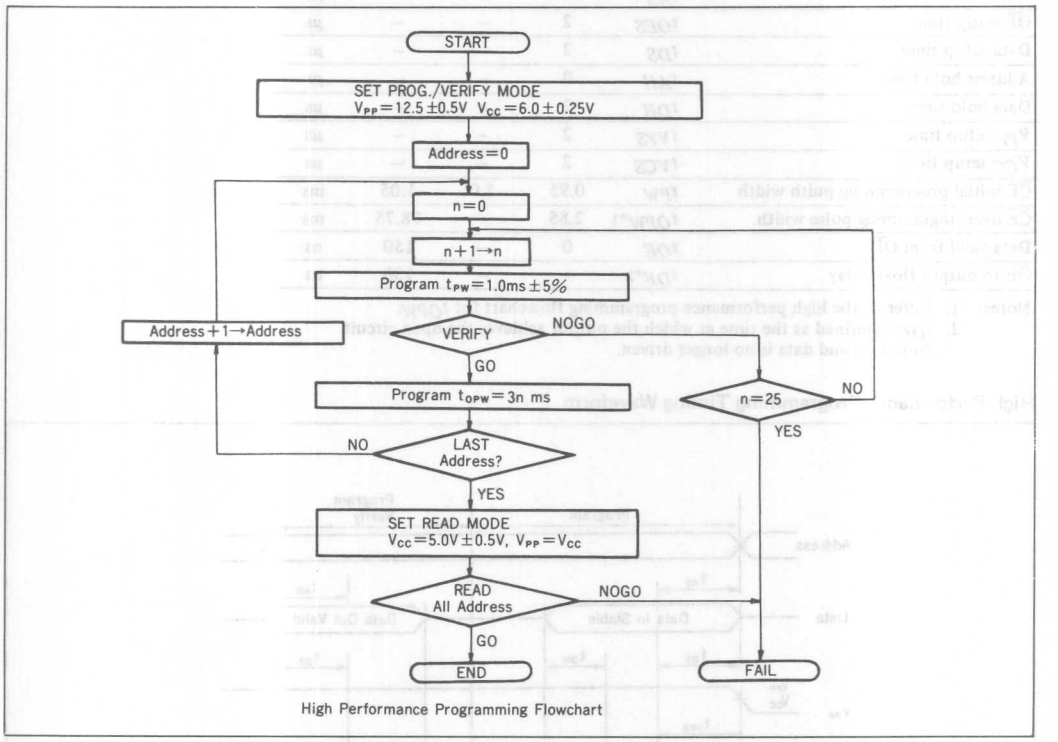
Fast High-Reliability Programming Timing Waveform



HITACHI
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High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series, so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	–0.1 *5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = –400 μA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

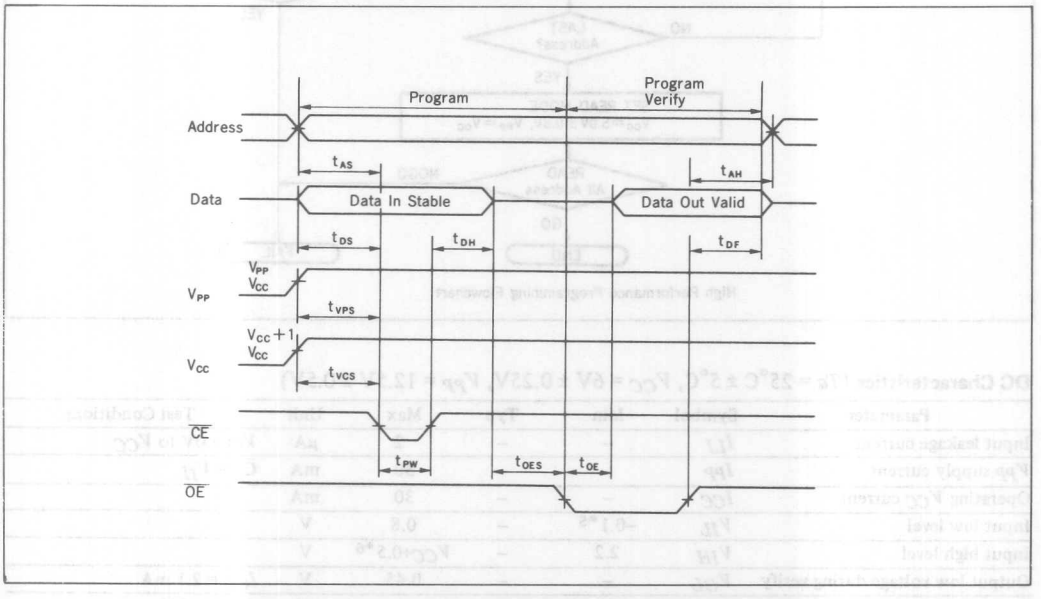
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 1.5V
  Outputs; 1.5V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	µs
$\overline{OE}$ setup time	t_{OES}	2	–	–	µs
Data setup time	t_{DS}	2	–	–	µs
Address hold time	t_{AH}	0	–	–	µs
Data hold time	t_{DH}	2	–	–	µs
V_{PP} setup time	t_{VPS}	2	–	–	µs
V_{CC} setup time	t_{VCS}	2	–	–	µs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

Notes: 1. Refer to the high performance programming flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Erase

Erasure of HN27C256HG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W•sec/cm^2.

Mode Description

Device Identifier Mode

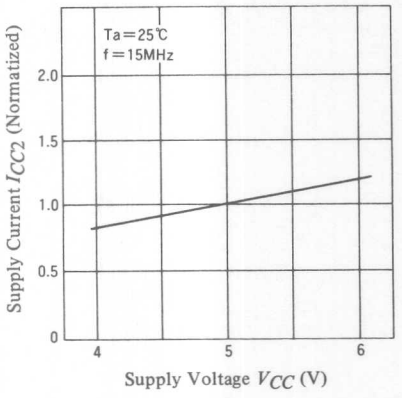
Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. The countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

HN27C256HG Series Identifier Code

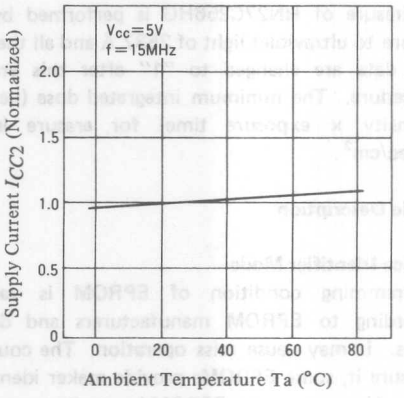
Identifier	A0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0V ± 0.5V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

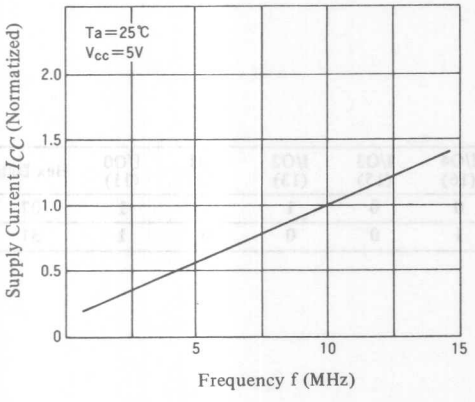
SUPPLY CURRENT vs. SUPPLY VOLTAGE



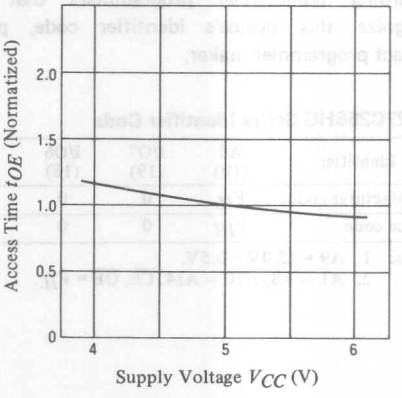
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



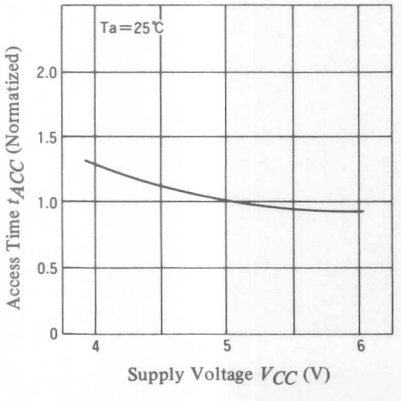
SUPPLY CURRENT-FREQUENCY



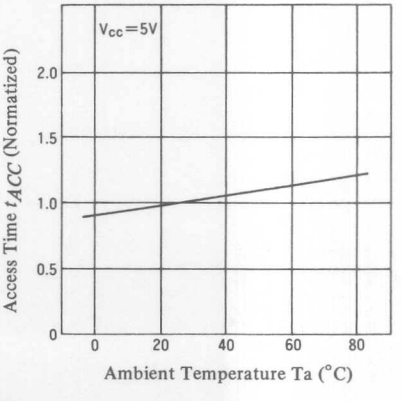
ACCESS TIME – SUPPLY VOLTAGE



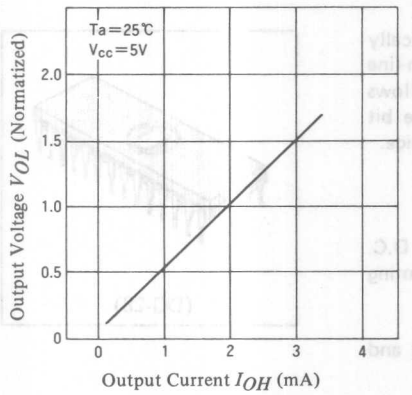
ACCESS TIME – SUPPLY VOLTAGE



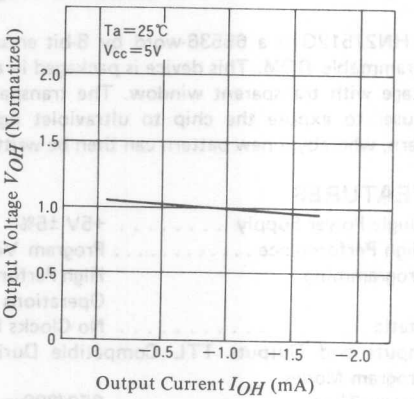
ACCESS TIME – AMBIENT TEMPERATURE



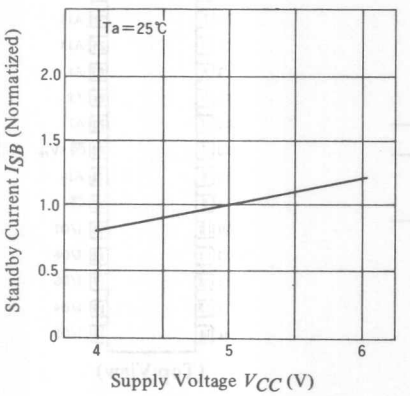
OUTPUT VOLTAGE vs. OUTPUT CURRENT



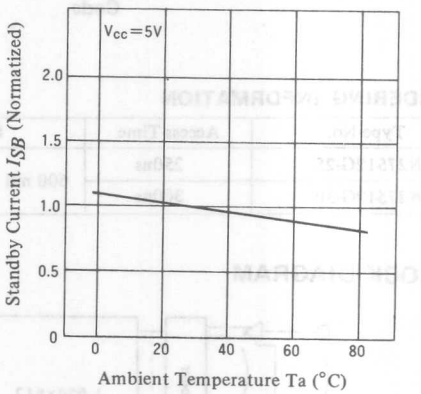
OUTPUT VOLTAGE vs. OUTPUT CURRENT



STANDBY CURRENT vs. SUPPLY VOLTAGE



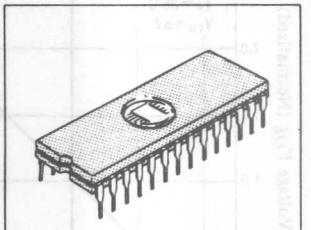
STANDBY CURRENT vs. AMBIENT TEMPERATURE



HN27512G Series

65536-word x 8-bit UV Erasable and Programmable ROM

The HN27512G is a 65536-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin dual in-line package with transparent window. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

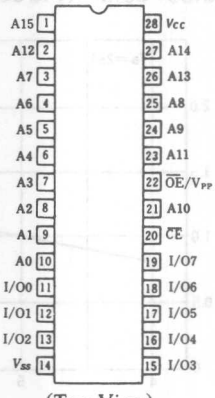


(DG-28)

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V (max.)
- Low Stand-by Current . . . . . 40mA (max.)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

■ PIN ARRANGEMENT

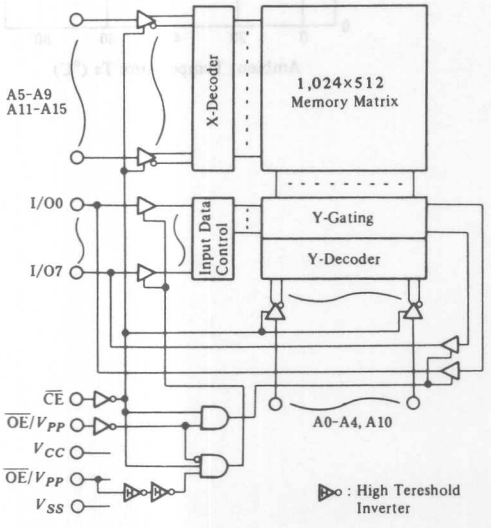


(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27512G-25	250ns	600 mil 28 pin Cerdip
HN27512G-30	300ns	

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	I/O (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H *2	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. with respect to V_{SS}.

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	−	−	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	−	−	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	45	100	mA
Input Low voltage	V_{IL}		−0.1*1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	−	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	−	−	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

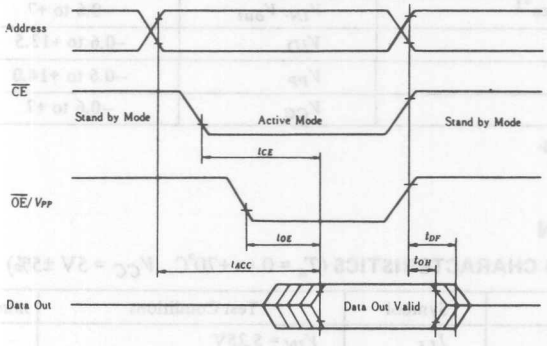
Parameter	Symbol	Test Condition	HN27512G-25		HN27512G-30		Unit
			min.	max.	min.	max.	
Addres to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1 TTL Gate +100pF
Reference Level for Measuring Timing:	0.8V and 2.0V

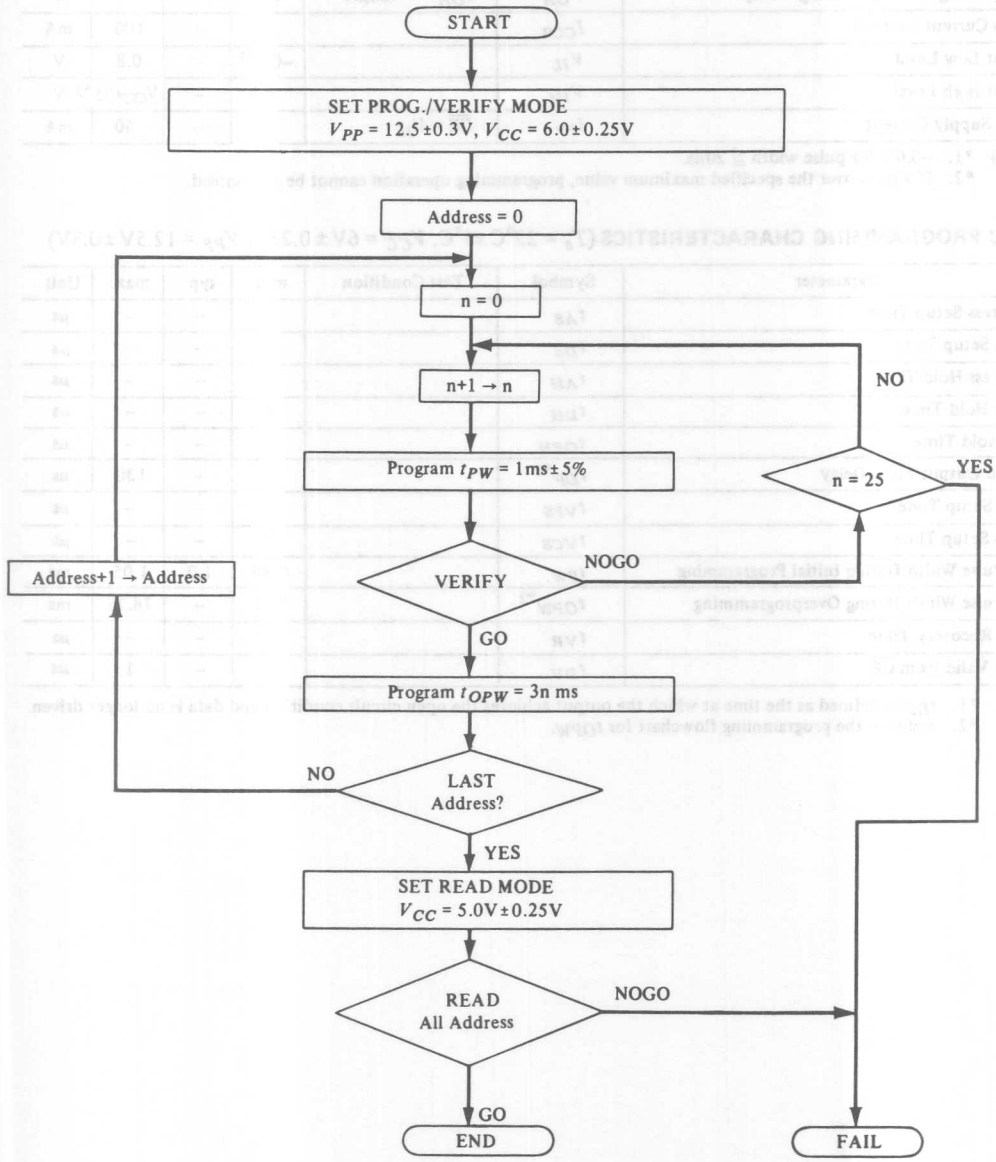


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	except $\overline{OE}/V_{PP}$	C_{in1}	V_{in} = 0V	–	4	6	pF
	$\overline{OE}/V_{PP}$ Pin	C_{in2}	V_{in} = 0V	–	12	20	pF
Output Capacitance		C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

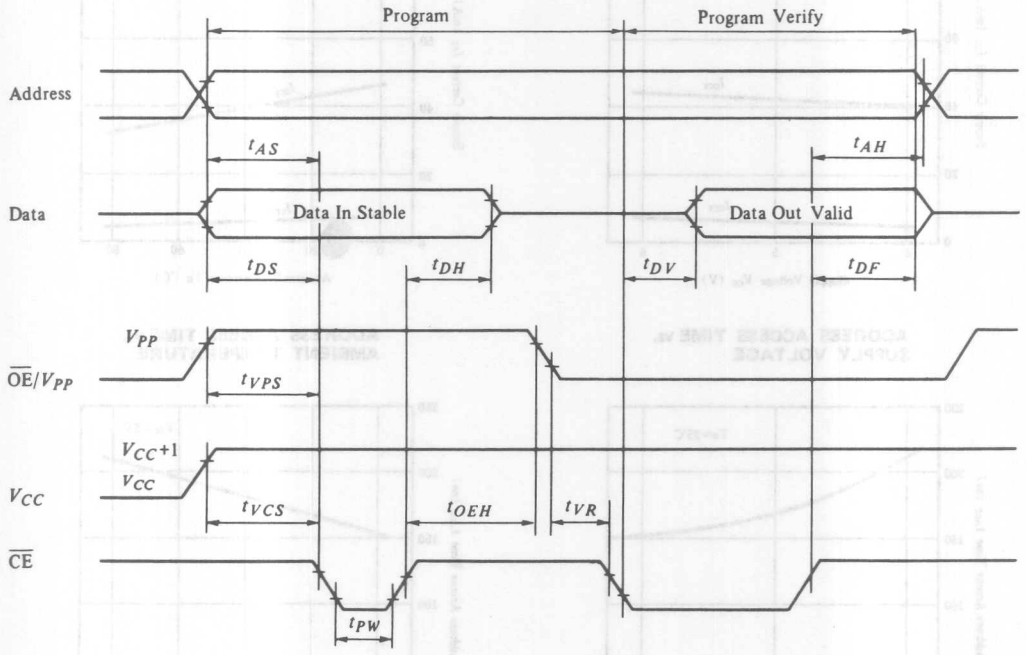
● AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
$\overline{CE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
V_{PP} Recovery Time	t_{VR}		2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}		–	–	1	μs

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ ERASE

Erasure of HN27512G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W • sec/cm^2.

■ DEVICE IDENTIFIER MODE

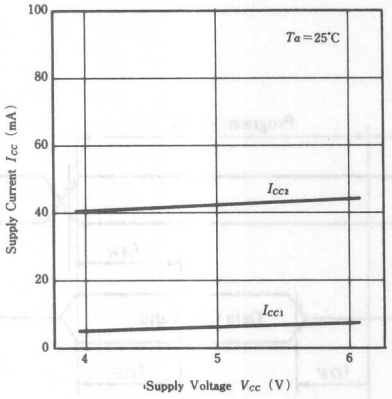
The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

• HN27512G SERIES IDENTIFIER CODE

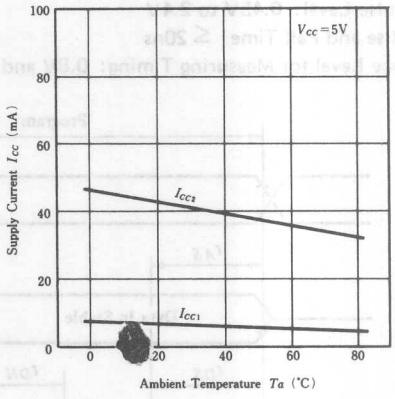
Pins / Identifier	A_0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	1	0	1	0	0	94

Notes: 1. $A_9 = 12.0 \pm 0.5V$.
2. $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$.

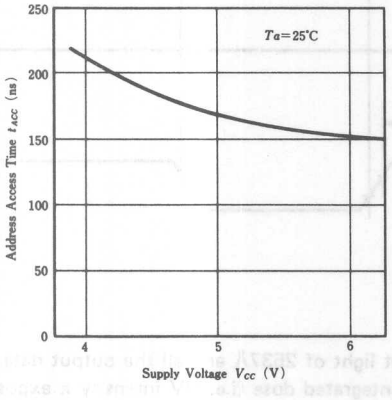
SUPPLY CURRENT vs. SUPPLY VOLTAGE



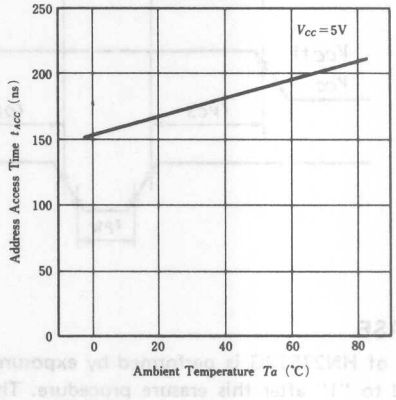
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



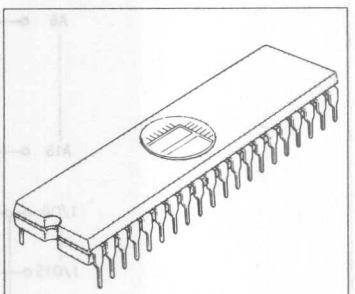
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HN27C1024HG Series

65536-Word × 16-Bit CMOS UV Erasable and Programmable ROM

The Hitachi NH27C1024HG is a 1-Mbit (64-kword × 16-bit) ultraviolet erasable and electrically programmable ROM. Fabricated on new advanced fine process technique, the HN27C1024HG makes high speed access time 85/100 ns (max) possible. (HN27C1024HG is a fastest 1-Mbit EPROM.) Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 8086 and 68000. The HN27C1024HG offers high speed programming using page programming mode.



(DG-40A)

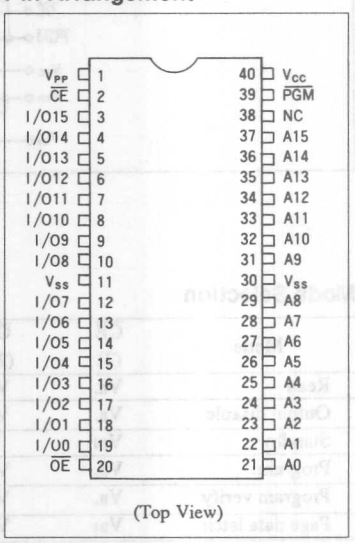
Features

- Fast high-reliability programming mode and Fast high-reliability page programming mode
  - Programming voltage: +12.5 V DC
  - Fast High-reliability page programming 14 sec (typ)
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation
  - 60 mW/MHz (typ)
- Device identifier mode
  - Manufacturer code and device code
- JEDEC standard

Ordering Information

Type No.	Access Time	Package
HN27C1024HG-85	85 ns	600-mil
HN27C1024HG-10	100 ns	40-pin cerdip (DG-40A)

Pin Arrangement

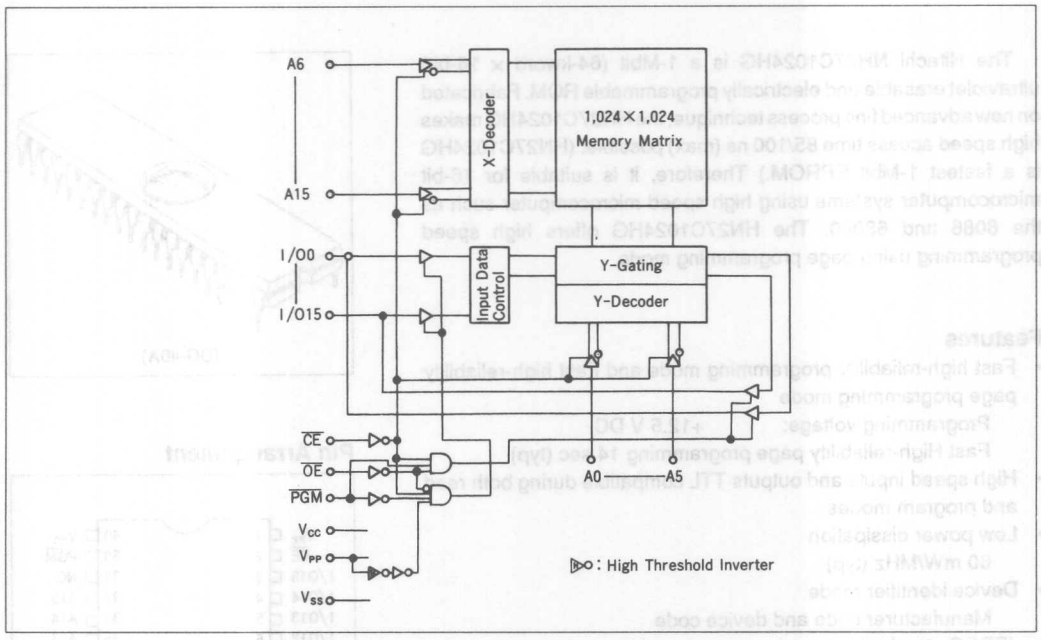


(Top View)

Pin Description

Pin Name	Function
A0–A15	Address
I/O0–I/O15	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	V_{PP} (1)	V_{CC} (40)	A9 (31)	I/O (3–10, 12–19)
Read	V_{IL}	V_{IL}	V_{IH}	Vcc	Vcc	×	Dout
Output disable	V_{IL}	V_{IH}	V_{IH}	Vcc	Vcc	×	High-Z
Standby	V_{IH}	×	×	Vcc	Vcc	×	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	Vcc	×	Din
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	Vcc	×	Dout
Page data latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	Vcc	×	Din
Page program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	Vcc	×	High-Z
Program inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	Vcc	×	High-Z
	V_{IL}	V_{IH}	V_{IH}				
	V_{IH}	V_{IL}	V_{IL}				
	V_{IH}	V_{IH}	V_{IH}				
Identifier	V_{IL}	V_{IL}	V_{IH}	Vcc	Vcc	V_H	Code

Notes: × = Don't care, V_H = 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: *1. Relative to V_{SS}
*2. Vin, Vout, V_{ID} min = –1.0 V for pulse width ± 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	12	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{PP} = V_{CC})

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 5.25 V
Output leakage current	I_{LO}	—	—	2	µA	Vout = 5.25 V/0.45 V
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby Vcc current	I_{SB}	—	—	25	mA	$\overline{CE}$ = V_{IH}
Operating Vcc current	I_{CC1}	—	—	50	mA	$\overline{CE}$ = V_{IL}, Iout = 0 mA
	I_{CC2}	—	—	110	mA	f = 12 MHz, Iout = 0 mA
	I_{CC3}	—	—	25	mA	f = 1 MHz, Iout = 0 mA
Input low voltage*3	V_{IL}	–0.3*1	—	0.8	V	
Input high voltage*3	V_{IH}	2.2	—	Vcc+1.0*2	V	
Output low voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: *1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns.
*2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
*3. Only defined for DC and long cycle function test.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5 %, V_{PP} = V_{CC})

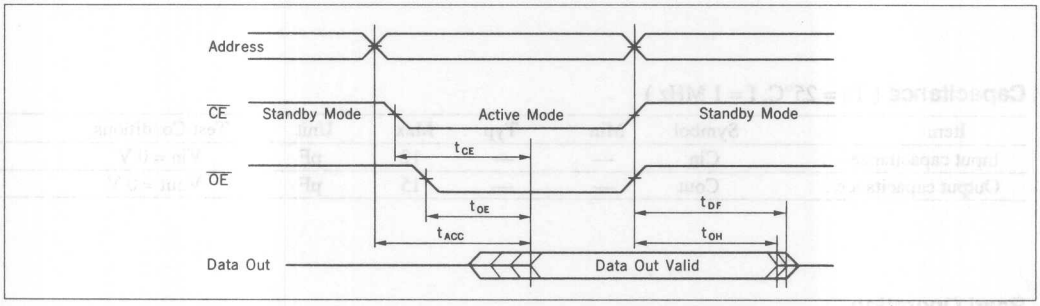
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1TTL Gate + 100 pF
- Reference levels for measuring timing:
  Inputs; 1.5V
  Outputs; 1.5V

Item	Symbol	HN27C1024HG-85		HN27C1024HG-10		Unit	Test Conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	—	85	—	100	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}	—	85	—	100	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	—	45	—	50	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	t_{DF}	0	30	0	50	ns	$\overline{CE} = V_{IL}$
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

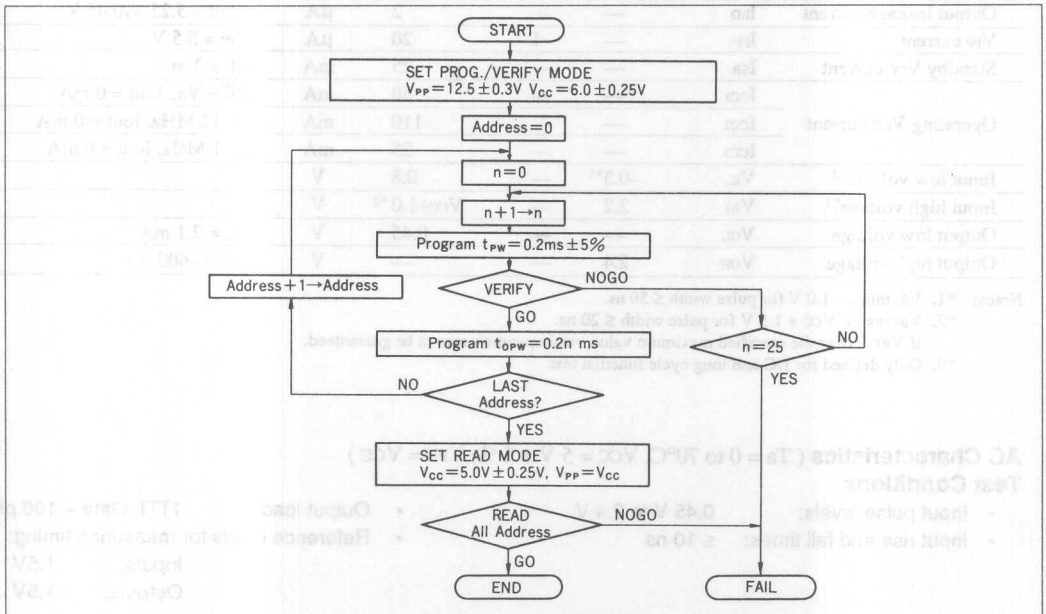
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.25 V/0.45 V
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating Vcc current	I_{CC}	—	—	50	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*6	V	
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes: *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13 V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
*4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
*5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

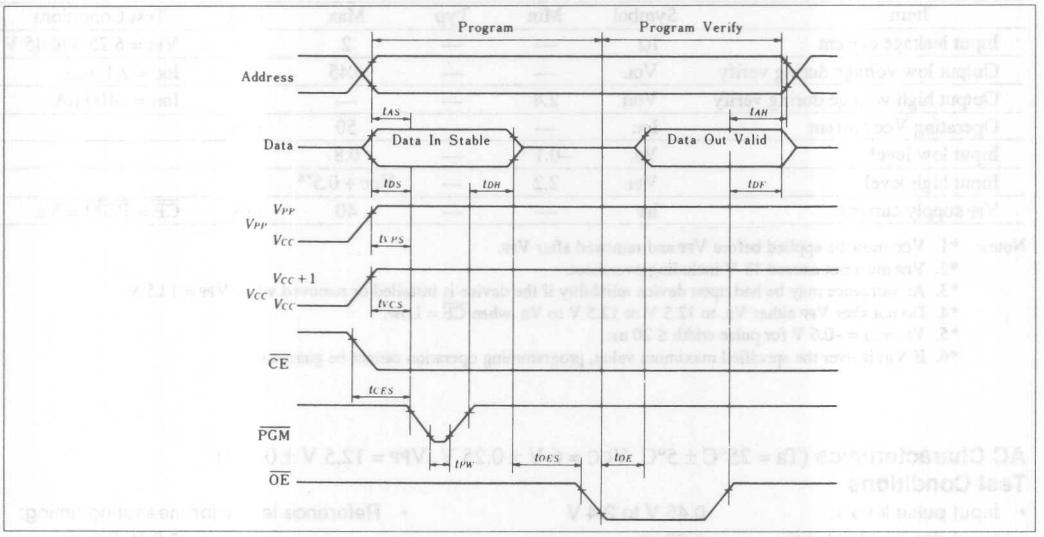
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
V_{CC} setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns

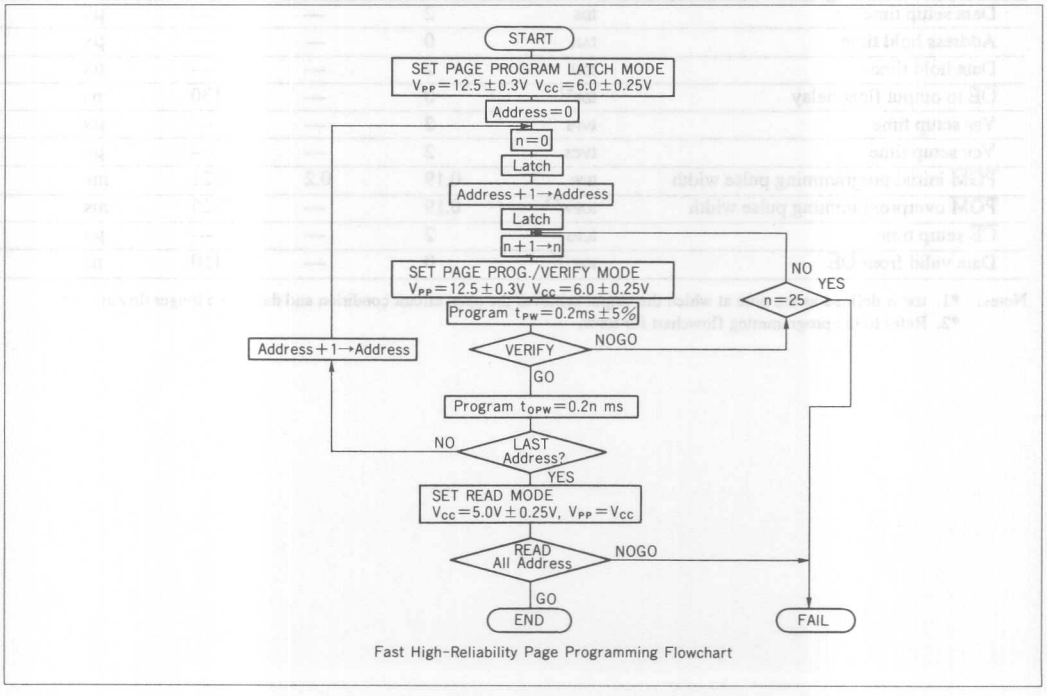
Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics ($Ta = 25°C \pm 5°C$, $V_{CC} = 6\ V \pm 0.25\ V$, $V_{PP} = 12.5\ V \pm 0.3\ V$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.25 V/0.45 V
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating Vcc current	I_{CC}	—	—	50	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	Vcc + 0.5*6	V	
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{PGM} = V_{IL}$

Notes: *1. Vcc must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13 V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
*4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
*5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, Vcc = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

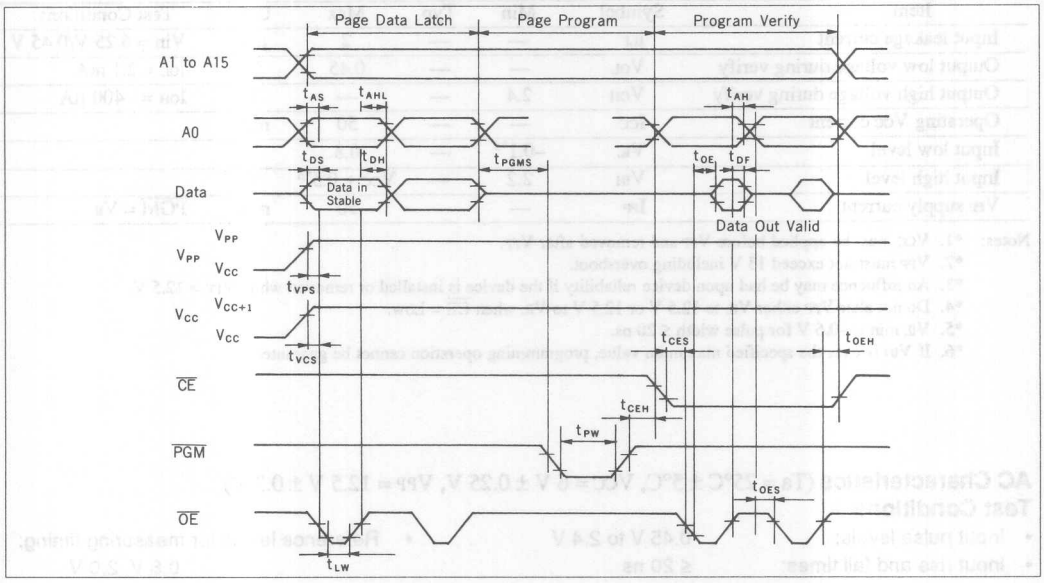
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
	t_{AHL}	2	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
Vcc setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	µs
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	µs
$\overline{CE}$ hold time	t_{CEH}	2	—	—	µs
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Page Programming Timing Waveform



Erase

Erasure of HN27C1024HG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W.sec/cm².

Mode Description

Device Identifier Mode

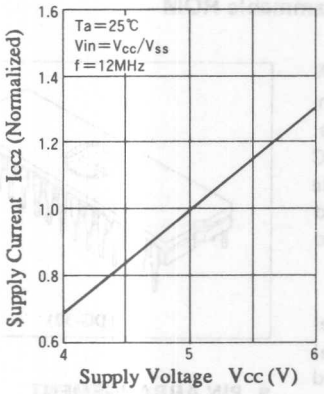
The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C1024HG Identifier Code

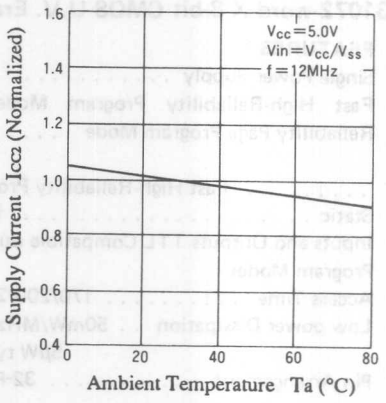
Identifier	A0 (21)	I/O8 to I/O15 (10) to (3)	I/O7 (12)	I/O6 (13)	I/O5 (14)	I/O4 (15)	I/O3 (16)	I/O2 (17)	I/O1 (18)	I/O0 (19)	Hex Data
Manufacturer code	V_{IL}	×	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	×	1	0	1	1	1	0	1	0	BA

Notes: × = Don't care, A9 = 12.0 V ± 0.5 V, A1–A8, A10–A15, CE, OE = V_{IL}, PGM = V_{IH}

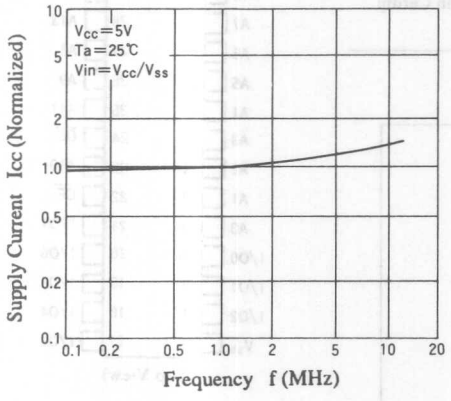
Supply Current vs. Supply Voltage



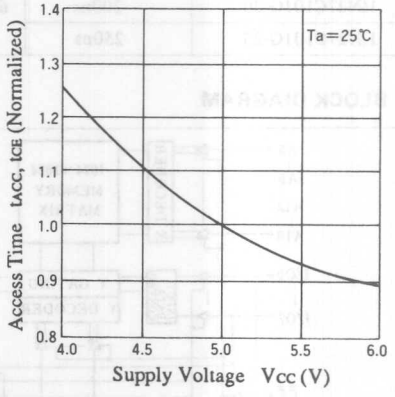
Supply Current vs. Ambient Temperature



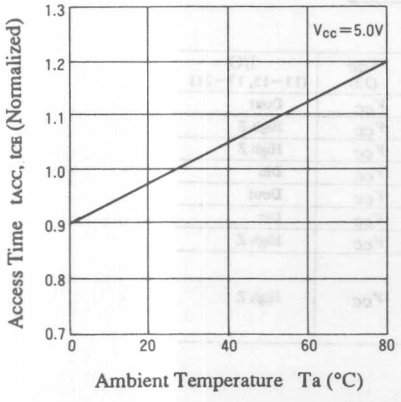
Supply Current vs. Frequency



Access Time vs. Supply Voltage



Access Time vs. Ambient Temperature

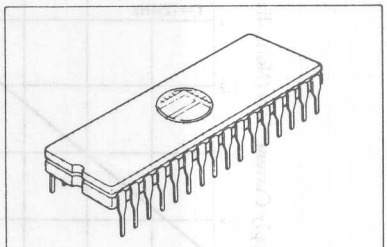


HN27C101G Series

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Fast High-Reliability Program Mode and Fast High-Reliability Page Program Mode . . . . . Program Voltage: +12.5V DC
  . . . . . Fast High-Reliability Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible during Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode)
  5μW typ. (Standby Mode)
- Pin Arrangement . . . . . 32-Pin JEDEC Standard



(DG-32)

■ ORDERING INFORMATION

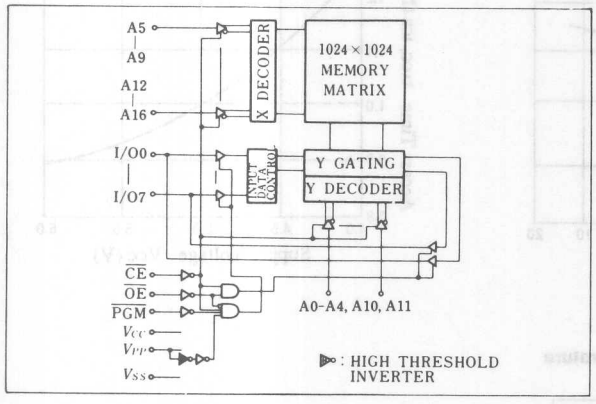
Type No.	Access Time	Package
HN27C101G-17	170ns	600-mil 32-pin Cerdip
HN27C101G-20	200ns	
HN27C101G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

● DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.5V	–	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$=V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$=V_{CC} ±0.3V	–	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{out}=0mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0mA	–	–	30	mA
	I_{CC3}	f=1MHz, I_{out}=0mA	–	–	15	mA
Input Low Voltage	V_{IL}		−0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

● AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

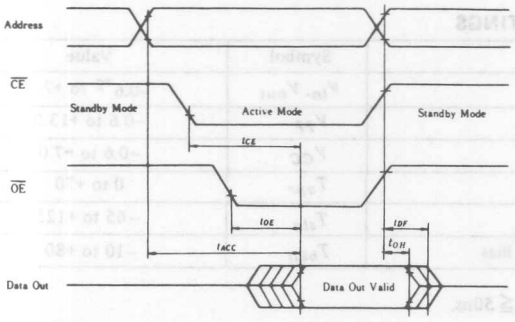
Parameter	Symbol	Test Conditions	HN27C101G-17		HN27C101G-20		HN27C101G-25		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	70	10	70	10	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	0	–	ns

Note) t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

● **Test Condition**

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

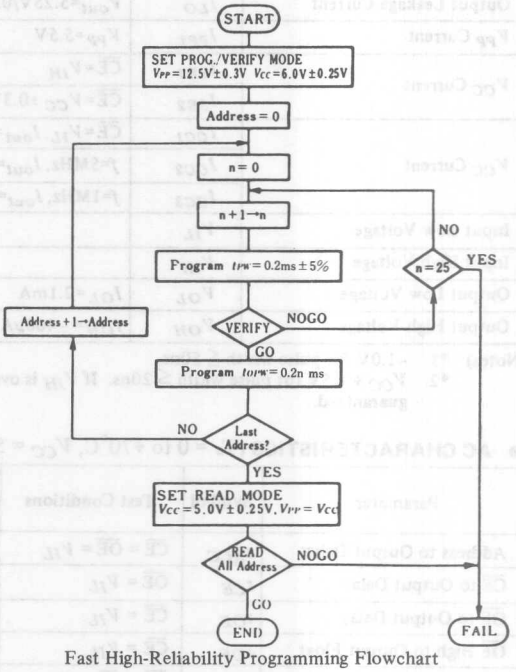


- **CAPACITANCE** (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	15	pF

■ FAST HIGH-RELIABILITY PROGRAMMING

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$=V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

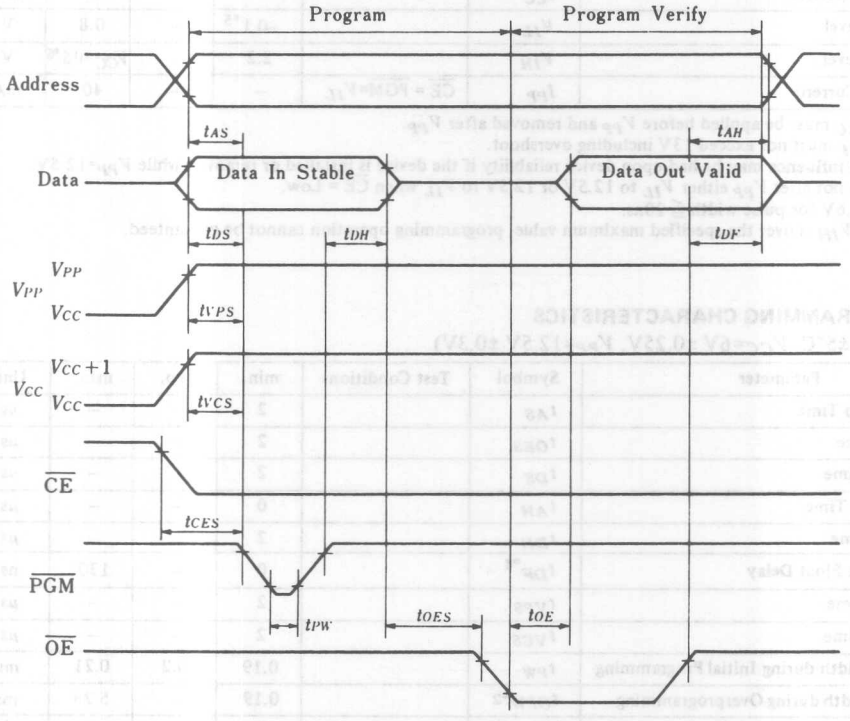
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

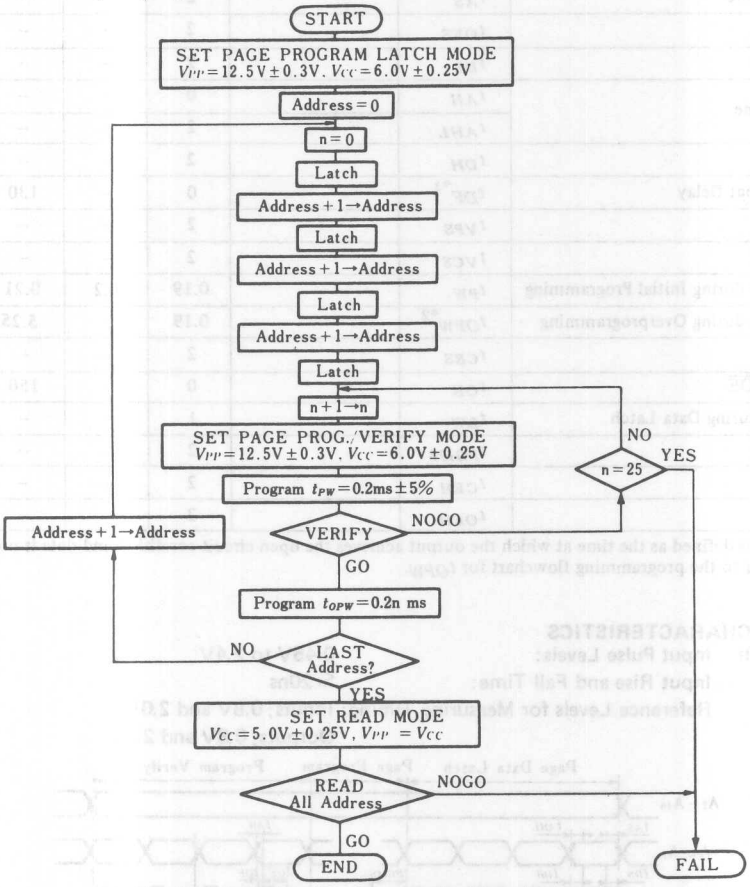
Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



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■ FAST HIGH-RELIABILITY PAGE PROGRAMMING

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH}= –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1 *5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5 *6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{OE}$=V_{IH}, $\overline{PGM}$=V_{IL}	–	–	50	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

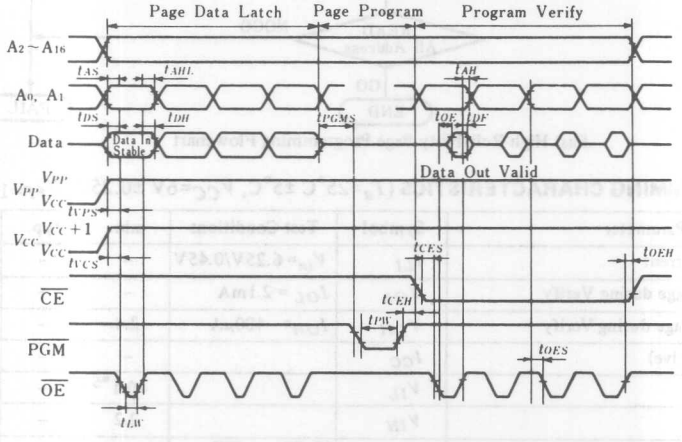
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	µs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	µs
Data Setup Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
	t_{AHL}		2	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	µs
V_{CC} Setup Time	t_{VCS}		2	–	–	µs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	µs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}		1	–	–	µs
$\overline{PGM}$ Setup Time	t_{PGMS}		2	–	–	µs
$\overline{CE}$ Hold Time	t_{CEH}		2	–	–	µs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	µs

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

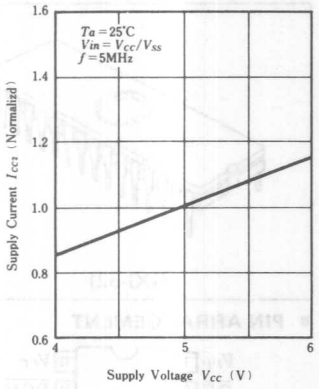
• **Test Condition**
Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



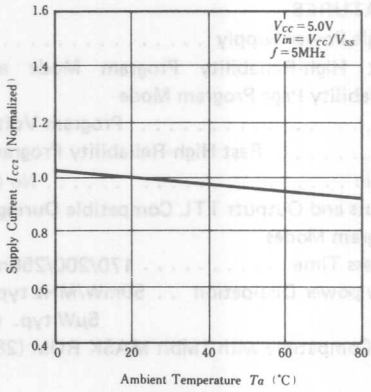
■ ERASE

Erasure of HN27C101G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W•sec/cm^2

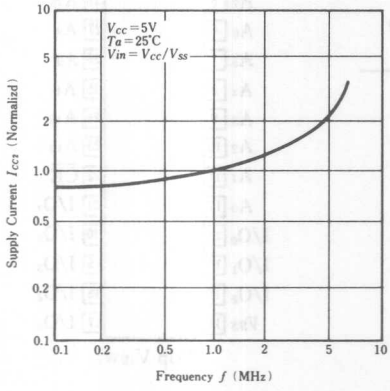
SUPPLY CURRENT vs. SUPPLY VOLTAGE



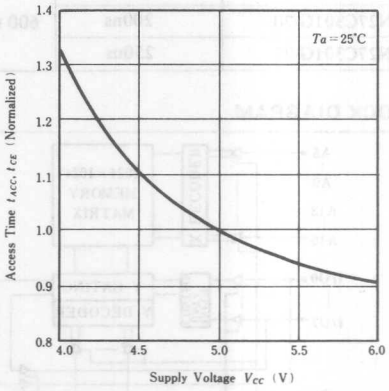
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



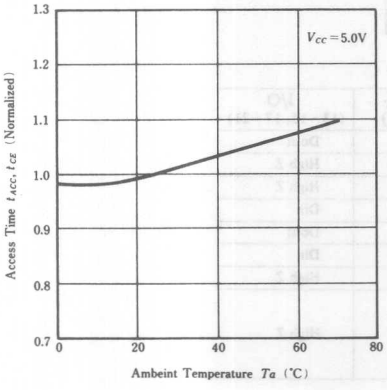
SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE

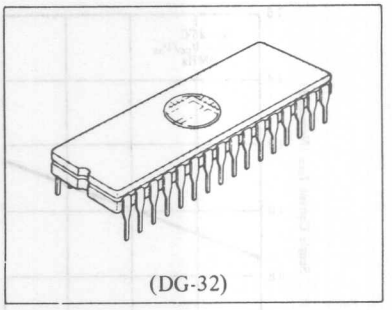


HN27C301G Series

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Fast High-Reliability Program Mode and Fast High-Reliability Page Program Mode
  . . . . . Program Voltage: +12.5V DC
  . . . . . Fast High-Reliability Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode)
  5μW typ. (Standby Mode)
- Pin Compatible with 1Mbit MASK ROM (28pin type)

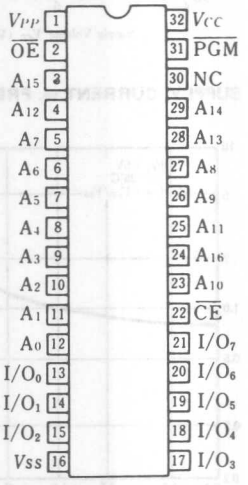


(DG-32)

■ ORDERING INFORMATION

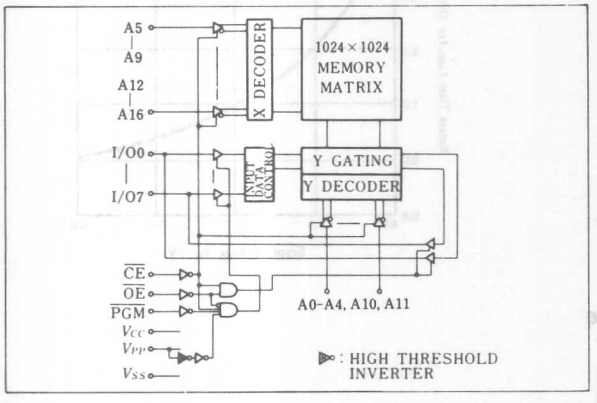
Type No.	Access Time	Package
HN27C301G-17	170ns	600 mil 32 pin Cerdip
HN27C301G-20	200ns	
HN27C301G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) *1. X: Don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}.
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

• DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.5V	–	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$=V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$=V_{CC} ±0.3V	–	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{out}=0mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0mA	–	–	30	mA
	I_{CC3}	f=1MHz, I_{out}=0mA	–	–	15	mA
Input Low Voltage	V_{IL}		−0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

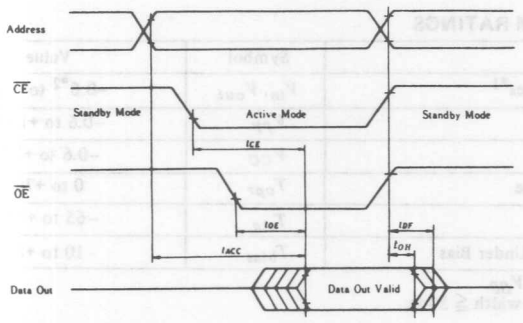
Parameter	Symbol	Test Conditions	HN27C301G-17		HN27C301G-20		HN27C301G-25		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	70	10	70	10	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	0	–	ns

Note) t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

• **Test Condition**

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

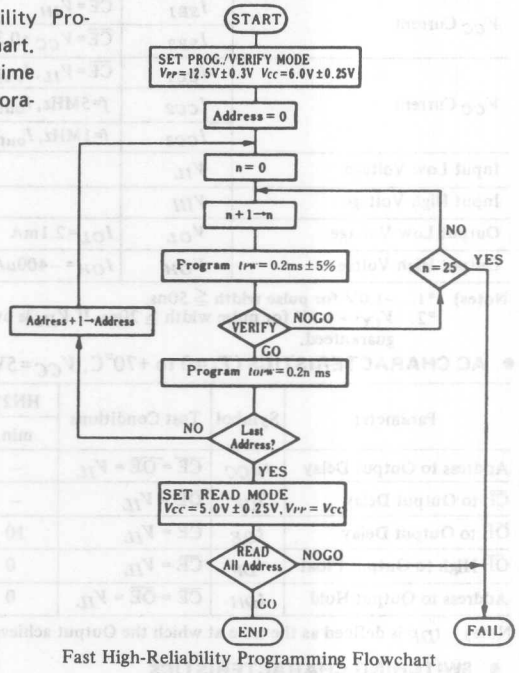


- **CAPACITANCE** (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	15	pF

■ FAST HIGH-RELIABILITY PROGRAMMING

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$=V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

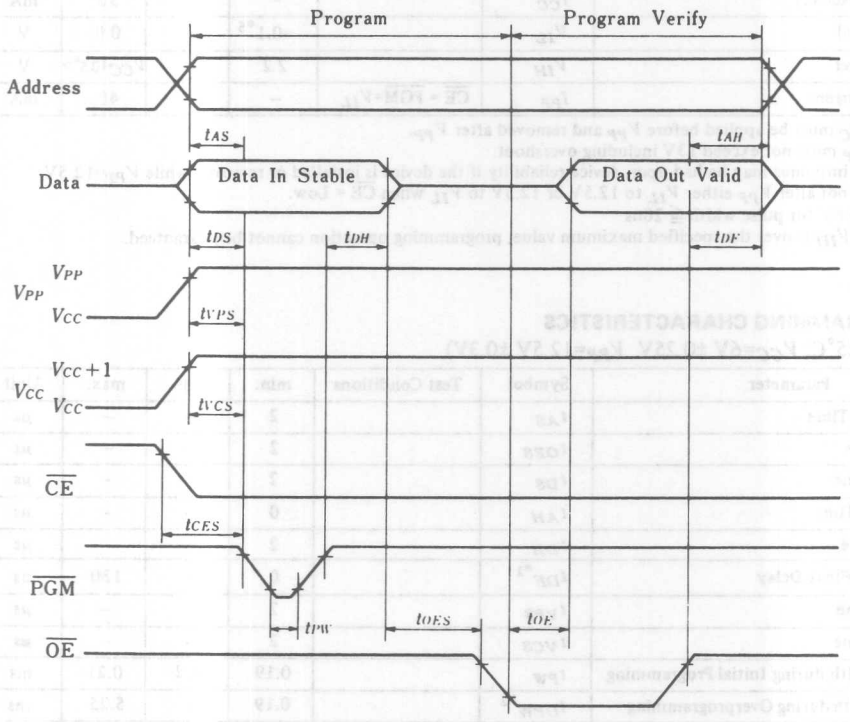
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

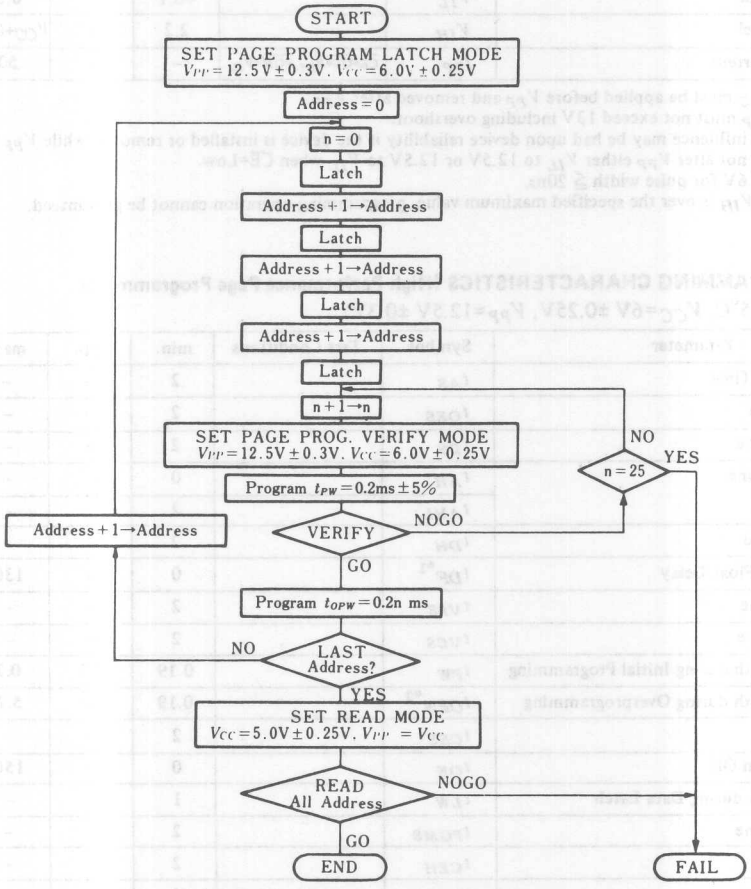
Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



■ FAST HIGH-RELIABILITY PAGE PROGRAMMING

This device can be applied the Fast High-Reliability Page Programming algorithm shown in following flowchart.

This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH}= –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{OE}$=V_{IH}, $\overline{PGM}$=V_{IL}	–	–	50	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

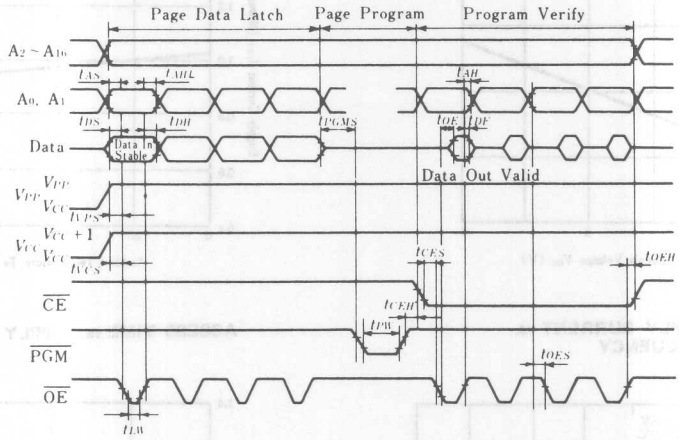
• AC PROGRAMMING CHARACTERISTICS (High Performance Page Programming)

(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Adress Hold Time	t_{AH}		0	–	–	μs
	t_{AHL}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}		1	–	–	μs
$\overline{PGM}$ Setup Time	t_{PGMS}		2	–	–	μs
$\overline{CE}$ Hold Time	t_{CEH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

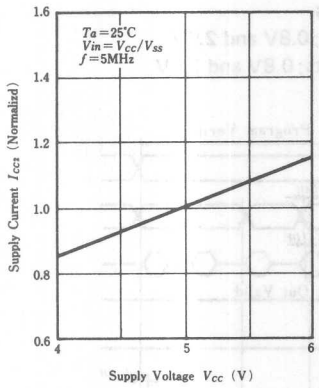
- **SWITCHING CHARACTERISTICS**
- **Test Condition** Input Pulse Levels: 0.45V to 2.4V
  Input Rise and Fall Time: ≤ 20ns
  Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V



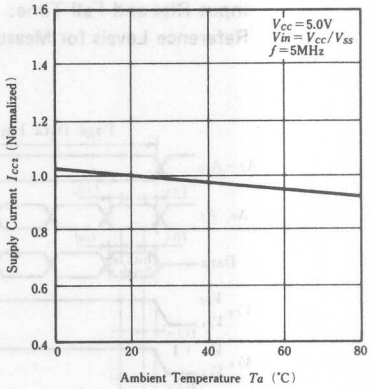
■ ERASE

Erasure of HN27C301G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W · sec/cm^2.

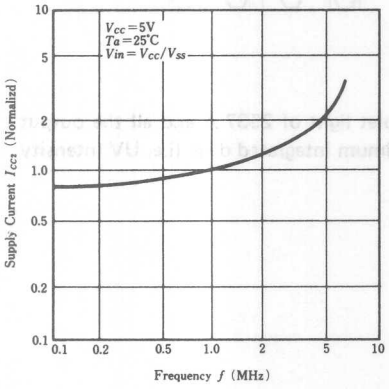
SUPPLY CURRENT vs. SUPPLY VOLTAGE



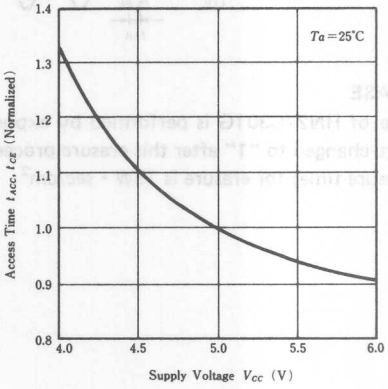
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



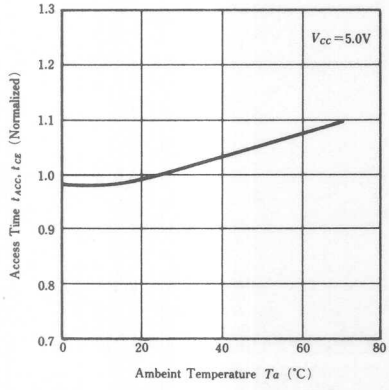
SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



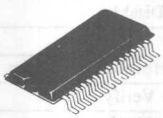
ACCESS TIME vs. AMBIENT TEMPERATURE



HN27C256FP Series

32768-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C256FP is a 32768-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C256FP are in the "1" State (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin plastic flat package (SOP). Therefore, this device cannot be re-written.

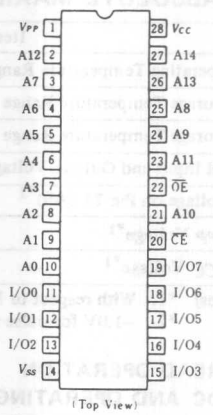


(FP-28DA)

■ FEATURES

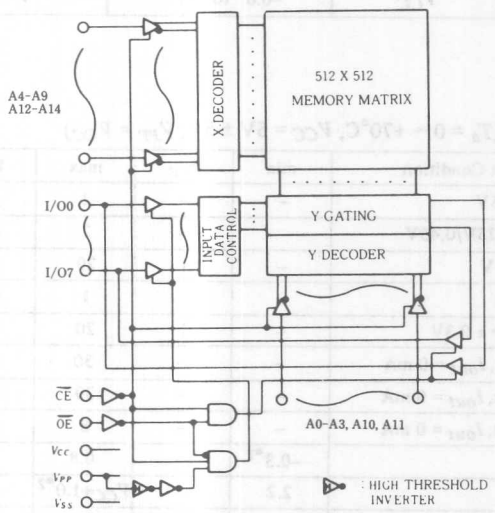
- Low Power Dissipation . . . . . 40mW/MHz max. (Active Mode)
  110μW max (Standby Mode)
- Access Time . . . . . 250ns max. (HN27C256FP-25T)
  300ns max. (HN27C256FP-30T)
- Single Power Supply . . . . . 5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V DC
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Absolute Max. Rating of V_{PP} pin. . . 14.0V
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H *2	V_{CC}	V_{CC}	Code

Notes) *1. X: Don't care.
*2. V_H: 12.0 ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltage*1	V_{IN}, V_{OUT}	−0.6*2 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6*2 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Notes) *1. With respect to V_{SS}.
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a = 0 ~ +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5V	–	1	20	μA
V_{CC} Current (Standby)	I_{SB1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$ = V_{CC} ± 0.3V	–	1	20	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{out} = 0 mA	–	–	30	mA
	I_{CC2}	f = 5 MHz, I_{out} = 0 mA	–	–	30	mA
	I_{CC3}	f = 1 MHz, I_{out} = 0 mA	–	–	8	mA
Input Voltage	V_{IL}		−0.3*1	–	0.8	V
	V_{IH}		2.2	–	V_{CC}+1.0*2	V
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
	V_{OH1}	I_{OH} = −400 μA	2.4	–	–	V
	V_{OH2}	I_{OH} = −100 μA	V_{CC}−0.7	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

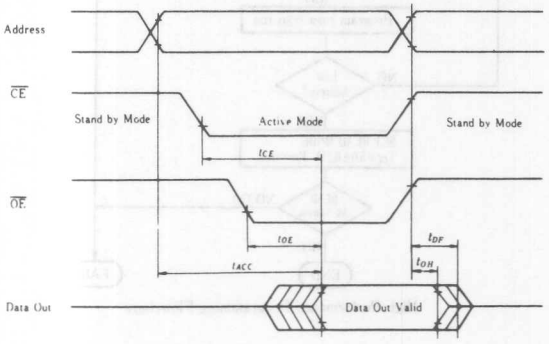
Parameter	Symbol	Test Condition	HN27C256FP-25T		HN27C256FP-30T		Unit
			Min	Max	Min	Max	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	100	0	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Output load: 1 TTL Gate +100pF
Reference level for measuring timing: 0.8V and 2.0V

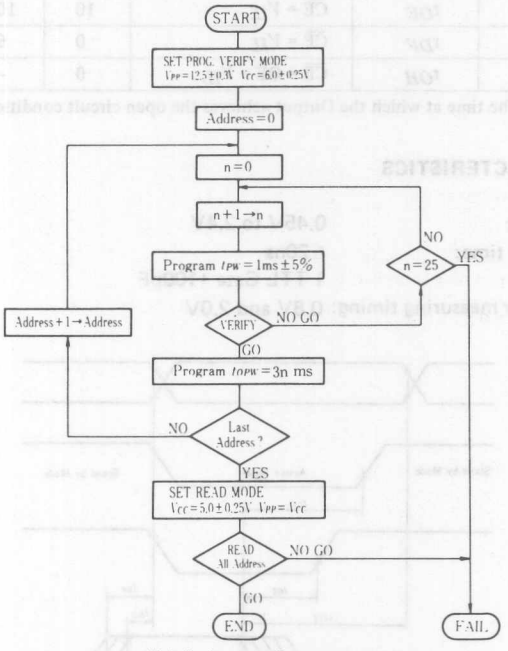


• CAPACITANCE (T_a=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 6.25V/0.45V	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	30	mA
Input Low Level	V_{IL}		−0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 14V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. −0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

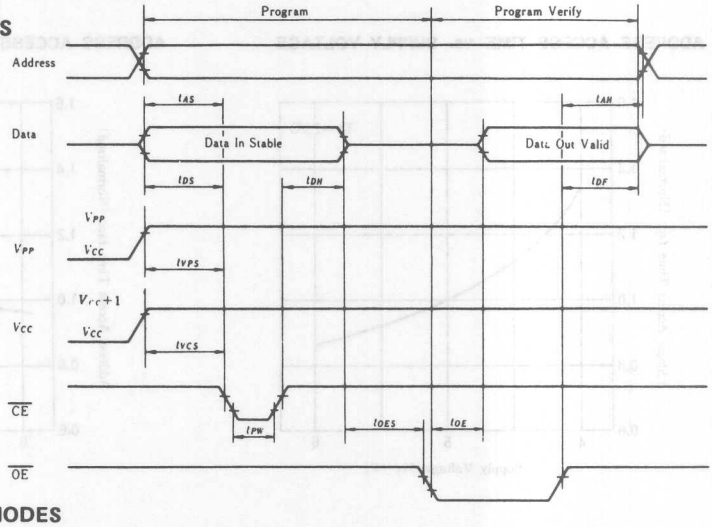
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse level: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Reference level for measuring timing: 0.8V and 2V



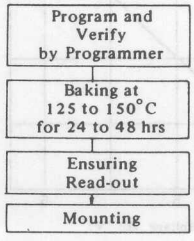
• HN27C256FP IDENTIFIER MODES

Identifier \ Pins	A_0 (10)	I/O_7 (19)	I/O_6 (18)	I/O_5 (17)	I/O_4 (16)	I/O_3 (15)	I/O_2 (13)	I/O_1 (12)	I/O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	1	1	0	0	0	0	B0

Notes: 1. A_9 = 12.0V ± 0.5V.
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

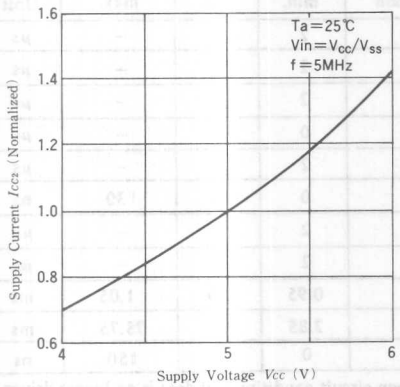
■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.

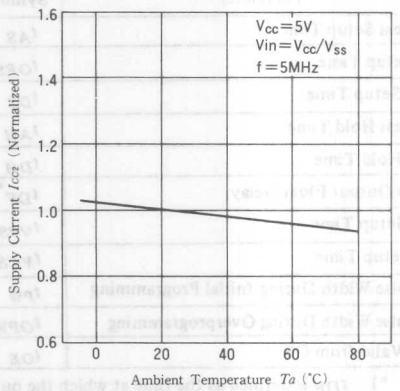


Recommended Screening conditions

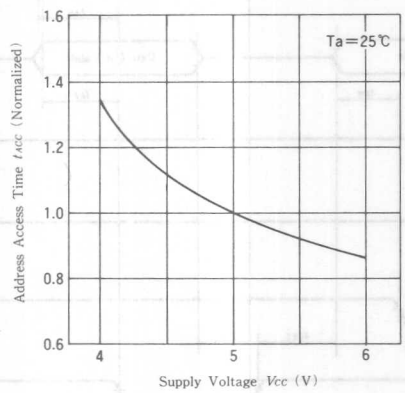
SUPPLY CURRENT vs. SUPPLY VOLTAGE



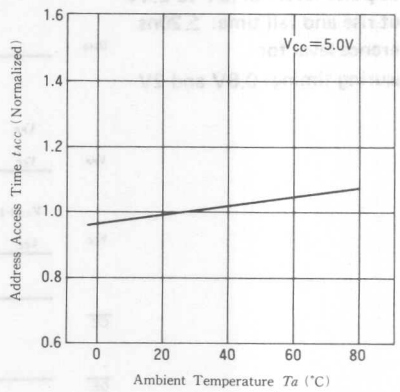
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



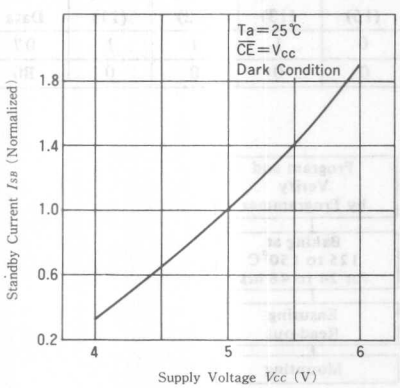
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



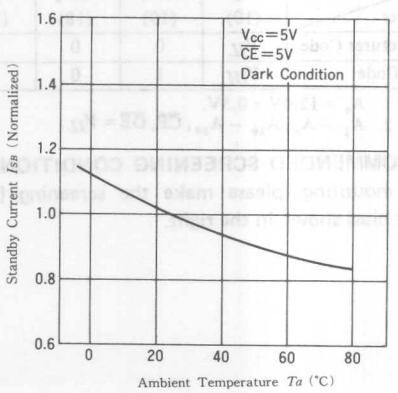
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE

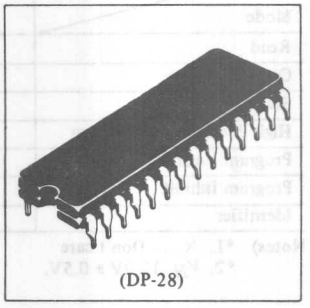


* See Supply Voltage vs. Active Frequency, Access Time vs. Lord Capacitance, and Output Current vs. Output Voltage (1), (2) of HN27C256G.

HN27512P Series

65536-word x 8-bit One Time Electrically Programmable Read Only Memory

The HN27512P is a 65536-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27512P are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic dual in-line package. Therefore, this device can not be re-written.


(DP-28)

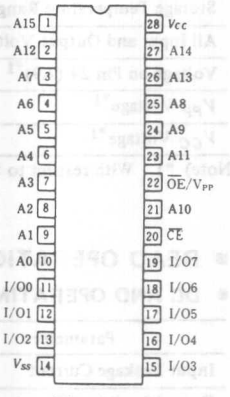
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V (max.)
- Low Stand-by Current . . . . . 40mA (max.)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code.

Ordering Information

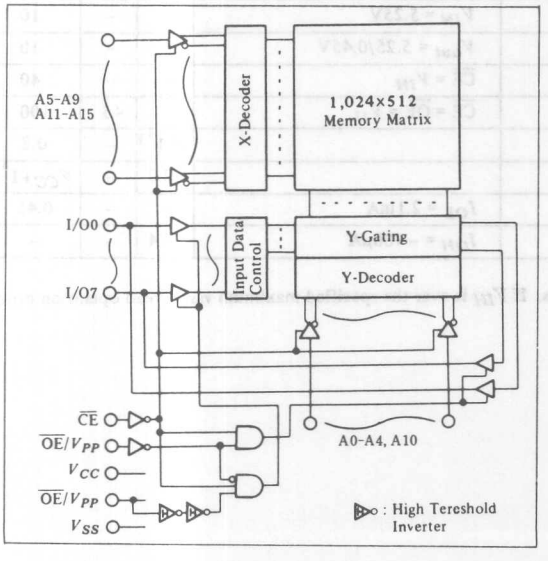
Part No.	Access	Package
HN27512P-25	250ns	600 mil 28-pin Plastic DIP
HN27512P-30	300ns	

Pin Arrangement



(Top View)

Block Diagram



Pin Description

Pin Name	Function
A0 – A15	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Power Supply
V_{SS}	Ground

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	I/O (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. With respect to V_{SS}

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25/0.45V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	45	100	mA
Input Low voltage	V_{IL}		−0.1*1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Condition	HN27512P-25		HN27512P-30		Unit
			min.	max.	min.	max.	
Addres to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

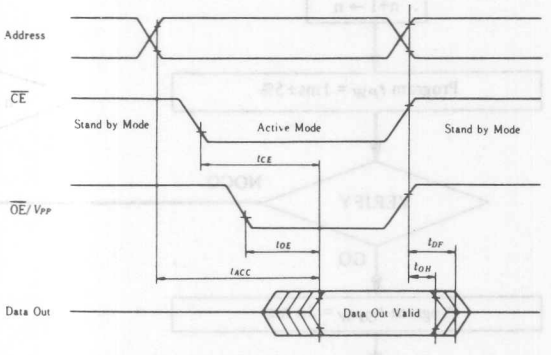
Test Condition

Input Pulse Levels: 0.45V to 2.4V

Input Rise and Fall Time: ≤ 20ns

Output Load: 1 TTL Gate +100pF

Reference Level for Measuring Timing: 0.8V and 2.0V

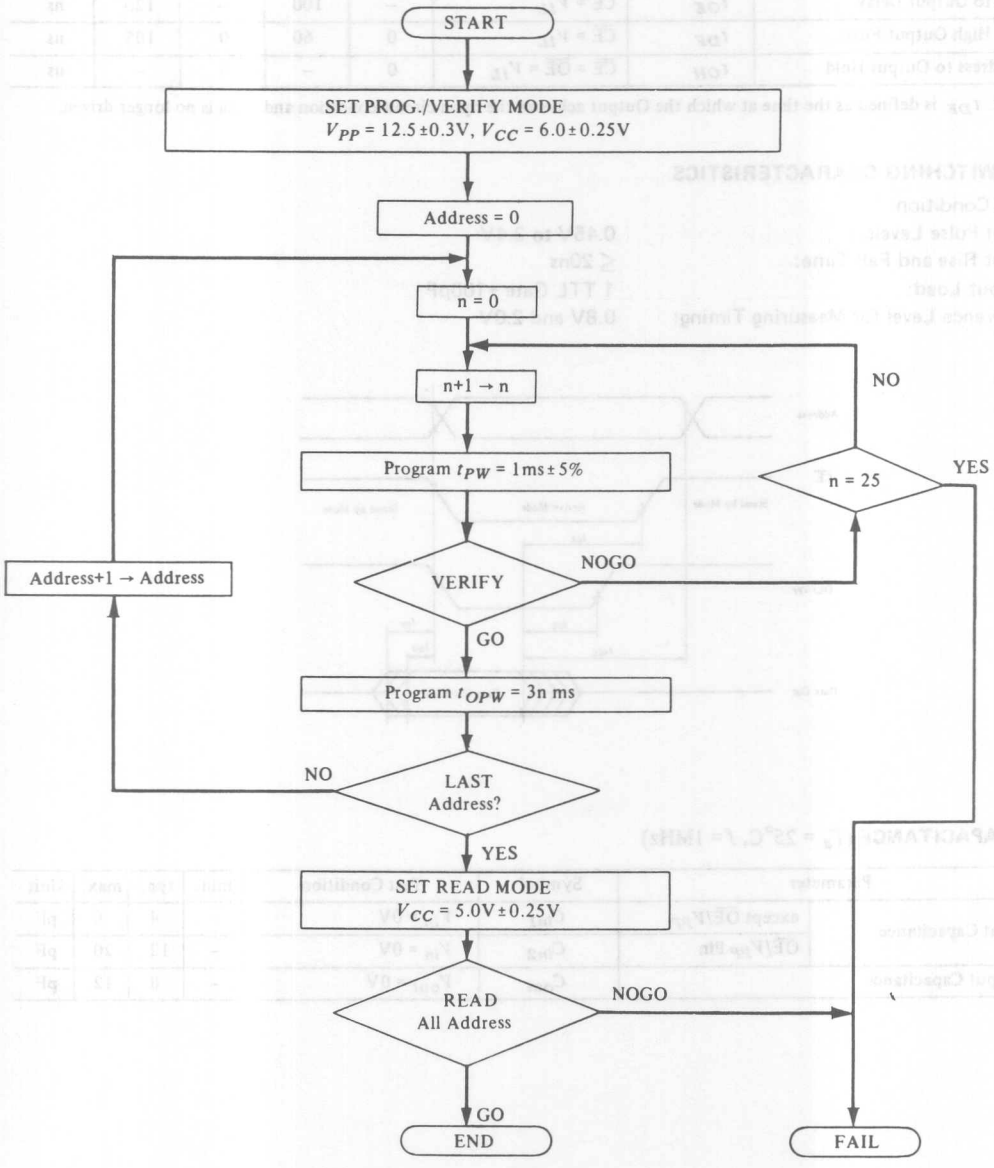


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	except $\overline{OE}/V_{PP}$	C_{in1}	V_{in} = 0V	–	4	6	pF
	$\overline{OE}/V_{PP}$ Pin	C_{in2}	V_{in} = 0V	–	12	20	pF
Output Capacitance		C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

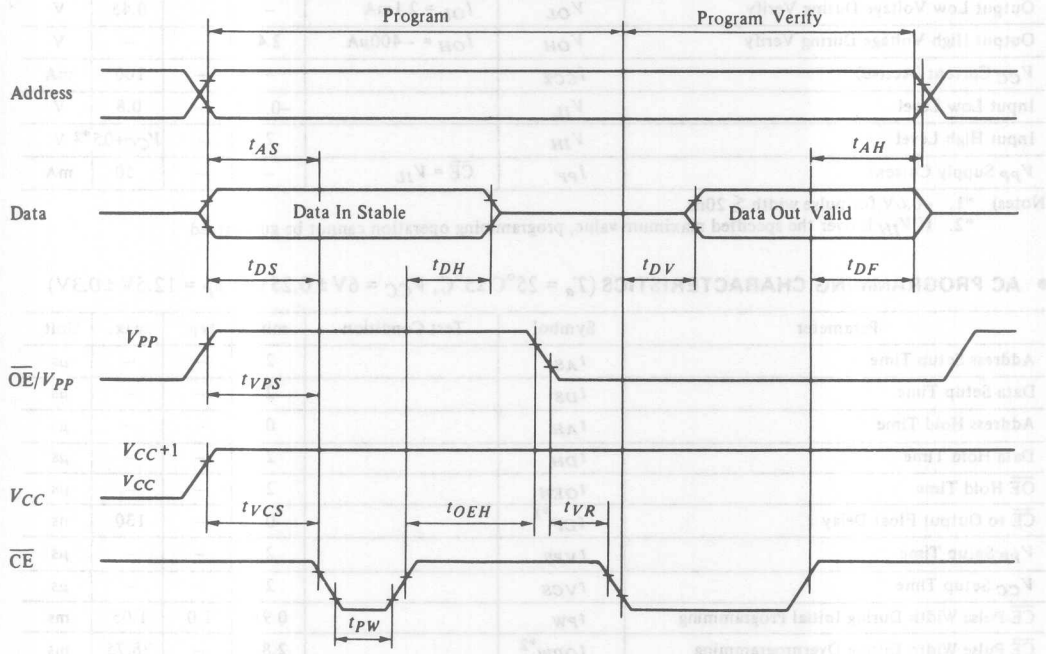
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
$\overline{CE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
V_{PP} Recovery Time	t_{VR}		2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}		–	–	1	μs

Notes: *1. t_{DF} is de fined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of OTPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

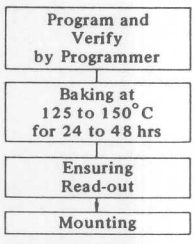
• HN27512P SERIES IDENTIFIER CODE

Identifier \ Pins	A_0 (10)	O_7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IL}	1	0	0	1	0	1	0	0	94

Notes: 1. $A_9 = 12.0V \pm 0.5V$.
2. $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$.

■ RECOMMENDED SCREENING CONDITIONS

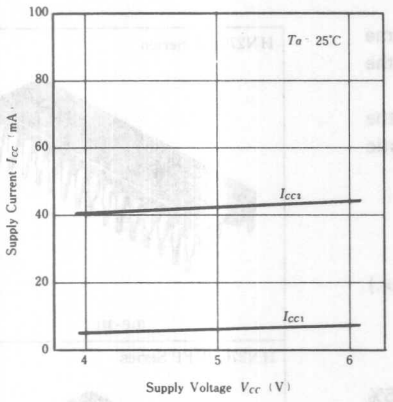
Before mounting, please make the screening (baking without bias) shown in the right.



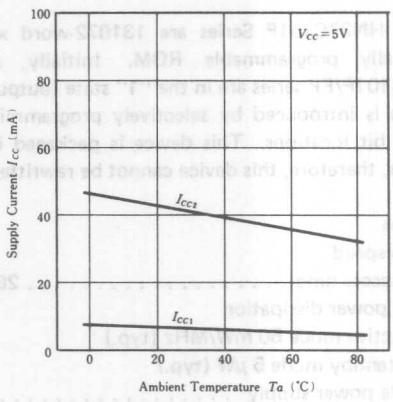
Recommended Screening conditions

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

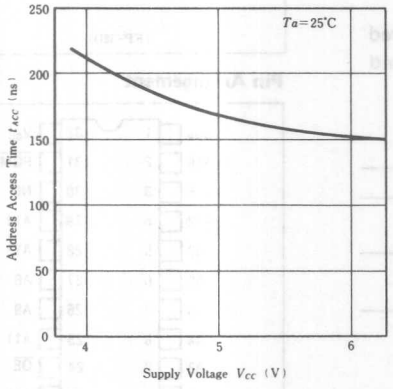
SUPPLY CURRENT vs. SUPPLY VOLTAGE



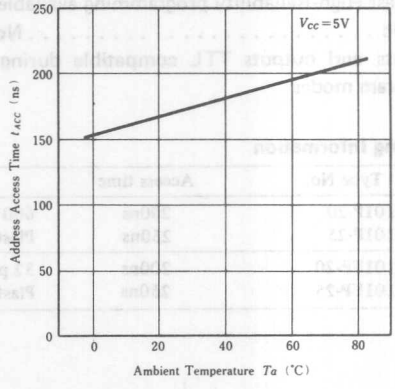
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



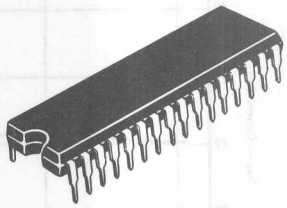
HN27C101P/FP Series

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C101P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C101P/FP series are in the "1" state (output high).

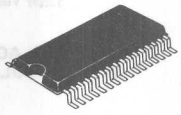
Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C101 Series



(DP-32)

HN27C101FP Series



(FP-32D)

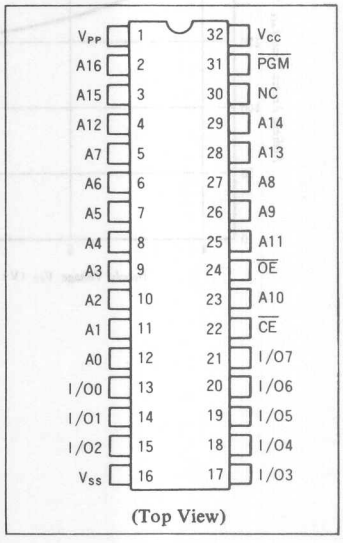
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply . . . . . +5 V ± 5%
- Fast High-Reliability program mode and Fast High-Reliability page program mode
  - Program voltage: +12.5V DC
  - Fast High-Reliability programming available
- Static . . . . . No clocks required
- Inputs and outputs TTL compatible during both read and program modes

Ordering Information

Type No.	Access time	Package
HN27C101P-20	200ns	600 mil 32 pin
HN27C101P-25	250ns	Plastic DIP
HN27C101FP-20	200ns	32 pin
HN27C101FP-25	250ns	Plastic SOP

Pin Arrangement

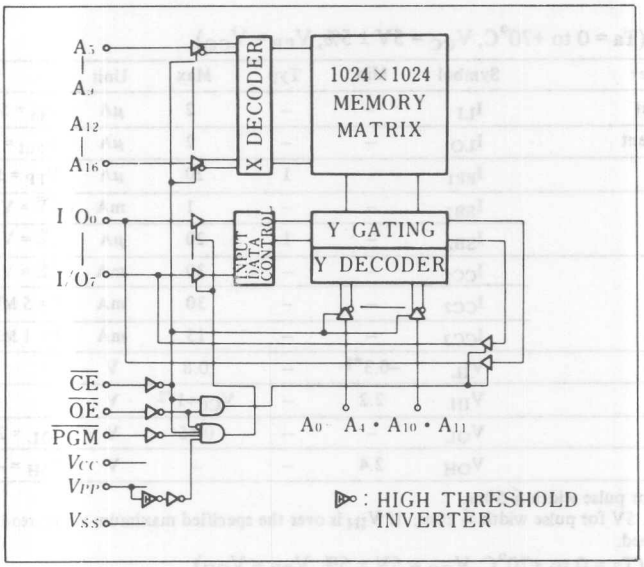


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



■ Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IH}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0 V for pulse width ≦ 50 ns

Read Operation

DC Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	$V_{in} = 5.25V$
Output Leakage Current	I_{LO}	–	–	2	μA	$V_{out} = 5.25V/0.45V$
V_{PP} Current	I_{PP1}	–	1	20	μA	$V_{PP} = 5.5V$
V_{CC} Current	I_{SB1}	–	–	1	mA	$\overline{CE} = V_{IH}$
	I_{SB2}	–	1	20	μA	$\overline{CE} = V_{CC} \pm 0.3V$
V_{CC} Current	I_{CC1}	–	–	30	mA	$\overline{CE} = V_{IL}$, $I_{out} = 0mA$
	I_{CC2}	–	–	30	mA	$f = 5$ MHz, $I_{out} = 0mA$
	I_{CC3}	–	–	15	mA	$f = 1$ MHz, $I_{out} = 0mA$
Input Low Voltage	V_{IL}	−0.3*1	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	$V_{CC}+1$*2	V	
Output Low Voltage	V_{OL}	–	–	0.45	V	$I_{OL} = 2.1mA$
Output High Voltage	V_{OH}	2.4	–	–	V	$I_{OH} = -400μA$

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. $V_{CC} + 1.5V$ for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

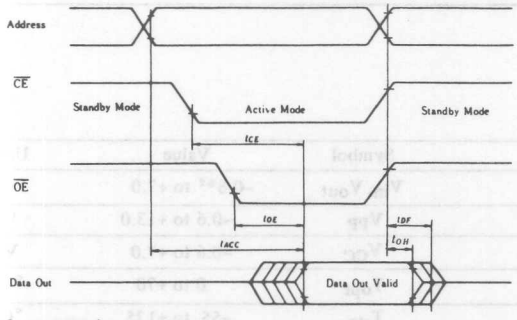
Item	Symbol	HN27C101-20		HN27C101-25		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	200	–	250	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$\overline{CE}$ to output delay	t_{CE}	–	200	–	250	ns	$\overline{OE}=V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	10	70	10	100	ns	$\overline{CE}=V_{IL}$
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	ns	$\overline{CE}=V_{IL}$
Address to output hold	t_{OH}	0	–	0	–	ns	$\overline{CE}=\overline{OE}=V_{IL}$

Note) t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

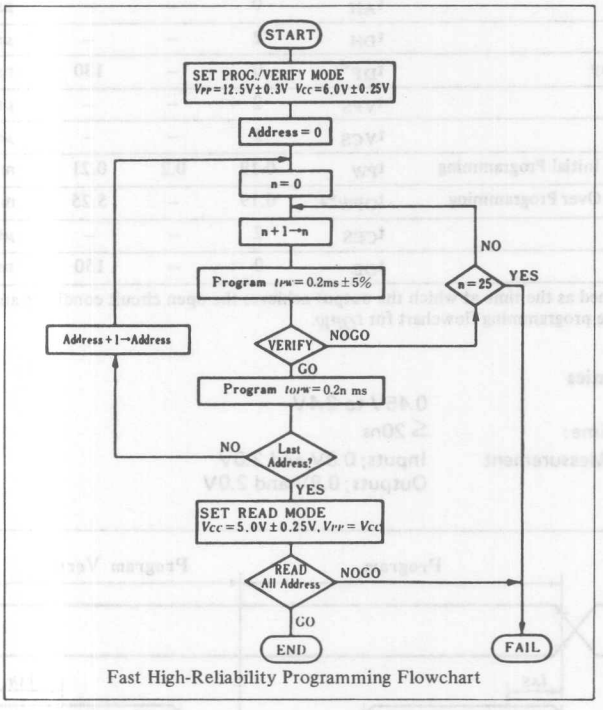


Capacitance ($Ta = 25°C$, $f = 1$ MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	–	–	10	pF	$V_{in} = 0V$
Output Capacitance	C_{out}	–	–	15	pF	$V_{out} = 0V$

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5 V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

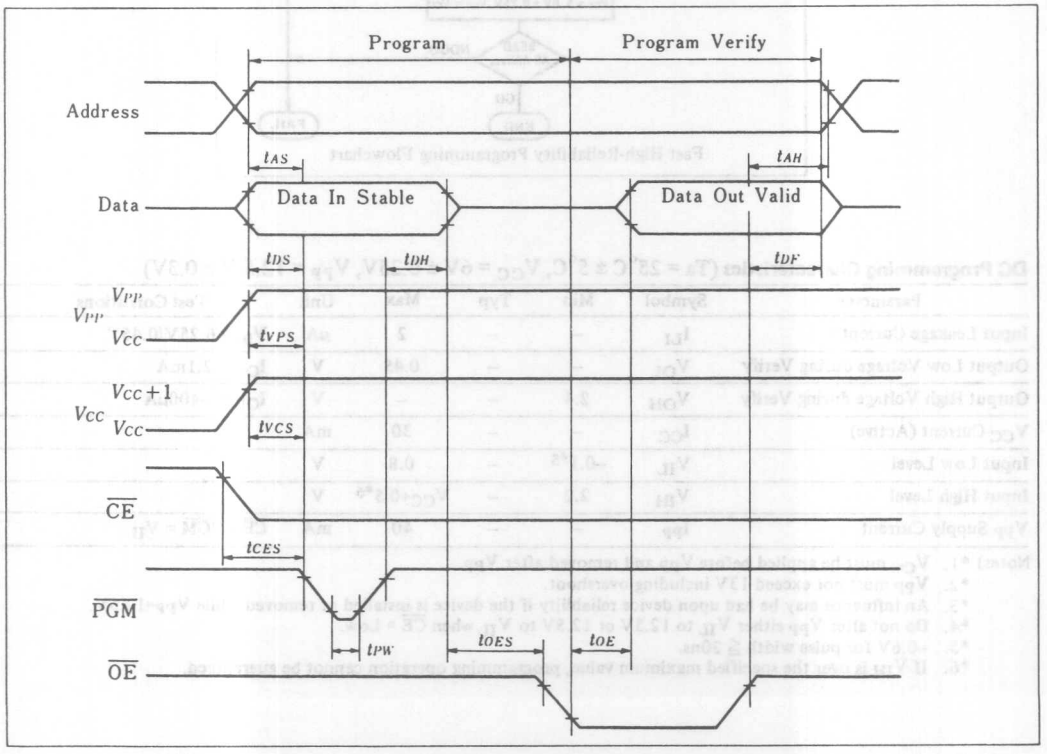
($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	µs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	µs	
Data Setup Time	t_{DS}	2	–	–	µs	
Address Hold Time	t_{AH}	0	–	–	µs	
Data Hold Time	t_{DH}	2	–	–	µs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	µs	
V_{CC} Setup Time	t_{VCS}	2	–	–	µs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	µs	
Data Valid from OE	t_{OE}	0	–	150	ns	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

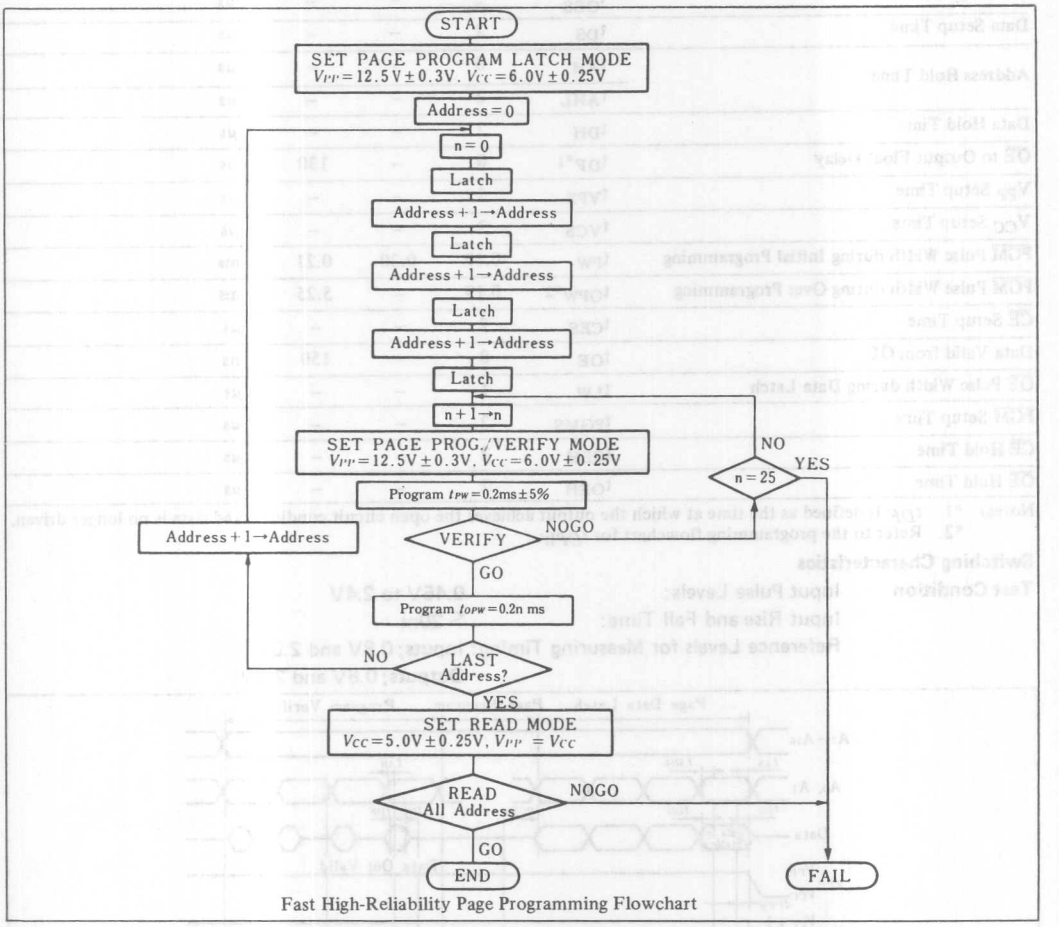
Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



Fast High-Reliability Page Programming

This device can be applied the Fast High-Reliability Page Programming algorithm shown in following flowchart.

This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

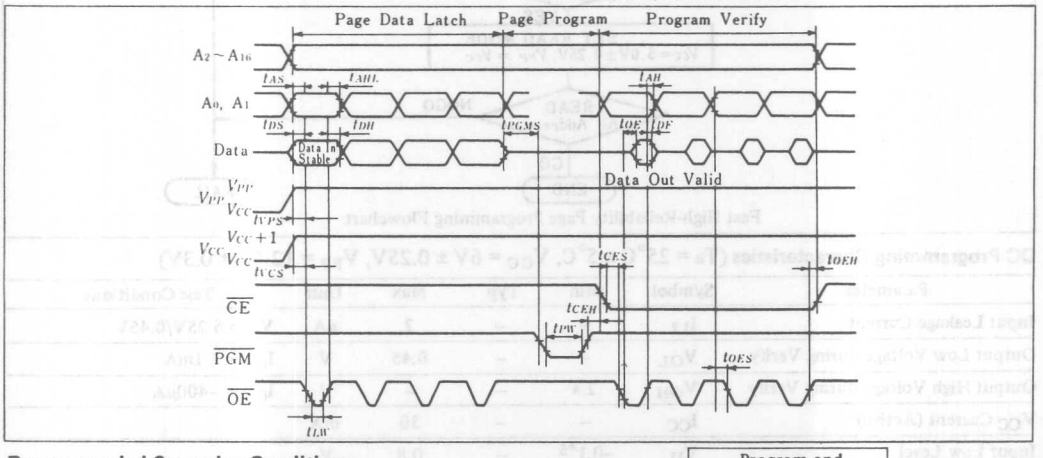
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	µs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	µs	
Data Setup Time	t_{DS}	2	–	–	µs	
Address Hold Time	t_{AH}	0	–	–	µs	
	t_{AHL}	2	–	–	µs	
Data Hold Time	t_{DH}	2	–	–	µs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	µs	
V_{CC} Setup Time	t_{VCS}	2	–	–	µs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	µs	
Data Valid from $\overline{OE}$	t_{OE}	0	–	150	ns	
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}	1	–	–	µs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	–	–	µs	
$\overline{CE}$ Hold Time	t_{CEH}	2	–	–	µs	
$\overline{OE}$ Hold Time	t_{OEH}	2	–	–	µs	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

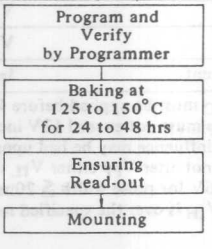
Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

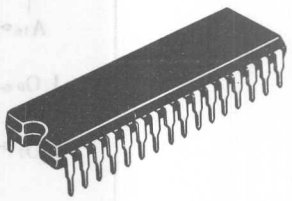
HN27C301P/FP Series

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C301P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C301P/FP Series are in the "1" state (output high).

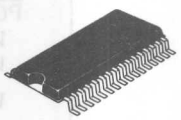
Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C301P Series



(DP-32)

HN27C301FP Series



(FP-32D)

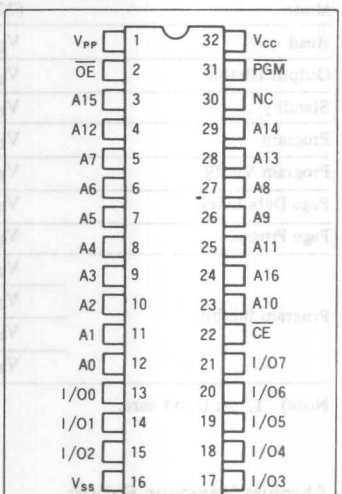
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply +5V ± 5%
- Fast High-Reliability program mode and Fast High-Reliability page program mode
  - Program voltage: +12.5V DC
  - Fast High-Reliability programming available
- Static . . . . . No clocks required
- Inputs and output TTL compatible during both read and program modes.

Ordering Information

Type No.	Access time	Package
HN27C301P-20	200ns	600 mil 32 pin
HN27C301P-25	250ns	Plastic DIP
HN27C301FP-20	200ns	32 pin
HN27C301FP-25	250ns	Plastic SOP

Pin Arrangement

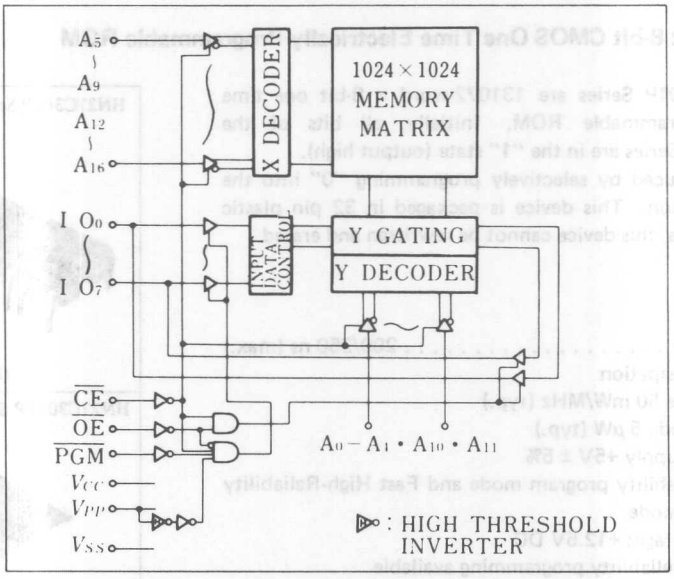


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0 V for pulse width ≦ 50 ns

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 5.25V
Output Leakage Current	I_{LO}	–	–	2	μA	V_{out} = 5.25V/0.45V
V_{PP} Current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
V_{CC} Current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ±0.3V
V_{CC} Current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, I_{out} = 0mA
	I_{CC2}	–	–	30	mA	f = 5 MHz, I_{out} = 0mA
	I_{CC3}	–	–	15	mA	f = 1 MHz, I_{out} = 0mA
Input Low Voltage	V_{IL}	–0.3*1	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	V_{CC}+1*2	V	
Output Low Voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –400μA

Notes) *1. –1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

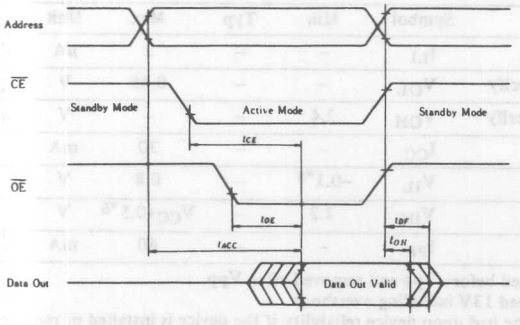
Item	Symbol	HN27C301P-20		HN27C301P-25		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	200	–	250	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	200	–	250	ns	$\overline{OE}$= V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	70	10	100	ns	$\overline{CE}$= V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	ns	$\overline{CE}$= V_{IL}
Address to output hold	t_{OH}	0	–	0	–	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}

Note) t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≦ 20ns
Output Load:	1 TTL Gate + 100pF
Reference Levels for Measuring Timing:	Inputs; 0.8V and 2.0V
	Outputs; 0.8V and 2.0V

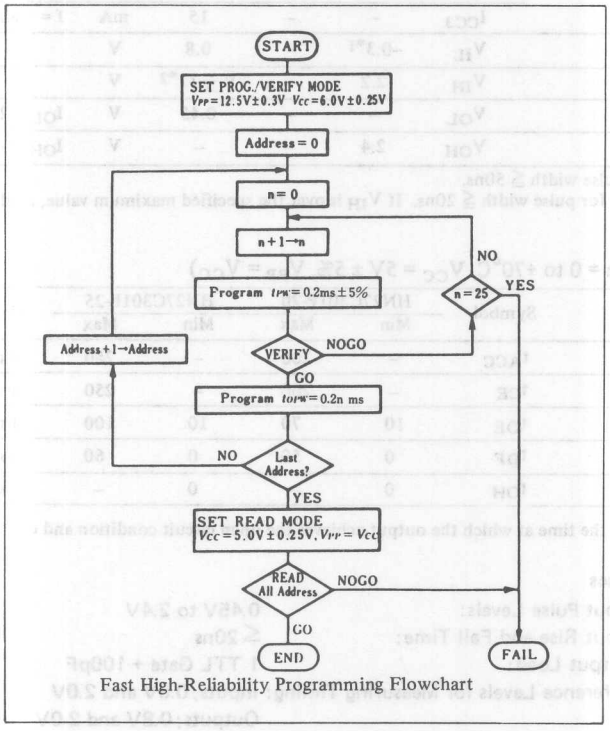


Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	–	–	10	pF	V_{in} = 0V
Output Capacitance	C_{out}	–	–	15	pF	V_{out} = 0V

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1 *5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
V_{PP} Supply Current	I_{PP}	–	–	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

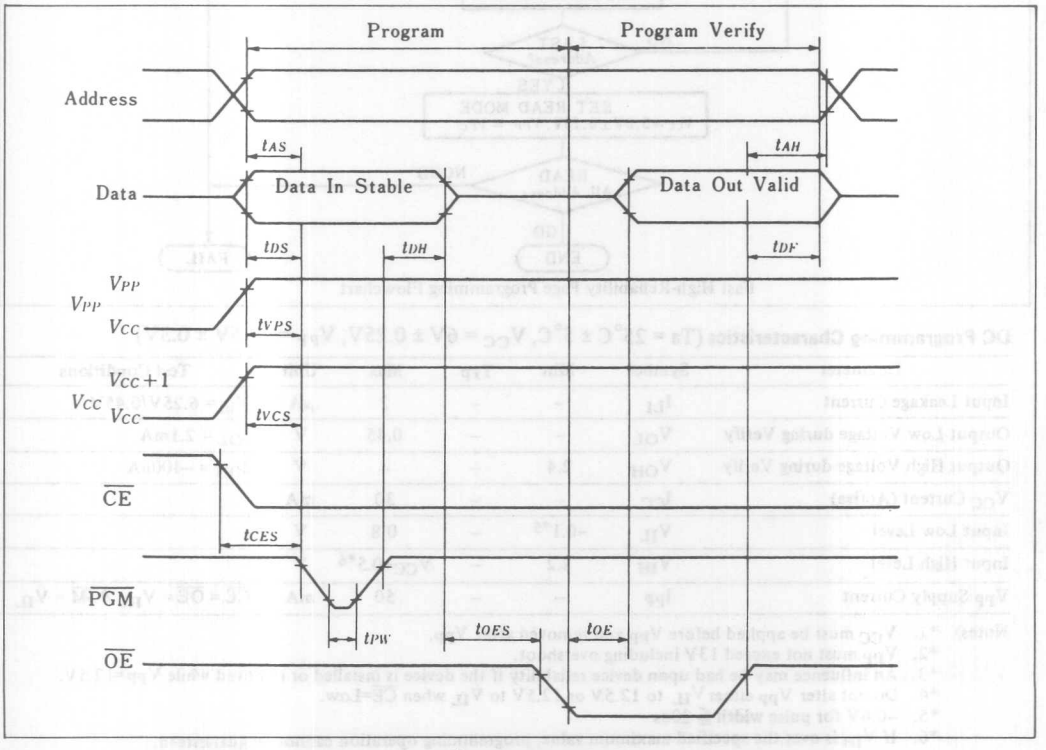
($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from OE	t_{OE}	0	–	150	ns	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

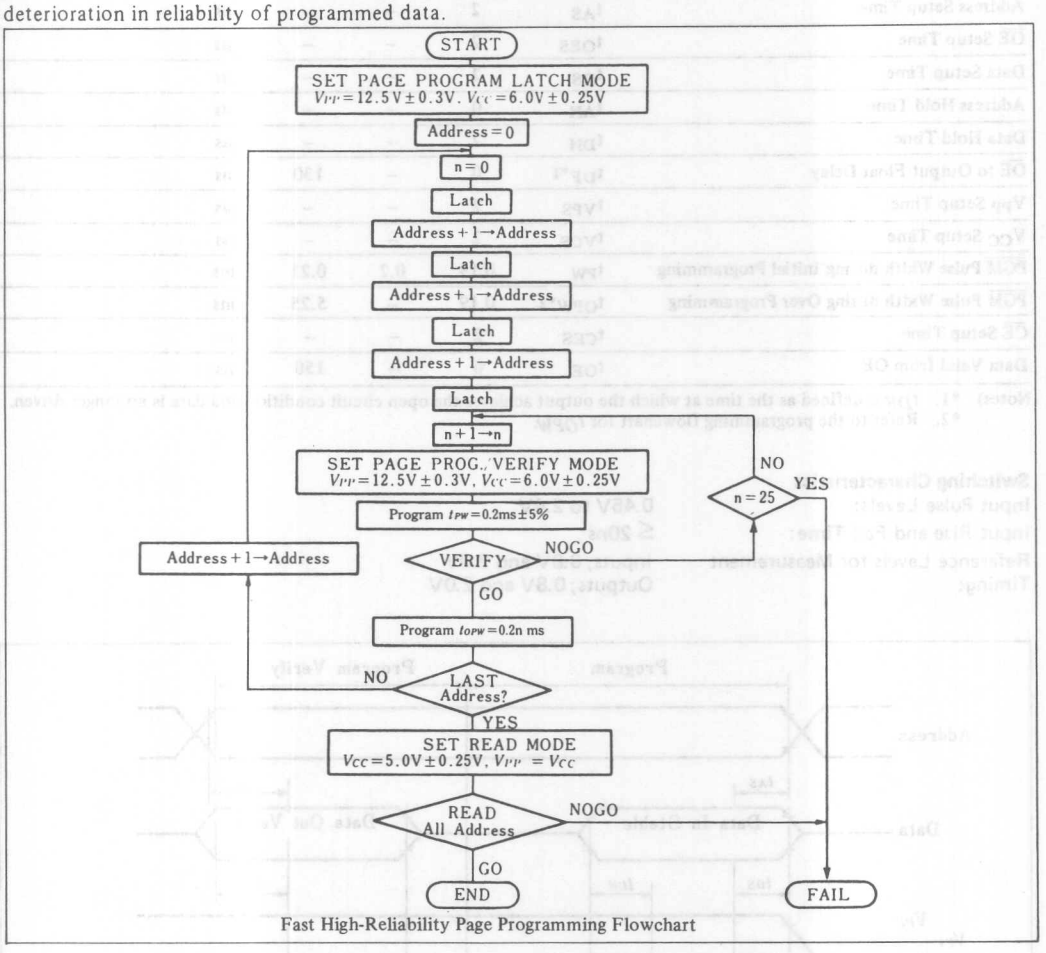
Switching Characteristics

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



Fast High-Reliability Page Programming

This device can be applied the Fast High-Reliability Page Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

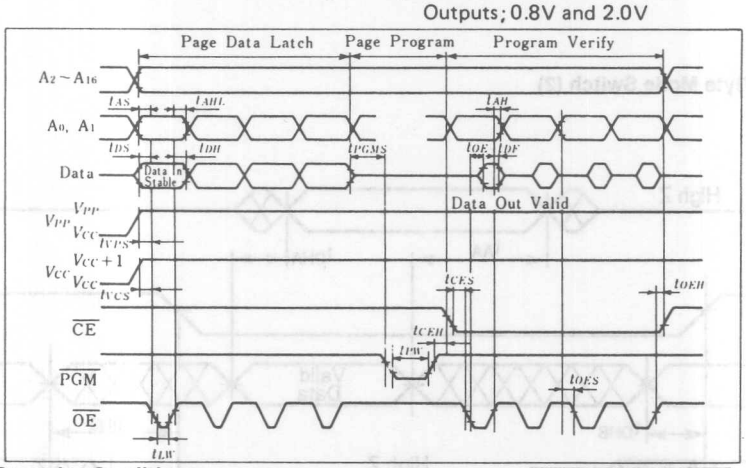
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
	t_{AHL}	2	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from $\overline{OE}$	t_{OE}	0	–	150	ns	
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}	1	–	–	μs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	–	–	μs	
$\overline{CE}$ Hold Time	t_{CEH}	2	–	–	μs	
$\overline{OE}$ Hold Time	t_{OEH}	2	–	–	μs	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

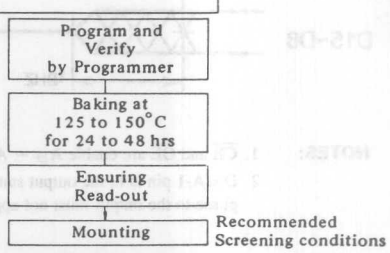
Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



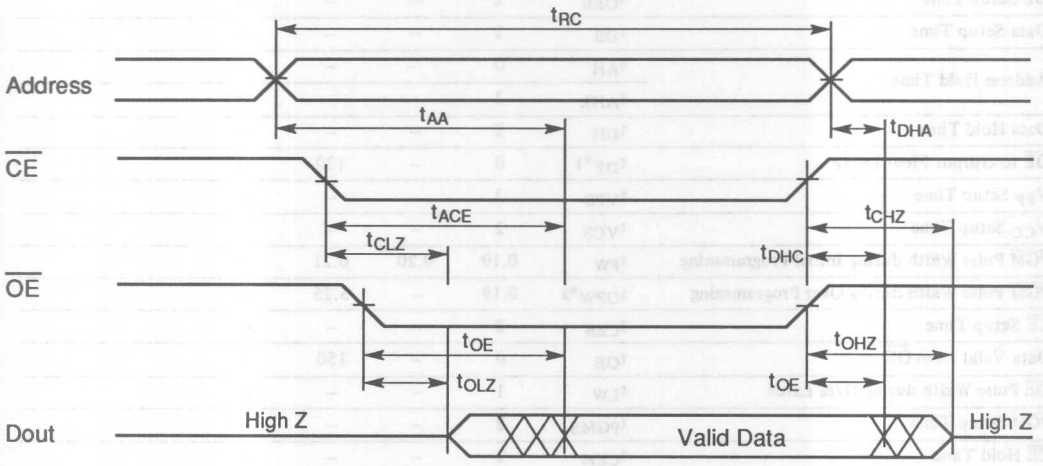
Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



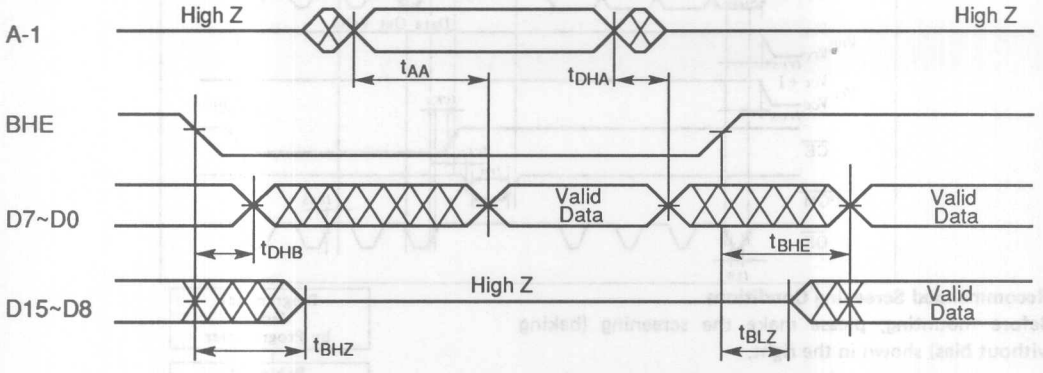
■ TIMING WAVEFORM

• Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}') (1)



NOTES:
1. t_{DHA}, t_{DHC}, t_{DHO}; determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; determined by slower.
3. t_{CLZ}, t_{OLZ}; determined by slower.

• Word Mode, Byte Mode Switch (2)



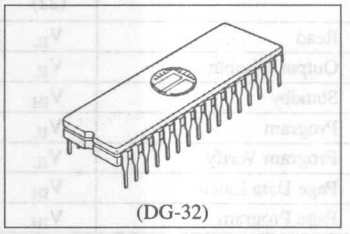
NOTES:
1. $\overline{CE}$ and $\overline{OE}$ are enable $A_{19} \sim A_0$ are valid.
2. D_{15}/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not apply to them.

HN27C101AG Series — Preliminary
CMOS 1Mb EPROM

131,072-Word × 8-Bit CMOS UV Erasable and Programmable ROM

■ DESCRIPTION

The HN27C101AG is a 131,072 word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 32-pin, dual-in-line package with transparent lid. The transparent lid allows the memory content to be erased with ultraviolet light, whereby a new pattern can then be written into the device.



(DG-32)

■ FEATURES

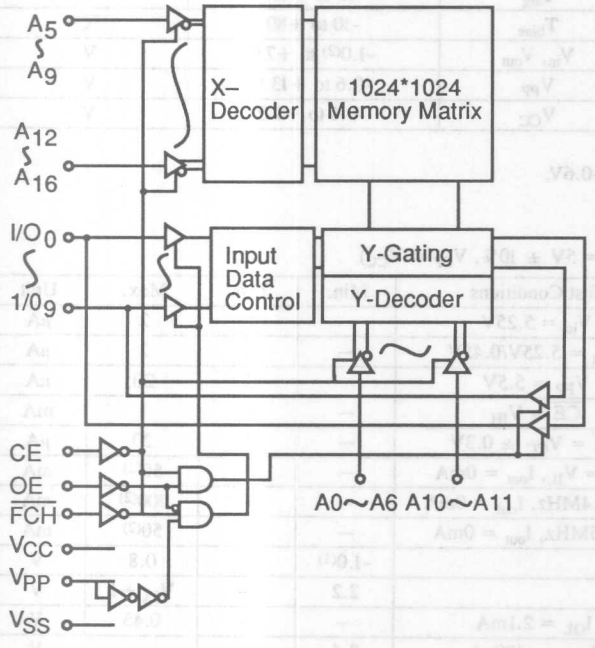
- Single Power Supply . . . . . +5V ±10%
- High Performance Program Mode and High Performance Page Program Mode . . . . . .Program Voltage: +12.5V DC
  High Speed Page Programming: 14 seconds typ.
- Static . . . . . .No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . .100ns max. (HN27C101AG-10)
  120ns max. (HN27C101AG-12)
  150ns max. (HN27C101AG-15)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	A_9 (26)	Outputs (13 ~ 15, 17 ~ 21)
Read		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	D_{out}
Output Disable		V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	X	High Z
Standby		V_{IH}	X	X	V_{CC}	V_{CC}	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	D_{in}
Program Verify		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	D_{out}
Page Data Latch		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	D_{in}
Page Program		V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	High Z
Program Inhibit		V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	X	High Z
		V_{IL}	V_{IH}	V_{IH}				
		V_{IH}	V_{IL}	V_{IL}				
		V_{IH}	V_{IH}	V_{IH}				
Identifier		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_H	Code

NOTE: 1. X = Don't Care.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages(1)	V_{in}, V_{out}	−1.0(2) to +7.0	V
V_{PP} Voltage(1)	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage(1)	V_{CC}	−0.6 to +7.0	V

NOTES: 1. With respect to GND.
2. Pulse width: 50ns, DC: V_{IL} min. = −0.6V.

■ READ OPERATION

• **DC Characteristics** (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.25V	—	—	2	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	—	—	2	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5V	—	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$ = V_{IH}	—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{CC} ± 0.3V	—	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{out} = 0mA	—	—	50(2)	mA
	I_{CC2}	f = 8.4MHz, I_{out} = 0mA	—	—	100(2)	mA
	I_{CC3}	f = 5MHz, I_{out} = 0mA	—	—	50(2)	mA
Input Low Voltage	V_{IL}		−1.0(1)	—	0.8	V
Input High Voltage	V_{IH}		2.2	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	—	—	V

NOTES: 1. Pulse width: 50ns, DC: V_{IL} min. = −0.3V.
2. Tentative.

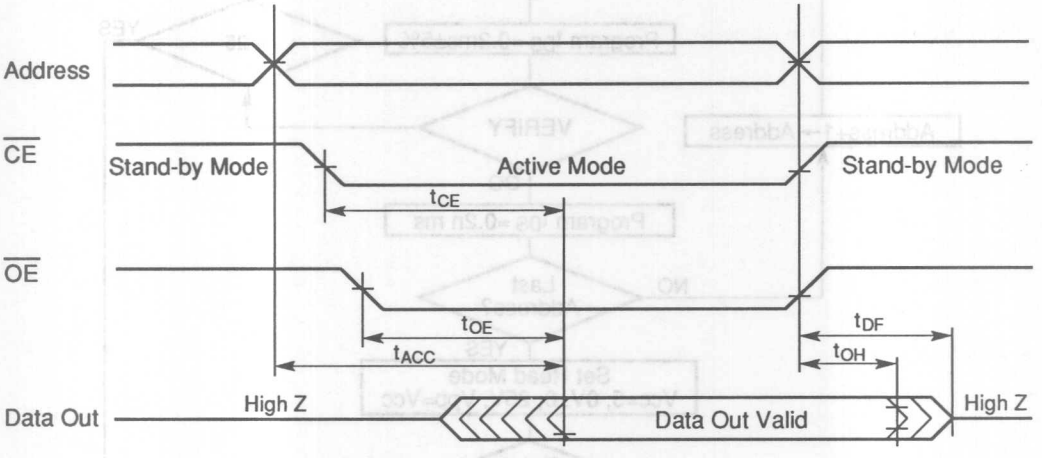
■ AC CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditons	HN27C101AG						Unit
			-10		-12		-15		
			Min.	Max.	Min.	Max.	Min.	Max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	—	100	—	120	—	150	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	—	100	—	120	—	150	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	60	10	60	10	70	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	50	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	—	0	—	0	—	ns

NOTE: t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

■ SWITCHING CHARACTERISTICS

- **Test Conditions**
  - Input Pulse Levels: 0.45V to 2.4V
  - Reference Levels for Measuring Timing; Inputs: 0.8V, 2.0V
    Outputs: 0.8V, 2.0V
  - Input Rise and Fall Time: ≤ 20ns
  - Output Load: 1 TTL Gate + 100pF

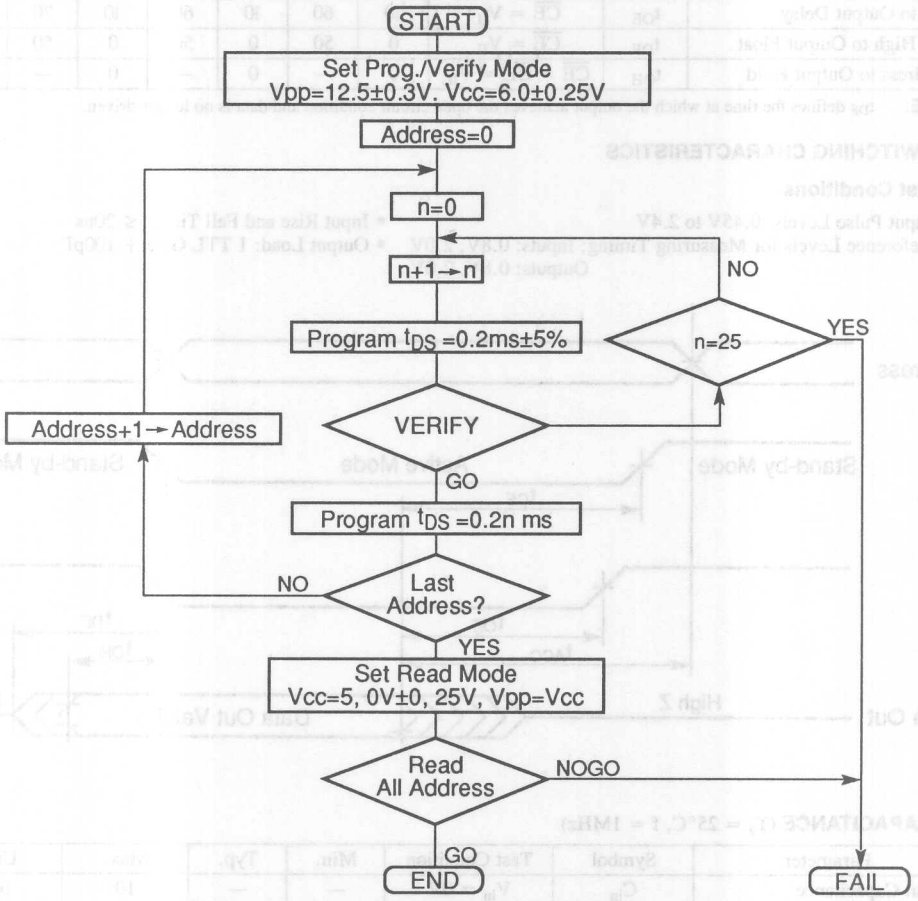


■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	—	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	—	15	pF

High Performance Programming

This device can be applied the High Performance Programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage strəss to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC Programming Characteristics (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 6.25V/0.45V	—	—	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = –400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC}		—	—	30	mA
Input Low Level	V_{IL}		–0.1	—	0.8	V
Input High Level	V_{IH}		2.2	—	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	—	—	40	mA

NOTES: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.

■ AC PROGRAMMING CHARACTERISTICS (High Performance Programming)

(T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

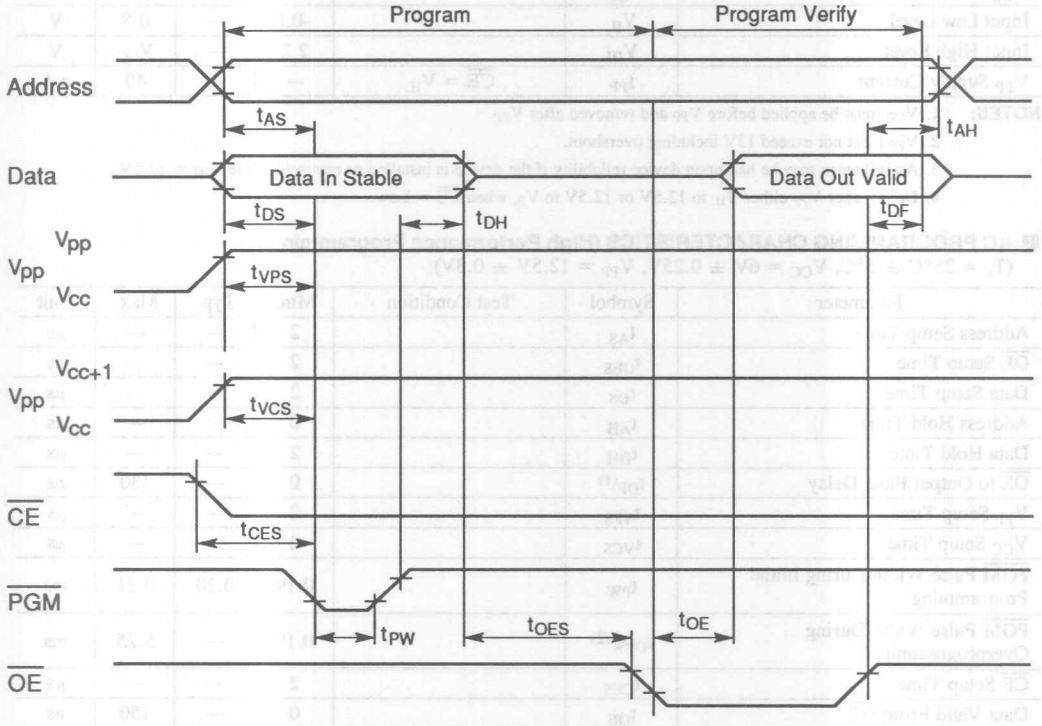
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}(1)		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Initial Programming	t_{PW}		0.19	0.20	0.21	ms
$\overline{PGM}$ Pulse Width During Overprogramming	t_{OPW}(2)		0.19	—	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid From $\overline{OE}$	t_{OE}		0	—	150	ns

NOTES: 1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
2. t_{OPW} is defined as mentioned in flowchart.

■ SWITCHING CHARACTERISTICS

• Test Conditions

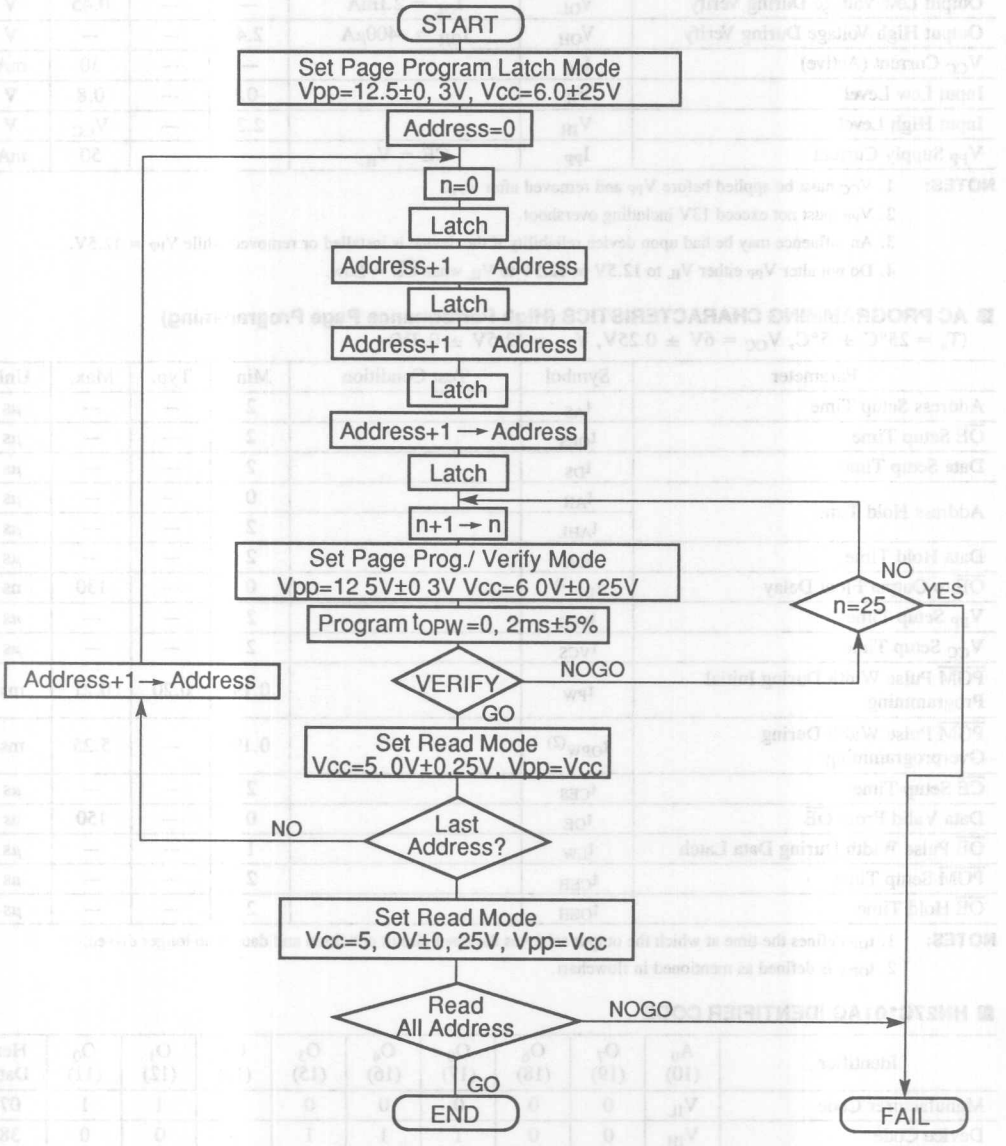
- Input Pulse Levels: 0.45V to 2.4V
- Reference Levels for Measuring Timing; Inputs: 0.8V, 2.0V
  Outputs: 0.8V, 2.0V
- Input Rise and Fall Time: ≤ 20ns



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High Performance Page Programming

This device can be applied the High Performance Programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

■ HIGH PERFORMANCE PAGE PROGRAMMING OPERATION

• DC Programming Characteristics (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 6.25V/0.45V	—	—	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = –400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC}		—	—	30	mA
Input Low Level	V_{IL}		–0.1	—	0.8	V
Input High Level	V_{IH}		2.2	—	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	—	—	50	mA

NOTES: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.

■ AC PROGRAMMING CHARACTERISTICS (High Performance Page Programming)

(T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
	t_{AHL}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}(1)		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Initial Programming	t_{PW}		0.19	0.20	0.21	ms
$\overline{PGM}$ Pulse Width During Overprogramming	t_{OPW}(2)		0.19	—	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid From $\overline{OE}$	t_{OE}		0	—	150	ns
$\overline{OE}$ Pulse Width During Data Latch	t_{LW}		1	—	—	μs
$\overline{PGM}$ Setup Time	t_{CEH}		2	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	—	—	μs

NOTES: 1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
2. t_{OPW} is defined as mentioned in flowchart.

■ HN27C101AG IDENTIFIER CODE

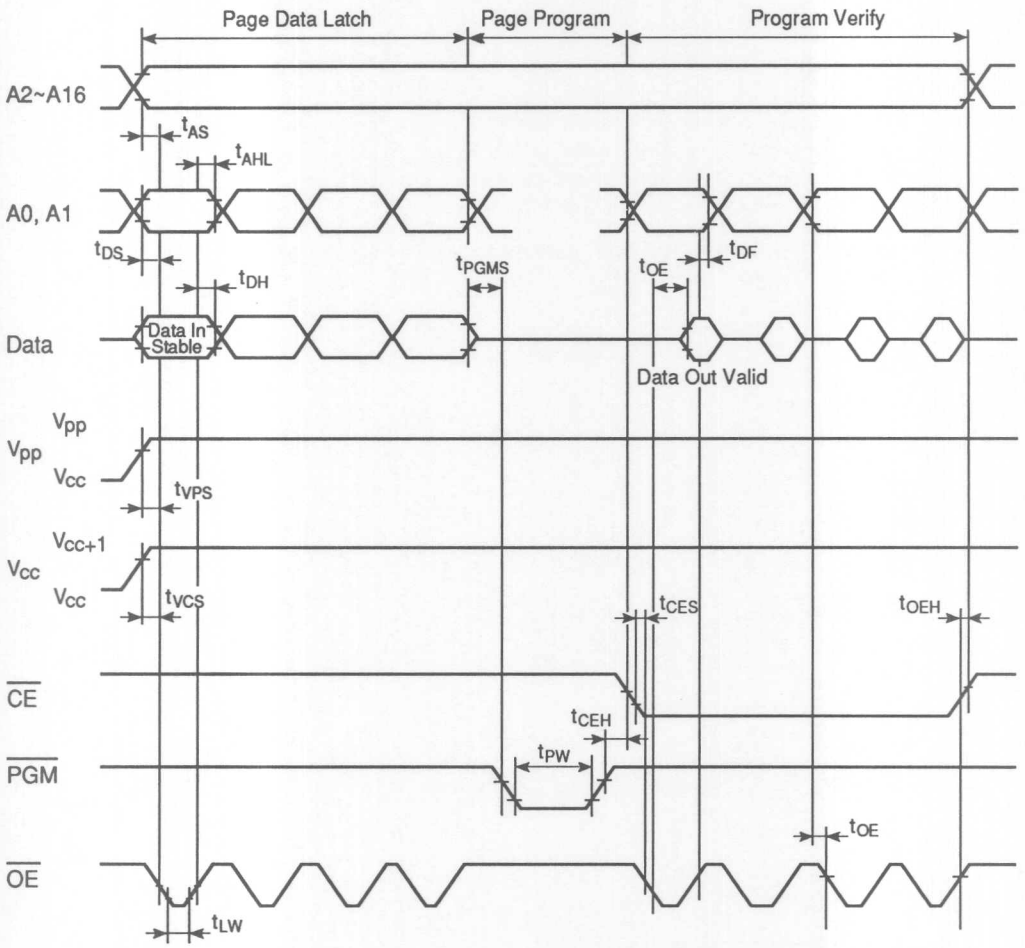
Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	1	0	0	0	38

NOTES: 1. A_9 = 12.0V ± 0.5V
2. A_1–A_8, A_{10}–A_1, $\overline{CE}$, $\overline{OE}$ = V_{IL}

■ SWITCHING CHARACTERISTICS

• Test Conditions

- Input Pulse Levels: 0.45V to 2.4V
- Input Rise and Fall Time: ≤ 20ns
- Reference Levels for Measuring Timing; Inputs: 0.8V, 2.0V
  Outputs: 0.8V, 2.0V

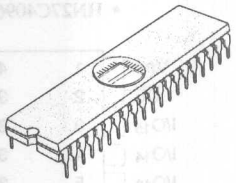


HN27C4096 Series — Preliminary

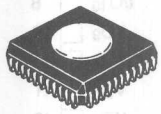
262,144-Word × 16-Bit CMOS UV Erasable and Programmable ROM

■ DESCRIPTION

The Hitachi HN27C4096G/CC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4096 makes high speed access time possible. Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 80286 and 68020. The HN27C4096 offers high speed programming using page programming mode. This device has the package variation of cerdip-40 pin and JLCC-44 pin.



(DG-40A)



(CC-44)

■ FEATURES

- High Speed
  - Access Time . . . . . .100/120/150ns (max.)
- Low Power Dissipation
  - Standby Mode . . . . . .5μW (typ.)
  - Active Mode . . . . . .35mW/MHz (typ.)
- Fast High Reliability Page Programming and Fast High Reliability Programming
  - Programming Voltage . . . . . + 12.5V D.C.
  - Program Time. . . . . .7 sec. (min.)
  - (Theoretical in Page Programming)
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Pin Arrangement . . . . . .40-Pin JEDEC Standard
  - 44-Pin JLCC JEDEC Standard
- Device Identifier Mode . . . .Manufacturer Code and Device Code

■ PIN DESCRIPTION

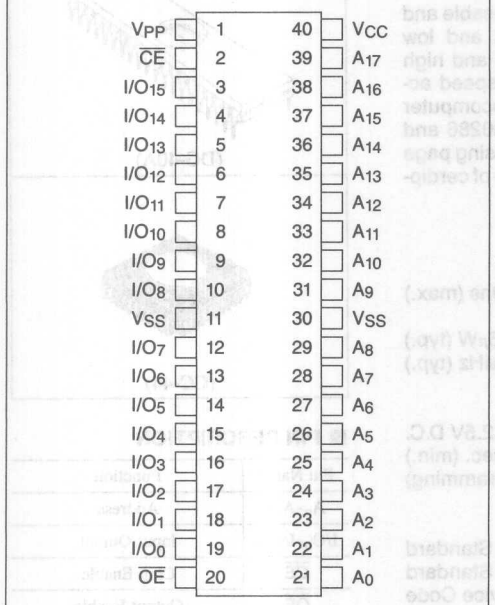
Pin Name	Function
A_0–A_{17}	Address
I/O_0–I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Power Supply
V_{SS}	Ground

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096G-10 HN27C4096G-12 HN27C4096G-15	100ns 120ns 150ns	600 mil 40 pin Cerdip (DG-40A)
HN27C4096CC-10 HN27C4096CC-12 HN27C4096CC-15	100ns 120ns 150ns	44 pin JLCC (CC-44)

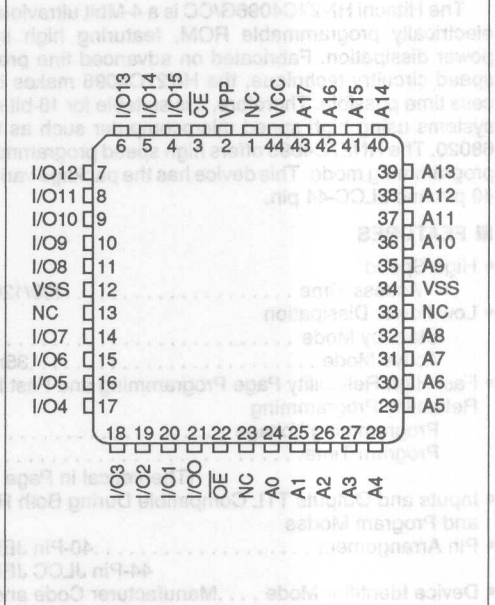
■ PIN ARRANGEMENT

• HN27C4096G



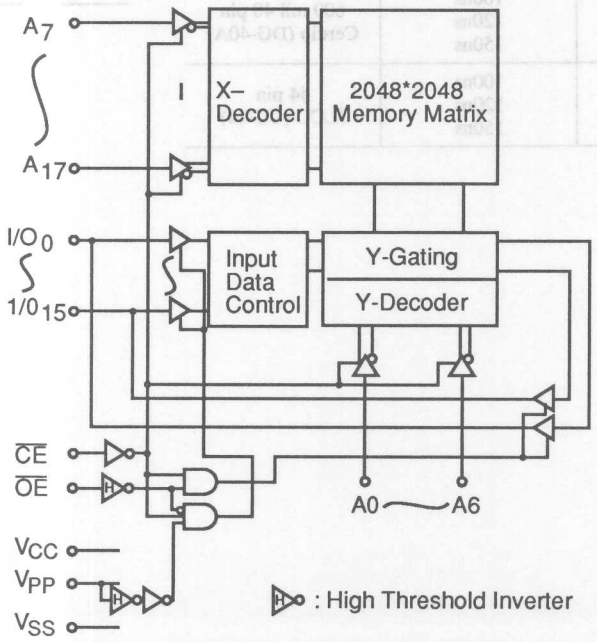
(Top View)

• HN27C4096CC



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode		Pin	$\overline{CE}$	$\overline{OE}$	A_9	V_{PP}	V_{CC}	I/O
		CC-44	(3)	(22)	(35)	(2)	(44)	(4–11, 14–21)
		DG-40A	(2)	(20)	(31)	(1)	(40)	(3–10, 12–19)
Read			V_{IL}	V_{IL}	X	V_{SS}–V_{CC}	V_{CC}	D_{out}
Output Disable			V_{IL}	V_{IH}	X	V_{SS}–V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	V_{SS}–V_{CC}	V_{CC}	High Z
Page Prog.	Page Program Set		V_{IH}	V_H(2)	X	V_{PP}	V_{CC}	High Z
	Page Data Latch		V_{IL}	V_H(2)	X	V_{PP}	V_{CC}	D_{in}
	Page Program		V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	High Z
	Page Program Verify		V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{out}
	Page Program Reset		V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Word Prog.	Program		V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{in}
	Program Verify		V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{out}
	Optional Verify		V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{out}
	Program Inhibit		V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier			V_{IL}	V_{IL}	V_H(2)	V_{SS}–V_{CC}	V_{CC}	Code

NOTES: 1. X = Don't Care.
2. V_H = 12.0V ± 0.5V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages(1)	V_{in}, V_{out}	–0.6(2) to +7.0	V
Voltage on Pin A_9 and $\overline{OE}$	V_{ID}	–6.0(2) to +13.0	V
V_{PP} Voltage(1)	V_{PP}	–0.6 to +13.5	V
V_{CC} Voltage(1)	V_{CC}	–0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range(3)	T_{stg}	–65 to +125	°C
Storage Temperature Under Bias	T_{bias}	–20 to +80	°C

NOTES: 1. Relative to V_{SS}.
2. V_{in}, V_{out}, V_{ID}, min. = –2.0V for pulse width ≤ 20ns.
3. Storage temperature range of device before programming.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	—	12	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	—	20	pF

■ READ OPERATION

• DC Characteristics (V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.5V	—	—	2	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5V/0.45V	—	—	2	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5V	—	1	20	μA
Standby V_{CC} Current	I_{SB1}	$\overline{CE}$ = V_{IH}	—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{CC} ± 0.3V	—	1	20	μA
Operating V_{CC} Current	I_{CC1}	I_{out} = 0mA, f = 1MHz	—	—	30	mA
	I_{CC2}	I_{out} = 0mA, f = 10MHz	—	1	100	mA
Input Voltage	V_{IL}		−0.3[1]	—	0.8	V
	V_{IH}		2.2	—	V_{CC}+1[2]	V
Output Voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V
	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V

NOTES: 1. V_{IL} min. = −1.0V for pulse width ≤ 50ns.
V_{IL} min. −2.0V for pulse width ≤ 20ns.
2. V_{IH} max. = V_{CC} + 1.5V for pulse width ≤ 20ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to +70°C)

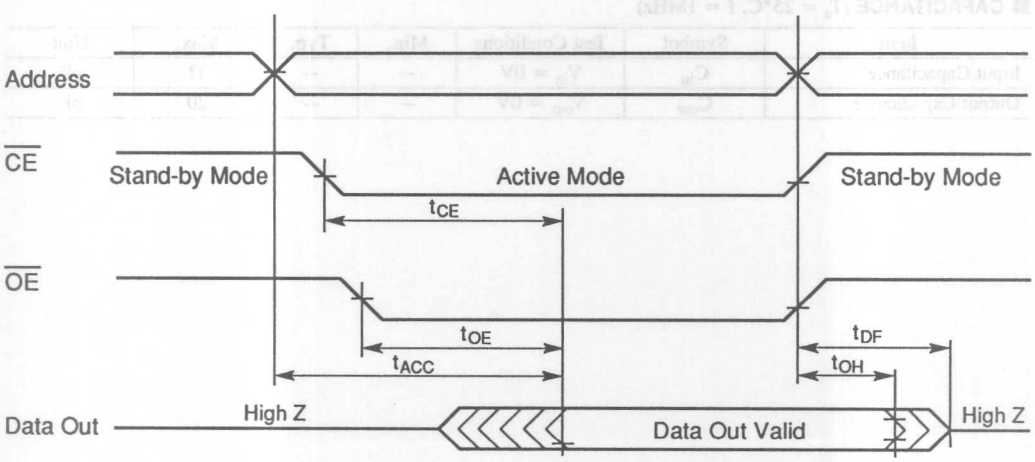
• Test Conditions

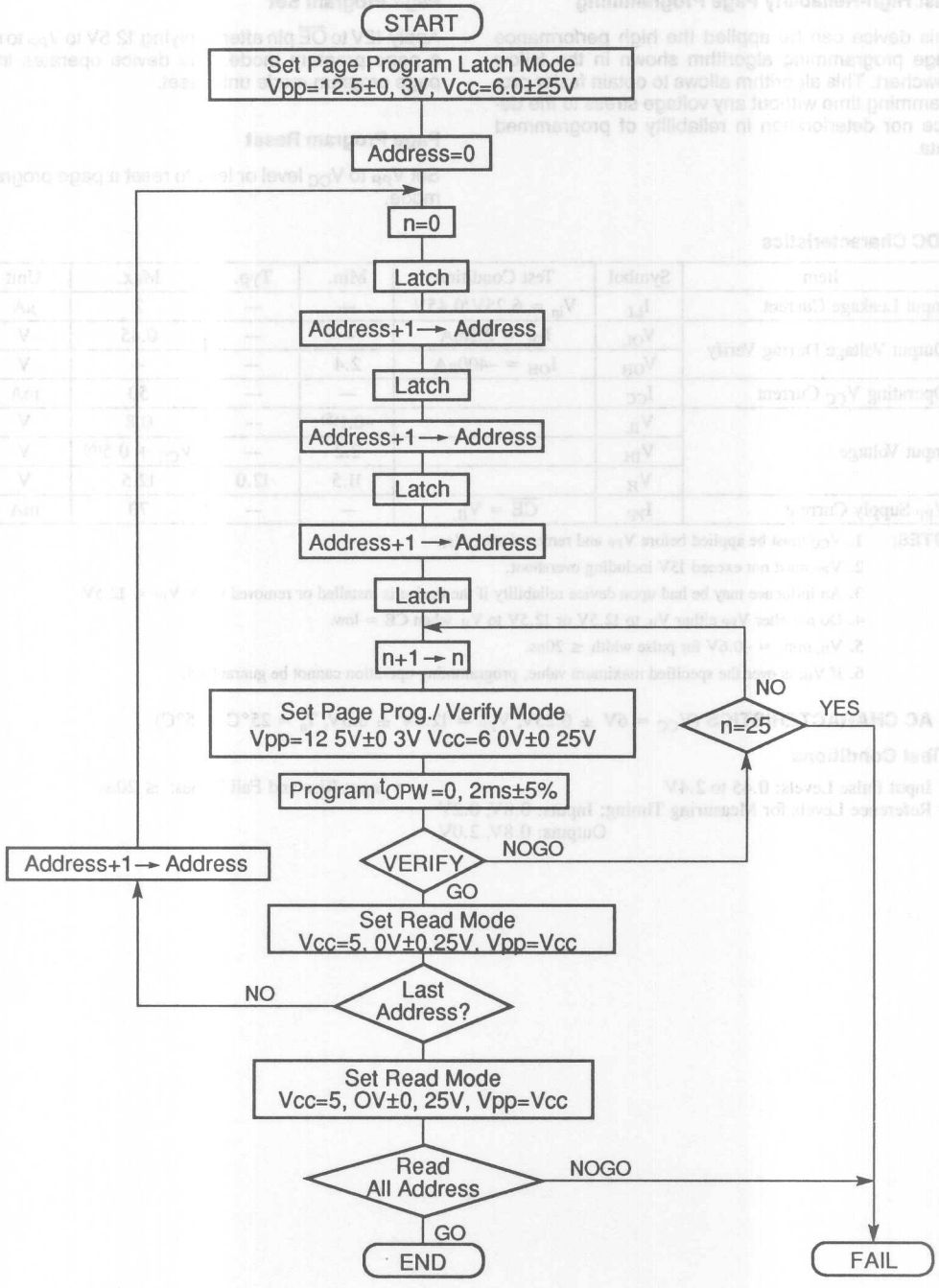
- Input Pulse Levels: 0.45 to 2.4V
- Reference Levels for Measuring Timing: 0.8V, 0.2V
- Input Rise and Fall Times: ≤ 10ns
- Output Load: 1 TTL Gate + 100pF

Item	Symbol	Test Conditions	HN27C4096-10		HN27C4096-12		HN27C4096-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	—	100	—	120	—	150	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	—	100	—	120	—	150	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	—	60	—	60	—	70	ns
$\overline{OE}$ High to Output Float[1]	t_{DF}	$\overline{CE}$ = V_{IL}	0	35	0	40	0	50	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	5	—	5	—	5	—	ns

NOTE: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

• Read Timing Waveform





Fast High-Reliability Page Programming Flowchart

Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in the follow flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

Page Program Set

Apply 12V to $\overline{OE}$ pin after applying 12.5V to V_{PP} to set a page program mode. The device operates in a page program mode until reset.

Page Program Reset

Set V_{PP} to V_{CC} level or less to reset a page program mode.

• DC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 6.25V/0.45V	—	—	2	μA
Output Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V
	V_{OH}	I_{OH} = –400μA	2.4	—	—	V
Operating V_{CC} Current	I_{CC}		—	—	50	mA
Input Voltage	V_{IL}		–0.1(5)	—	0.8	V
	V_{IH}		2.2	—	V_{CC} + 0.5(6)	V
	V_H		11.5	12.0	12.5	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	—	—	70	mA

NOTES:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min. = –0.6V for pulse width ≤ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

■ AC CHARACTERISTICS (V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V, T_a = 25°C ± 5°C)

• Test Conditions

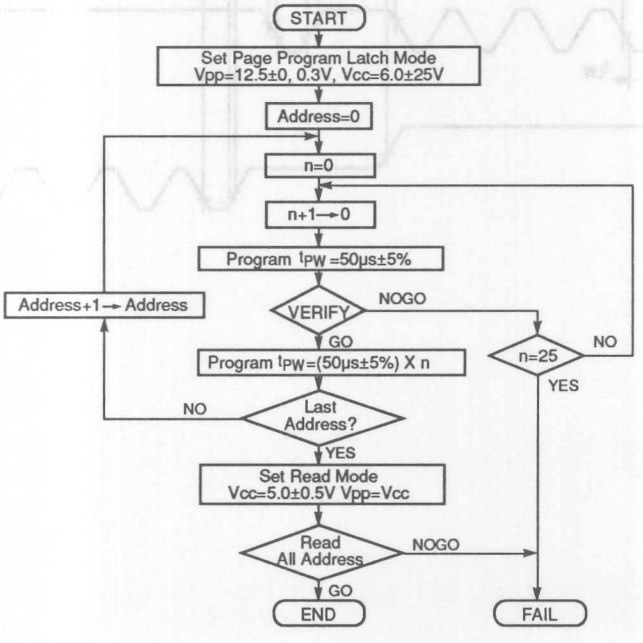
- Input Pulse Levels: 0.45 to 2.4V
- Input Rise and Fall Times: ≤ 20ns
- Reference Levels for Measuring Timing; Inputs: 0.8V, 2.0V
  Outputs: 0.8V, 2.0V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ High to Output Float Delay	t_{DF}(1)		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{CE}$ Initial Programming Pulse Width	t_{PW}		47.5	50.0	52.5	μs
$\overline{CE}$ Overprogramming Pulse Width	t_{OPW}(2)		47.5	—	525.0	μs
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid From $\overline{OE}$	t_{OE}		0	—	150	ns
$\overline{CE}$ Pulse Width During Data Latch	t_{LW}		1	—	—	μs
$\overline{OE}$ = V_H Setup Time	t_{OHS}		2	—	—	μs
$\overline{OE}$ = V_H Hold Time	t_{OHH}		2	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	—	—	μs
V_{PP} Hold Time(3)	t_{VRS}		1	—	—	μs

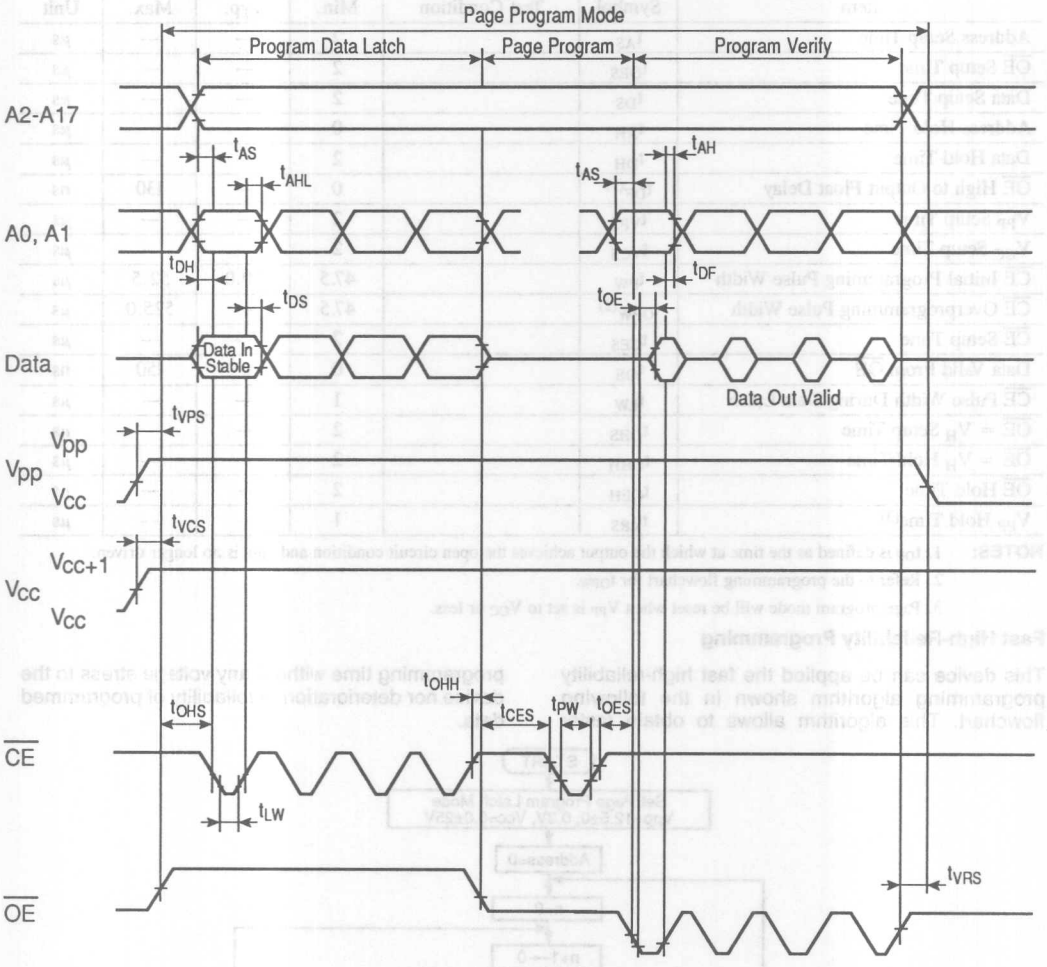
NOTES: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.
3. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart



Fast High-Reliability Page Programming Timing Waveform

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Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

• **DC Characteristics** (V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V, T_a = 25°C ± 5°C)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.5V/0.45V	—	—	2	μA
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	—	—	40	mA
Operating V_{CC} Current	I_{CC}		—	—	50	mA
Input Voltage	V_{IL}		-0.1[5]	—	0.8	V
	V_{IH}		2.2	—	V_{CC}+0.5[6]	V
Output Voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V
	V_{OH}	I_{OH} = -400 μA	2.4	—	—	V

NOTES: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_H, when $\overline{CE}$ = low.
5. V_{IL} min. = -0.6V for pulse width ≤ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

■ **AC CHARACTERISTICS** (V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V, T_a = 25°C ± 5°C)

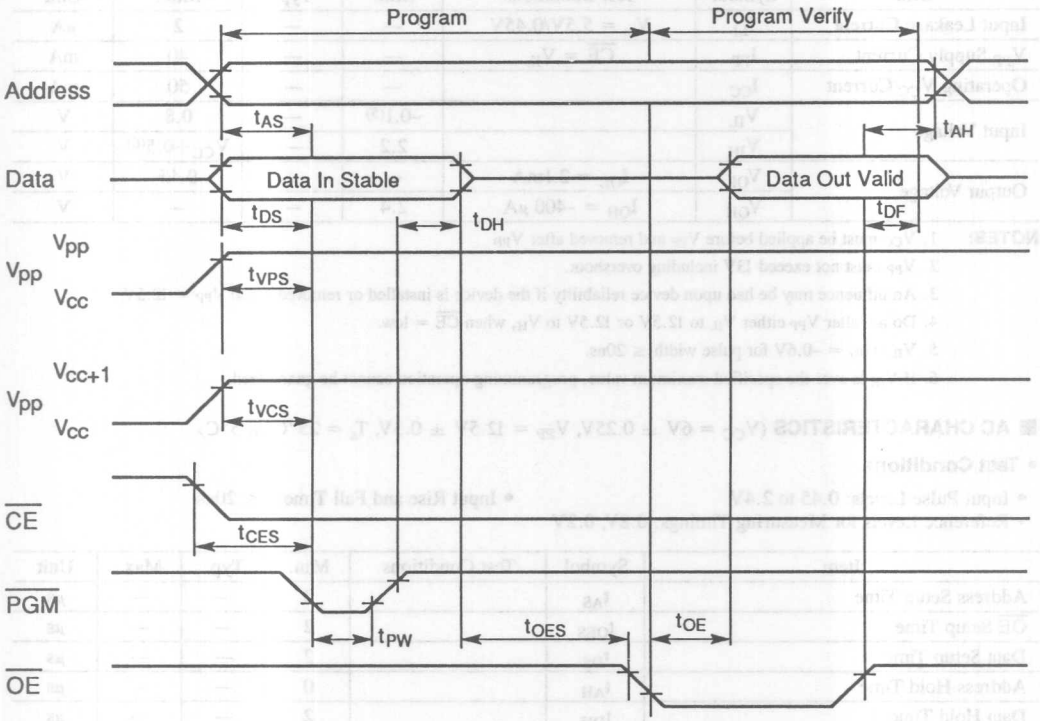
• **Test Conditions**

- Input Pulse Levels: 0.45 to 2.4V
- Input Rise and Fall Times: ≤ 20ns
- Reference Levels for Measuring Timings: 0.8V, 0.2V

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Flow at Delay	t_{DF}[1]		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{CE}$ Initial Programming Pulse Width	t_{PW}		4.75	50.0	52.5	μs
$\overline{CE}$ Overprogramming Pulse Width	t_{OPW}[2]		47.5	—	525.0	μs
Data Valid From $\overline{OE}$	t_{OE}		0	—	150	ns

NOTES: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

• **Fast High-Reliability Programming Timing Waveform**



Erase

Erasure of HN27C4096G/C is performed by exposure to ultraviolet light of 2537 A and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e., UV intensity × exposure time) for erasure is 15 sec/cm².

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

• **HN27C4096 Identifier Code**

Identifier		A_0	I/O_8–I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
	CC-44	(24)	(11)–(4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	
	DG-40A	(21)	(10)–(3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	
Manufacture Code		V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code		V_{IH}	X	1	0	1	0	0	0	1	0	A2

NOTES: 1. X = Don't Care.
2. V_H = 12.0V ± 0.5V

Section 9
ECL RAM

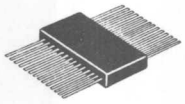
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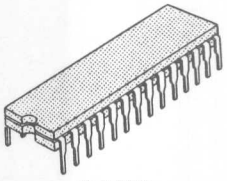
HM10494 Series — Preliminary

16384-word × 4-bit Fully Decoded Random Access Memory

The HM10494 is ECL 10K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.



(FG-28D)



(DG-28N)

Features

- 16384-word × 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 800 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

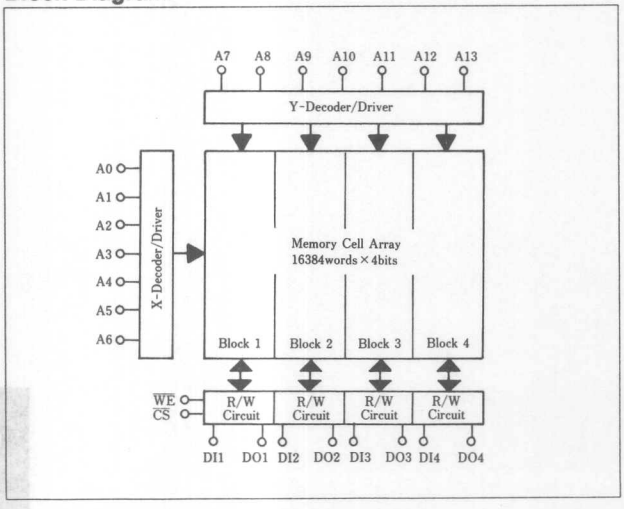
Type No.	Access Time	Package
HM10494-10	10 ns	400 mil 28 pin Cerdip
HM10494-12	12 ns	(DG-28N)
HM10494F-10	10 ns	28 pin Ceramic Flat
HM10494F-12	12 ns	(FG-28D)

Function Table

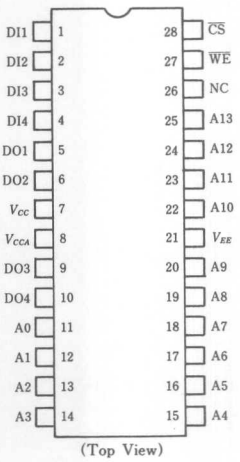
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to –7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	–30	mA
Storage Temperature	Tstg	–65 to +150	°C
Storage Temperature	Tstg (Bias)*1	–55 to +125	°C

Note: *1; Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = –5.2V, R_L = 50Ω to –2.0 V, Ta = 0 to +75°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions	
Output Voltage	V_{OH}	–1000	—	–840	mV	Vin = V_{IHA} or V_{ILB}	0°C
		–960	—	–810			+25°C
		–900	—	–720			+75°C
	V_{OL}	–1870	—	–1665			0°C
		–1850	—	–1650			+25°C
		–1830	—	–1625			+75°C
Output Threshold Voltage	V_{OHC}	–1020	—	—	mV	Vin = V_{IHB} or V_{ILA}	0°C
		–980	—	—			+25°C
		–920	—	—			+75°C
	V_{OLC}	—	—	–1645			0°C
		—	—	–1630			+25°C
		—	—	–1605			+75°C
Input Voltage	V_{IH}	–1145	—	–840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		–1105	—	–810			+25°C
		–1045	—	–720			+75°C
	V_{IL}	–1870	—	–1490		Guaranteed Input Voltage Low for All Inputs	0°C
		–1850	—	–1475			+25°C
		–1830	—	–1450			+75°C
Input Current	I_{IH}	—	—	220	μA	Vin = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		Vin = V_{ILB} $\overline{CS}$	0 to +75°C
		–50	—	—		Vin = V_{ILB} Others	0 to +75°C
Supply Current	I_{EE}	–180	—	—	mA	All Inputs and Outputs Open	Ta = 0°C
		–180	—	—			Ta = 75°C

AC Characteristics (V_{EE} = –5.2 V ± 5%, Ta = 0 to +75°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	t_W	6	—	—	8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	$t_W = t_W$ min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

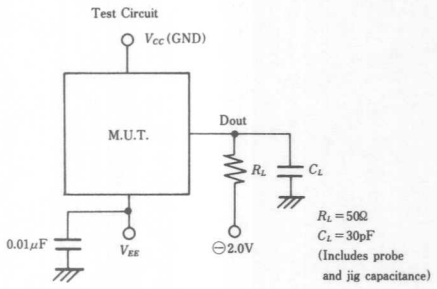
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

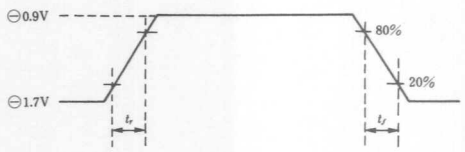
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

Loading Condition

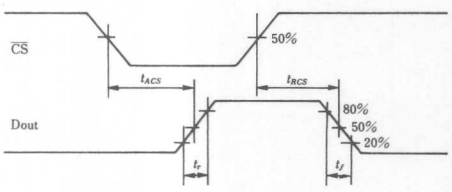


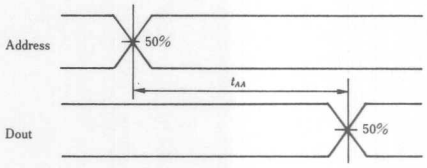
Input Pulse



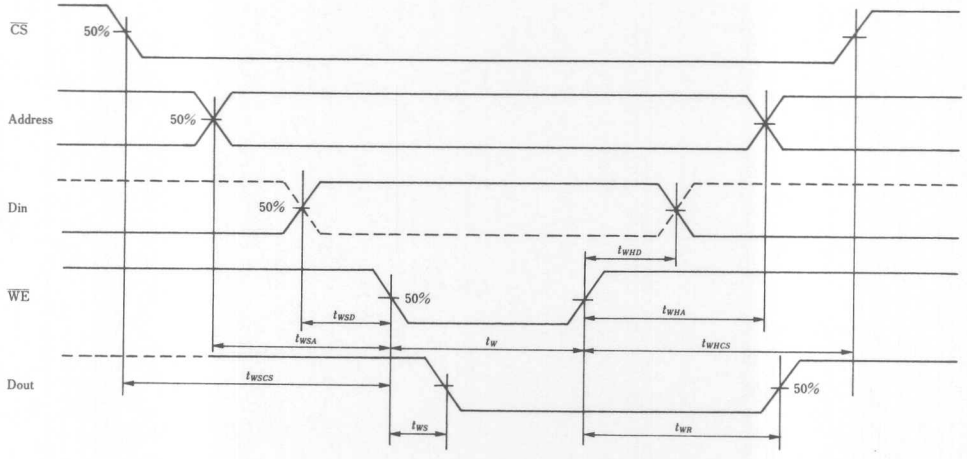
$t_r = t_f = 2.0$ns typ.

Read Mode





Write Mode



HM10490 Series — Preliminary

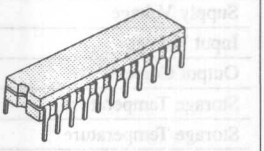
65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM10490 is ECL 10K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

- 65536 × 1 Bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .6/8ns (min.)
- Low Power Dissipation . . . . . .570mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

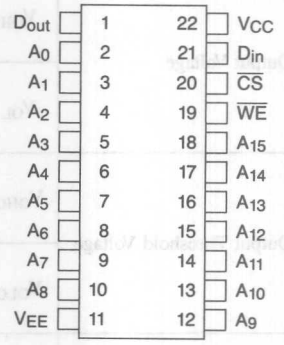


(DG-22N)

■ ORDERING INFORMATION

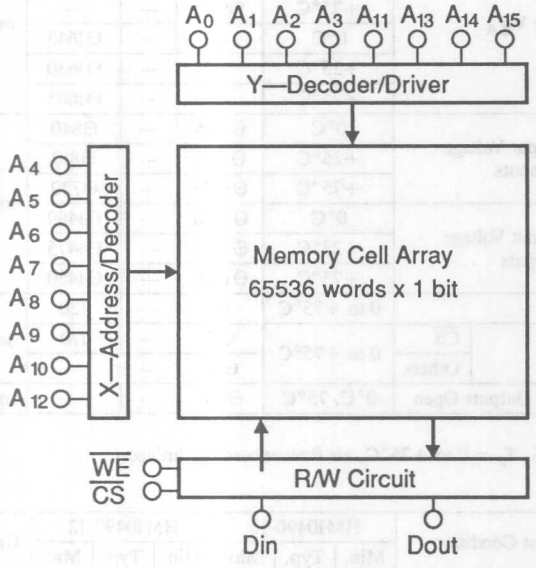
Type No.	Access Time	Package
HM10490-10	10ns	300 mil 22 pin Cerdip (DG-22N)
HM10490-12	12ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$*	Θ55 to +125	°C

NOTE: * = Under bias.

■ DC CHARACTERISTICS (V_{EE} = Θ5.2V, R_L = 50Ω to Θ2.0V, T_a = 0 to +75°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}	0°C	Θ1000	—	Θ840	mV
			+25°C	Θ960	—	Θ810	
			+75°C	Θ900	—	Θ720	
	V_{OL}		0°C	Θ1870	—	Θ1665	
			+25°C	Θ1850	—	Θ1650	
			+75°C	Θ1830	—	Θ1625	
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}	0°C	Θ1020	—	—	mV
			+25°C	Θ980	—	—	
			+75°C	Θ920	—	—	
	V_{OLC}		0°C	—	—	Θ1645	
			+25°C	—	—	Θ1630	
			+75°C	—	—	Θ1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	Θ1145	—	Θ840	mV
			+25°C	Θ1105	—	Θ810	
			+75°C	Θ1045	—	Θ720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	Θ1870	—	Θ1490	
			+25°C	Θ1850	—	Θ1475	
			+75°C	Θ1830	—	Θ1450	
Input Current	I_{IH}	V_{in} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0 to +75°C	0.5	—	170
			Others		Θ50	—	—
Supply Current	I_{EE}	All Inputs and Outputs Open	0°C, 75°C	Θ140	—	—	mA

■ AC CHARACTERISTICS (V_{EE} = Θ5.2V ± 5%, T_a = 0 to +75°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM10490-10			HM10490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Write Pulse Width	t_W	$t_{WSA} = t_{WSA}$ min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

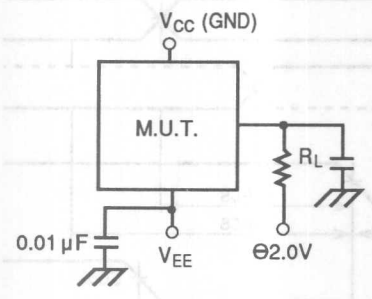
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

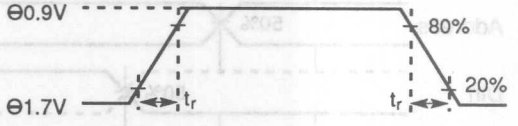
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

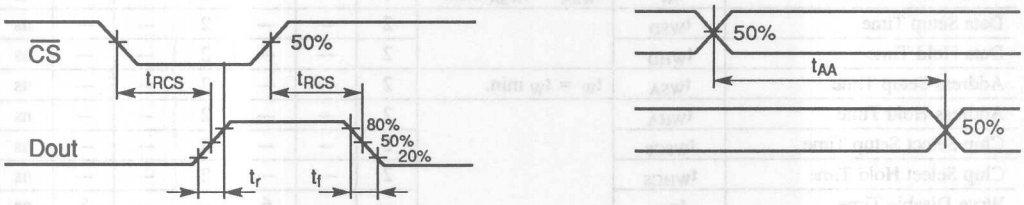
1. Loading Condition



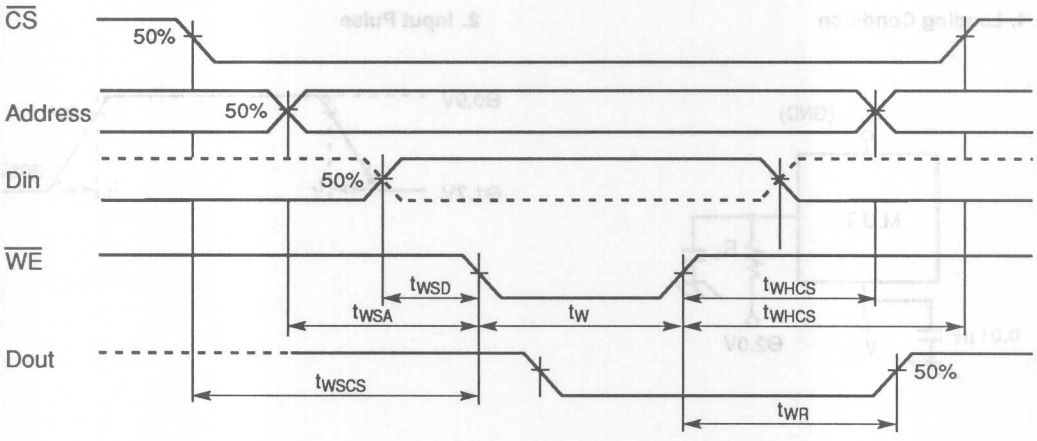
2. Input Pulse



3. Read Mode



4. Write Mode



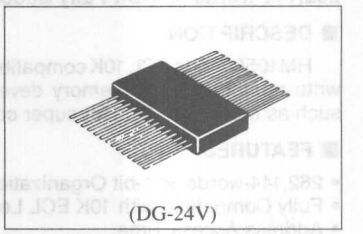
HITACHI
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HM10504-10/12 — Preliminary

65536-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM10504 is ECL 10K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

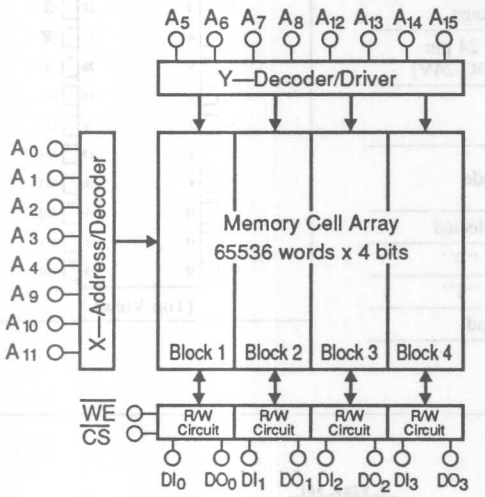


(DG-24V)

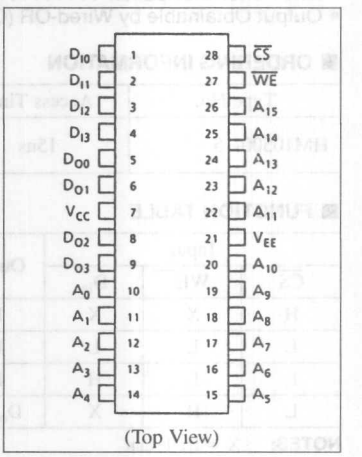
■ FEATURES

- 65536 × 4 Bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .8ns (min.)
- Low Power Dissipation . . . . . .620mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM10504-10	10 ns	300 mil 28 pin Cerdip (DG-24V)
HM10504-12	12 ns	

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

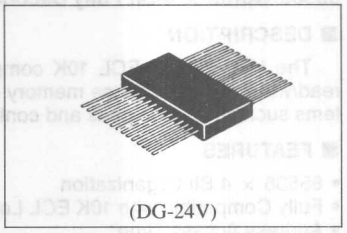
NOTES: X = Irrelevant;
* = Read out noninvert

■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{15}	Address Input
D_{I0}-D_{I3}	Data Input
D_{O0}-D_{O3}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

HM10500-15 — Preliminary

262,144 Words × 1-Bit Fully Decoded Random Access Memory



(DG-24V)

■ DESCRIPTION

HM10500-15 is ECL 10K compatible, 262,144-words × 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

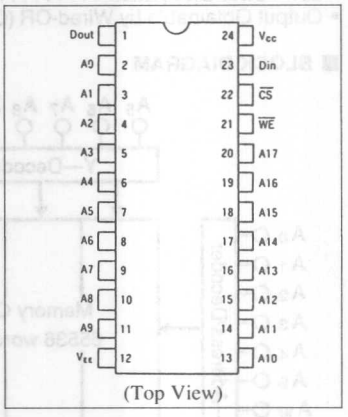
■ FEATURES

- 262,144-words × 1-bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time . . . . . .15ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .520mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM10500-15	15ns	300 mil 24 pin Cerdip (DG-24V)

■ PIN ARRANGEMENT



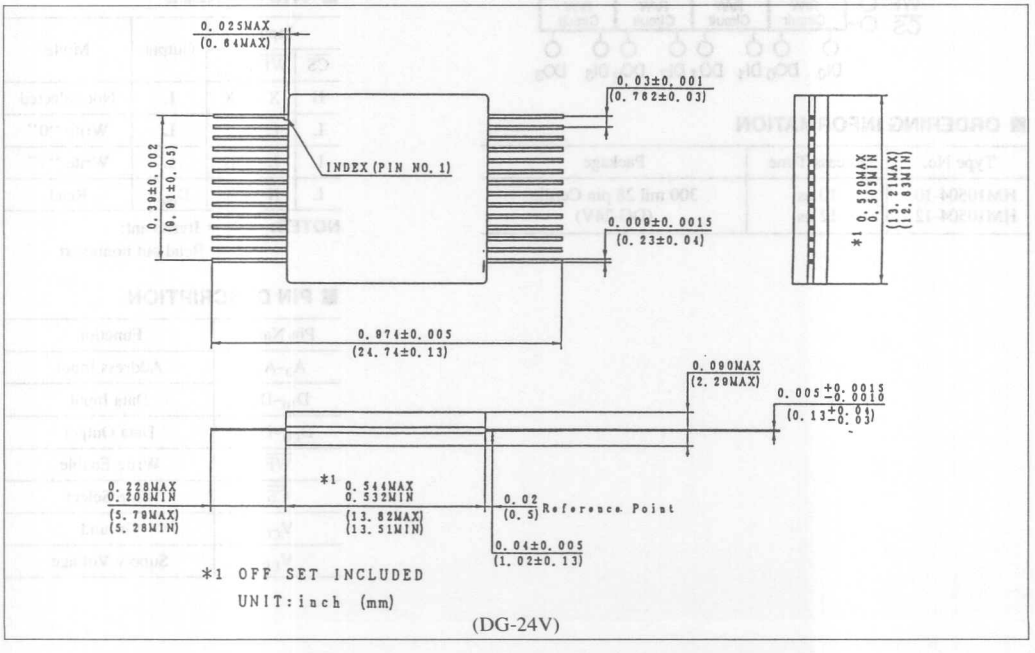
(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*1	Read

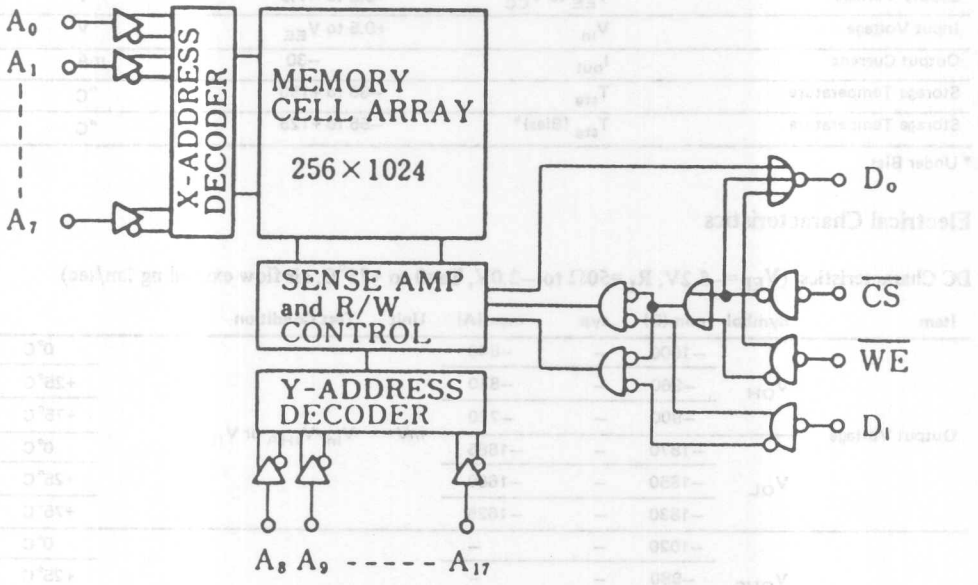
NOTES: X = Irrelevant

*1 = Read Out Noninvert



(DG-24V)

■ BLOCK DIAGRAM



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{In}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

Electrical Characteristics

DC Characteristics (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min (B)	typ	max (A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	–	−840	mV	V_{in}=V_{IHA} or V_{ILB}	0°C
		−960	–	−810			+25°C
		−900	–	−720			+75°C
	V_{OL}	−1870	–	−1665			0°C
		−1850	–	−1650			+25°C
		−1830	–	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	–	–	mV	V_{in}=V_{IHB} or V_{ILA}	0°C
		−980	–	–			+25°C
		−920	–	–			+75°C
	V_{OLC}	–	–	−1645			0°C
		–	–	−1630			+25°C
		–	–	−1605			+75°C
Input Voltage	V_{IH}	−1145	–	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	–	−810			+25°C
		−1045	–	−720			+75°C
	V_{IL}	−1870	–	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	–	−1475			+25°C
		−1830	–	−1450			+75°C
Input Current	I_{IH}	–	–	220	μA	V_{in}=V_{IHA}	0 to +75°C
	I_{IL}	0.5	–	170		$\overline{CS}$ — V_{in}=V_{ILB}	0 to +75°C
		−50	–	–		Others — V_{in}=V_{ILB}	
Supply Current	I_{EE}	−180	–	–	mA	All Inputs and Outputs Open, Test Pin 12	Ta=0°C
		−180	–	–			Ta=75°C

AC Characteristics (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	–	–	15	ns	
Chip Select Recovery Time	t_{RCS}	–	–	10	ns	
Address Access Time	t_{AA}	–	–	15	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	–	–	ns	t_{WSA}=2ns
Data Setup Time	t_{WSD}	2	–	–	ns	
Data Hold Time	t_{WHD}	3	–	–	ns	
Address Setup Time	t_{WSA}	2	–	–	ns	t_W=10ns
Address Hold Time	t_{WHA}	3	–	–	ns	
Chip Select Setup Time	t_{WSCS}	2	–	–	ns	
Chip Select Hold Time	t_{WHCS}	3	–	–	ns	
Write Disable Time	t_{WS}	–	–	10	ns	
Write Recovery Time	t_{WR}	–	–	18	ns	

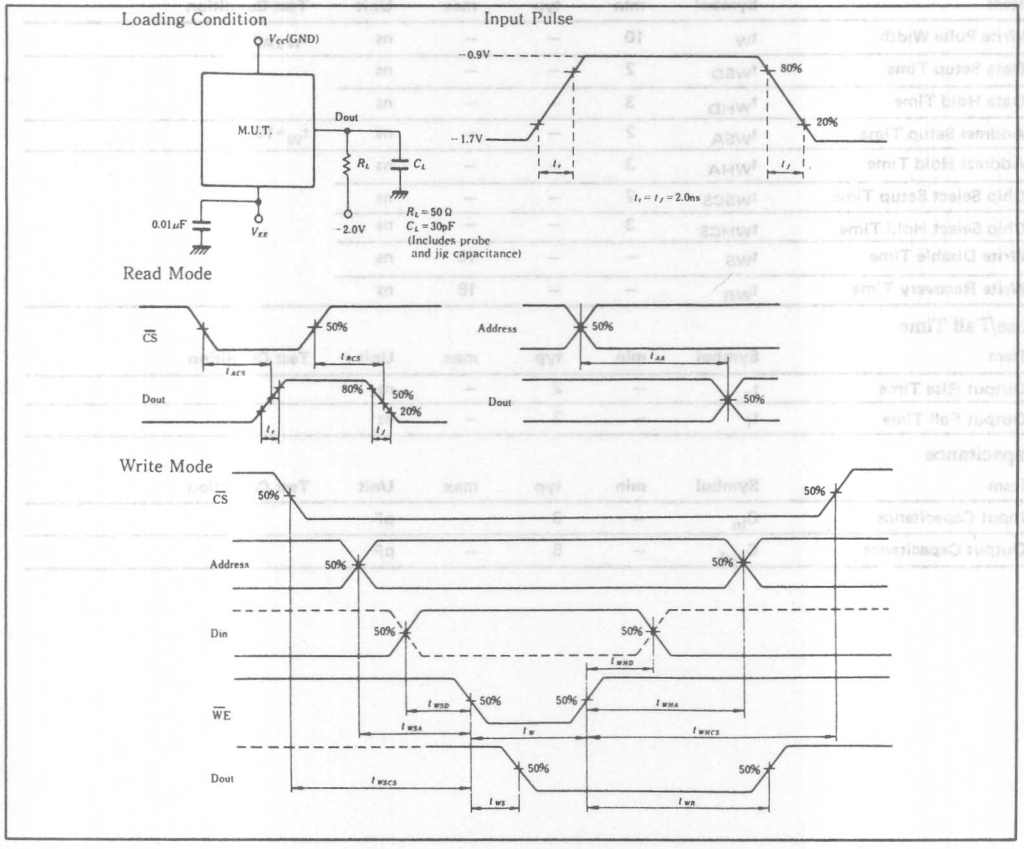
Rise/Fall Time

Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	–	2	–	ns	
Output Fall Time	t_f	–	2	–	ns	

Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{in}	–	3	–	pF	
Output Capacitance	C_{out}	–	5	–	pF	

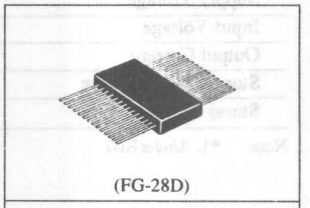
Test Circuit and Waveforms



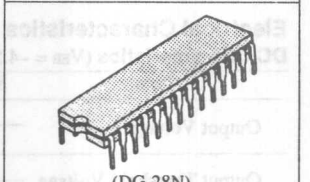
HM100494 Series — Preliminary

16384-word × 4-bit Fully Decoded Random Access Memory

The HM100494 is ECL 100K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.



(FG-28D)



(DG-28N)

Features

- 16384-word × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 650 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

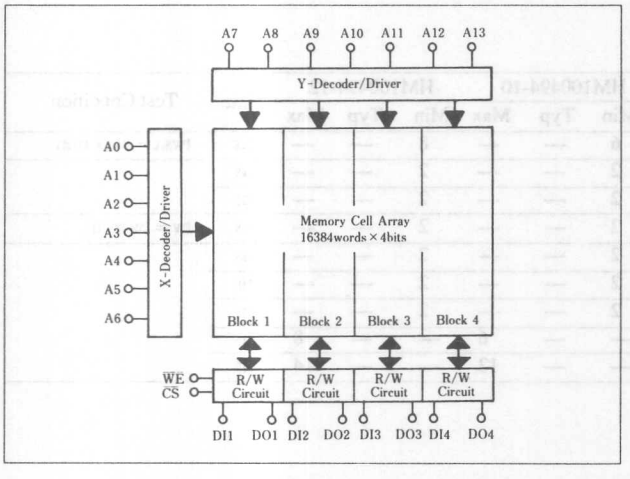
Type No.	Access Time	Package
HM100494-10	10 ns	400 mil 28-pin Cerdip
HM100494-12	12 ns	(DG-28N)
HM100494F-10	10 ns	28-pin Ceramic Flat
HM100494F-12	12 ns	(FG-28D)

Function Table

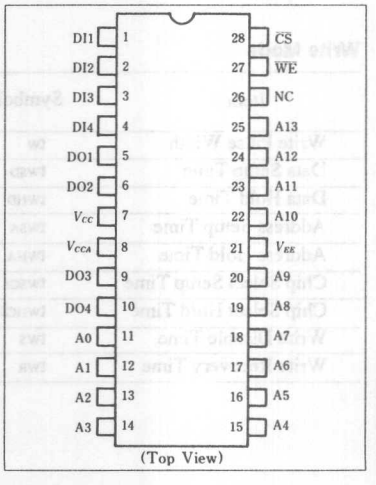
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to –7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	–30	mA
Storage Temperature	Tstg	–65 to +150	°C
Storage Temperature	Tstg (Bias)[1]*	–55 to +125	°C

Note: *1: Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = –4.5 V, R_L = 50Ω to –2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage
	V_{IL}	–1810	—	–1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—		Others
Supply Current	I_{EE}	–180	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = –4.5 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM100494-10			HM100494-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM100494-10			HM100494-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	t_W	6	—	—	8	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	t_W = t_W min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

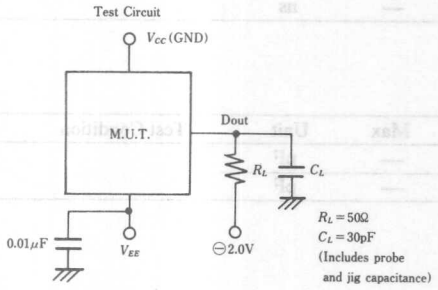
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

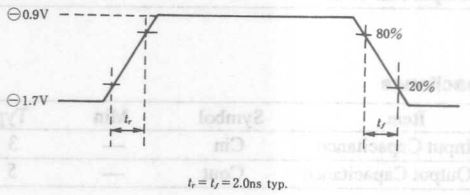
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

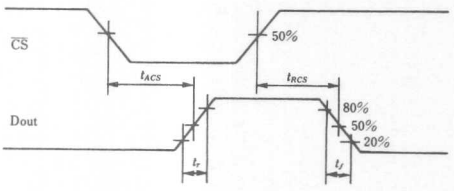
Loading Condition

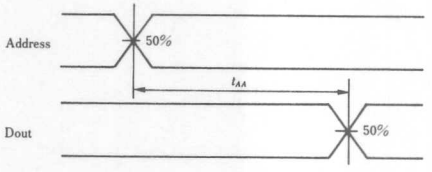


Input Pulse

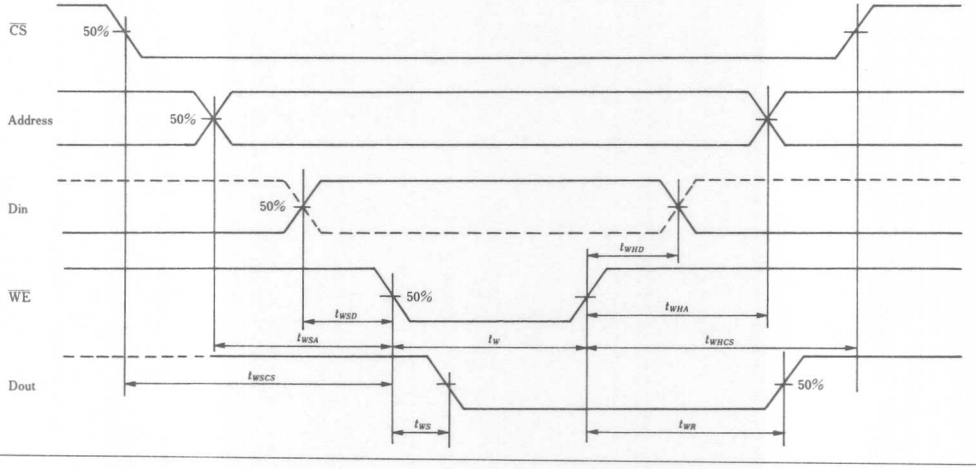


Read Mode





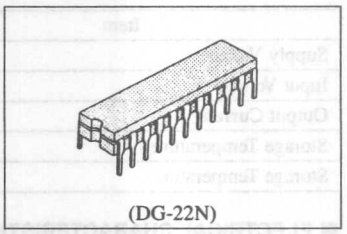
Write Mode



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HM100490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory



(DG-22N)

■ DESCRIPTION

The HM100490 is ECL 100K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

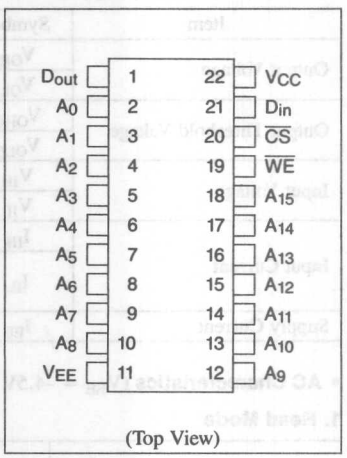
■ FEATURES

- 65536 × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .6/8ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

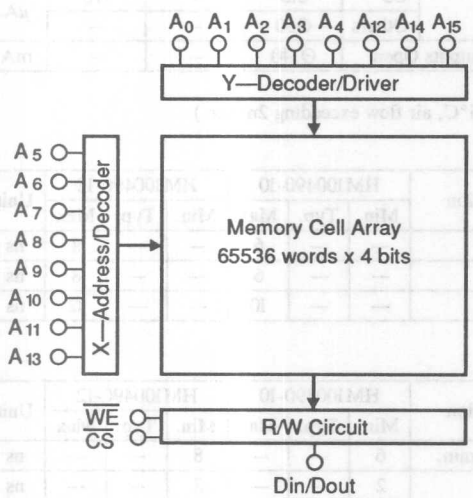
Type No.	Access Time	Package
HM100490-10 HM100490-12	10ns 12ns	300 mil 22 pin Cerdip (DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to Θ3.0	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(under\ bias)}$	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = –4.5V, R_L = 50Ω to –2.0V, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		Θ1165	—	Θ880	mV
	V_{IL}	High/Low for All Inputs		Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ140	—	—	mA

• AC Characteristics (V_{EE} = –4.5V ± 5%, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM100490-10			HM100490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM100490-10			HM100490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

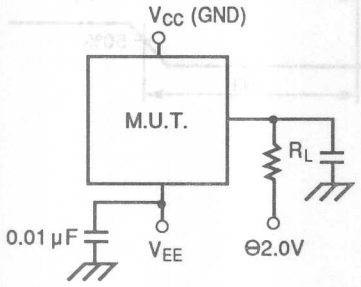
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

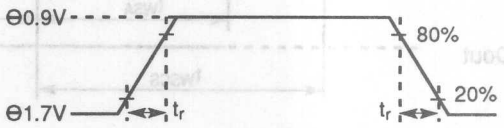
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

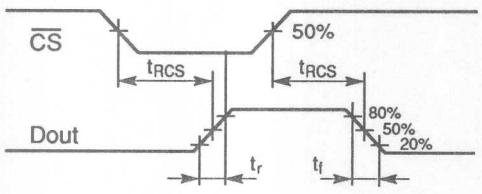
1. Loading Condition

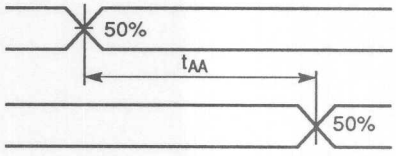


2. Input Pulse

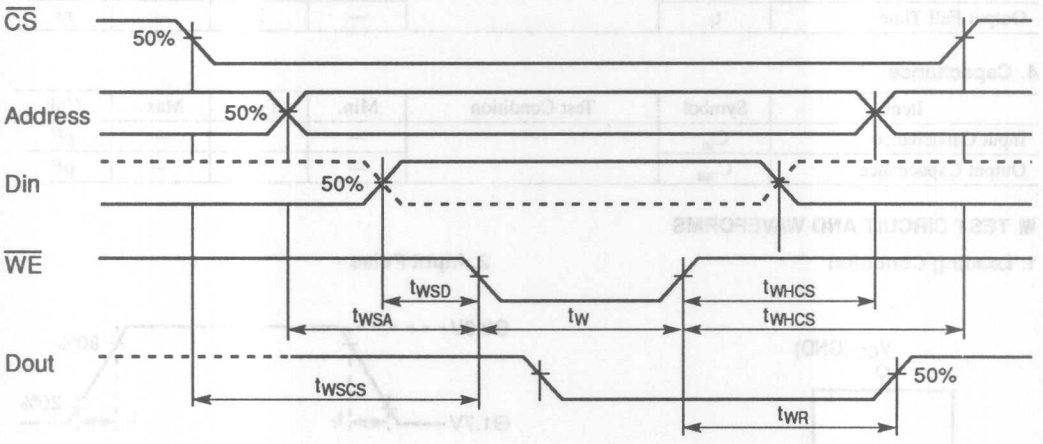


3. Read Mode





4. Write Mode



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HM100504F-10/12 — Preliminary

65536-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM100504 is ECL 100K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

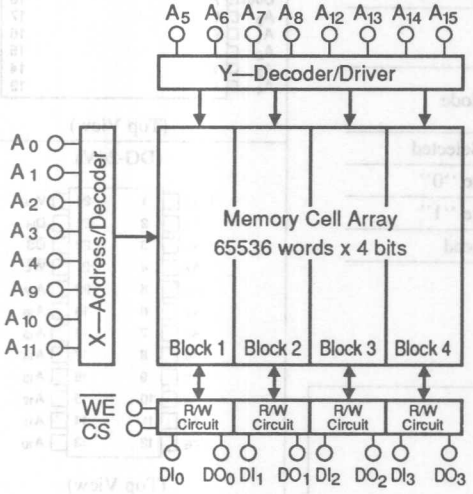
■ FEATURES

- 65536 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .8ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

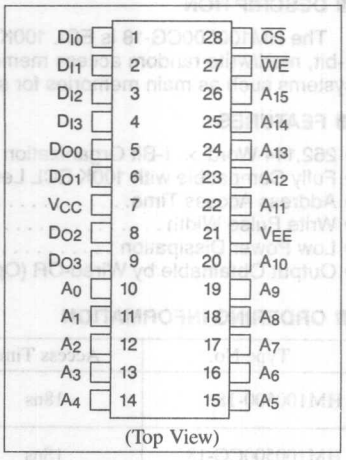
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM100504F-10	10 ns	28 pin Ceramic Flat Package
HM100504F-12	12 ns	(30 mil lead Pitch)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

HM100500CG-18 — Preliminary

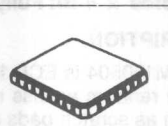
262,144-Word × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

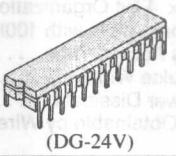
The HM100500CG-18 is ECL 100K compatible, 262,144-word × 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-Word × 1-Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time. . . . . .18ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)



(CG-28B)



(DG-24V)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM100500-18	18ns	24 pin CERDIP (DG-24V)
HM100500CG-18	18ns	28 pin LCC (CG-28B)
HM100500F-18	18ns	24 pin Ceramic Flat (FG-24A)

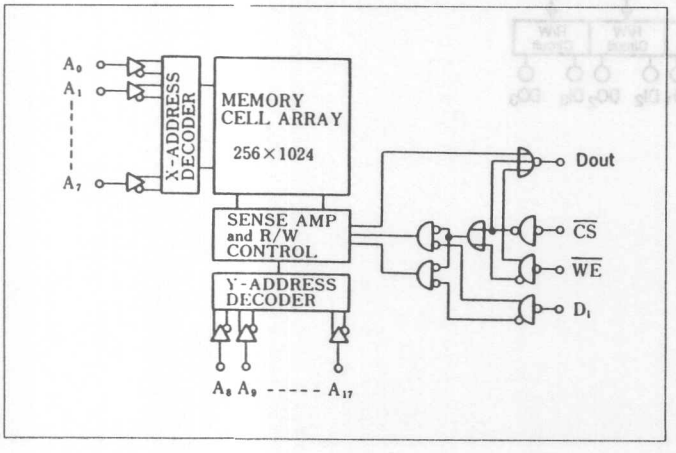
■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*1	Read

NOTES: X = Irrelevant

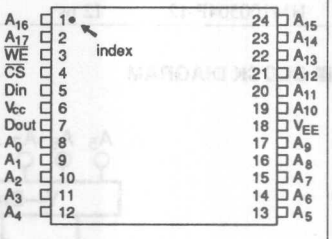
*1 = Read Out Noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

(FG-24A)



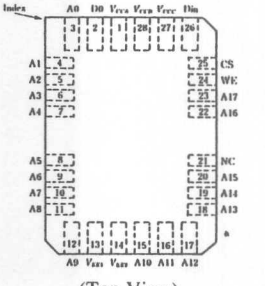
(Top View)

(DG-24V)



(Top View)

(CG-28B)



(Top View)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to –7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	–30	mA
Storage Temperature	Tstg	–65 to +150	°C
Storage Temperature	Tstg (Bias)*1	–55 to +125	°C

Note: *1; Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = –4.5 V, R_L = 50Ω to –2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions
Output Voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage
	V_{IL}	–1810	—	–1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—		Others
Supply Current	I_{EE}	–160	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = –4.5 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	Min	Typ	CG-18 Max	F-18 Max	Unit	Test Conditions
Chip Select Access Time	t_{ACS}	—	—	18	15	ns	
Chip Select Recovery Time	t_{RCS}	—	—	18	10	ns	
Address Access Time	t_{AA}	—	—	18	18	ns	

Write Mode

Item	Symbol	Min	Typ	CG-18 Max	F-18 Max	Unit	Test Conditions
Write Pulse Width	tw	10	—	—		ns	t_{WSA} = 2 ns
Data Setup Time	t_{WSD}	2	—	—			
Data Hold Time	t_{WHD}	3	—	—		ns	
Address Setup Time	t_{WSA}	2	—	—		ns	t_W = 10 ns
Address Hold Time	t_{WHA}	3	—	—		ns	
Chip Select Setup Time	t_{WSCS}	2	—	—		ns	
Chip Select Hold Time	t_{WHCS}	3	—	—		ns	
Write Disable Time	t_{WS}	—	—	15	10	ns	
Write Recovery Time	t_{WR}	—	—	21	21	ns	

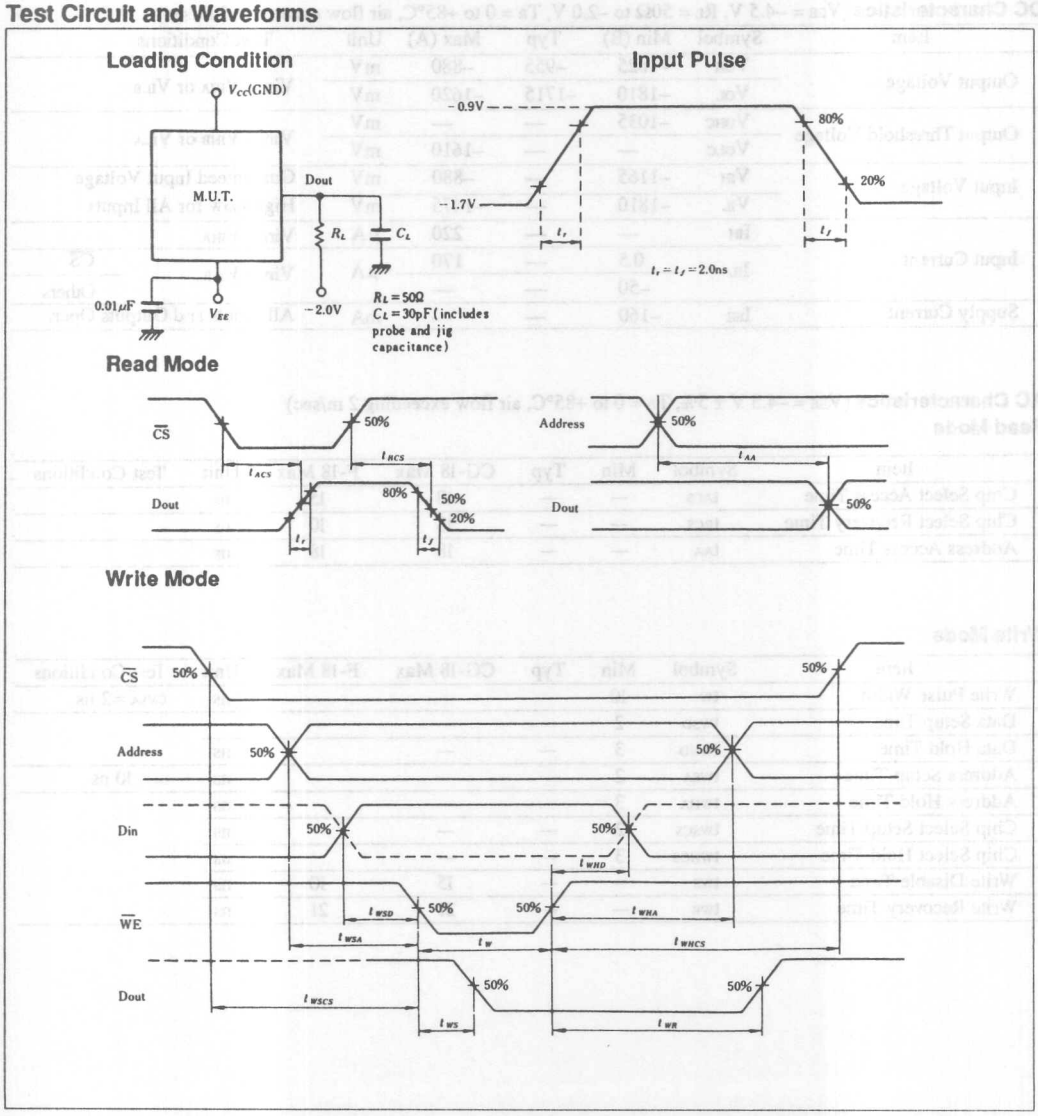
Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms



HM101494 Series — Preliminary

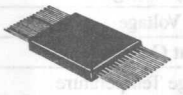
16384-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

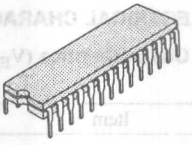
The HM101494 is ECL 100K compatible, 16384-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

- 16384 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .6/8ns (min.)
- Low Power Dissipation . . . . . .750mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)



(FG-28D)

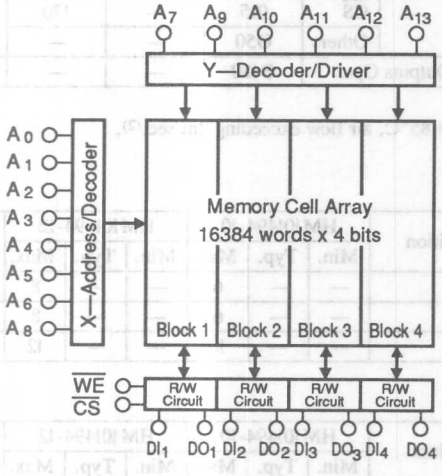


(DG-28N)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101494-10 HM101494-12	10ns 12ns	400 mil 28 pin Cerdip (DG-28N)
HM101494F-10 HM101494F-12	10ns 12ns	28 pin Ceramic Flat (FG-28D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$(1)	Θ55 to +125	°C

NOTES: 1. Under bias.
2. Ceramic flat . . . T_C, Cerdip . . . T_a.

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V(2), T_a = 0 to +85°C, air flow exceeding 2m/sec.(2), T_C = 0 to +85°C)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ180	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%(2), T_a = 0 to +85°C, air flow exceeding 2m/sec.(2), T_C = 0 to +85°C)

1. Read Mode

Item	Symbol	Test Condition	HM101494-10			HM101494-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM101494-10			HM101494-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

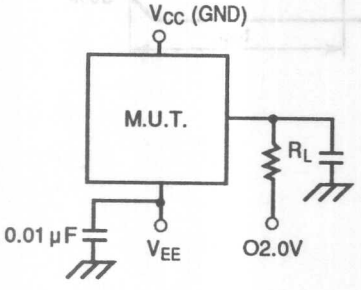
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

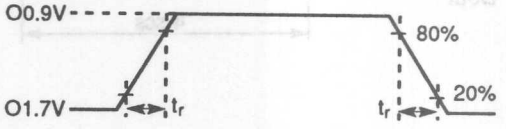
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	$\overline{WE}$, $\overline{CS}$, D_{I1}, D_{I2}	—	5	—	pF
		Others	—	3	—	pF
Output Capacitance	C_{out}		—	3	—	pF

■ TEST CIRCUIT AND WAVEFORMS

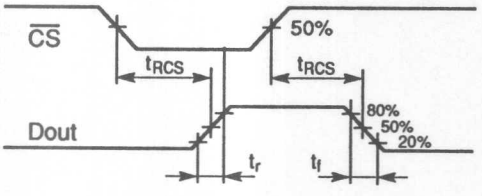
1. Loading Condition

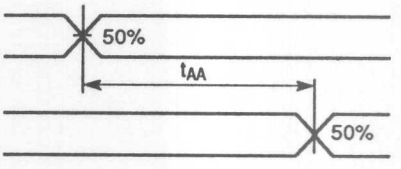


2. Input Pulse

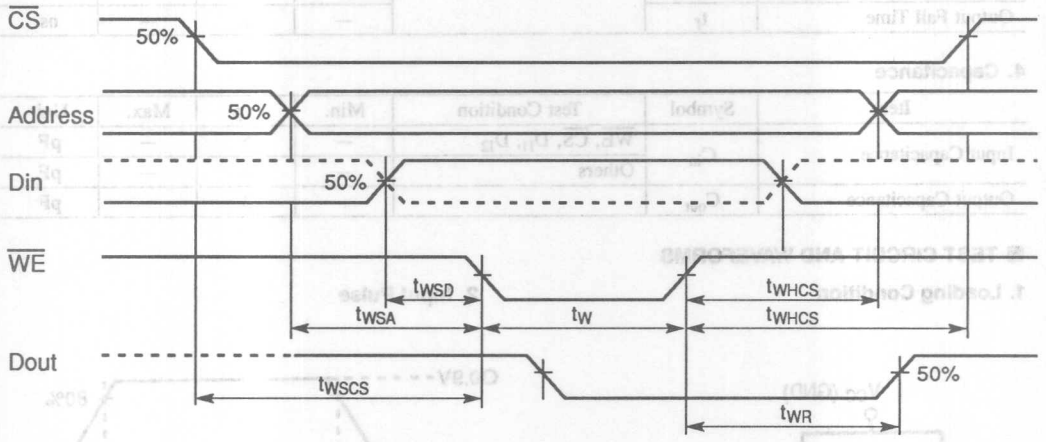


3. Read Mode





4. Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWSD
tWSA
tW
tWHCS
tWHCS
tWSCS
tWR

HM101490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM101490 is ECL 100K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

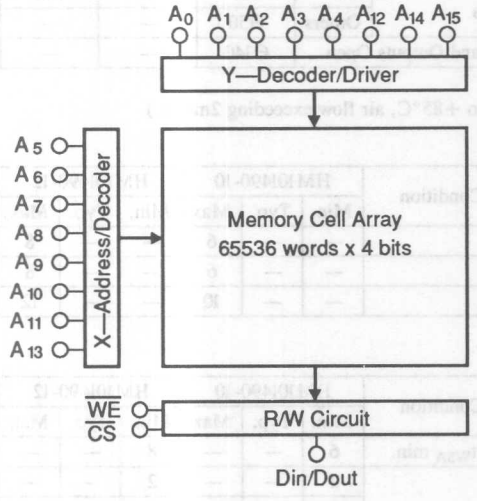
■ FEATURES

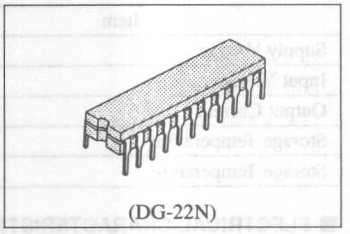
- 65536 × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .6/8ns (min.)
- Low Power Dissipation . . . . . .570mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101490-10 HM101490-12	10ns 12ns	300 mil 22 pin Cerdip (DG-22N)

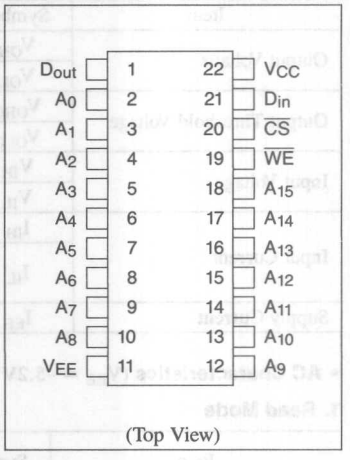
■ BLOCK DIAGRAM





(DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to Θ3.0	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(under\ bias)}$	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = –5.2V, R_L = 50Ω to –2.0V, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ140	—	—	mA

• **AC Characteristics** (V_{EE} = –5.2V ± 5%, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM101490-10			HM101490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM101490-10			HM101490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

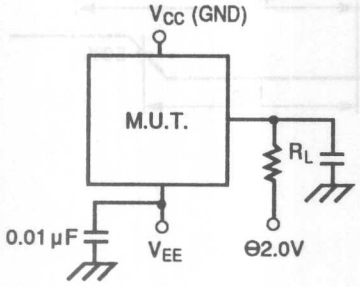
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

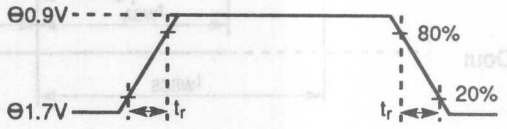
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

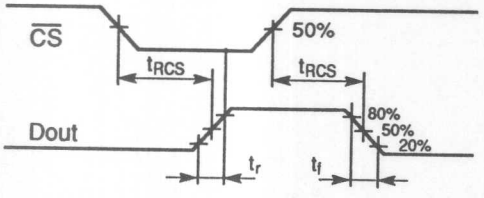
1. Loading Condition

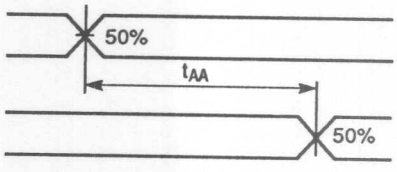


2. Input Pulse

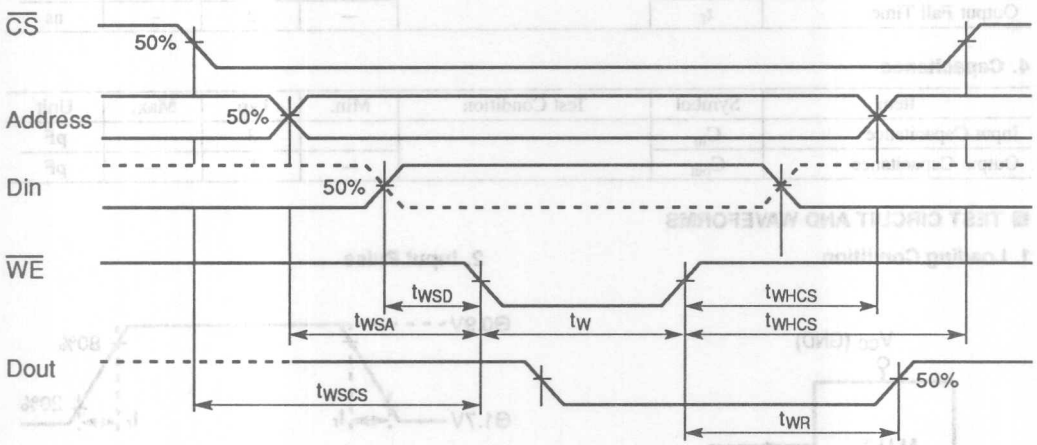


3. Read Mode





4. Write Mode


$\overline{CS}$
50%
Address
50%
Din
50%
$\overline{WE}$
t_{WSD}
t_{WSA}
t_W
t_{WHCS}
t_{WHCS}
Dout
t_{WSCS}
50%
t_{WR}

HM101504F-10/12 — Preliminary

65536-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM101504 is ECL 100K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

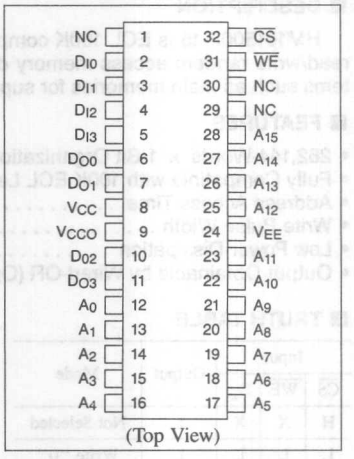
■ FEATURES

- 65536 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .8ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

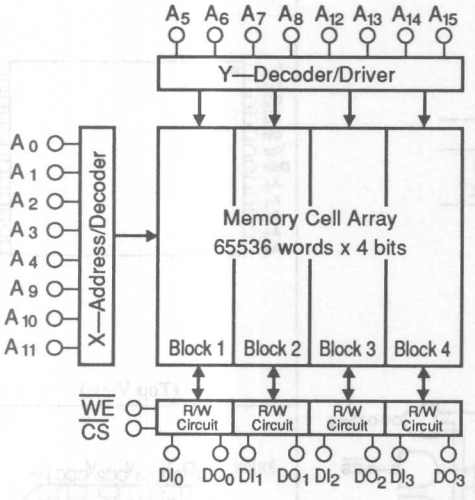
Type No.	Access Time	Package
HM101504F-10	10 ns	(TBD)
HM101504F-12	12 ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

HM101500F-15 — Preliminary

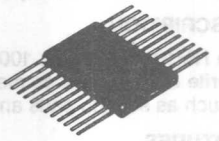
262144-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

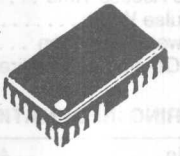
HM101500F-15 is ECL 100K compatible, 262144-words by 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-Words × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time. . . . . .15ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)



(FG-24A)



(CG-28B)

■ TRUTH TABLE

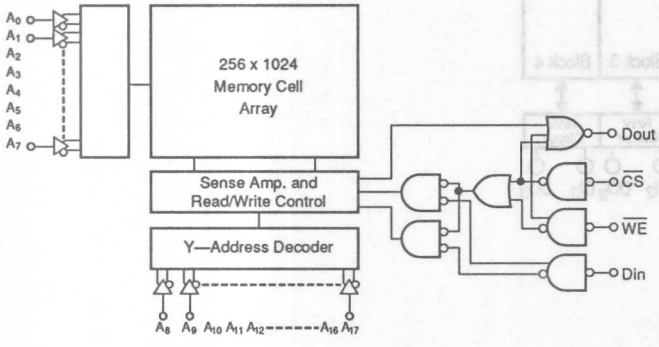
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

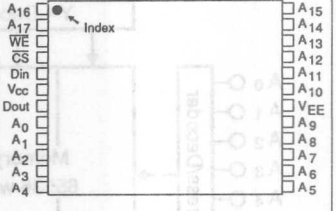
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101500F-15	15 ns	24 pin Ceramic Flat
HM101500CG-15	15 ns	28 pin Ceramic LCC

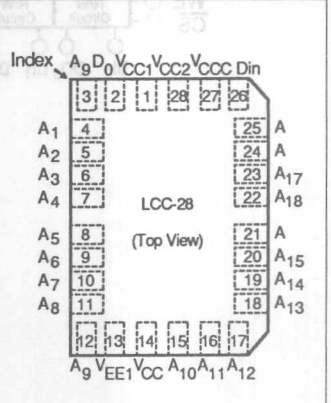
■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$*	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_C = 0 to +85°C)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ200	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%, T_C = 0 to +85°C)

1. Read Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Chip Select Access Time	t_{ACS}		—	—	15	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	15	ns

2. Write Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	10	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		3	—	—	ns
Address Setup Time	t_{WSA}	t_W = 10ns	2	—	—	ns
Address Hold Time	t_{WHA}		3	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		3	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	18	

3. Rise/Fall Time

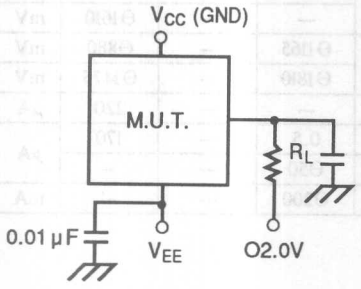
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

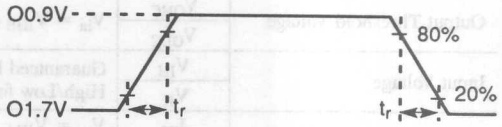
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

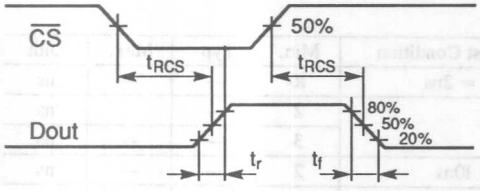
1. Loading Condition

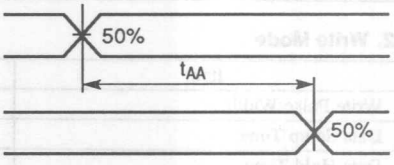


2. Input Pulse

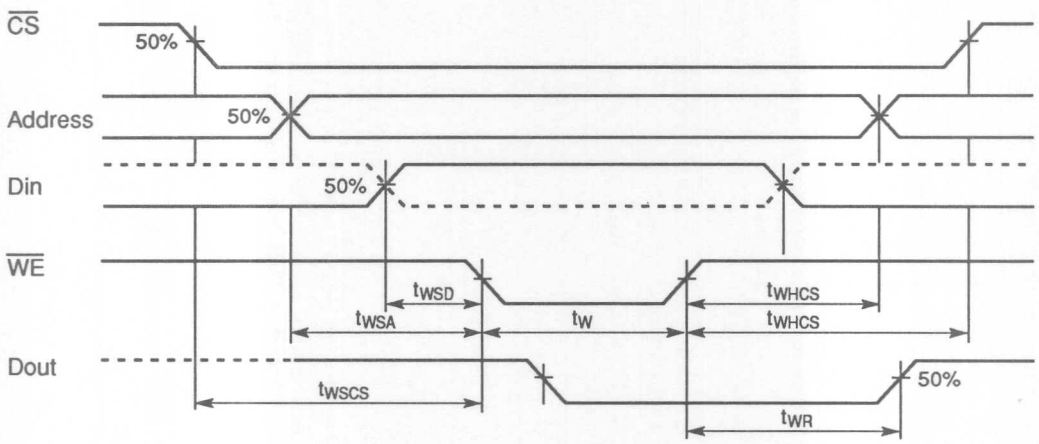


3. Read Mode





4. Write Mode


$\overline{CS}$
50%
Address
50%
Din
50%
$\overline{WE}$
t_{WSD}
t_{WHCS}
t_{WSA}
t_W
t_{WHCS}
Dout
50%
t_{WSCS}
t_{WR}

NOTES: